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H8SX Family

Sleep Interrupt

Introduction

A SLEEP instruction is used to place the CPU in a low-power-consumption state. Generation of a sleep interrupt will take the CPU out of the low-power-consumption state, unless an interrupt from a releasing source was generated immediately before the SLEEP instruction, in which case release from the low-power-consumption state is by a reset or the next interrupt.

A new sleep interrupt function has been added to this LSI. In the example given in this application note, this function releases the LSI from the low-power-consumption state independently of the timing of interrupts from releasing sources.

Target Device

H8SX/1653F

Contents

1. Specification

A SLEEP instruction is used to place the CPU in a low-power-consumption state. Generation of a sleep interrupt will take the CPU out of the low-power-consumption state, unless an interrupt from a releasing source was generated immediately before the SLEEP instruction, in which case release from the low-power-consumption state is by a reset or the next interrupt.

A new sleep interrupt function has been added to this LSI. In the example given in this application note, this function releases the LSI from the low-power-consumption state independently of the timing of interrupts from releasing sources.

1. For the program execution state in this sample task, the software generates pulses on the PF4 pin.
2. After a certain period of program execution, a SLEEP instruction is executed to place the CPU in the low-power-consumption mode.
3. Release from the low-power-consumption mode is triggered by an IRQ0 interrupt.
4. When the IRQ0 interrupt is generated immediately before execution of the SLEEP instruction, the interrupt handling routine makes settings for the sleep interrupt.
5. When the SLEEP instruction is executed under the condition described in (4), a sleep interrupt is generated. The handler for the sleep interrupt generates a single-shot pulse on the PF3 pin. Also, to confirm that the CPU has not been placed in the sleep mode even though the SLEEP instruction has been executed, pulses continue to be generated on the PF4 pin.

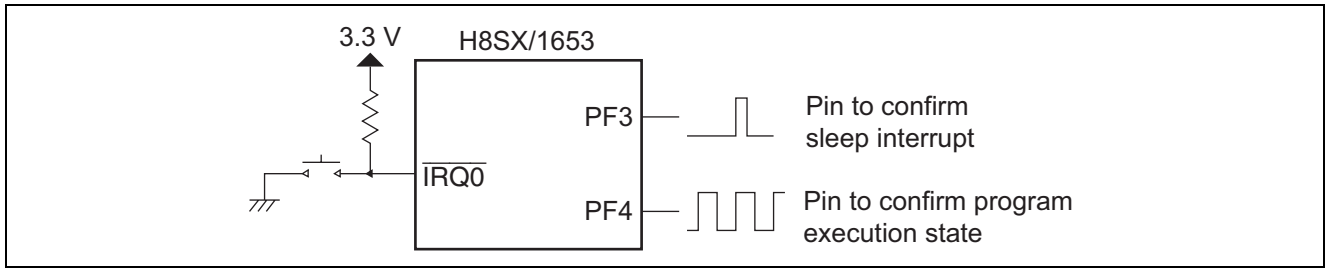


Figure 1 Connection Diagram for Confirmation of Sleep Interrupt Operation

2. Applicable Conditions

Table 1 Applicable Condition

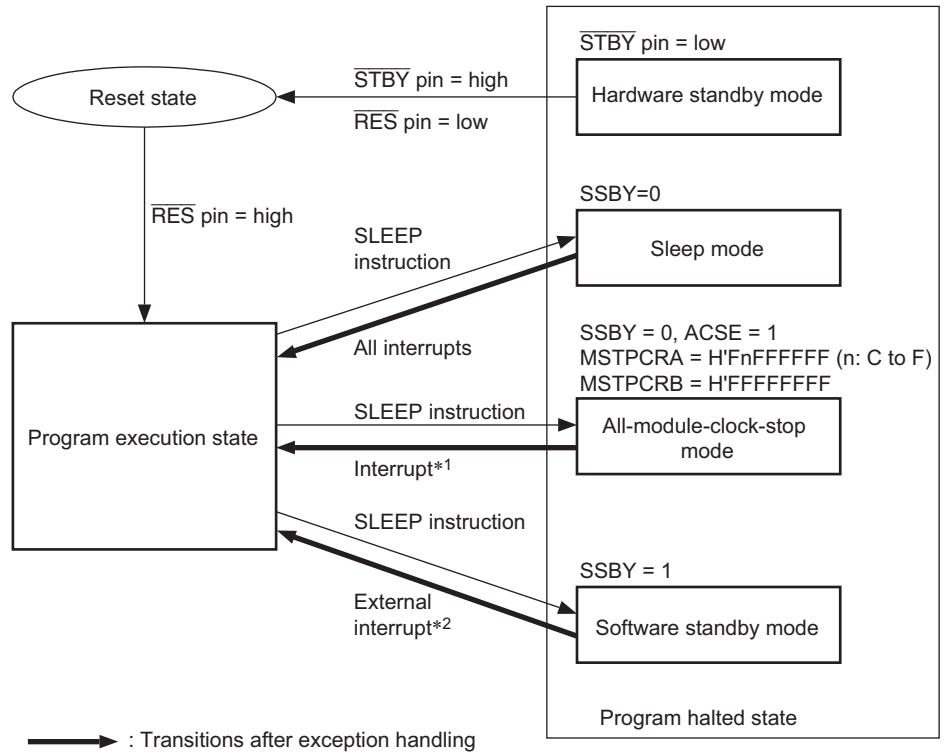
Item	Details
Operating frequency	Input clock: 16 MHz System clock (Iϕ): 32 MHz Peripheral module clock (Pϕ): 32 MHz External bus clock (Bϕ): 32 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Functions Used

A sleep interrupt is generated by executing a SLEEP instruction. The sleep interrupt is nonmaskable, and is always accepted regardless of the interrupt control mode or the settings of the CPU interrupt mask bits. The SLPIE bit in SBYCR selects whether the sleep interrupt function is enabled or not.

[Caution] The sleep interrupt function is only available on an actual device. It does not function with a full emulator such as the E6000H.

Figure 2 shows transitions to the low-power-consumption states, states of the CPU and peripheral modules, and the method of release from each mode. After a reset, modules other than the DTC and DMAC are halted in normal program operation.



Notes: From any state, a transition to hardware standby mode is triggered by driving $\overline{\text{STBY}}$ low.
From any state other than hardware standby mode, a transition to the reset state is triggered by driving $\overline{\text{RES}}$ low.

*1 NMI, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ11}}$, 8-bit timer interrupts, and watchdog timer interrupts.
A pair of 8-bit timers is enabled if the corresponding bit of MSPCRA9 or MSTPCRA8 is cleared to 0.

*2 NMI and $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ11}}$. Note that IRQ is valid only when the corresponding bit in SSIER is set to 1.

Figure 2 Mode Transitions

4. Principle of Operation

This section describes the relation between low-power-consumption states and interrupt handling.

4.1 SLEEP Instruction Operation 1

Figure 3 shows an example of operation when an interrupt from a releasing source is generated after execution of a SLEEP instruction. When the SLPIE bit in the SBYCR register is set to 0, the sleep interrupt function is disabled. When the SLEEP instruction is executed while the SLPIE bit is cleared to 0, the CPU makes the transition to a low-power-consumption state. Then, when an interrupt is generated by a releasing source, the CPU is taken out of the low-power-consumption state and starts exception handling.

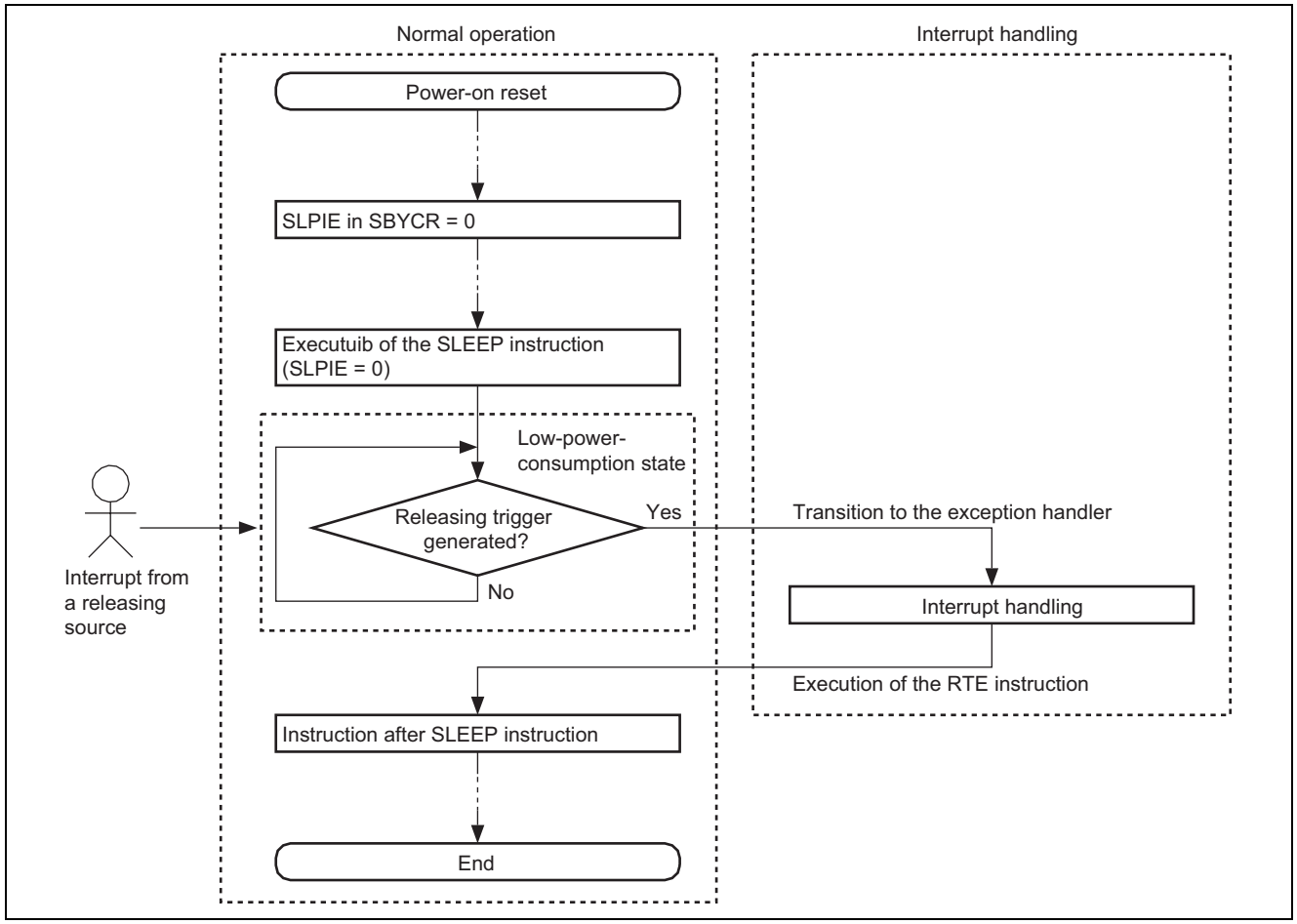


Figure 3 Generation of an Interrupt from a Releasing Source after SLEEP Instruction Execution

4.2 SLEEP Instruction Operation 2 (Sleep Interrupt Disabled)

Figure 4 shows an example of operation when an interrupt from a releasing source is generated (and disables the sleep interrupt) immediately before the SLEEP instruction. When the releasing-source interrupt is generated immediately before the SLEEP instruction while the SLPIE bit is clear (0), exception handling for the interrupt starts. On return from the interrupt handling routine, the SLEEP instruction is executed and the CPU makes the transition to the low-power-consumption state. In such a case, release from the low-power-consumption state will not proceed until the next interrupt from a releasing source.

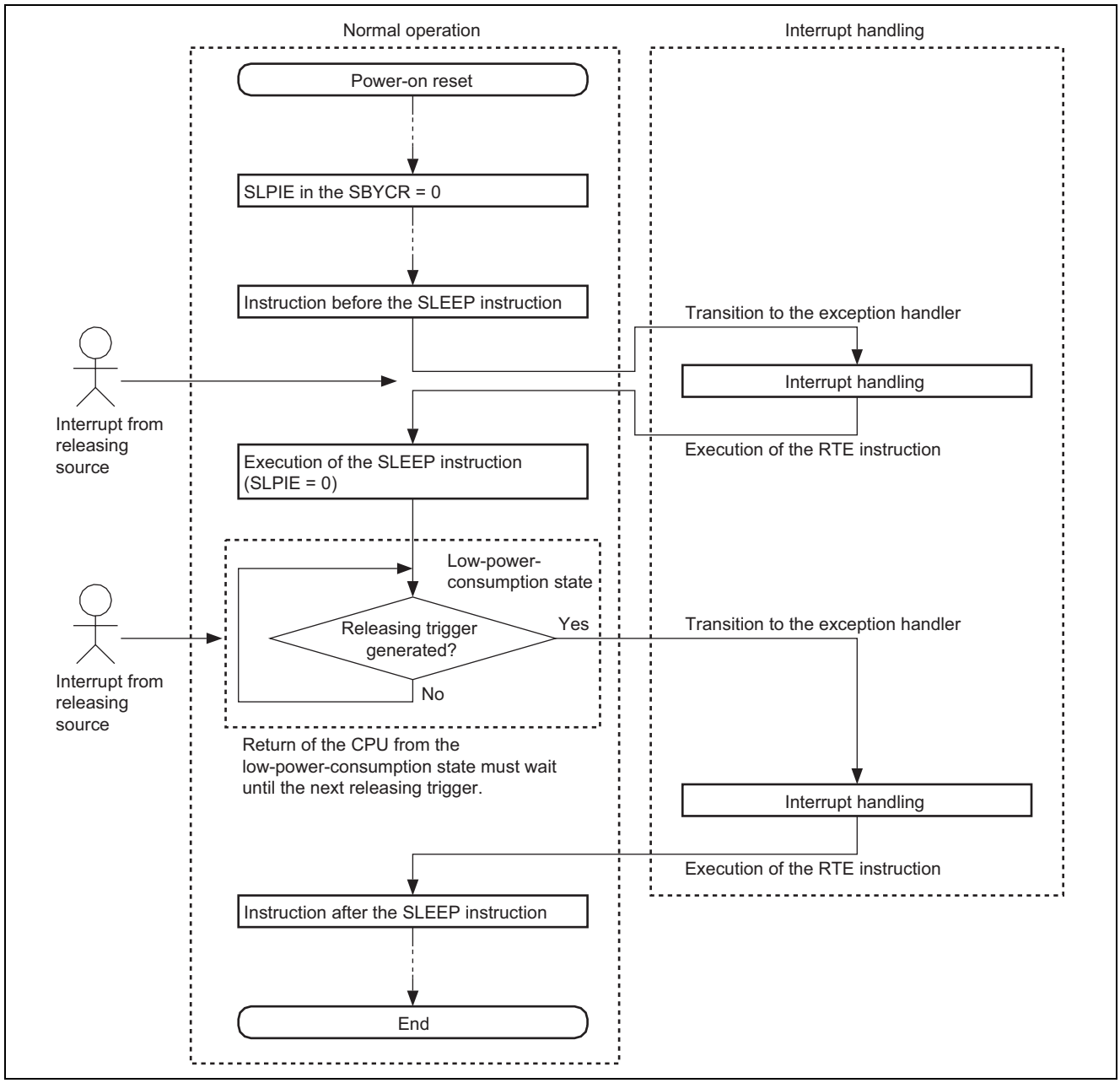


Figure 4 Generation of an Interrupt from a Releasing Source (Disabling the Sleep Interrupt) Immediately before SLEEP Instruction Execution

4.3 SLEEP Instruction Operation 3 (Sleep Interrupt Enabled)

Figure 5 shows an example of operation when an interrupt from a releasing source is generated (and enables the sleep interrupt) immediately before a SLEEP instruction. When the SLPIE bit is set to 1 to enable the sleep interrupt function in the handling routine of the interrupt from a releasing source, the operation of the system is as shown in figure 5. Even if the interrupt from a releasing source is generated immediately before the SLEEP instruction, the SLEEP instruction is executed and a sleep interrupt is generated. Therefore, the CPU promptly makes the transition to the execution state after exception handling, i.e. it is not placed in a low-power-consumption state.

When the SLPIE bit is set to 1 to enable the sleep interrupt function, clear the SSBY bin in the SBYCR register to 0.

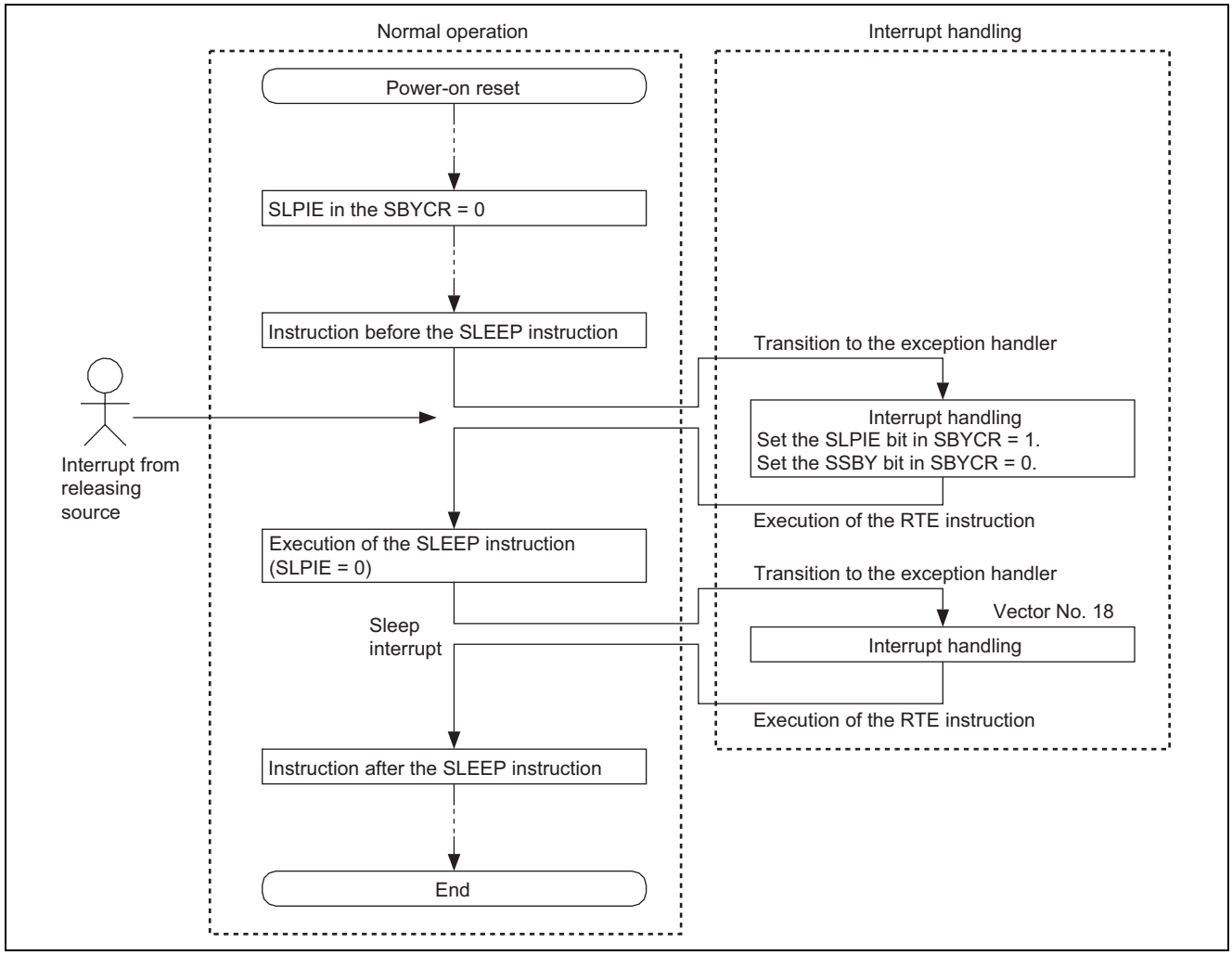


Figure 5 Generation of an Interrupt from a Releasing Source (Enabling the Sleep Interrupt) Immediately before SLEEP Instruction Execution

5. Description of Software

5.1 Operating Environment

Table 2 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.00.03
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
H8SX compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 3 Setting of Sections

Address	Section	Description
H'001000	P	Program area

Table 4 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Address of Vector Table Entry	Exception Handling Routine
Reset	0	H'000000	init
SLEEP instruction	18	H'000048	sleep_int
IRQ0	64	H'000100	irq0_int

5.2 List of Functions

Table 5 List of Functions

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function.
main	Main routine Switches the port pin used to confirm sleep operation on and off. Handles execution of the SLEEP instruction.
sleep_int	Sleep interrupt handler Software generation of a single -shot pulse on the PD3 pin, confirming the generation of a sleep interrupt
irq0_int	IRQ0 interrupt handling Enables the generation of a sleep interrupt by the SLEEP instruction.

5.3 RAM Usage

In this sample task, the only RAM used is the stack area.

5.4 Description of Functions

5.4.1 init Function

1. Functional overview

Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode Control Register (MDCR) Number of Bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 6). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by pins MD3 to MD0.

Table 6 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC.
8	ICK0	1	R/W	000: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	000: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

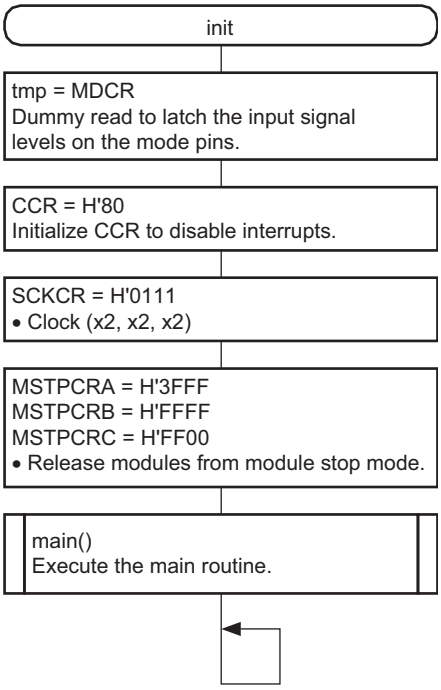
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communication interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communication interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communication interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communication interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communication interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0111
• Clock (x2, x2, x2)
MSTPCRA = H'3FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release modules from module stop mode.
main()
Execute the main routine.

5.4.2 main Function

1. Functional overview

The main routine switches a port pin on and off to confirm sleep operation and handles execution of the SLEEP instruction.

2. Argument

None

3. Return value

None

4. Description of internal registers

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Port 5 input buffer control register (P5ICR) Number of bits: 8 Address: H'FFFB94

Bit	Bit Name	Setting	R/W	Description
0	P50ICR	1	R/W	0: Disables input buffer of pin P50. 1: Enables input buffer of pin P50.

- Port function control register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
0	ITS0	1	R/W	$\overline{\text{IRQ0}}$ Pin Select 0: Specifies pin P10 as the $\overline{\text{IRQ0}}$-A input pin. 1: Specifies pin P50 as the $\overline{\text{IRQ0}}$-B input pin.

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: Interrupt requests are generated by falling edges of $\overline{\text{IRQ0}}$.

- DTC vector base register (DTCVBR) Number of bits: 32 Address: H'FFFD80
  Function: DTCVBR is a 32-bit register that specifies the base address for vector table address calculation.
  Setting: H'00002000

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	1	R/W	IRQ Enable 0: Disables IRQ0 interrupt request. 1: Enables IRQ0 interrupt request.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
0	IRQ0F	0	R/(W)*	IRQ0 Status 0: IRQ0 interrupt is not being generated. 1: IRQ0 interrupt is being generated.

Note: * Only 0 can be written here, to clear the flag.

- Port F data direction register (PFDDR) Number of bits: 8 Address: H'FFFB8E

Bit	Bit Name	Setting	R/W	Description
7	PF4DDR	1	R/W	0: Specifies the PF4 pin as an input pin. 1: Specifies the PF4 pin as an output pin.
6	PF3DDR	1	R/W	0: Specifies the PF3 pin as an input pin. 1: Specifies the PF3 pin as an output pin.

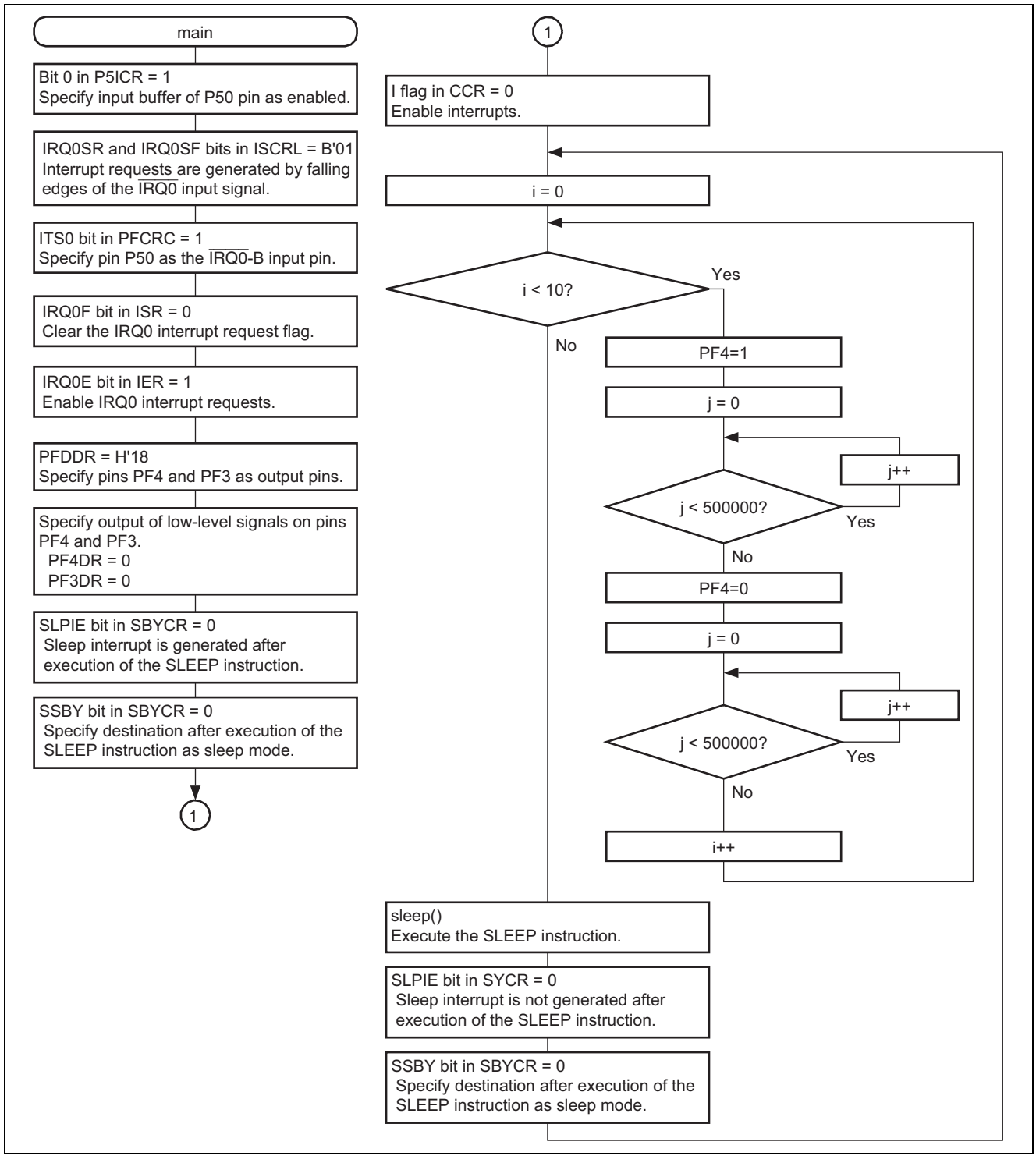
- Port F data register (PFDR) Number of bits: 8 Address: H'FFFF5E

Bit	Bit Name	Setting	R/W	Description
7	PF4DR	0	R/W	0: Signal output from the PF4 pin is at low level. 1: Signal output from the PF4 pin is at high level.
6	PF3DR	0	R/W	0: Signal output from the PF3 pin is at low level. 1: Signal output from the PF3 pin is at high level.

- Standby control register (SBYCR) Number of bits: 16 Address: H'FFFDC6

Bit	Bit Name	Setting	R/W	Description
15	SSBY	0	R/W	Software Standby This bit specifies the destination mode for the transition initiated by executing the SLEEP instruction. 0: Shift to sleep mode after execution of the SLEEP instruction 1: Shift to sleep mode after execution of the SLEEP instruction Initiation of release from the software standby mode and the transition to normal operation by an external interrupt does not change the value of this bit. To clear the bit, write 0 to it. When the WDT is used as the watchdog timer, the setting of this bit is disabled. In this case, a transition is always made to sleep mode or all-module-clock-stop mode after the SLEEP instruction is executed. When the SLPIE bit is set to 1, this bit should be cleared to 0.
7	SLPIE	0	R/W	Sleep Interrupt Enable This bit selects whether a sleep interrupt is or is not generated or not when the SLEEP instruction is executed. 0: A sleep interrupt is not generated when the SLEEP instruction is executed. 1: A sleep interrupt is generated when a SLEEP instruction is executed. Even after handling of a sleep interrupt, this bit remains set to 1. To clear the bit, write 0 to it.

5. Flowchart


main
Bit 0 in P5ICR = 1
Specify input buffer of P50 pin as enabled.
IRQ0SR and IRQ0SF bits in ISCRL = B'01
Interrupt requests are generated by falling edges of the IRQ0 input signal.
ITS0 bit in PFCRC = 1
Specify pin P50 as the IRQ0-B input pin.
IRQ0F bit in ISR = 0
Clear the IRQ0 interrupt request flag.
IRQ0E bit in IER = 1
Enable IRQ0 interrupt requests.
PFDDR = H'18
Specify pins PF4 and PF3 as output pins.
Specify output of low-level signals on pins PF4 and PF3.
PF4DR = 0
PF3DR = 0
SLPIE bit in SBYCR = 0
Sleep interrupt is generated after execution of the SLEEP instruction.
SSBY bit in SBYCR = 0
Specify destination after execution of the SLEEP instruction as sleep mode.
1
1
I flag in CCR = 0
Enable interrupts.
i = 0
i < 10?
Yes
No
PF4=1
j = 0
j++
j < 500000?
Yes
No
PF4=0
j = 0
j++
j < 500000?
Yes
No
i++
sleep()
Execute the SLEEP instruction.
SLPIE bit in SYCR = 0
Sleep interrupt is not generated after execution of the SLEEP instruction.
SSBY bit in SBYCR = 0
Specify destination after execution of the SLEEP instruction as sleep mode.

5.4.3 sleep_int Function

1. Functional overview

Handles sleep interrupts and includes the software that generates a single-shot pulse on the PF3 pin to confirm generation of the sleep interrupt.

2. Argument

None

3. Return value

None

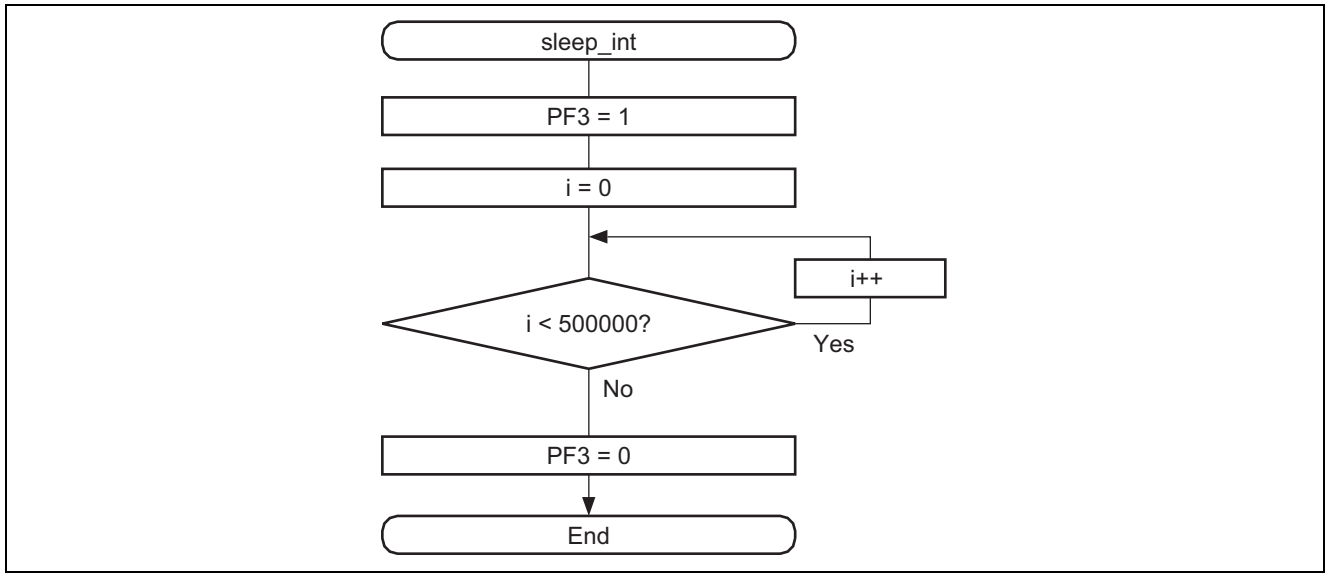
4. Description of internal registers

The internal register used in this sample task is described below. The setting shown in the table is the value used in this sample task and differ from the initial value.

- Port F data register (PFDR) Number of bits: 8 Address: H'FFFF5E

Bit	Bit Name	Setting	R/W	Description
6	PF3DR	0/1	R/W	0: Signal output from the PF3 pin is at the low level. 1: Signal output from the PF3 pin is at the high level.

5. Flowchart



5.4.4 irq0_int Function

1. Functional overview

Handles IRQ0 interrupts.

2. Argument

None

3. Return value

None

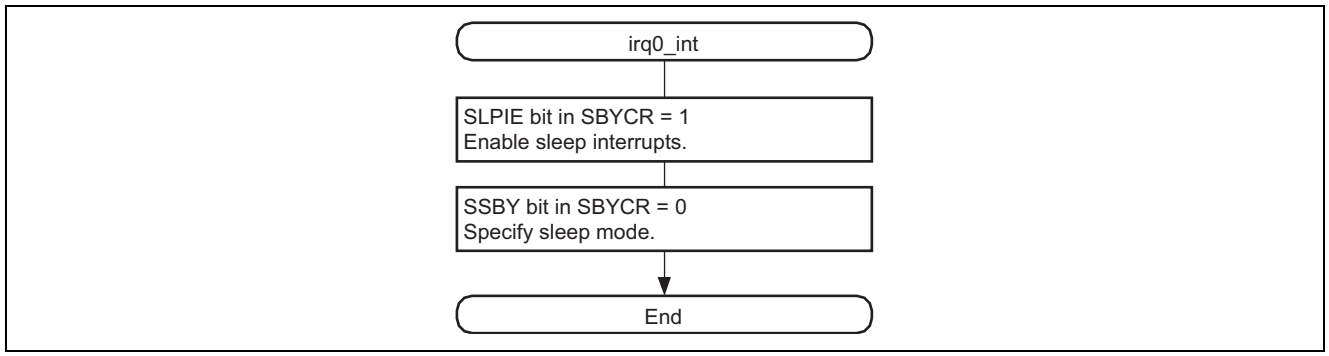
4. Description of internal registers

The internal register used in this sample task is described below. The settings shown in the table are the values used in this sample task and differ from the initial values.

- Standby control register (SBYCR) Number of bits: 16 Address: H'FFFDC6

Bit	Bit Name	Setting	R/W	Description
15	SSBY	0	R/W	Software Standby This bit specifies the destination mode for the transition initiated by executing the SLEEP instruction. 0: Shift to sleep mode after execution of the SLEEP instruction 1: Shift to sleep mode after execution of the SLEEP instruction Initiation of release from the software standby mode and the transition to normal operation by an external interrupt does not change the value of this bit. To clear the bit, write 0 to it. When the WDT is used as the watchdog timer, the setting of this bit is disabled. In this case, a transition is always made to sleep mode or all-module-clock-stop mode after the SLEEP instruction is executed. When the SLPIE bit is set to 1, this bit should be cleared to 0.
7	SLPIE	1	R/W	Sleep Interrupt Enable This bit selects whether a sleep interrupt is or is not generated or not when the SLEEP instruction is executed. 0: A sleep interrupt is not generated when the SLEEP instruction is executed. 1: A sleep interrupt is generated when a SLEEP instruction is executed. Even after handling of a sleep interrupt, this bit remains set to 1. To clear the bit, write 0 to it.

5. Flowchart



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csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun.18.07	—	First edition issued

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