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H8SX Family

Simultaneous Use of Three A/D Converter Units for High-Speed Sampling

Introduction

Three A/D converter units are simultaneously used to sample data at high speed for A/D conversion. The A/D converted data are transferred to on-chip RAM by the DMAC.

Target Device

H8SX/1648F

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2. Applicable Conditions 3
3. Description of Modules Used 4
4. Principles of Operation 15
5. Description of Software 20
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1. Specification

Three A/D converter units are simultaneously used for accelerated data sampling.

- An example of the connection for this sample task is shown in figure 1.
- Using A/D converters and controlling the timing of the start of A/D conversion for each unit shortens the sampling interval for A/D conversion to one-third (at an intervals between 0.84 to 0.86 µm when Pϕ = 25 MHz) of the interval for a single unit (an interval of 2.56 µm when Pϕ = 25 MHz).*
- The A/D converters are operated in scan mode, and each unit sequentially converts four channels of analog input. Twelve channels on a total of three A/D converter units are used.
- The timing of the start of A/D conversion is controlled by software.
- Results of A/D conversion are transferred to on-chip RAM by DMAC processing.
- Analog signals are simultaneously input to twelve pins: AN0 to AN11.

Note: * The high-speed sampling for A/D conversion in this sample task does not guarantee a regular sampling intervals.

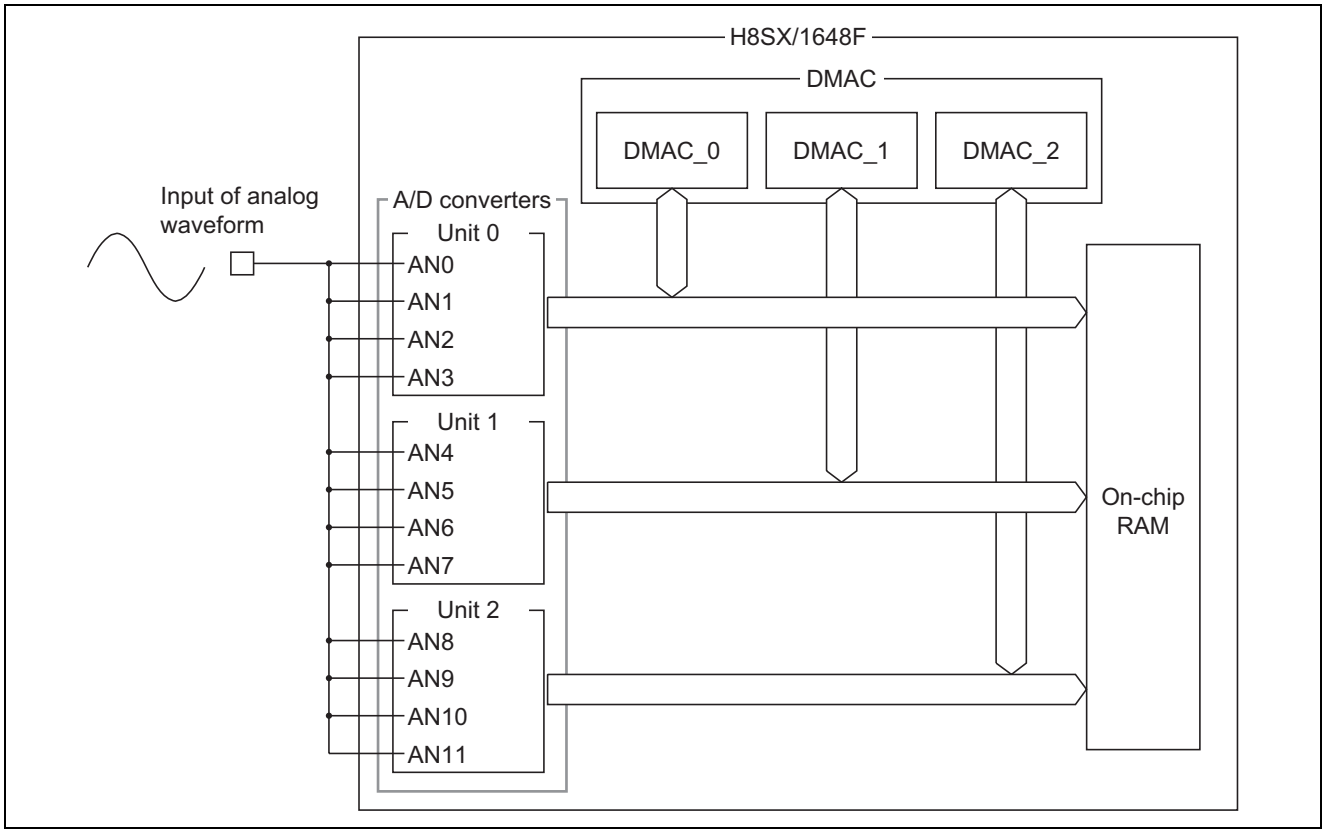


Figure 1 High-Speed Sampling Configuration of A/D Converters

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock	: 12.5 MHz
	System clock (Iϕ)	: 50 MHz (input clock frequency × 4)
	Peripheral mode clock (Pϕ)	: 25 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 50 MHz (input clock frequency × 4)
Mode of operation	Mode 7 (MD2 = 1, MD1 = 1, MD0 = 1)	

3. Description of Modules Used

3.1 A/D Converters

3.1.1 Basic Functions of A/D Converters

Figures 2 to 4 are block diagrams of A/D converter units 0 (AD_0) to 2 (AD_2). The below functions of the A/D converters are used in this sample task.

- Consecutive A/D conversion of analog inputs on four channels (scan mode)
- A/D conversion end interrupt (ADI)

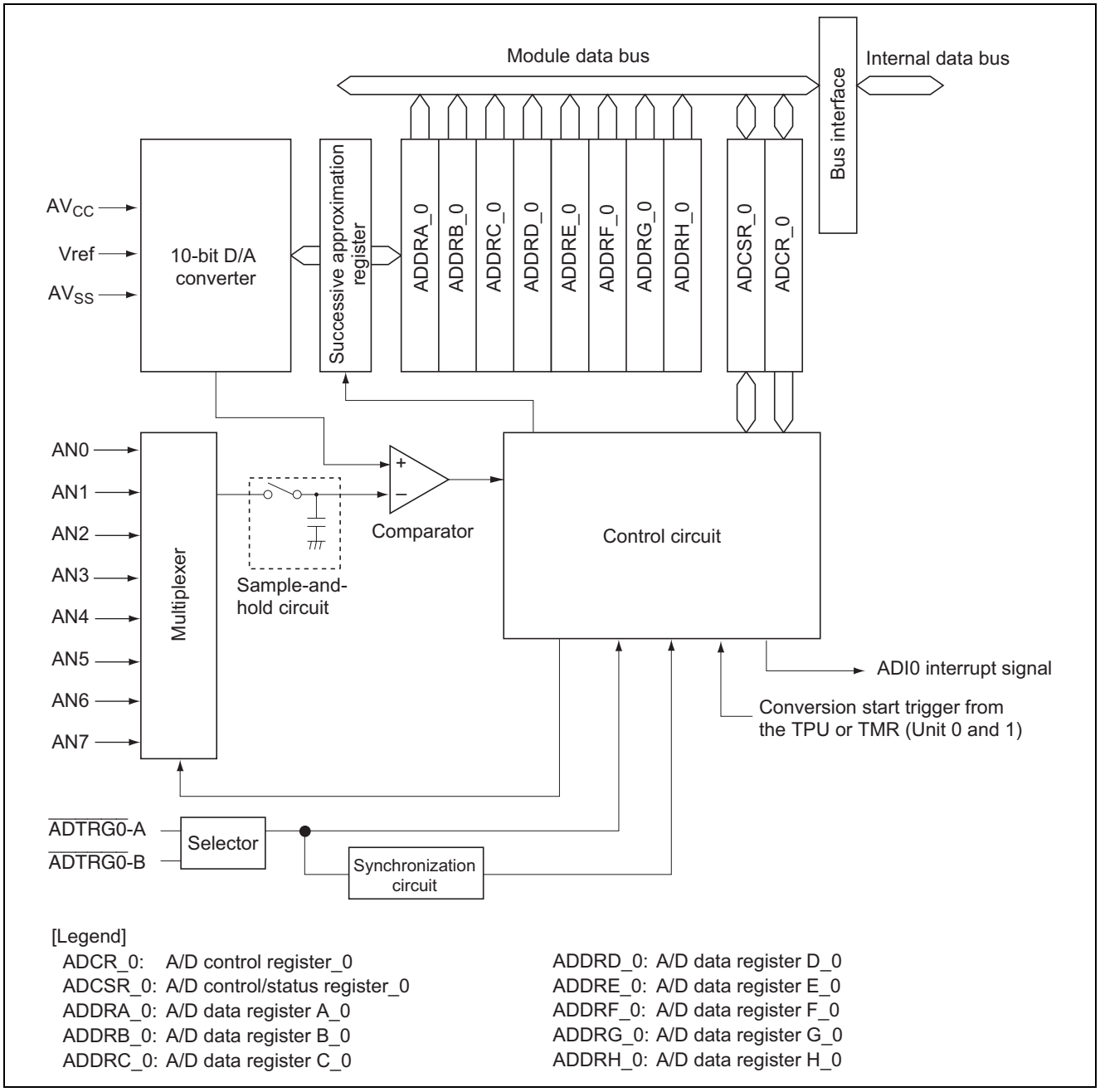


Figure 2 Block Diagram of an A/D Converter (Unit 0/AD_0)

The description which concerns the blocks shown in figure 2 is stated below.

- A/D control register_0 (ADCR_0)
  ADCR_0 enables A/D conversion to be started by an external trigger input.
- A/D control/status register_0 (ADCSR_0)
  ADCSR_0 controls A/D conversion operations.
- A/D data register A_0 (ADDRA_0)
- A/D data register B_0 (ADDRB_0)
- A/D data register C_0 (ADDRC_0)
- A/D data register D_0 (ADDRD_0)
  ADDRA_0 to ADDRD_0 are 16-bit read-only registers for storing the results of A/D conversion. The 10 bits of data produced by conversion are stored in bits 15 to 6. The six lower-order-bits of data are always read as 0.

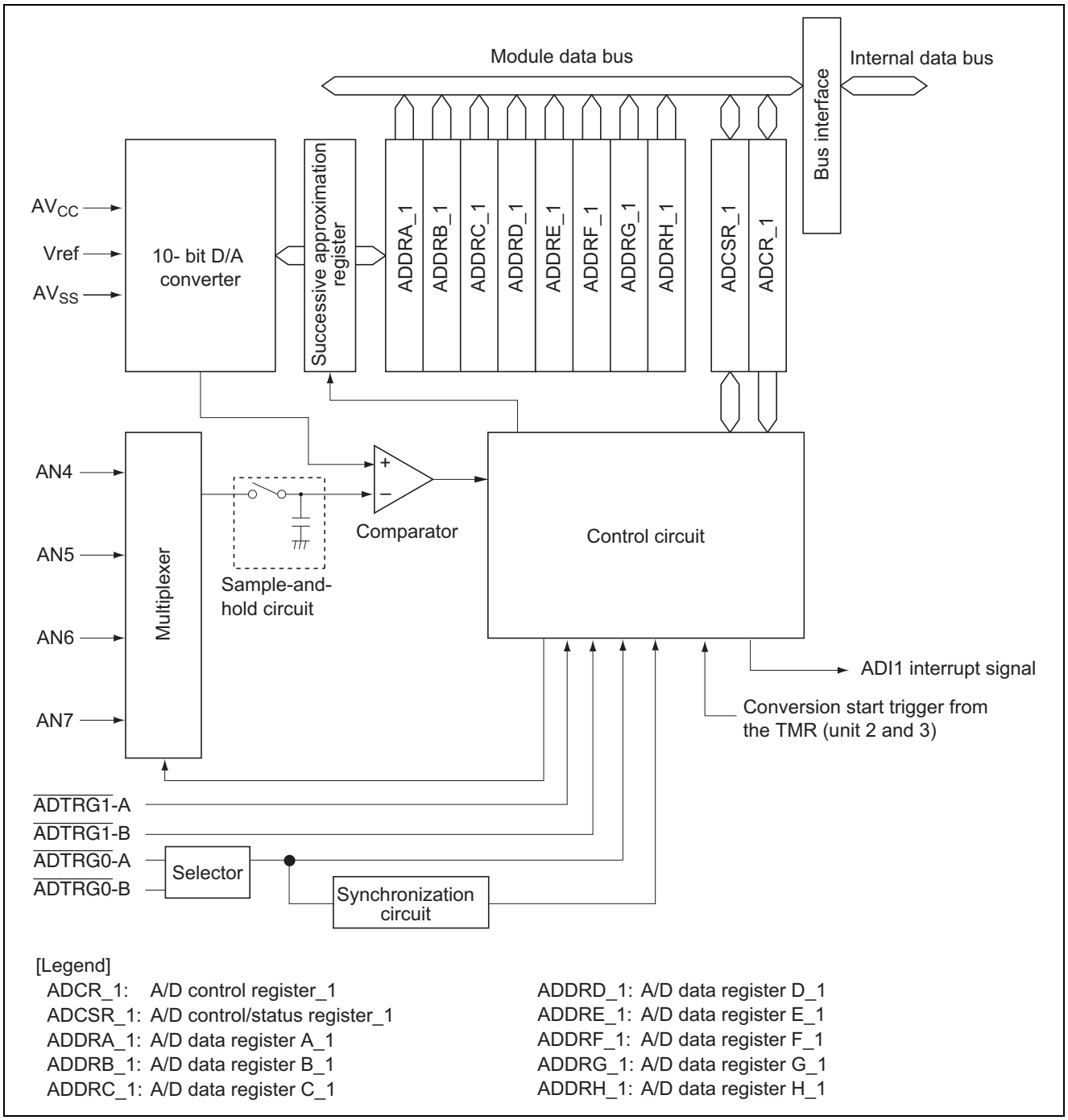


Figure 3 Block Diagram of an A/D Converter (Unit 1/AD_1)

The description which concerns the blocks shown in figure 3 is stated below.

- A/D control register_1 (ADCR_1)
  ADCR_1 enables A/D conversion to be started by an external trigger input.
- A/D control/status register_1 (ADCSR_1)
  ADCSR_1 controls A/D conversion operations.
- A/D data register E_1 (ADDRE_1)
- A/D data register F_1 (ADDRF_1)
- A/D data register G_1 (ADDRG_1)
- A/D data register H_1 (ADDRH_1)
  ADDRE_1 to ADDRH_1 are 16-bit read-only registers for storing the results of A/D conversion. The 10 bits of data produced by conversion are stored in bits 15 to 6. The six lower-order-bits of data are always read as 0.

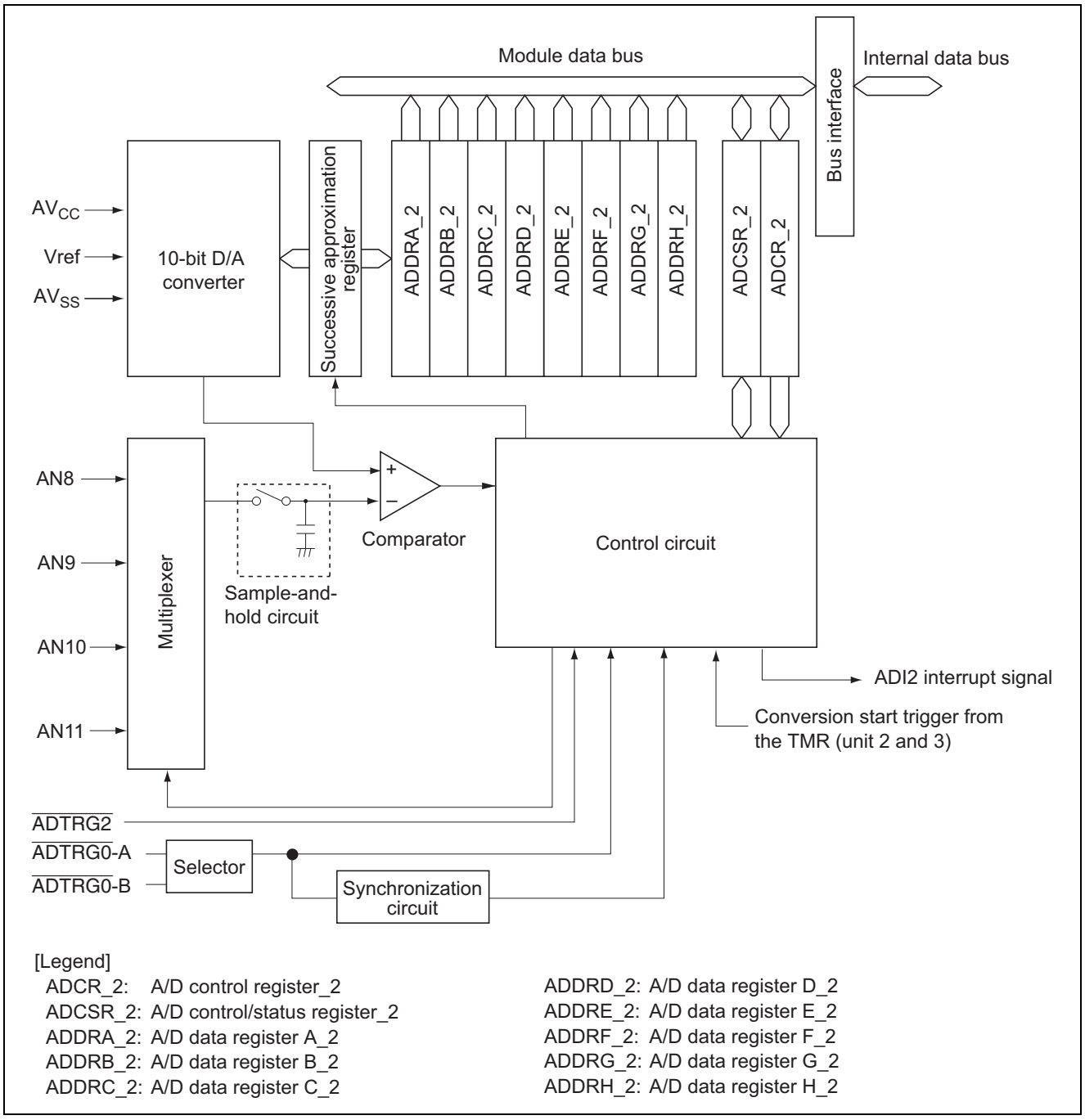


Figure 4 Block Diagram of an A/D Converter (Unit 2/AD_2)

The description which concerns the blocks shown in figure 4 is stated below.

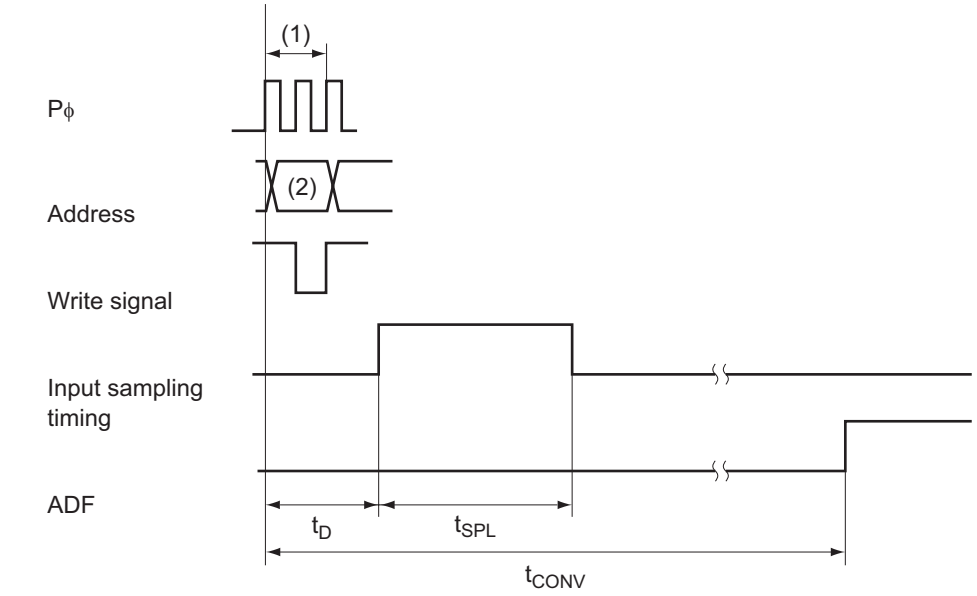
- A/D control register_2 (ADCR_2)
  ADCR_2 enables A/D conversion to be started by an external trigger input.
- A/D control/status register_2 (ADCSR_2)
  ADCSR_1 controls A/D conversion operations.
- A/D data register A_2 (ADDRA_2)
- A/D data register B_2 (ADDRB_2)
- A/D data register C_2 (ADDRC_2)
- A/D data register D_2 (ADDRD_2)
  ADDRA_2 to ADDRD_2 are 16-bit read-only registers for storing the results of A/D conversion. The 10 bits of data produced by conversion are stored in bits 15 to 6. The six lower-order-bits of data are always read as 0.

3.1.2 Setting of A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit. The A/D converter samples the analog input when the A/D conversion start delay time (t_D) passes after the ADST bit in ADCSR is set to 1, then starts A/D conversion. Figure 5 shows the A/D conversion timing. Tables 2 and 3 indicate the A/D conversion time.

As indicated in figure 5, the A/D conversion time (t_{CONV}) includes t_D and the input sampling time (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCSR. The total conversion time therefore varies within the ranges indicated in tables 2 and 3.

In scan mode, the values given in tables 2 and 3 apply to the first conversion time. The values given in table 4 apply to the second and subsequent conversions. In either case, bits CKS1 and CKS0 in ADCR should be set so that the conversion time is within the ranges indicated by the A/D conversion characteristics.



[Legend]
(1): ADCSR write cycle
(2): ADCSR address
t_D: A/D conversion start delay time
t_{SPL}: Input sampling time
t_{CONV}: A/D conversion time

Figure 5 A/D Conversion Timing

Table 2 A/D Conversion Characteristics (when EXCKS = 0)

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	18	—	33	10	—	17	6	—	9	4	—	5
Input sampling time	t_{SPL}	—	319	—	—	159	—	—	79	—	—	29	—
A/D conversion time	t_{CONV}	515	—	530	259	—	266	131	—	134	67	—	68

Note: Values in the table are the number of cycles.

Table 3 A/D Conversion Characteristics (when EXCKS = 1)

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	3	—	10	3	—	6	3	—	5	3	—	4
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	325	—	332	165	—	168	85	—	87	45	—	46

Note: Values in the table are the number of cycles.

Table 4 A/D Conversion Time (Scan Mode)

EXCKS*	**CKS1**	**CKS0**	**Conversion Time (Number of Cycles)**
0	0	0	512 (fixed)
		1	256 (fixed)
	1	0	128 (fixed)
		1	64 (fixed)
1	0	0	320 (fixed)
		1	160 (fixed)
	1	0	80 (fixed)
		1	40 (fixed)

Note: * The EXCKS bit setting is only available for units 1 and 2.

3.1.3 Correspondence between Analog Input Channels and A/D Data Registers (ADDR)

The ADDRx registers are 16-bit read-only registers which are used to store the results of A/D conversion.
The correspondence between analog input channels and ADDRx differs with the settings of SCANE and SCANS in ADCR and CH3 to 0 in ADCSR. Table 5 shows the correspondence between analog input channels and ADDRx when each unit is set to operate in 4-channele scan mode.

Table 5 Correspondence between Analog Input Channels and A/D Data Registers*

Unit of A/D Converter	Analog Input Channel	A/D Data Register
Unit 0	AN0	ADDRA_0
	AN1	ADDRB_0
	AN2	ADDRC_0
	AN3	ADDRD_0
Unit 1	AN4	ADDRE_1
	AN5	ADDRF_1
	AN6	ADDRG_1
	AN7	ADDRH_1
Unit 2	AN8	ADDRA_2
	AN9	ADDRB_2
	AN10	ADDRC_2
	AN11	ADDRD_2

Note: * Setting conditions for A/D converters
SCANE and SCANS in ADCR_0, ADCR_1, and ADCR_2 = 1, 0
CH3 to 0 in ADCSR_0 = B'0011
CH3 to 0 in ADCSR_1 = B'0111
CH3 to 0 in ADCSR_2 = B'1011

3.2 DMAC Functions

A block diagram of the DMAC is given in figure 6.

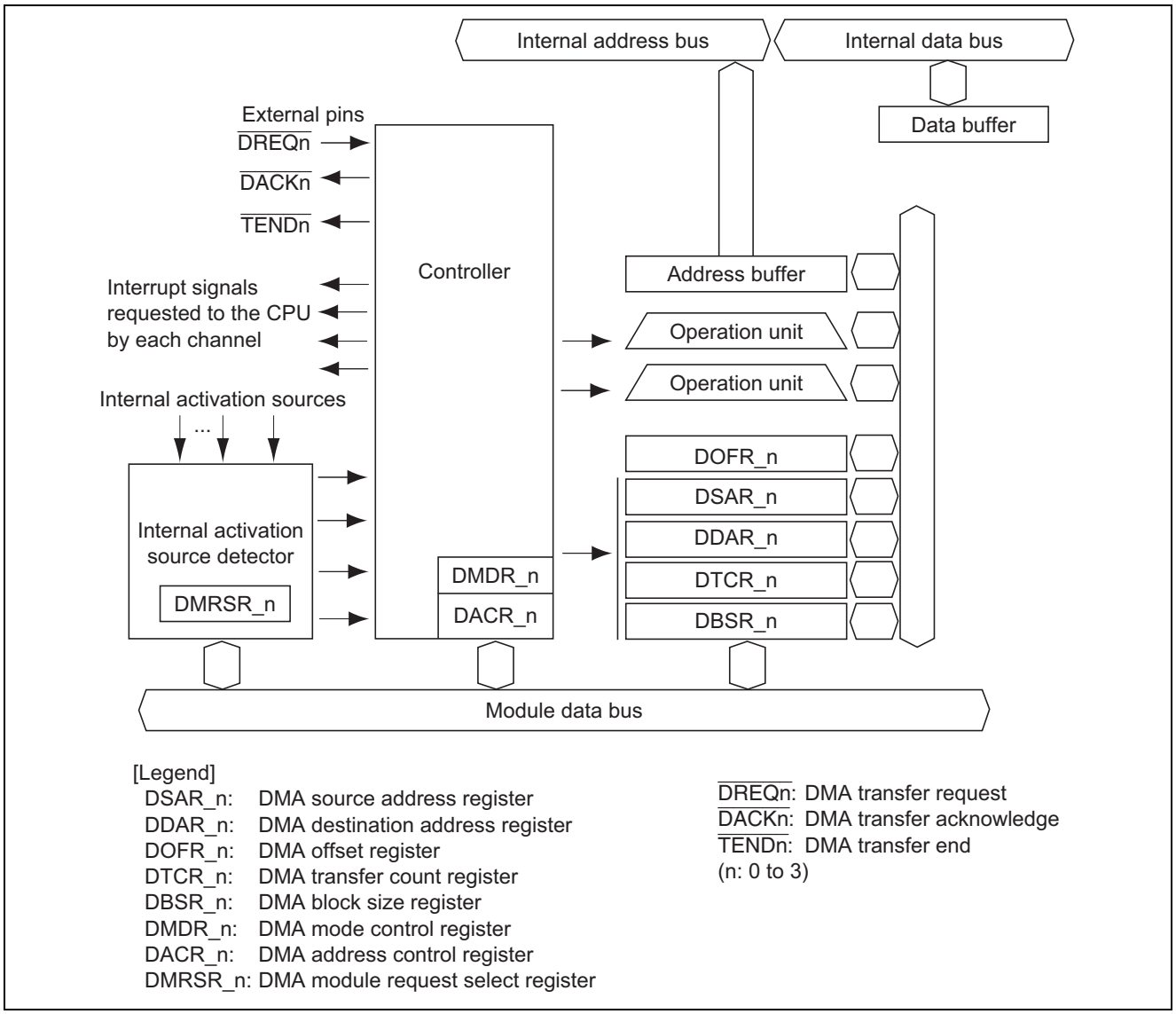


Figure 6 Block Diagram of DMAC

The description with reference to figure 6 is stated below.

- DMA source address register _n (DSAR_n)
  DSAR_n is a 32-bit readable/writable register and specifies the source address for the transfer. Each register is equipped with an address-updating function, so the source address is updated to that for the next transfer each time a transfer operation takes place.
- DMA destination address register _n (DDAR_n)
  DDAR_n is a 32-bit readable/writable register and specifies the destination address for the transfer. Each register is equipped with an address-updating function, so the destination address is updated to that for the next transfer each time a transfer operation takes place.
- DMA offset register _n (DOFR_n)
  DOFR_n is a 32-bit readable/writable register that specifies the offset for updating of the source and destination addresses.
- DMA transfer count register_n (DTCR_n)
  DTCR_n is a 32-bit readable/writable register that specifies the size of data to be transferred (total transfer size). The value corresponding to its data access size is subtracted every time data is transferred.
- DMA block size register_n (DBSR_n)
  DBSR_n specifies the repeat size or block size. DBSR_n is enabled in repeat transfer mode and block transfer mode and is disabled in normal transfer mode.
- DMA mode control register _n (DMDR_n)
  DMDR_n controls DMAC operation.
- DMA address control register_n (DACR_n)
  DACR_n sets the operating mode and transfer method.
- DMA module request select register_n (DMRSR_n)
  DMRSR_n is an 8-bit readable/writable register that specifies the on-chip module interrupt source.

4. Principles of Operation

4.1 Outline of High-Speed Sampling Timing for A/D Conversion

Examples of the timing when one A/D converter unit and three A/D converter units are in use are illustrated in figures 7 and 8, respectively. Using three A/D converter units accelerates the speed of sampling so that the sampling interval is one-third of that for a single unit.

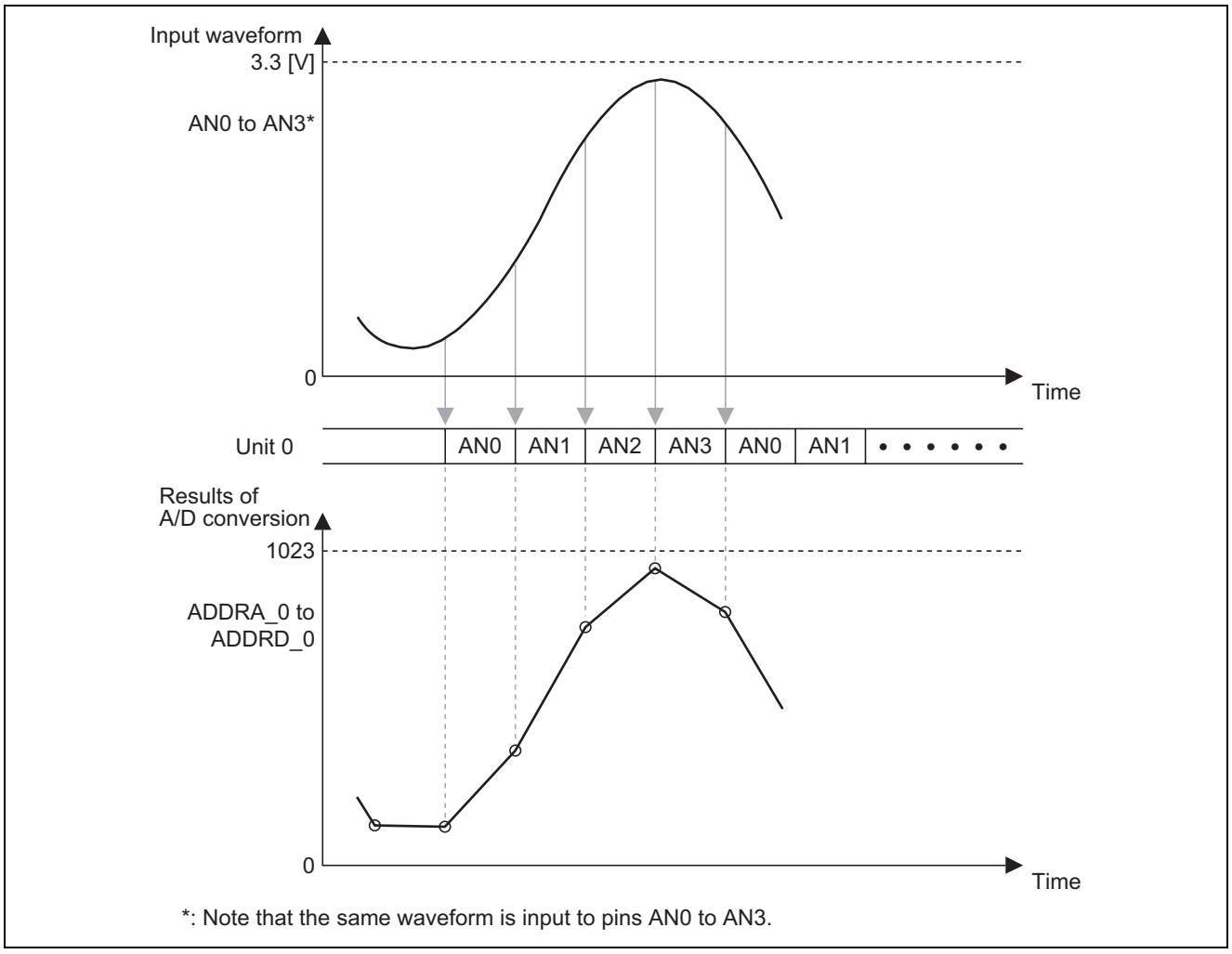


Figure 7 Example of Sampling when One A/D Converter Unit is Used

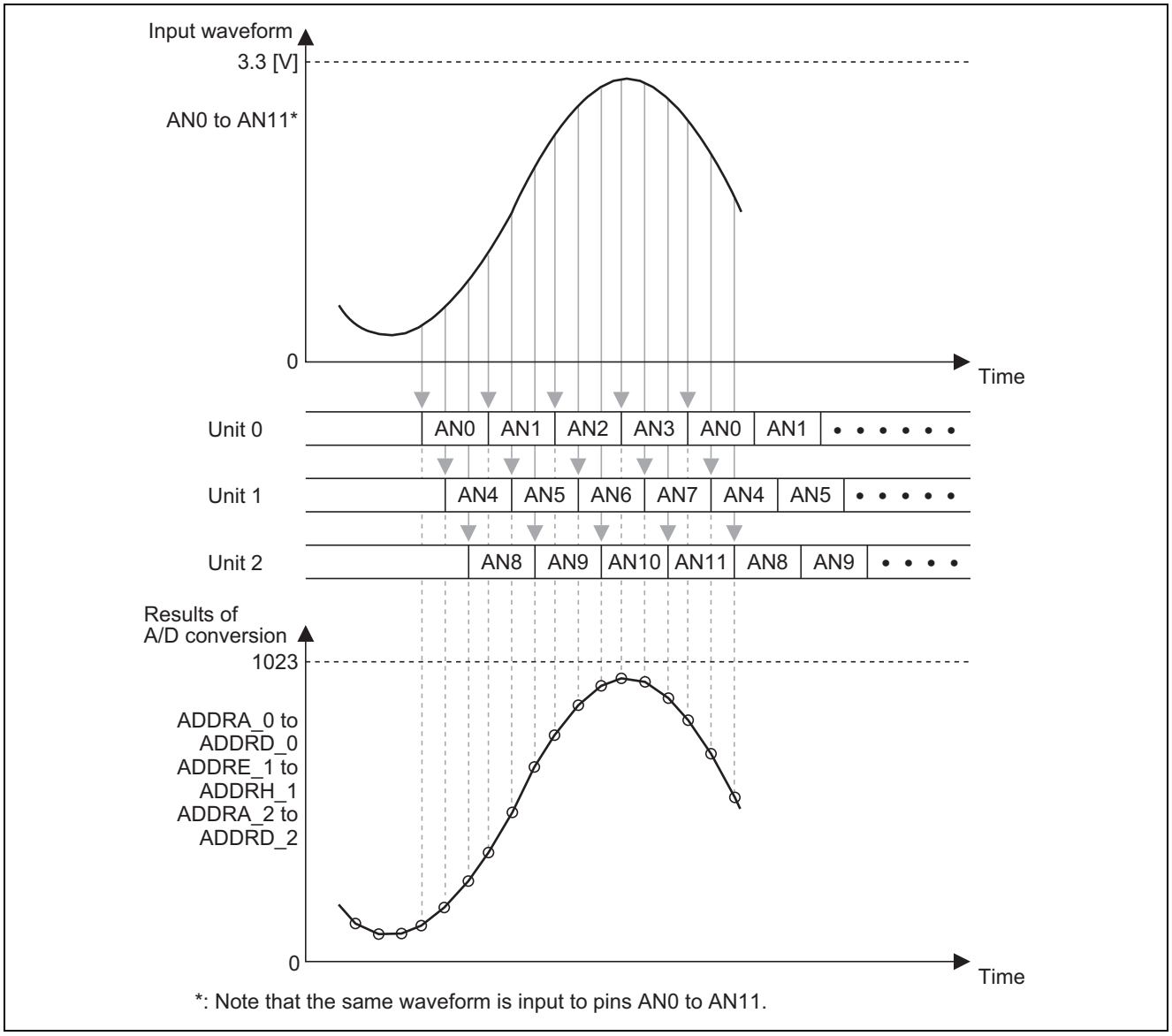


Figure 8 Example of Sampling when Three A/D Converter Units are Used

4.2 A/D Conversion Time

In this sample task, setting conditions are as follows: Pϕ 1 cycle = 0.04 µs, EXCKS = 0, CKS1 = 1, and CKS0 = 1. In this case the A/D conversion times are as listed below. The EXCKS bit setting is only available for units 1 and 2.

First conversion time (min.):	67 cycles × 0.04 µs = 2.68 µs
(max.):	68 cycles × 0.04 µs = 2.72 µs
Second and subsequent conversion:	64 cycles × 0.04 µs = 2.56 µs
(Refer to tables 2 to 4.)	

As is described above, the time for the first conversion varies. Use the times for second and subsequent conversions as a reference.

Realization of high-speed sampling requires simultaneous operation of three A/D converter units and equal sampling periods.

Since the time for second and subsequent conversions is 2.56 µs,

activation interval of each-unit A/D converter: 2.56 µs/3 ≈ 0.853 µs.

Since the software processing time: Iϕ1 cycle = 0.02 when Iϕ = 50 MHz,

number of Iϕ cycles = 0.853 µs / 0.02 µs = 42.65.

Therefore, since the number of Iϕ cycles = 43 in this sample task,

activation interval for each-A/D converter unit: 0.02 µs × 43 cycles = 0.86 µs.

As a result, A/D conversion intervals between the respective pairs of units are set as follows:

A/D conversion interval between unit 0 and unit 1:	0.86 µs*
A/D conversion interval between unit 1 and unit 2:	0.86 µs*
A/D conversion interval between unit 2 and unit 0:	0.84 µs*
	(2.56 µs – 0.86 µs – 0.86 µs = 0.84 µs).

Note: * Sampling intervals in this sample task are not even.

4.3 Timing of High-Speed Sampling Operation in Simultaneous Using of 3-Unit A/D Converters

Figure 9 illustrates the timing of high-speed sampling operation with three A/D converter units. Table 6 is a list of the hardware and software processing at the numbered points in figure 9.

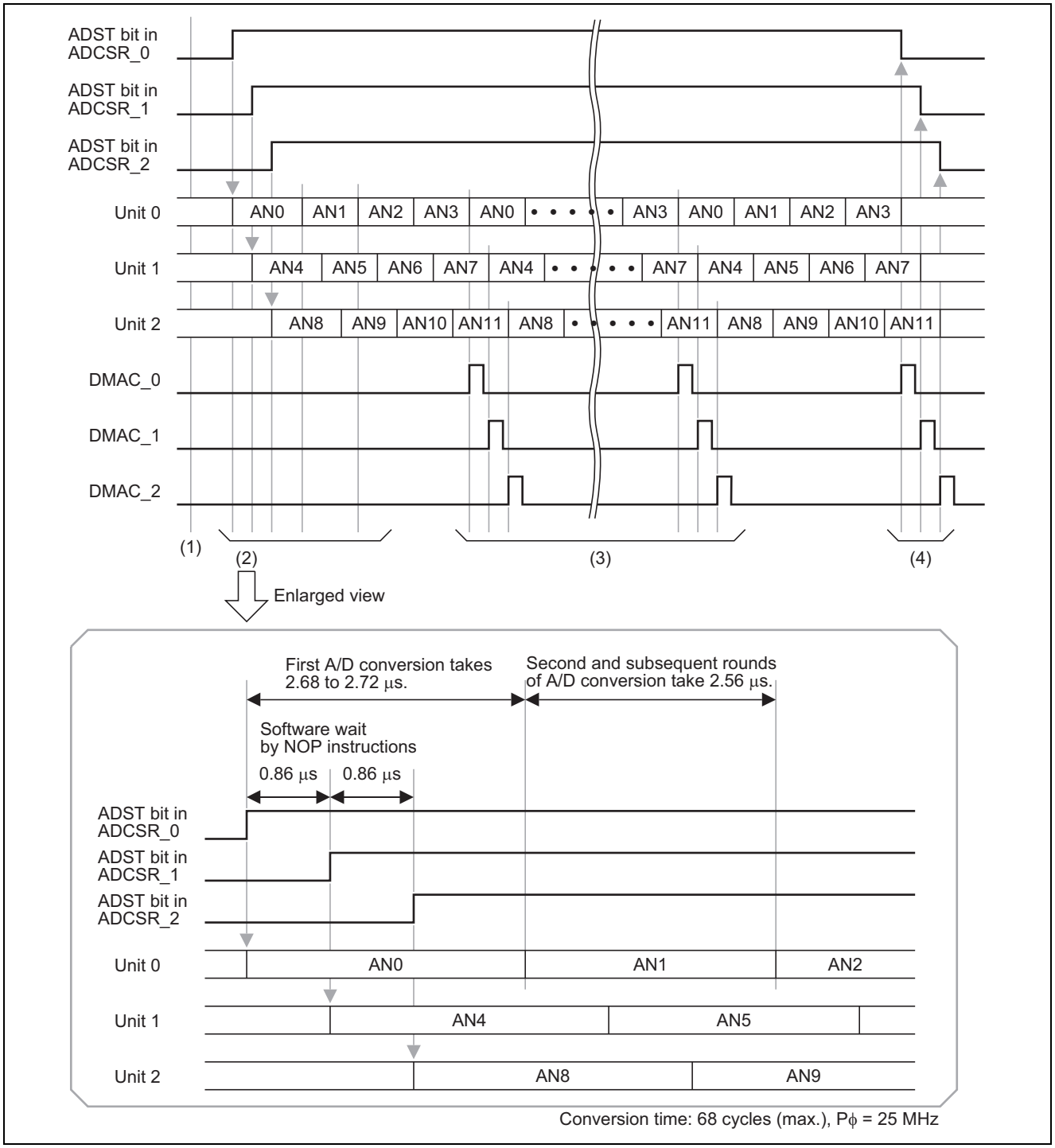


Figure 9 Timing of High-Speed Sampling Operation in Simultaneous Use of Three A/D Converter Units

Table 6 Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings*
(2)	None	Use NOP instructions to adjust the timing of the start of A/D conversion, and activate A/D_0, 1, and 2 in sequence with an interval of 0.86 µs.
(3)	Transfer on DMAC_0 to 2 a. ADI0–2 interrupts from the A/D converter activate DMAC_0–2, which transfers A/D-converted data from ADDRx to on-chip RAM.	None
(4)	DMAC_0–2 transfer a. ADI0–2 interrupts from the A/D converter activate DMAC_0–2, which transfers A/D-converted data from ADDRx to on-chip RAM. b. End of DMAC_0–2 transfer	DMAC0–2 transfer end interrupt a. Disable DMAC0–2 transfer end interrupt requests. b. Stop A/D conversion by clearing ADST in ADCSR_0–2 to 0. c. Disable A/D conversion end interrupt.

Notes: * Initial settings

DMAC_0–2 settings

a. Source for DMAC_0–2 activation: A/D_0–2 conversion end interrupts.
b. Source address: First address of the A/D data registers.
c. Destination address: First address of the destination area for data transfer in on-chip RAM.
d. Block transfer mode: Block size of data is four words.
e. Offset transfer: Offset value is six bytes (three words).
f. Since the DTE bit in DMDR = 1, DMAC transfer is enabled.

A/D converter settings

a. Enable A/D conversion end interrupt requests.
b. Set to the scan mode: continuous A/D conversion on 4 channels.
c. Set the A/D conversion time to 68 cycles (max.), ADCLK = Pϕ/1 = 25 MHz.
d. End of A/D conversion

5. Description of Software

5.1 Operating Environment

Table 7 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.02.00
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.03 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 8 Section Setting

Address	Section Name	Description
H'001000	P	Program area
H'FEE000	B	Non-initialized data area (RAM area)

Table 9 Vector Table for Interrupt Exception Handling

Exception Handling Source		Vector No.	Vector Address	Function to Interrupt Destination
Reset		0	H'000000	init
DMAC_0	DMTEND0	128	H'000202	dmtend0_int
DMAC_1	DMTEND1	129	H'000204	dmtend1_int
DMAC_2	DMTEND2	130	H'000206	Dmtend2_int

5.2 List of Functions

Table 10 lists the functions used in this sample task. Figure 10 shows the structure of hierarchy.

Table 10 List of Functions

Function Name	Description
init	Initialization routine: Takes the chip out of module stop mode, performs clock settings, and calls the main function.
main	Main routine Handles software control of the timing of the start of A/D conversion by each A/D converter unit. Sets up DMAC activation by A/D conversion end interrupts as the means for A/D data transfer to on-chip RAM.
dmtend0_int	DMAC_0 transfer end interrupt Starts interrupt processing after transfer of A/D converted data to on-chip RAM a specified number of times. Sets DMAC_0 transfer end interrupt requests, A/D unit 0 conversion, and ADI0 interrupts disabled.
dmtend1_int	DMAC_1 transfer end interrupt Starts interrupt processing after transfer of A/D converted data to on-chip RAM a specified number of times. Sets DMAC_1 transfer end interrupt requests, A/D unit 1 conversion, and ADI1 interrupts disabled.
dmtend2_int	DMAC_2 transfer end interrupt Starts interrupt processing after transfer of A/D converted data to on-chip RAM a specified number of times. Sets DMAC_2 transfer end interrupt requests, A/D unit 2 conversion, and ADI2 interrupts disabled.

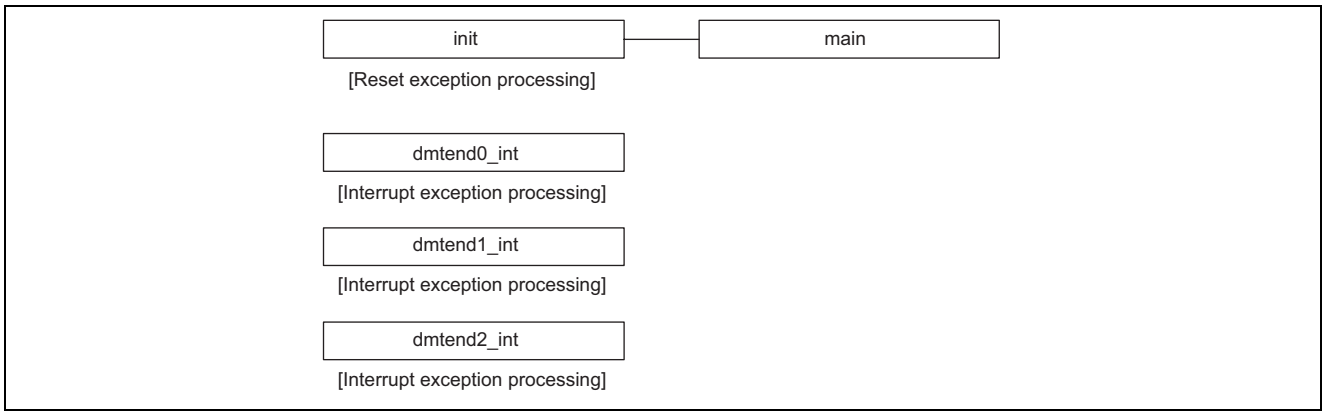


Figure 10 Hierarchy of Calls in the User Program

5.3 Symbolic Constants

Table 11 Symbolic Constants

Constant Name	Setting	Description
UNIT	3	Number of units to handle A/D conversion
SIZE	2	Data size of ADDRx: 16 bits = 2 bytes
CNT	6	Number of times for scan-mode A/D conversion
SCAN	4	Number of channels for A/D conversion in scan mode

5.4 RAM Usage

Table 12 RAM Usage

Type	Variable Name	Description	Used in
unsigned short	scn[SCAN*CNT][UNIT]	Destination area for transfer of A/D conversion results SCAN × CNT × UNIT = 4 × 6 × 3 = 72 words = 144 bytes	main

5.5 Description of Functions

5.5.1 init Function

1. Functional overview
   Initialization routine. (Releases the required modules from module stop mode, makes clock settings, and calls the main function.)
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 13). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD2 to MD0.

Table 13 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
3	0	1	1	0	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock signal,
8	ICK0	0	R/W	which is provided to the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	0	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

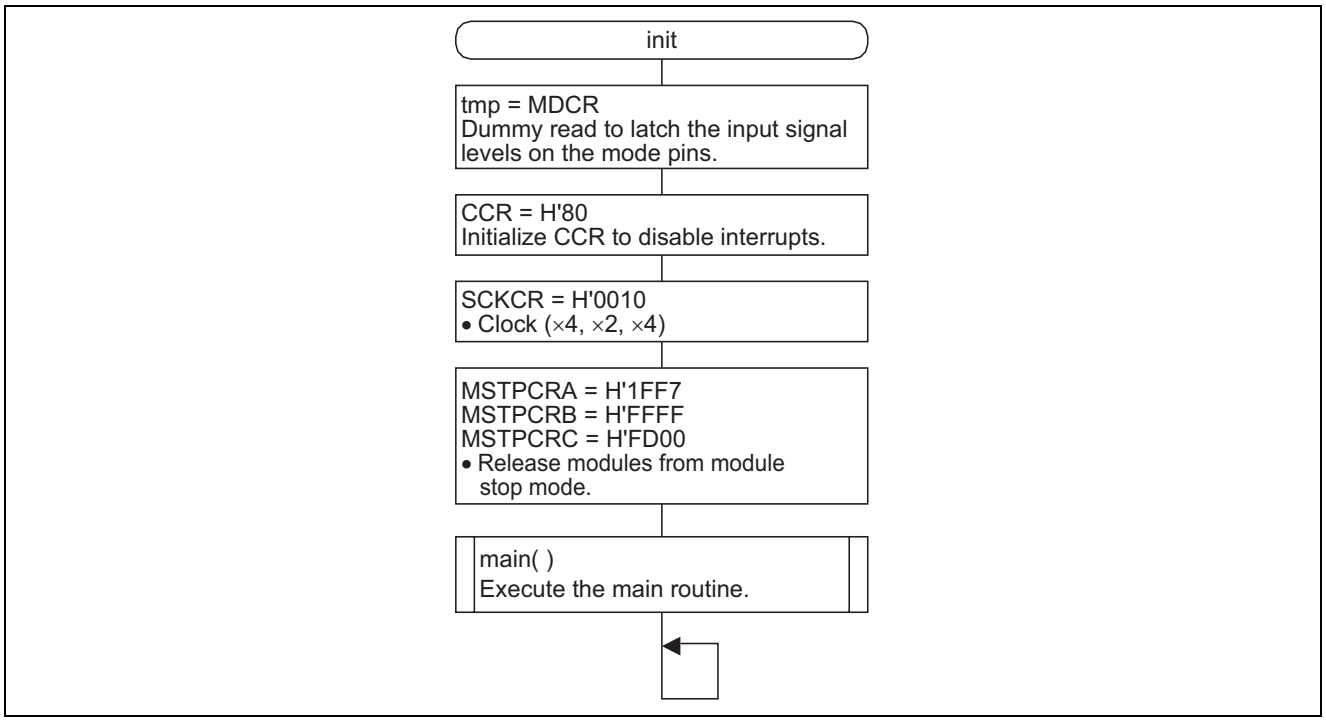
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG_0: PO15 to PO0)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)
5	MSTPB5	1	R/W	User break controller (UBC)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	I^2C bus interface 2_3, 2_2 (IIC2_3/IIC2_2)
10	MSTPC10	1	R/W	Cyclic redundancy check module
9	MSTPC9	0	R/W	10-bit A/D converter (unit 2/1)
8	MSTPC8	1	R/W	Programmable pulse generator (PPG_1: PO31 to PO16)
7	MSTPC7	0	R/W	• For 56 KB of on-chip RAM: On-chip RAM_6 (H'FEE000 to H'FEFFFF) • For 40 KB of on-chip RAM: Reserved bits Be sure to always set MSTPC7 and MSTPC6 to the same value.
6	MSTPC6	0	R/W	
5	MSTPC5	0	R/W	• For 56 KB of on-chip RAM: On-chip RAM_5 and _4 (H'FF0000 to H'FF3FFF) • For 40 KB of on-chip RAM: On-chip RAM_4 (H'FF2000 to H'FF3FFF) Be sure to always set MSTPC5 and MSTPC4 to the same value.
4	MSTPC4	0	R/W	
3	MSTPC3	0	R/W	On-chip RAM_3 and _2 (H'FF4000 to H'FF7FFF) Be sure to always set MSTPC3 and MSTPC2 to the same value.
2	MSTPC2	0	R/W	
1	MSTPC1	0	R/W	On-chip RAM_1 and _0 (H'FF8000 to H'FFBFFF) Be sure to always set MSTPC1 and MSTPC0 to the same value.
0	MSTPC0	0	R/W	

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize CCR to disable interrupts.
SCKCR = H'0010
• Clock (×4, ×2, ×4)
MSTPCRA = H'1FF7
MSTPCRB = H'FFFF
MSTPCRC = H'FD00
• Release modules from module stop mode.
main( )
Execute the main routine.

5.5.2 main Function

1. Functional overview
   Main routine. (Handles software control of the timing of the start of A/D conversion by each A/D converter unit. Sets up DMAC activation by A/D conversion end interrupts as the means for transferring A/D data to on-chip RAM.)
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- DMA source address register_0 (DSAR_0) Number of bits: 32 Address: H'FFFC00
  Function: DSAR_0 specifies the transfer source address.
  Setting: Address of ADDRA_0

- DMA source address register_1 (DSAR_1) Number of bits: 32 Address: H'FFFC20
  Function: DSAR_1 specifies the transfer source address.
  Setting: Address of ADDRE_1

- DMA source address register_2 (DSAR_2) Number of bits: 32 Address: H'FFFC40
  Function: DSAR_2 specifies the transfer source address.
  Setting: Address of ADDRA_2

- DMA destination address register_0 (DDAR_0) Number of bits: 32 Address: H'FFFC04
  Function: DDAR_0 specifies the transfer destination address.
  Setting: Address of scn[0][0]

- DMA destination address register_1 (DDAR_1) Number of bits: 32 Address: H'FFFC24
  Function: DDAR_1 specifies the transfer destination address.
  Setting: Address of scn[0][1]

- DMA destination address register_2 (DDAR_2) Number of bits: 32 Address: H'FFFC44
  Function: DDAR_2 specifies the transfer destination address.
  Setting: Address of scn[0][2]

- DMA transfer count register_0 (DTCR_0) Number of bits: 32 Address: H'FFFC0C
  Function: DTCR_0 specifies the size of data to be transferred.
  Setting: SIZE × CNT × SCAN = 2 × 6 × 4 = 48

- DMA transfer count register_1 (DTCR_1) Number of bits: 32 Address: H'FFFC2C
  Function: DTCR_1 specifies the size of data to be transferred.
  Setting: SIZE × CNT × SCAN = 2 × 6 × 4 = 48

- DMA transfer count register_2 (DTCR_2) Number of bits: 32 Address: H'FFFC4C
  Function: DTCR_2 specifies the size of data to be transferred.
  Setting: SIZE × CNT × SCAN = 2 × 6 × 4 = 48

- DMA offset register_0 (DOFR_0) Number of bits: 32 Address: H'FFFC08
  DMA offset register_1 (DOFR_1) Number of bits: 32 Address: H'FFFC28
  DMA offset register_2 (DOFR_2) Number of bits: 32 Address: H'FFFC48
  Function: DOFRn specifies the offset.
  Setting: SIZE × UNIT = 2 × 3 = 6

- DMA block size register_0 (DBSR_0) Number of bits: 32 Address: H'FFFC10
  DMA block size register_1 (DBSR_1) Number of bits: 32 Address: H'FFFC30
  DMA block size register_2 (DBSR_2) Number of bits: 32 Address: H'FFFC50
  Function: DBSRn specifies the block size in block transfer mode. When the data-access size is specified as "word", and DBSR_1 = H'00040004, the block size is 4 words (8 bytes).
  Setting: SCAN × H'10000 + SCAN = 4 × H'10000 + 4 = H'00040004

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14
- DMA mode control register_1 (DMDR_1) Number of bits: 32 Address: H'FFFC34
- DMA mode control register_2 (DMDR_2) Number of bits: 32 Address: H'FFFC54

Bit	Bit Name	Setting	R/W	Description
31	DTE	0/1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.
16	DTIF	Undefined	R/(W)*	Data Transfer Interrupt Flag Indicates that a transfer end interrupt by the transfer counter has been requested. 0: A transfer end interrupt by the transfer counter has not been requested 1: A transfer end interrupt by the transfer counter has been requested [Clearing conditions] • Writing of 1 to DTE • Writing of 0 to DTIF after having read DTIF = 1 [Setting condition] • Completion of transfer after DTCR = 0
15 14	DTSZ1 DTSZ0	0 1	R/W R/W	Data Access Size 1 and 0 Selects the data access size to be transferred. 01: Data access size for transfer is in words (16 bits).
13 12	MDS1 MDS0	0 1	R/W R/W	Transfer Mode Select 1 and 0 01: Block transfer mode
8	DTIE	1	R/W	Data Transfer End Interrupt Enable Enables/disables a transfer end interrupt request by the transfer counter. When the DTIF bit is set to 1 with this bit set to 1, a transfer end interrupt is requested to the CPU or DTC. The transfer end interrupt request is cleared by clearing this bit or the DTIF bit to 0. 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.
7 6	DTF1 DTF0	1 0	R/W R/W	Data Transfer Factor 1 and 0 Selects a DMAC activation source. When the source is to be an on-chip module interrupt, the source must also be selected in DMRSR. 10: On-chip module interrupt
5	DTA	1	R/W	Data Transfer Acknowledge This bit is valid in DMA transfer activated by an on-chip module interrupt source. This bit enables or disables clearing of the source flag selected by DMRSR. 0: Disables clearing of the on-chip module interrupt source that activates DMA transfer. Since the on-chip module interrupt source is not cleared by DMA transfer, it should be cleared by the CPU or DTC transfer. 1: Enables clearing of the on-chip module interrupt source that activates DMA transfer. Since the on-chip module interrupt source is cleared by DMA transfer, interrupt generation for the CPU or for DTC transfer is not required.

Note: * Only 0 can be written here, to clear the flag.

- DMA address control register_0 (DACR_0) Number of bits: 32 Address: H'FFFC18
- DMA address control register_1 (DACR_1) Number of bits: 32 Address: H'FFFC38
- DMA address control register_2 (DACR_2) Number of bits: 32 Address: H'FFFC58

Bit	Bit Name	Setting	R/W	Description
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
25	ARS1	0	R/W	Area Select 1 and 0
24	ARS0	0	R/W	00: The block area or repeat area is on the source address side.
21	SAT1	1	R/W	Source Address Update Mode 1 and 0
20	SAT0	0	R/W	10: Increments the source address.
17	DAT1	0	R/W	Destination Address Update Mode 1 and 0
16	DAT0	1	R/W	01: The relevant offset is added to the destination address.

- DMA module request select register_0 (DMRSR_0) Number of bits: 8 Address: H'FFFD20
  Function: The source of on-chip module interrupts which activate the DMAC is specified in DMRSR_0.
  Setting: 86 (ADI0)

- DMA module request select register_1 (DMRSR_1) Number of bits: 8 Address: H'FFFD21
  Function: The source of on-chip module interrupts which activate the DMAC is specified in DMRSR_1.
  Setting: 237 (ADI1)

- DMA module request select register_2 (DMRSR_2) Number of bits: 8 Address: H'FFFD22
  Function: The source of on-chip module interrupts which activate the DMAC is specified in DMRSR_2.
  Setting: 232 (ADI2)

- A/D control/status register_0 (ADCSR_0) Number of bits: 8 Address: H'FFFFA0

Bit	Bit Name	Setting	R/W	Description
7	ADF	0	R/(W)*	A/D End Flag 0: A/D conversion is in progress. 1: A/D conversion has been completed.
6	ADIE	1	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0/1	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.
3	CH3	0	R/W	Channel Select 3 to 0
2	CH2	0	R/W	When SCANE and SCANS in ADCR = B'10,
1	CH1	1	R/W	0011: Analog inputs are AN0 to AN3.
0	CH0	1	R/W	

Note: * Only 0 can be written here, to clear the flag.

- A/D control register_0 (ADCR_0) Number of bits: 8 Address: H'FFFFA1

Bit	Bit Name	Setting	R/W	Description
7	TRGS1	0	R/W	Timer Trigger Select 1 and 0
6	TRGS0	0	R/W	These bits are set together with EXTRGS. TRGS1 and 0 = B'00, EXTRGS = 0: Disables initiation of A/D conversion by an external trigger signal.
5	SCANE	1	R/W	Scan Mode
4	SCANS	0	R/W	10: Scan mode. A/D conversion is performed continuously for channels 1 to 4.
3	CKS1	1	R/W	Clock Select 1 and 0
2	CKS0	1	R/W	11: A/D conversion time = 68 cycles (max.)
0	EXTRGS	0	R/W	Extension Timer Trigger Select For details, refer to the description of bits TRGS1/0.

- A/D control/status register_1 (ADCSR_1) Number of bits: 8 Address: H'FFEAA0

Bit	Bit Name	Setting	R/W	Description
7	ADF	0	R/(W)*	A/D End Flag 0: A/D conversion is in progress. 1: A/D conversion has been completed.
6	ADIE	1	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0/1	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.
4	EXCKS	0	R/W	Extension Clock Select Along with CKS1 and 0 in ADCR, this bit sets the A/D conversion time. For details, refer to the description of ADCR. Writing to EXCKS has to be performed at the same time as writing to CKS1 and 0.
3	CH3	0	R/W	Channel Select 3 to 0
2	CH2	1	R/W	When SCANE and SCANS in ADCR = B'10,
1	CH1	1	R/W	0111: Analog inputs are AN4 to AN7.
0	CH0	1	R/W	

Note: * Only 0 can be written here, to clear the flag.

- A/D control register_1 (ADCR_1) Number of bits: 8 Address: H'FFEAA1

Bit	Bit Name	Setting	R/W	Description
7	TRGS1	0	R/W	Timer Trigger Select 1 and 0
6	TRGS0	0	R/W	These bits are set together with EXTRGS. TRGS1 and 0 = B'00, EXTRGS = 0: Disables initiation of A/D conversion by an external trigger signal.
5	SCANE	1	R/W	Scan Mode
4	SCANS	0	R/W	10: Scan mode. A/D conversion is performed continuously for channels 1 to 4.
3	CKS1	1	R/W	Clock Select 1 and 0
2	CKS0	1	R/W	Writing to CKS1 and 0 has to be performed at the same time as writing to EXCKS in ADCRS. EXCKS = 0, CKS1 and 0 = B'11: A/D conversion time = 68 cycles (max.)
0	EXTRGS	0	R/W	Extension Timer Trigger Select For details, refer to the description of bits TRGS1/0.

- A/D control/status register_2 (ADCSR_2) Number of bits: 8 Address: H'FFEAB0

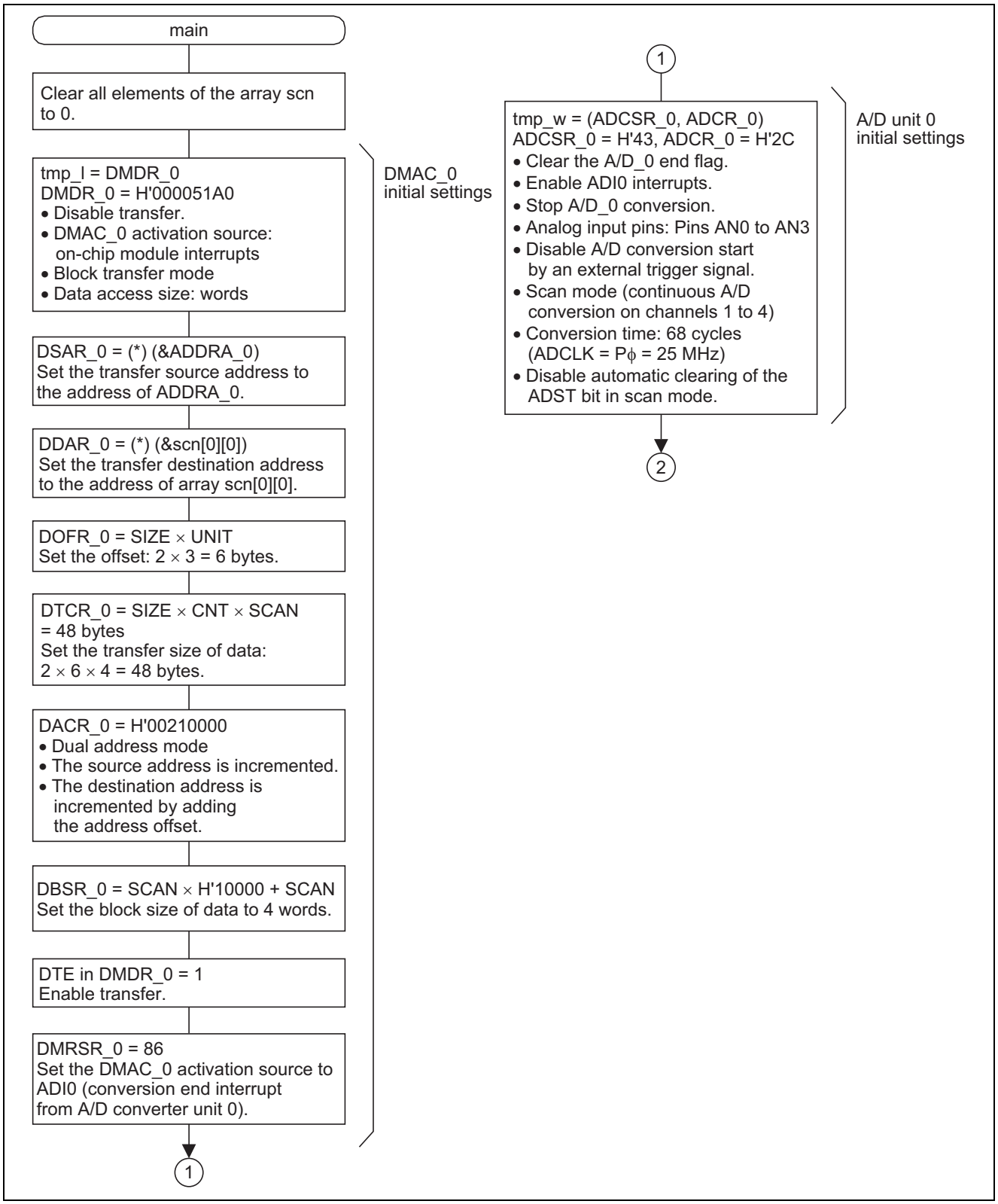
Bit	Bit Name	Setting	R/W	Description
7	ADF	0	R/(W)*	A/D End Flag 0: A/D conversion is in progress. 1: A/D conversion has been completed.
6	ADIE	1	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0/1	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.
4	EXCKS	0	R/W	Extension Clock Select Along with CKS1 and 0 in ADCR, this bit sets the A/D conversion time. For details, refer to the description of ADCR. Writing to EXCKS has to be performed at the same time as writing to CKS1 and 0.
3	CH3	1	R/W	Channel Select 3 to 0
2	CH2	0	R/W	When SCANE and SCANS in ADCR = B'10,
1	CH1	1	R/W	1011: Analog inputs are AN4 to AN7.
0	CH0	1	R/W	

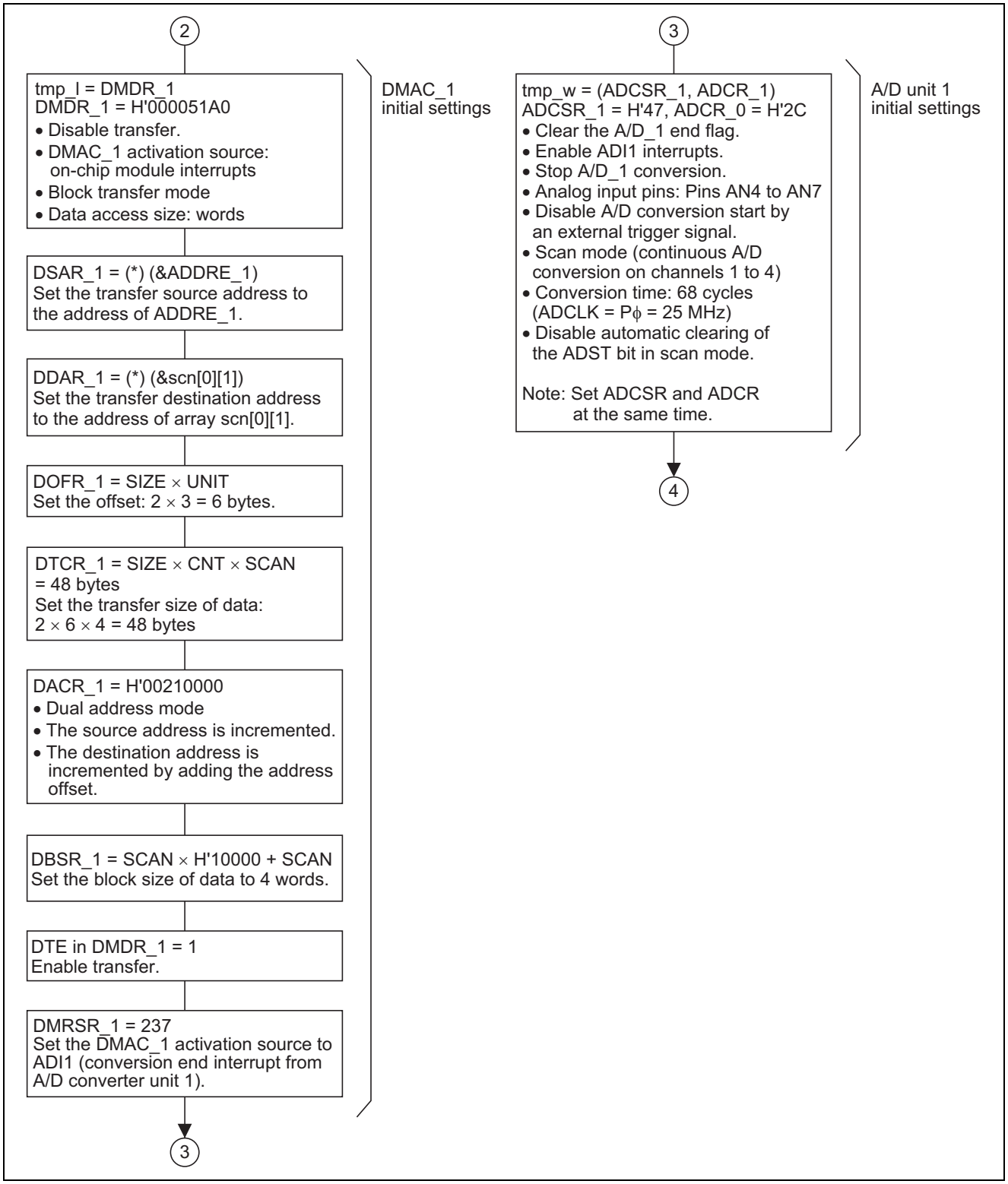
Note: * Only 0 can be written here, to clear the flag.

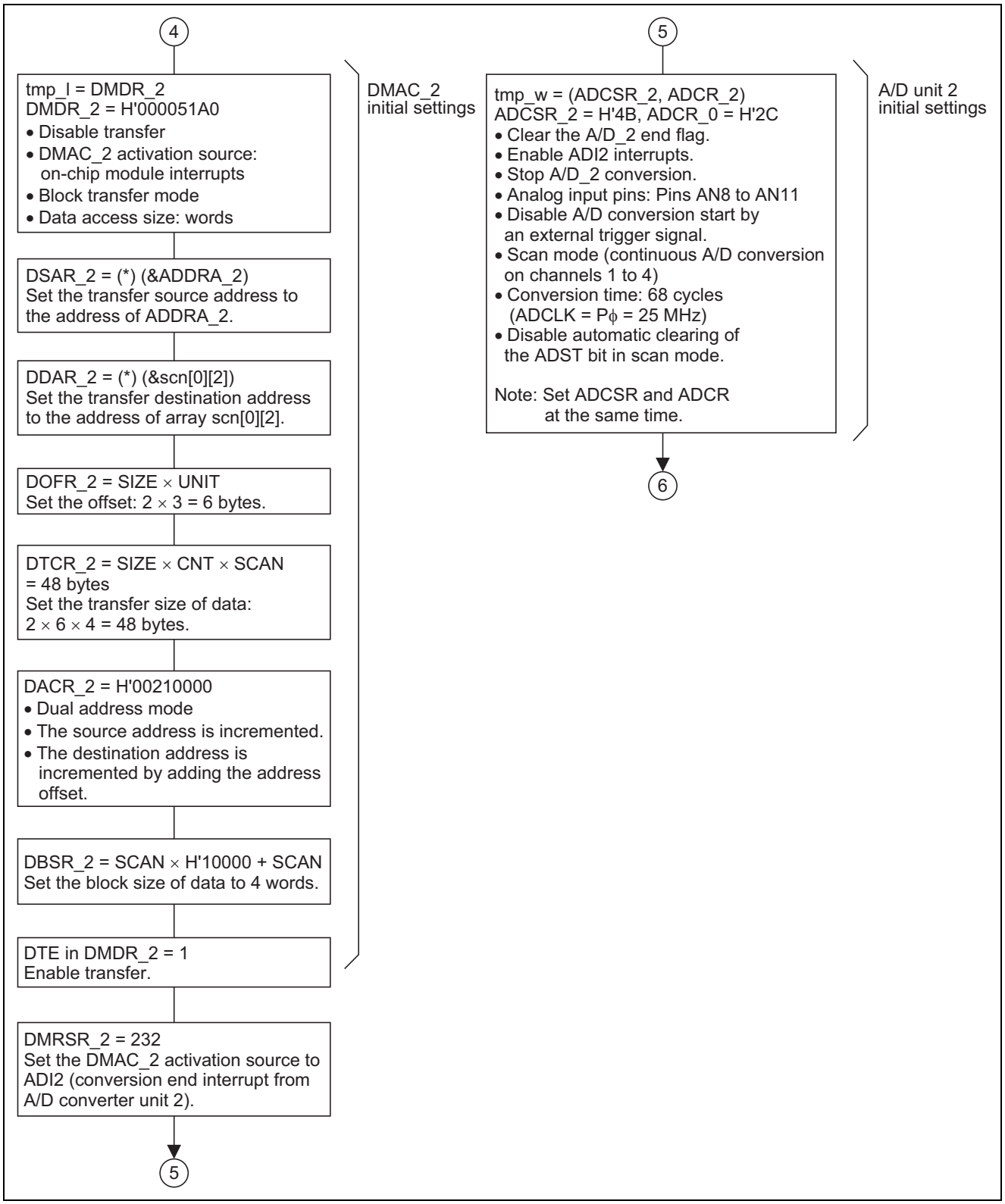
- A/D control register_2 (ADCR_2) Number of bits: 8 Address: H'FFEAB1

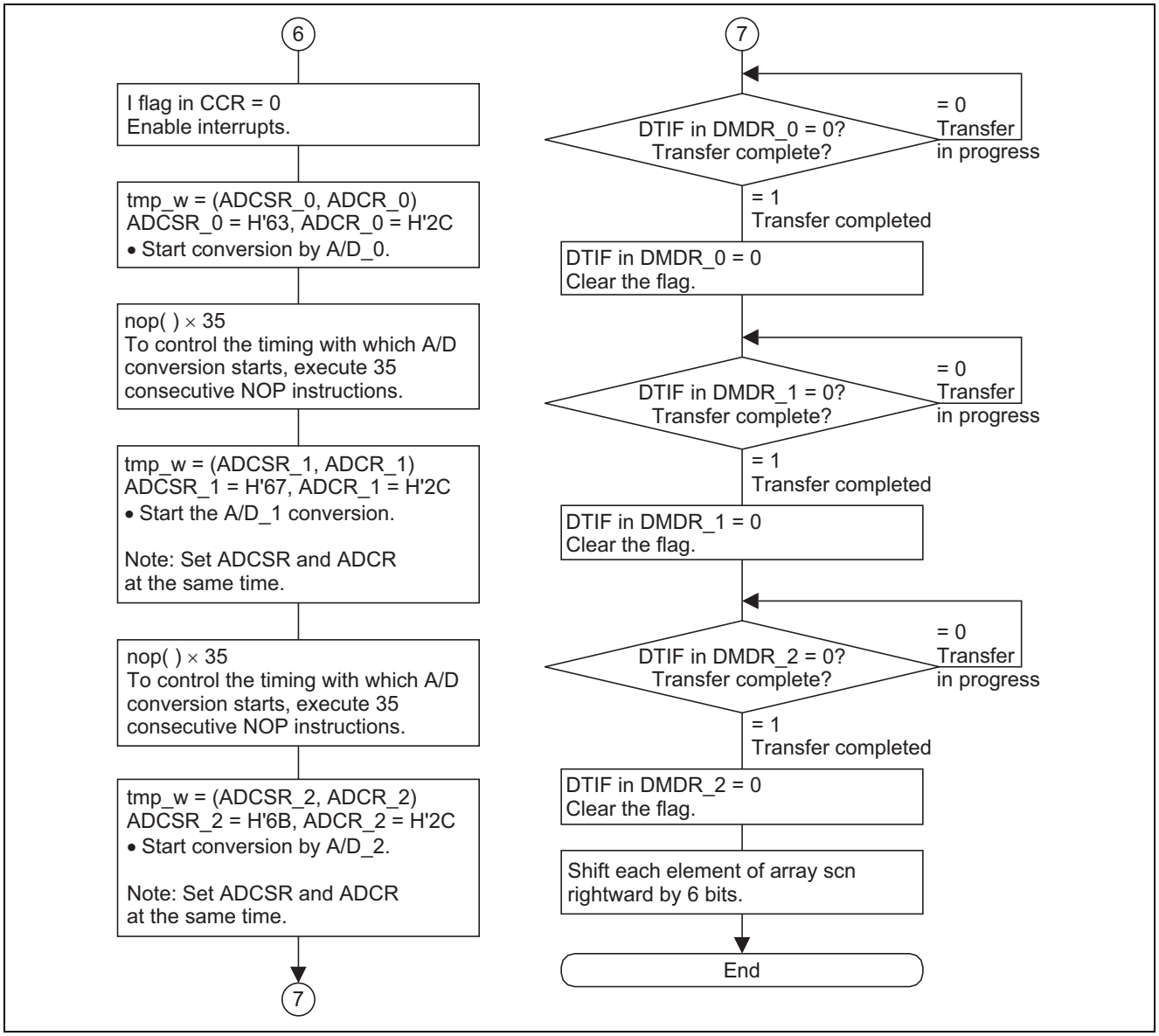
Bit	Bit Name	Setting	R/W	Description
7	TRGS1	0	R/W	Timer Trigger Select 1 and 0
6	TRGS0	0	R/W	These bits are set together with EXTRGS. TRGS1 and 0 = B'00, EXTRGS = 0: Disables initiation of A/D conversion by an external trigger signal.
5	SCANE	1	R/W	Scan Mode
4	SCANS	0	R/W	10: Scan mode. A/D conversion is performed continuously for channels 1 to 4.
3	CKS1	1	R/W	Clock Select 1 and 0
2	CKS0	1	R/W	Writing to CKS1 and 0 has to be performed at the same time as writing to EXCKS in ADCRS. EXCKS = 0, CKS1 and 0 = B'11: A/D conversion time = 68 cycles (max.)
0	EXTRGS	0	R/W	Extension Timer Trigger Select For details, refer to the description of bits TRGS1/0.

5. Flowchart


main
Clear all elements of the array scn to 0.
tmp_l = DMDR_0
DMDR_0 = H'000051A0
• Disable transfer.
• DMAC_0 activation source: on-chip module interrupts
• Block transfer mode
• Data access size: words
DSAR_0 = (*) (&ADDRA_0)
Set the transfer source address to the address of ADDRA_0.
DDAR_0 = (*) (&scn[0][0])
Set the transfer destination address to the address of array scn[0][0].
DOFR_0 = SIZE × UNIT
Set the offset: 2 × 3 = 6 bytes.
DTCR_0 = SIZE × CNT × SCAN
= 48 bytes
Set the transfer size of data:
2 × 6 × 4 = 48 bytes.
DACR_0 = H'00210000
• Dual address mode
• The source address is incremented.
• The destination address is incremented by adding the address offset.
DBSR_0 = SCAN × H'10000 + SCAN
Set the block size of data to 4 words.
DTE in DMDR_0 = 1
Enable transfer.
DMRSR_0 = 86
Set the DMAC_0 activation source to ADI0 (conversion end interrupt from A/D converter unit 0).
1
DMAC_0 initial settings
1
tmp_w = (ADCSR_0, ADCR_0)
ADCSR_0 = H'43, ADCR_0 = H'2C
• Clear the A/D_0 end flag.
• Enable ADI0 interrupts.
• Stop A/D_0 conversion.
• Analog input pins: Pins AN0 to AN3
• Disable A/D conversion start by an external trigger signal.
• Scan mode (continuous A/D conversion on channels 1 to 4)
• Conversion time: 68 cycles (ADCLK = Pϕ = 25 MHz)
• Disable automatic clearing of the ADST bit in scan mode.
2
A/D unit 0 initial settings


2
tmp_l = DMDR_1
DMDR_1 = H'000051A0
• Disable transfer.
• DMAC_1 activation source: on-chip module interrupts
• Block transfer mode
• Data access size: words
DSAR_1 = (*) (&ADDRE_1)
Set the transfer source address to the address of ADDRE_1.
DDAR_1 = (*) (&scn[0][1])
Set the transfer destination address to the address of array scn[0][1].
DOFR_1 = SIZE × UNIT
Set the offset: 2 × 3 = 6 bytes.
DTCR_1 = SIZE × CNT × SCAN
= 48 bytes
Set the transfer size of data:
2 × 6 × 4 = 48 bytes
DACR_1 = H'00210000
• Dual address mode
• The source address is incremented.
• The destination address is incremented by adding the address offset.
DBSR_1 = SCAN × H'10000 + SCAN
Set the block size of data to 4 words.
DTE in DMDR_1 = 1
Enable transfer.
DMRSR_1 = 237
Set the DMAC_1 activation source to ADI1 (conversion end interrupt from A/D converter unit 1).
3
DMAC_1
initial settings
3
tmp_w = (ADCSR_1, ADCR_1)
ADCSR_1 = H'47, ADCR_0 = H'2C
• Clear the A/D_1 end flag.
• Enable ADI1 interrupts.
• Stop A/D_1 conversion.
• Analog input pins: Pins AN4 to AN7
• Disable A/D conversion start by an external trigger signal.
• Scan mode (continuous A/D conversion on channels 1 to 4)
• Conversion time: 68 cycles (ADCLK = Pϕ = 25 MHz)
• Disable automatic clearing of the ADST bit in scan mode.
Note: Set ADCSR and ADCR at the same time.
4
A/D unit 1
initial settings


4
tmp_l = DMDR_2
DMDR_2 = H'000051A0
• Disable transfer
• DMAC_2 activation source: on-chip module interrupts
• Block transfer mode
• Data access size: words
DSAR_2 = (*) (&ADDRA_2)
Set the transfer source address to the address of ADDRA_2.
DDAR_2 = (*) (&scn[0][2])
Set the transfer destination address to the address of array scn[0][2].
DOFR_2 = SIZE × UNIT
Set the offset: 2 × 3 = 6 bytes.
DTCR_2 = SIZE × CNT × SCAN
= 48 bytes
Set the transfer size of data:
2 × 6 × 4 = 48 bytes.
DACR_2 = H'00210000
• Dual address mode
• The source address is incremented.
• The destination address is incremented by adding the address offset.
DBSR_2 = SCAN × H'10000 + SCAN
Set the block size of data to 4 words.
DTE in DMDR_2 = 1
Enable transfer.
DMRSR_2 = 232
Set the DMAC_2 activation source to ADI2 (conversion end interrupt from A/D converter unit 2).
5
DMAC_2 initial settings
5
tmp_w = (ADCSR_2, ADCR_2)
ADCSR_2 = H'4B, ADCR_0 = H'2C
• Clear the A/D_2 end flag.
• Enable ADI2 interrupts.
• Stop A/D_2 conversion.
• Analog input pins: Pins AN8 to AN11
• Disable A/D conversion start by an external trigger signal.
• Scan mode (continuous A/D conversion on channels 1 to 4)
• Conversion time: 68 cycles (ADCLK = Pϕ = 25 MHz)
• Disable automatic clearing of the ADST bit in scan mode.
Note: Set ADCSR and ADCR at the same time.
6
A/D unit 2 initial settings


6
I flag in CCR = 0
Enable interrupts.
tmp_w = (ADCSR_0, ADCR_0)
ADCSR_0 = H'63, ADCR_0 = H'2C
• Start conversion by A/D_0.
nop( ) × 35
To control the timing with which A/D conversion starts, execute 35 consecutive NOP instructions.
tmp_w = (ADCSR_1, ADCR_1)
ADCSR_1 = H'67, ADCR_1 = H'2C
• Start the A/D_1 conversion.
Note: Set ADCSR and ADCR at the same time.
nop( ) × 35
To control the timing with which A/D conversion starts, execute 35 consecutive NOP instructions.
tmp_w = (ADCSR_2, ADCR_2)
ADCSR_2 = H'6B, ADCR_2 = H'2C
• Start conversion by A/D_2.
Note: Set ADCSR and ADCR at the same time.
7
7
DTIF in DMDR_0 = 0?
Transfer complete?
= 0
Transfer in progress
= 1
Transfer completed
DTIF in DMDR_0 = 0
Clear the flag.
DTIF in DMDR_1 = 0?
Transfer complete?
= 0
Transfer in progress
= 1
Transfer completed
DTIF in DMDR_1 = 0
Clear the flag.
DTIF in DMDR_2 = 0?
Transfer complete?
= 0
Transfer in progress
= 1
Transfer completed
DTIF in DMDR_2 = 0
Clear the flag.
Shift each element of array scn rightward by 6 bits.
End

5.5.3 dmtend0_int Function

1. Functional overview
   Handler for the DMAC_0 transfer end interrupt. Enables interrupt processing after transfer of A/D converted data to on-chip RAM the specified number of times, and sets DMAC_0 transfer end interrupt requests, A/D unit 0 conversion, and ADI0 interrupts disabled.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

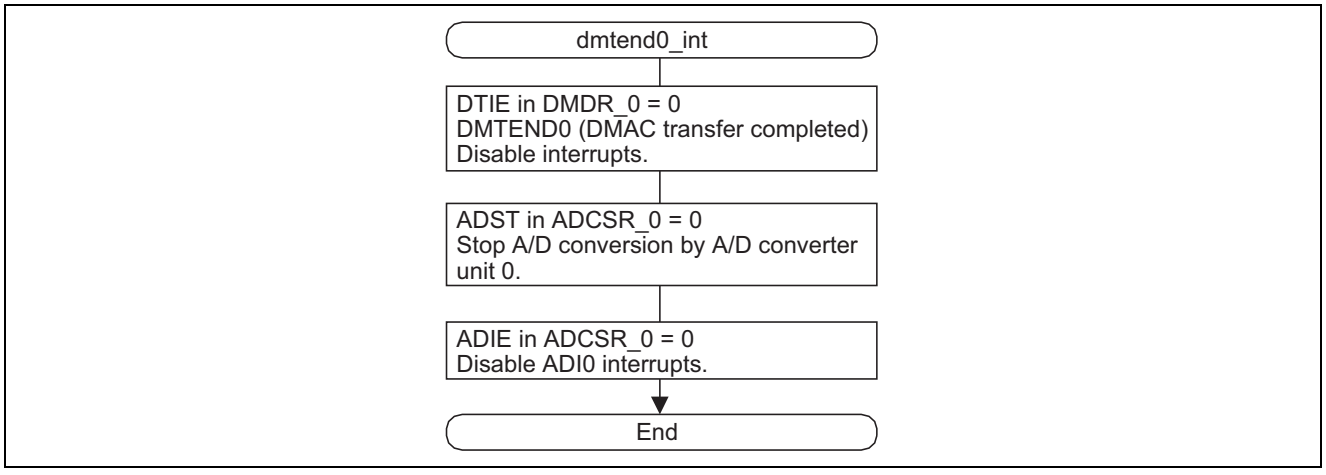
- DMA mode control register _0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
8	DTIE	0	R/W	Data Transfer End Interrupt Enable Enables or disables a transfer end interrupt request by the transfer counter. When the DTIF bit is set to 1 with this bit set to 1, a transfer end interrupt is requested to the CPU or DTC. The transfer end interrupt request is cleared by clearing this bit or the DTIF bit to 0. 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

- A/D control/status register_0 (ADCSR_0) Number of bits: 8 Address: H'FFFFA0

Bit	Bit Name	Setting	R/W	Description
6	ADIE	0	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.

5. Flowchart



5.5.4 dmtend1_int Function

1. Functional overview
   Handler for the DMAC_1 transfer end interrupt. Enables interrupt processing after transfer of A/D converted data to on-chip RAM the specified number of times, and sets DMAC_1 transfer end interrupt requests, A/D unit 1 conversion, and ADI1 interrupts disabled.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

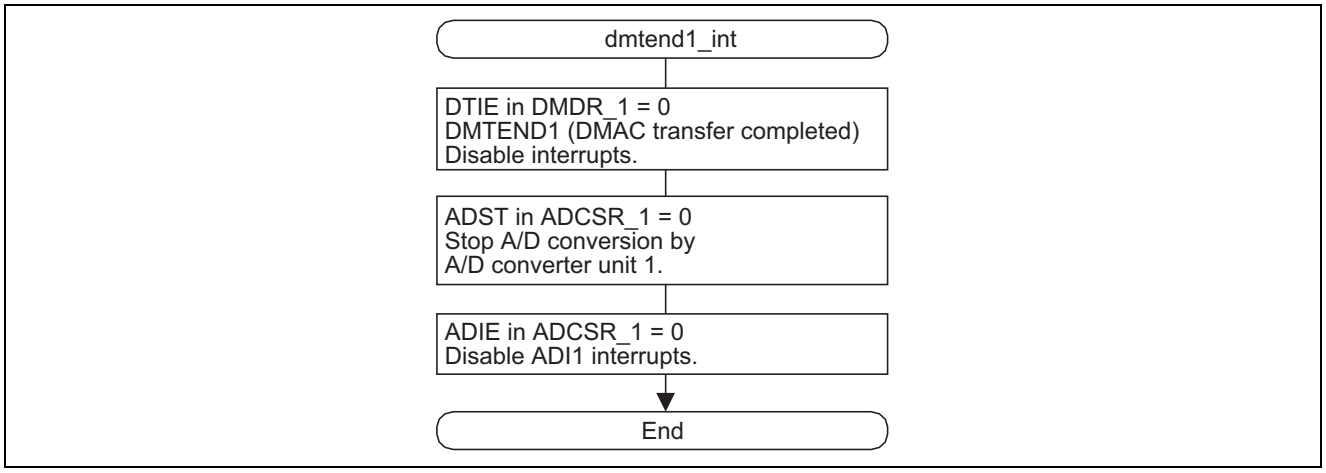
- DMA mode control register _1 (DMDR_1) Number of bits: 32 Address: H'FFFC34

Bit	Bit Name	Setting	R/W	Description
8	DTIE	0	R/W	Data Transfer End Interrupt Enable Enables or disables a transfer end interrupt request by the transfer counter. When the DTIF bit is set to 1 with this bit set to 1, a transfer end interrupt is requested to the CPU or DTC. The transfer end interrupt request is cleared by clearing this bit or the DTIF bit to 0. 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

- A/D control/status register_1 (ADCSR_1) Number of bits: 8 Address: H'FFEAA0

Bit	Bit Name	Setting	R/W	Description
6	ADIE	0	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.

5. Flowchart



5.5.5 dmtend2_int Function

1. Functional overview
   Handler for the DMAC_2 transfer end interrupt. Enables interrupt processing after transfer of A/D converted data to on-chip RAM for the specified number of times, and sets DMAC_2 transfer end interrupt requests, A/D unit 2 conversion, and ADI2 interrupts disabled.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

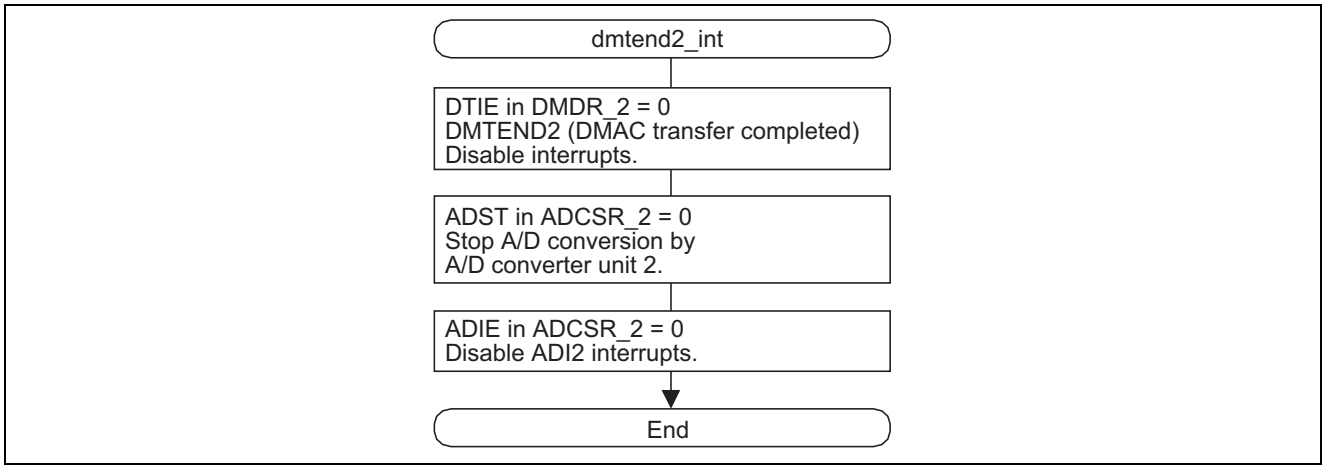
- DMA mode control register _2 (DMDR_2) Number of bits: 32 Address: H'FFFC54

Bit	Bit Name	Setting	R/W	Description
8	DTIE	0	R/W	Data Transfer End Interrupt Enable Enables or disables a transfer end interrupt request by the transfer counter. When the DTIF bit is set to 1 with this bit set to 1, a transfer end interrupt is requested to the CPU or DTC. The transfer end interrupt request is cleared by clearing this bit or the DTIF bit to 0. 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

- A/D control/status register_2 (ADCSR_2) Number of bits: 8 Address: H'FFEEAB0

Bit	Bit Name	Setting	R/W	Description
6	ADIE	0	R/W	A/D Interrupt Enable 0: Disables ADI interrupts. 1: Enables ADI interrupts.
5	ADST	0	R/W	A/D Start 0: Stops A/D conversion. 1: Starts A/D conversion.

5. Flowchart



6. Documents for Reference (Note)

- Hardware Manual
  H8SX/1648 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

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