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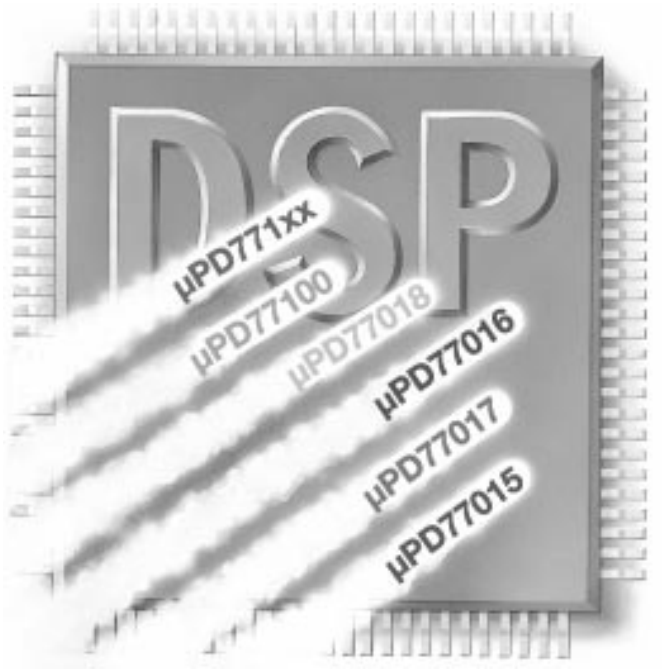


Simply the Best: Benchmarks for the µPD7701x Family

Performance comparisons of DSPs are one of the most important tasks when a DSP for a certain application needs to be selected. The simple but popular Mips and Mops figures do not reflect a DSP's performance precisely enough. Benchmarking with suitable algorithms is a reliable way out of this dilemma.

If selected and programmed carefully benchmarks translate the many aspects of DSP performance into simple and easy to interprete figures. Nevertheless benchmarks can also be used to mislead customers by unrealistic benchmark tuning. This application note presents some benchmarks for the µPD7701x family devices and their direct competitors based on the most serious DSP market study, the "Buyer's Guide to DSP Processors".

What are benchmarks?

In the early 80s the world of engineers who were dealing with digital signal processors (DSPs) was very simply structured: They could chose between two different products, the TMS32010 from Texas Instruments and the µPD7720 from NEC. Both devices were 16-bit fixed-point DSPs with similar performance and complexity. Consequently the processor's price was the most frequently applied decision criterion.

Today, in 1996, not only life has become more complicated but also the choice of the "right" DSP. Due to the fast growing DSP market about ten suppliers with more or less big product portfolios try to get their piece of the cake.

Comparing the DSP architectures helps to find the best processor for a given application but this method requires a priori application and processor knowhow. Benchmarks translate the processor's performance into figures which can be compared directly and rather objectively without detailed knowhow about the actual benchmark program.

Benchmarks are (or should be) implementations of precisely defined signal processing algorithms thus allowing an almost objective comparison of different DSP processors. They can be compared under different aspects with sometimes surprisingly different results:

- required execution time, Mips or time load (performance/efficiency aspect)
- required instruction and data memory sizes (efficiency aspect; the differences in this category are sometimes surprisingly big)
- required power consumption for a certain function (of big importance for battery powered equipment)
- required cost per function (economical efficiency)

The priorisation of these different aspects depends on the actual application background and cannot be generalised. In the next sections we will take a look at some typical benchmark algorithms.

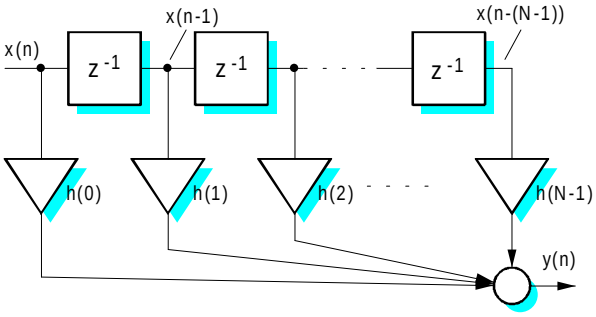
The presented figures are taken from the 1995 "DSP Buyer's Guide", an extensive (and expensive) market study, annually performed by Berkeley Design Technology Inc. **Improvements made within 1996 are not taken into account.** These results will be interpreted critically and the µPD7701x devices will be positioned in the DSP market arena.

The single-sample FIR filter

Due to its simplicity the single-sample FIR filter is one of the most popular benchmark programs. The undesired side effect of this simplicity is the fact that it reflects only a limited aspect of the DSP performance. Almost all currently available DSPs can do the operations which are required for an FIR filter calculation

- multiplication/accumulation
- 2 address manipulations
- 2 data transfers

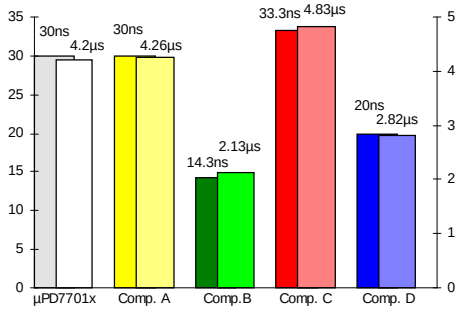
in a single instruction cycle. Slight differences occur in the amount of overhead to prepare the filter algorithm. But for typical filter lengths like N=128 the contribution of these preparations to the total processor load is negligible compared to the time required for the actual filter computation.



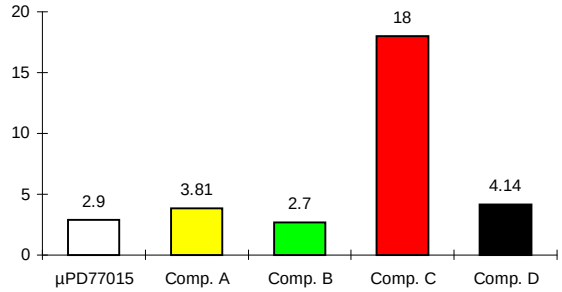
Therefore, the FIR filter benchmark is roughly speaking, just a measure for instruction cycle times. The following diagram shows the instruction cycle times and the 128-tap FIR filter execution times for the µPD7701x processors and their major competitors. A µPD7701x DSP with its 30 ns cycle time executes the filter in 4.2 µs.

The diagram proves that these two quantities are almost proportional and that an FIR benchmark seen under the aspect of execution time does not provide more information than the DSP's instruction cycle time.

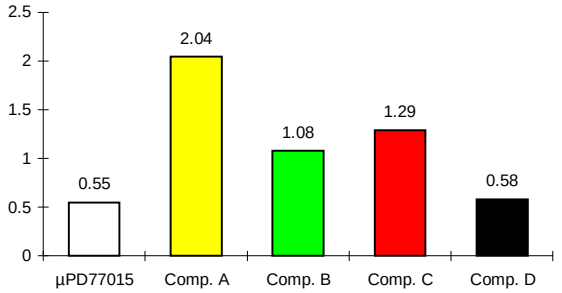
instruction cycle and FIR filter execution times



power consumption for 128-tap FIR filter / mW



cost for 128-tap FIR filter kernel / $



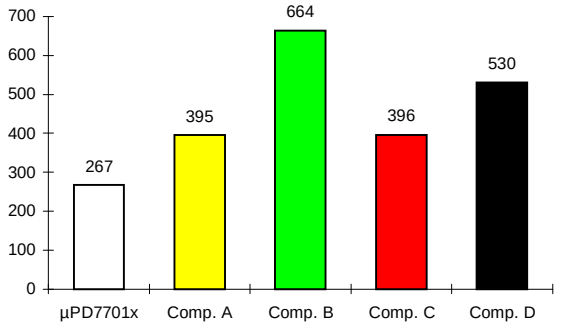
Due to the few possibilities to vary FIR filter programming this benchmark is very suitable for power consumption and cost analysis. On this page we show two figures that illustrate these aspects for the µPD77015 and some of its competitors based on a 128-tap FIR filter kernel.

The adaptive FIR filter

In an adaptive FIR filter the coefficients h(n) vary according to optimisation strategies like the **l**east **m**ean **s**quare (LMS) algorithm. An effective implementation of this algorithm needs tricky addressing of filter data and coefficients, and it is a good indication for a DSP's addressing facilities. Another requirement is flexible usability of working and accumulation registers. For most DSPs the execution time is tripled compared with the fixed FIR filter; for the µPD7701x devices, however, it is only doubled. We would like to indicate that the figures given in the DSP Buyer's Guide for the adaptive FIR filter on the µPD7701x are **not** optimised. In this document we use the optimised figures.

The next diagram shows the classical benchmark figure, the number of instruction cycles, for a 128-tap adaptive FIR, implemented on the µPD7701x devices and their competitors.

cycle count for 128-tap adaptive FIR filter kernel



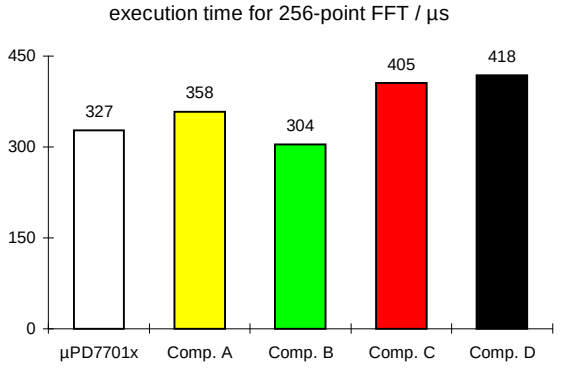
It can easily be seen that the µPD7701x processors offer the most efficient implementation for adaptive filter algorithms. This still holds true, if power consumption or cost aspects are investigated because a low cycle count reduces the load for the DSP and therewith the relative cost.

A 256-point Fast Fourier Transform (FFT)

Fast **F**ourier **T**ransforms (FFTs) are another classical benchmark program. It takes not primarily the instruction cycle time of a DSP into account, but also its addressing skills, register structures, loop mechanisms and available memory spaces. One big problem about the usage of the FFT as a benchmark is the multitude of variations within the algorithm itself. The "free parameters" for an FFT implementation include

- type of algorithm (decimation in time/ frequency, radix 2 or 4)
- complex or real inputs
- internal scaling of data
- arrangement of data in memory
- inclusion of support functions
- inclusion of I/O functions
- "straight line" or looped coding
- "in place computation" or not

execution time for 256-point FFT / µs



Keeping this in mind it becomes almost impossible to compare FFT benchmarks of different DSP suppliers with each other as long as it is not clearly specified how the program was written. A comparison like the one in the DSP Buyer's Guide, in which all programs are coming from a single source, is therefore much more objective than just comparing silicon vendors' figures. In the next diagram you find the FFT performance for the µPD7701x devices and their competitors under the aspect of execution time. All figures have been taken from the DSP Buyer's Guide.

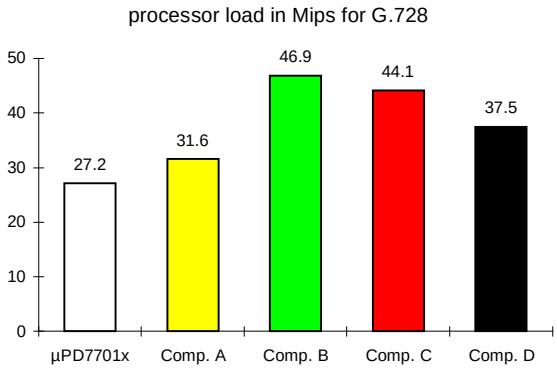
Performance evaluation with G.728

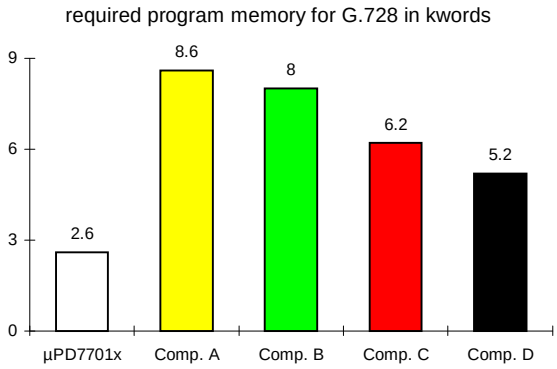
The more complex a benchmark program is, the better does it represent the overall processor performance. Therefore bit-exactly specified speech coding algorithms standardised by the CCITT are excellent candidates for benchmarking.

One of the most complex algorithms is the G.728 LD-CELP speech codec which realises high-quality speech coding at 16 kbits/s with a delay of only 0.625 ms. As this algorithm is of high commercial interest for usage in videophone/-conferencing systems and multiplexing equipment, implementations of G.728 are available for all major DSP families.

The diagrams in the right column compare the G.728 implementations of the major players in terms of processor load and instruction memory consumption, i.e. program effectiveness. Note that the "Comp. C" device offers only 30 Mips, thus two devices are needed for full-duplex G.728. The figures are taken from different articles.

The lower diagram illustrates the dramatic progress in programming efficiency with the µPD7701x processors which is partially caused by their 32-bit wide instruction word, but also by the careful definition of architecture and instruction set.





A Spotlight on Other Applications

The µPD7701x processors are very well suited for the implementation of different types of DSP algorithms and especially speech coding algorithms. To illustrate their performance we have compiled benchmark data for some other applications and compared the µPD7701x family with the devices that we have referred to as "Competition D". The result of these findings is summarised in the table on the right hand side.

The table highlights again that the µPD7701x devices are extremely efficient to program com-

	Mips		Instruction memory		Data Memory	
	µPD7701x	Comp. D	µPD7701x	Comp. D	µPD7701x	Comp. D
G.726	11.8	23	1.3k	2.2k	ROM: 0.1k RAM: 0.1k	0.25k
G.722	7.7	8.9	1k	2.5k	ROM: 0.3k RAM: 0.2k	0.5k
G.728	27.2	37.5	2.6k	5.2k	ROM: 1.2k RAM: 1.9k	3.1k
GSM-FR	3.75	4.7	1.7k	5.8k	ROM: 0.2k RAM: 1.4k	0.9k
GSM-HR	24.6	?	7.7k	?	ROM: 8k RAM: 3.7k	?

pared with the competition. The Mips figures and the required amounts of instruction memory are clearly lower than for others. The differences in terms of data memory consumption are not so remarkable, because it is mainly determined by the algorithm itself and not so much by the respective processor.

µPD7701x/1xx Families Overview

NECs new µPD7701x and µPD771xx 16-bit fixed-point DSP families offer one of the most advanced architectures on the market. Their members are characterised by a clearly structured Harvard architecture with:

- Two identical memory banks (X, Y) with separate address computation units
- 32-bit instructions for top efficiency and flexibility
- Powerful 16/40-bit arithmetic operation unit
- Program control unit with high performance loop counter
- Memory-mapped peripherals
- JTAG-based on-chip debug hardware with boundary scan facilities

All µPD7701x and µPD771xx devices share the same core architecture but have a couple of device specific characteristics which are summarised in the table. With the new µPD77100 core memory sizes and peripherals can be defined according to the actual requirements.

Devices under development will extend this family with a DSP core and more variants in performance/speed.

		µPD77016	µPD77015	µPD77017	µPD77018A	µPD771xx *	µPD77100 *
Internal memory	Instruction ROM	-	4k x 32 bit	12k x 32 bit	24k x 32 bit	24k x 32 bit	User defined
	Instruction RAM	1.5k x 32 bit	256 x 32 bit			4k x 32 bit	
	Data ROM	-	2 x 2k x 16 bit	2 x 4k x 16 bit	2 x 12k x 16 bit	2 x 12k x 16 bit	
	Data RAM	2 x 2k x 16 bit	2 x 1k x 16 bit	2 x 2k x 16 bit	2 x 3k x 16 bit	2 x 3k x 16 bit	
External memory	Instr. memory	48k x 32 bit	-				
	Data memory	2 x 48k x 16 bit	2 x 16k x 16 bit				
ALU bus		40 bit					
Multiplier		16 x 16 --> 31 bit					
Barrelshifter		40 bit					
Working registers		8 x 40 bit					
Loop/repeat counter		1 repeat counter / 4 nested loop counters					
Host I/F, throughput at 33 Mips		8 bit, 8.25 Mbytes/s					user defined
Serial I/F, throughput at 33 Mips		2 SIOs, 8/16 bit, 16.6 Mbits/s					user defined
Interrupts		4 external, 6 internal					10
Min. instruction cycle time		**30 ns**			**25 ns**	**20 ns**	**15 ns**
Master clock for 33 Mips		66 MHz	33, 16.5, 8.25, 4.125 MHz (internal PLL)				user defined
Power supply		5 V, ±10%	3 V, -10/+20%				
Power dissipation	at 33 Mips	0.7 W	120 mW	135 mW	100 mW	80 mW	30 mW
	halt mode	0.4 W	24 mW	30 mW	45 mW	2.1mW	
	stop mode	-	300 µW			30 µW	
Packages		160 QFP	100 TQFP				user defined

** under development*

How to get more info

Software and hardware development and improvement are ongoing processes, not only at NEC. Therefore the figures that were presented on the last pages can only be a snapshot. To provide you reliable information, most of the examples are based on the DSP Buyer's Guide 1995.

If you would like to get more precise information for example on the fact who is competition A,B, C or D, please contact your local NEC office or the technical product support staff in NEC's european headquarter in Düsseldorf, Germany.

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