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Renesas Electronics Corporation

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H8/300H Tiny Series

Signed 32-Bit Binary Division with a 32-Bit Divisor (DIVS)

Introduction

Performs division in this format:
dividend (signed, 32 bits) / divisor (signed, 32 bits) = quotient (signed, 32 bits) … remainder (signed, 32 bits).

Target Device

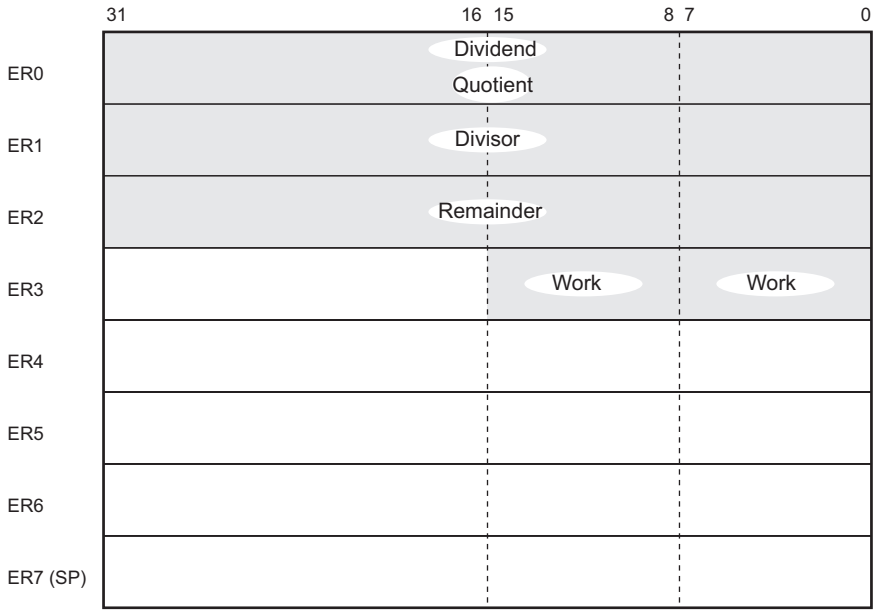
H8/300H Tiny Series

Contents

1. Arguments

Description		Storage Location	Data Length (Bytes)
Input	Dividend (signed, 32 bits)	ER0	4
	Divisor (signed, 32 bits)	ER1	4
Output	Quotient (signed, 32 bits)	ER0	4
	Remainder (signed, 32 bits)	ER2	4
	Occurrence of error	Z flag (CCR)	—

2. Changes to Internal Registers and Flags



I	UI	H	U	N	Z	V	C
–	–	↕	–	↕	↕	↕	↕

–: No change
↕: Varies
0: Fixed to 0
1: Fixed to 1

3. Programming Specifications

Program memory (bytes)
66
Data memory (bytes)
0
Stack (bytes)
0
Number of cycles
770
Re-entrant
Yes
Relocatable
Yes
Interrupts during execution
Yes

4. Note

The number of cycles in the programming specifications is the value for calculation of H'80000000 / H'7FFFFFFF.

5. Description

5.1 Description of Functions

1. The arguments are as follows.
   ER0: Set the divisor (signed, 32 bits) as an input argument. The quotient (signed, 32 bits) is also set here as an output argument.
   ER1: Set the divisor (signed, 32 bits) as an input argument.
   ER2: The remainder (signed, 32 bits) is set here as an output argument.
   Z flag (CCR): Indicates whether there are any errors (division by 0) after execution of DIVS.
   Z flag = 1: The division was in error.
   Z flag = 0: The division was processed without error.

2. The following figure illustrates the execution of the DIVS subroutine. When the input arguments are set as shown below, DIVS places the quotient in ER0 and the remainder in ER1.

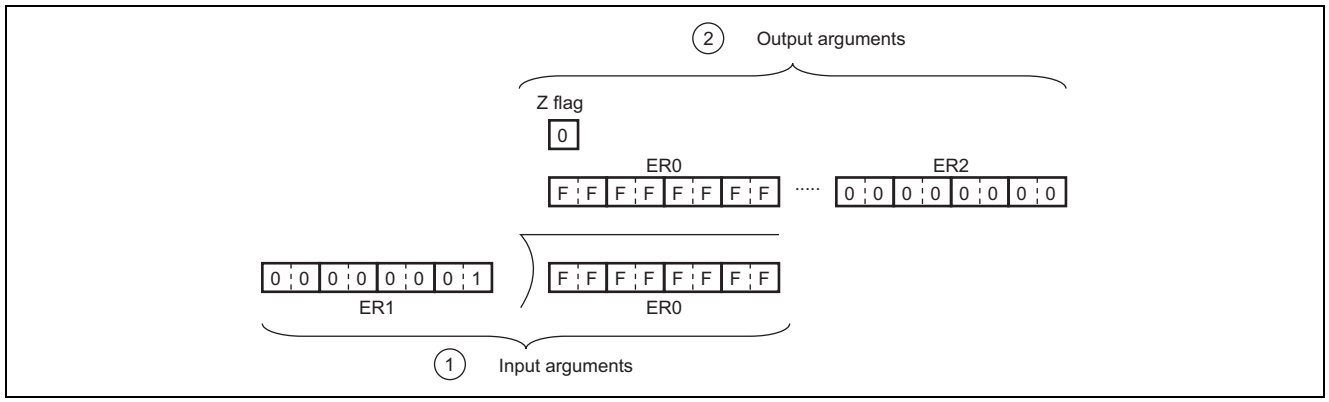


Figure 1 Example of DIVS Execution

3. When the divisor is 0, DIVS ends immediately.

5.2 Usage Notes

Since the quotient is set in ER0, the dividend is lost after DIVS is executed. When you will still require the dividend, save it elsewhere in memory beforehand.

5.3 Description of Data Memory

No data memory is used by DIVS.

5.4 Examples of Usage

After setting the dividend and divisor, call the DIVS subroutine.

```
WORK1   . RES. L 1          ..... Reservation of the data memory area for setting of the dividend (signed, 32 bits) by the user program.
WORK2   . RES. L 1          ..... Reservation of the data memory area for setting of the divisor (signed, 32 bits) by the user program.
          .
          .
          .
        MOV. L @WORK1, ER0  ..... Sets, as an input argument, the dividend (signed, 32 bits) specified by the user program.
        MOV. L @WORK2, ER1  ..... Sets, as an input argument, the divisor (signed, 32 bits) specified by the user program.
        JSR    @DIVS        ..... Subroutine call of DIVS.
```

5.5 Principles of Operation

1. Negative dividends and divisors are converted to positive numbers.
2. The quotient and remainder are found through repeated subtraction. In the figure below, the division of H'0D is by H'03 is given as an example of this division operation.
   1) The initial number of shifts is set in the counter R3L, which indicates the number of shifts.
   2) The dividend is shifted 1 bit to the left and the MSB thus loaded to the C bit is set as the LSB of ER2 (which will hold the remainder).
   3) The divisor is subtracted from ER2. When the result of subtraction is positive, the LSB of ER0 is set ((1) → (2) → (3) in the figure). When the result of subtraction is negative, the LSB of ER0 is cleared and the divisor is added to the result of subtraction, returning it to the state prior to subtraction ((4) → (5) → (6) in the figure).
   4) The shift counter set in step 1) above is decremented.
   5) Steps 2) through 4) are repeated until the shift counter reaches –1.

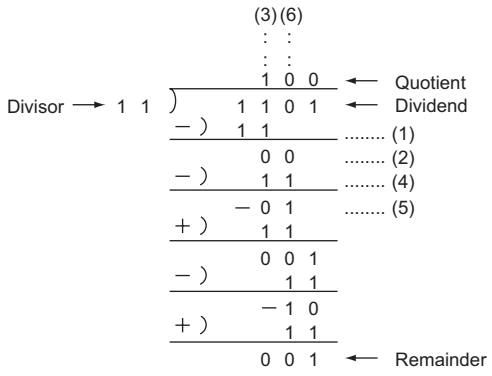


Figure 2 Division Example

3. The quotient and/or remainder is then converted to negative if the sign flag is 1, as shown in table 1.

Table 1 Sign of Division Results and the Sign Flag

Dividend	Divisor	Quotient	Remainder	Quotient Sign Flag	Remainder Sign Flag
Positive	Positive	Positive	Positive	0	0
	Negative	Negative	Positive	1	0
Negative	Positive	Negative	Negative	1	1
	Negative	Positive	Positive	0	0

6. Program Listing

```
 1                                1      ;*********************************************************************
 2                                2      ;*                                                                   *
 3                                3      ;*         NAME     :  32 BIT SIGNED DIVISION   (DIVS)               *
 4                                4      ;*                                                                   *
 5                                5      ;*********************************************************************
 6                                6      ;*
 7                                7      ;*         ENTRY    :  ER0                     (DIVIDEND)            *
 8                                8      ;*                     ER1                     (DIVISOR)             *
 9                                9      ;*         RETURNS  :  ER0                     (QUOTIENT)            *
10                               10      ;*                     ER2                     (REMAINDER)           *
11                               11      ;*                                                                   *
12                               12      ;*********************************************************************
13                               13      ;
14                               14                 .CPU        300HA
15      001000                   15                 .SECTION A,CODE,LOCATE=H'001000
16               00001000        16      DIVS       .EQU        $                       ;Entry point
17      001000   0F91            17                 MOV.L       ER1,ER1                 ;
18      001002   5870004E        18                 BEQ         DIVS7                   ;
19      001006   1833            19                 SUB.B       R3H,R3H                 ;Clear FLAG
20      001008   0F80            20                 MOV.L       ER0,ER0                 ;
21      00100A   58A00004        21                 BPL         DIVS1                   ;
22      00100E   17B0            22                 NIG.L       ER0                     ;If minus then change to plus
23      001010   7173            23                 BNOT        #7,R3H                  ;Clear FLAG
24      001012   0F91            24      DIVS1      MOV.L       ER1,ER1                 ;
25      001014   58A00008        25                 BPL         DIVS2                   ;
26      001018   17B1            26                 NEG.L       ER1                     ;If minus then change to plus
27      00101A   7173            27                 BNOT        #7,R3H                  ;Clear FLAG
28      00101C   58000008        28                 BRA         DIVS22                  ;
29      001020   7373            29      DIVS2      BTST        #7,R3H                  ;
30      001022   58700002        30                 BEQ         DIVS22                  ;
31      001026   7003            31                 BSET        #0,R3H                  ;
32      001028   FB20            32      DIVS22     MOV.B       #32,R3L                 ;Set shift counter
33      00102A   1AA2            33                 SUB.L       ER2,ER2                 ;Clear remainder
34      00102C   1030            34      DIVS3      SHLL.L      ER0                     ;Shift dividend 1 bit left
35      00102E   1232            35                 ROTXL.L     ER2                     ;Set MSB of dividend to LSB of remainder
36      001030   1A92            36                 SUB.L       ER1,ER2                 ;Sub divisor from residual
37      001032   58400006        37                 BCC         DIVS4                   ;Branch if residual >= divisor
38      001036   0A92            38                 ADD.L       ER1.ER2                 ;Add divisor to residual
39      001038   58000002        39                 BRA         DIVS5                   ;Branch always
40      00103C   7008            40      DIVS4      BSET        #0,R0L                  ;Set 1 to dividend LSB
41      00103E   1A0B            41      DIVS5      DEC.B       R3L                     ;Decrement shift counter
42      001040   46EA            42                 BNE         DIVS3                   ;Branch until shift counter = 0
43      001042   7373            43                 BTST        #7,R3H                  ;
44      001044   58700002        44                 BEQ         DIVS55                  ;
45      001048   17B0            45                 NEG.L       ER0                     ;If FLAG = 1 then change to minus
46      00104A   7303            46      DIVS55     BTST        #0,R3H                  ;
47      00104C   58700002        47                 BEQ         DIVS6                   ;
48      001050   17B2            48                 NEG.L       ER2                     ;quotient and residual
49      001052   06B2            49      DIVS6      ANDC        #B'11111011,CCR  ;
50      001054   5470            50                 RTS
51                               51                 .END
*****   TOTAL    ERRORS      0
*****   TOTAL    WARNINGS    0
```

Note: The program listing included in this application note assumes compilation under the option for the advanced mode of H8/300H CPU. If you use this sample program with an H8/300H Tiny Series product, make the following change to the program code:

.CPU 300HA → .CPU 300HN

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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