SH7763 Group

LCD Controller Setup Example

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Introduction

This application note describes how to use the LCD controller (LCDC) of the SH7763, and shows a display example by the TFT-LCD module.

Target Device

SH7763

Contents

1. Preface

1.1 Specifications

- In this application note, section 2 gives a supplementary explanation of the LCDC description in the hardware manual, and section 3 describes the LCDC bus load factor necessary for system design. Section 4 shows an application example in which four types of images are alternately displayed on the TFT-LCD module and the TFTLCD module is repeatedly turned on and off.

1.2 Modules Used

- LCDC

1.3 Applicable Conditions

- Evaluation board: SH7763 Solution Engine (product code: MS7763SE02) manufactured by Hitachi ULSI Systems Co., Ltd.
  External memory (area 0): 16-MB NOR-type flash memory: S29GL128M10TDIR90 from Spansion
  (area 2, 3): 128-MB DDR-SDRAM: MT46V32M16TG-6T × 2 from Micron
- MCU: SH7763 (R5S77630AY266BGV)
- Operating frequency:
  CPU clock: 266.6 MHz
  SH bus clock: 133.3 MHz
  Bus clock: 66.6 MHz
  DDR-SDRAM clock: 133.3 MHz
  Peripheral bus 0 clock: 66.6 MHz
- Bus width for area 0: 16-bit (with the MD3 pin at the low level, and MD4 pin at the high level)
- Clock operating mode: Mode 0 (with the MD0 to MD2 pin at the low level)
- Endian: Big endian (with the MD5 pin at the low level)
- Toolchain: SuperH RISC engine Standard Toolchain Ver.9.3.0.0 from Renesas Electronics
- Compiler options: Default settings of High-performance Embedded Workshop
  (-cpu=sh4aldsp -endian=little -include="$(PROJDIR)\inc"
  -object="$(CONFIGDIR)\$(FILELEAF).obj" –debug -optimize=0 -gbr=auto
  -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0
  -del_vacant_loop=0 -struct_alloc=1 -nologo)

1.4 Terms Used in This Application Note

- Frame:
  A frame is pixel information located in the memory in the same way the image is to be displayed on the screen. A buffer in which frame information is stored is called a frame buffer. The LCDC reads pixel information from the frame buffers and uses it to display images.
- Frame rate [Hz]:
  Indicates how many times the LCD module connected to the LCDC rewrites the screen in 1 second.

1.5 Scope of This Application Note

This application note describes the basic usage method of the LCDC without an OS, that is, to continuously display images in the frame buffers onto the LCD module supporting the RGB interface mode.

1.6 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the SH7763 Group application note, Example of Initialization (REJ06B0934). Please refer to that document in combination with this one.

2. LCDC Operation

2.1 Overview of LCDC

The LCDC is an image system module that can read image data from the frame buffers located in the external memory and display images onto the TFT-LCD module. This application note introduces a setup example in which RGB- or YCbCr-format image data is read and an image is displayed on the LCD module in RGB interface mode.

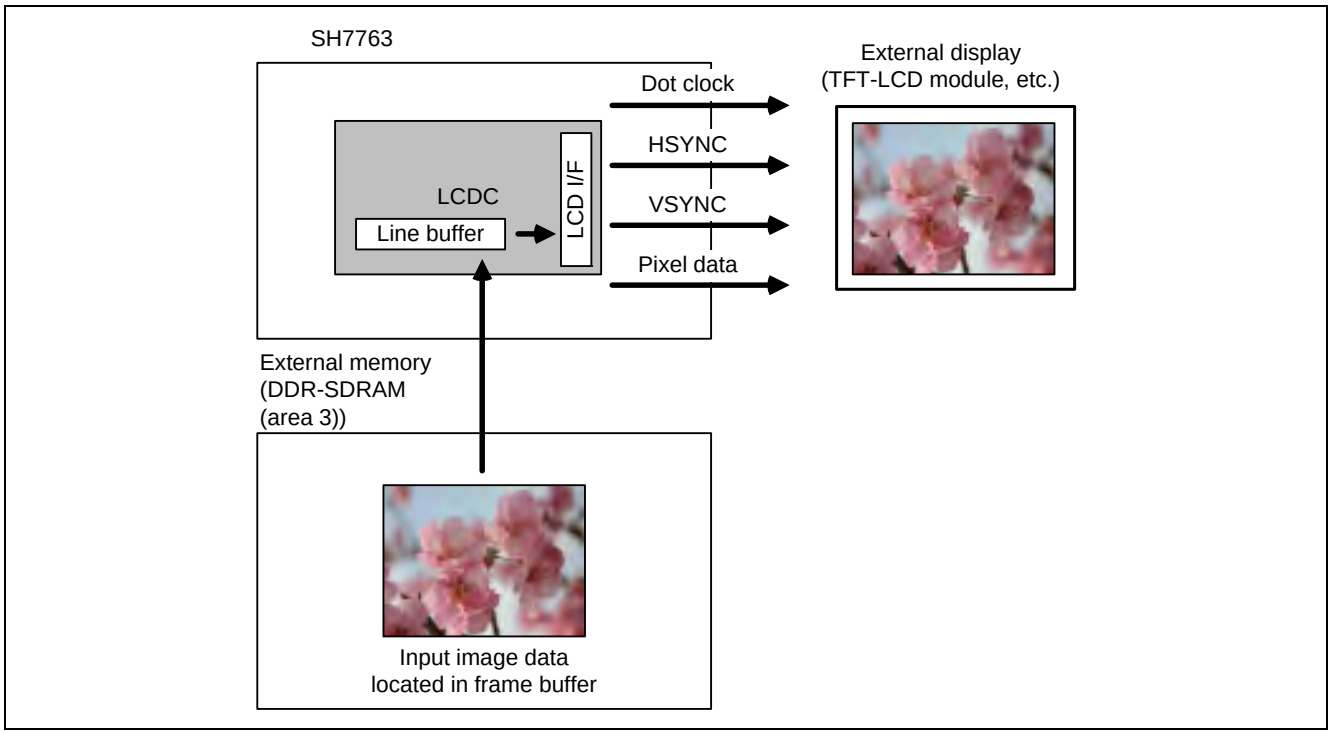

Figure 1 Image of LCDC Operation

2.1.1 Image Data Read

The LCDC reads from the frame buffer one pixel each rightward, starting from the base point of an image that is located at the top-left corner. The pixel information for the amount of the horizontal image size is called one line. After reading for one line has finished, reading is continued after returning to the left end one line down. Reading for one frame is completed when the number of lines equal to the vertical image size has been read. Reading of the next frame is started again from the base point.

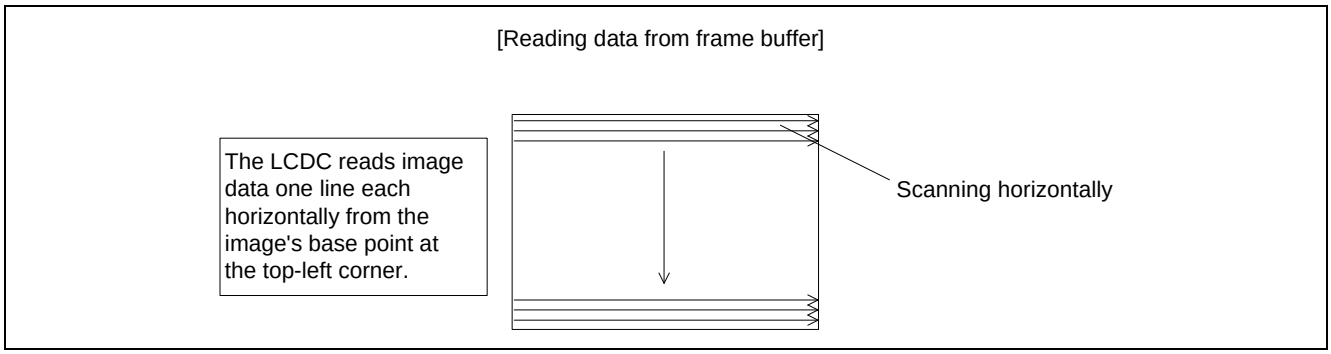

Figure 2 Image Data Input

2.1.2 Image Data Output

The LCDC outputs image data in synchronization with the following three sync signals.

- Dot clock (DOTCLK):
  The information for one pixel is output in synchronization with the dot clock. (Pin name: LCD_CL2, LCDM_CL2)
- Horizontal sync signal (HSYNC):
  The information for a single horizontal line of an image is output in synchronization with the horizontal sync signal. The periods that are before and after the sync signal and in which no pixel information is output are referred to as the horizontal front porch and horizontal back porch, respectively. (Pin name: LCD_CL1, LCDM_CL1)
- Vertical sync signal (VSYNC):
  The information for a single frame of an image is output in synchronization with the vertical sync signal. The periods that are before and after the sync signal and in which no pixel information is output are referred to as the vertical front porch and vertical back porch, respectively. (Pin name: LCD_FLM, LCDM_FLM)

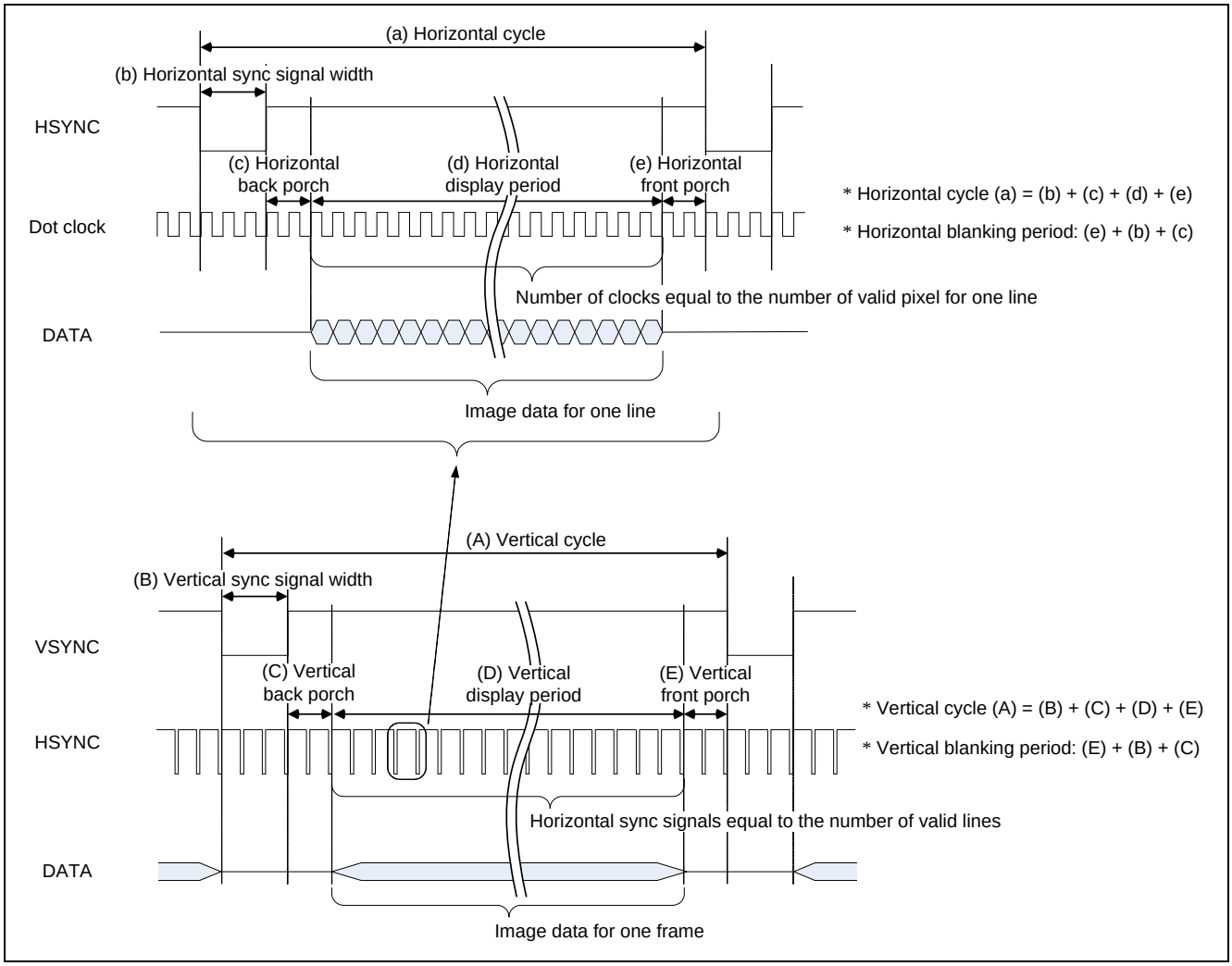

Figure 3 Input of Image Data and Sync Signals

Each cycle of the sync signal includes an image-display period and a non-display period. The non-display period in the horizontal direction starts from the end of displaying a single line from the left to the right and lasts until the beginning of displaying the next single line after returning to the left. This period is called the horizontal blanking period. The non-display period in the vertical direction starts from the end of displaying a single frame and lasts until the beginning of displaying the next single frame. This period is called the vertical blanking period.

2.2 LCDC Features

Table 1 lists the main features of the LCDC.

Table 1 LCDC Features

Item	Specifications
Display system configuration	Unified memory architecture: Display images are stored in the DDR-SDRAM in area 3 and no dedicated display memory is required. (Display is not available in areas other than the DDR-SDRAM in area 3.)
Supported display panel	• LCD type: STN, Dual STN, or TFT panel • Bus width: 4, 8, 12, 16, or 18* bits Note: * When a TFT panel with a bus width of 18 bits is connected, the lower unused bit signals should be connected to GND or the lowest data output bit.
Supported color display	• 4-, 8-, 15-, or 16-bpp (bits per pixel) color mode • 1-, 2-, 4-, or 6-bpp grayscale mode
Displayable LCD module size	16 × 1 to 1024 × 1024 LCD panel sizes are supported. Note: In actual applications, the bus occupation rate limits the displayable size because the display buffer is allocated in the external memory. In most cases, the displayable size will be around WVGA, but for details refer to the calculation shown in section 3.
Color control	The 24-bit color palette memory is used and 256 entries from among 16 million colors can be displayed at one time.

2.3 LCDC Setup

The LCDC functions and register setting methods are described here.

2.3.1 Setting the Frame Buffer

Figure 4 shows the frame buffer information required by the LCDC when reading image data from the memory.

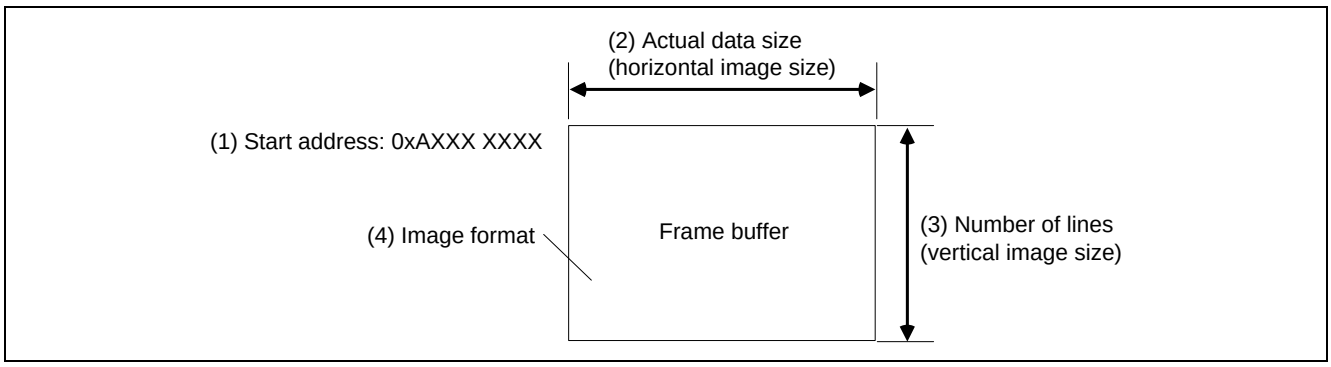

Figure 4 Frame Buffer Configuration

(1) Start address: Set a 512-byte aligned address for the base point address of the frame buffer. An address in a cache-disabled area that can be accessed by a physical address should be specified.
(2) Actual data size: Specify the horizontal image size in pixel units. Note that this setting must be a multiple of 8 because the LCDC handles data in the horizontal direction in units of characters (1 character: 8 pixels). (refer to section 2.3.5)
(3) Number of lines: Specify the vertical image size in pixel units. (refer to section 2.3.5)
(4) Image format: For the data formats that can be handled by the LCDC, refer to section 37.4.4, Data Format, in the SH7763 Hardware Manual (REJ09B0256). Table 2 shows the registers for setting the LCDC display data.
(5) Line address offset: Set the increment width for the Y coordinates of the frame buffer. The minimum alignment unit of LDLAOR is 16 bytes.

Table 2 LCDC Display Data Setting

Function	Register
• Sets the endian • Sets the data format	LCDC data format register (LDDFR)
Sets the start address for display data fetch	LCDC start address register for upper display data fetch (LDSARU)
Sets the start address for lower display data fetch (only for DSTN)	LCDC start address register for lower display data fetch (LDSARL)
Sets the increment width for the Y coordinates of the frame buffer	LCDC line address offset register for display data fetch (LDLAOR)

2.3.2 Setting the LCDC Output Pins

The LCDC output pins are provided in two groups — normal output group and mirror output group, as shown in table 3 — in order to enable the LCDC output functions and other pin functions multiplexed with the LCDC output pins. Use the pin select registers in the general purpose I/O port (GPIO) to select the pin group; no setting is required in the LCDC.

As pins in the two groups have different output timing, mixed use of pins in the two groups is not allowed.

Table 3 shows the LCDC input/output pin groups.

Table 3 LCDC Input/Output Pins

Pin Group Name	Pin Name
Normal output group	LCD_D15 to LCD_D0, LCD_DON, LCD_CL1, LCD_CL2, LCD_M_DISP, LCD_FLM, LCD_VCPWC, and LCD_VEPWC
Mirror output group	LCDM_D15 to LCDM_D0, LCDM_DON, LCDM_CL1, LCDM_CL2, LCDM_M_DISP, LCDM_FLM, LCDM_VCPWC, and LCDM_VEPWC
Common input pin	LCD_CLK

2.3.3 Setting the LCDC Input Clock

The operating clock source for the LCDC and the frequency division ratio for the input clock should be specified.

The specified clock is supplied as DOTCLK from LCD_CL2 (LCDM_CL2 when the mirror output pin is used) to the LCD module (when a TFT panel is used). Specify an appropriate clock according to the specifications of the connected LCD module.

Note that the clock should be specified so that the frequency input to the LCDC becomes 66 MHz or lower.

(1) Input clock select: Select peripheral clock 0 or an external clock as the LCDC input clock source.
(2) Clock division ratio: Set the frequency division ratio for the input clock.

Table 4 shows the register for setting the LCDC input clock.

Table 4 LCDC Input Clock Setting

Function	Register
Sets the LCD input clock	LCDC input clock register (LDICKR)

2.3.4 Setting the LCD Module Type

The LCD module interface, signal polarity, etc. should be set according to the specifications of the LCD module used. Set each value with reference to the datasheet for the LCD module used.

(1) Module interface: Selects the LCD panel type (STN, DSTN, or TFT) and the bus width of output data to the LCD panel. This application note shows settings for a case in which a TFT color module with a 16-bit data bus is selected.
(2) Sync signal polarity: Sets the vertical sync signal (LCD_FLM (VSYNC)) and horizontal sync signal (LCD_CL1 (HSYNC)) to low-active or high-active. When low-active is set, a low-level signal is output during the period of the sync signal (HSYNW/VSYNW in section 2.3.5). In contrast, a high-level signal is output when high-active is set.
(3) Horizontal sync signal output control: Sets whether or not to output horizontal sync signal (LCD_CL1 (HSYNC)) during the VSYNC blanking period.
(4) Dot clock control: Sets whether or not to output the dot clock (LCD_CL2) during the blanking period of VSYNC and HSYNC.
(5) Display enable signal polarity: Sets the display enable signal (LCD_M_DISP) to low-active or high-active.
(6) Display enable signal output control: Sets whether or not to output the display enable signal (LCD_M_DISP).
(7) Display data polarity: Sets the display data to high-active (bit value is output without change) or low-active (bit value is output after being inverted).

For details, please refer to the section 37.3.2 "LCDC Module Type Register (LDMTR)" in the SH7763 Group Hardware Manual (REJ09B0256)

Table 5 shows the LCDC registers used for setting the LCD module type.

Table 5 Setting the LCD Interface

Function	Register
• Setting the LCD module type • VSYNC polarity • HSYNC polarity • DISP (display enable) polarity • Display data polarity • M signal (LCD current-alternating signal) control • HSYNC control • DOTCLK control	LCDC module type register (LDMTR)

2.3.5 Setting the Sync Signals

The sync signal parameters in figure 5 should be set according to the characteristics (A) to (E) and (a) to (e) in figure 3 of the LCD module used.

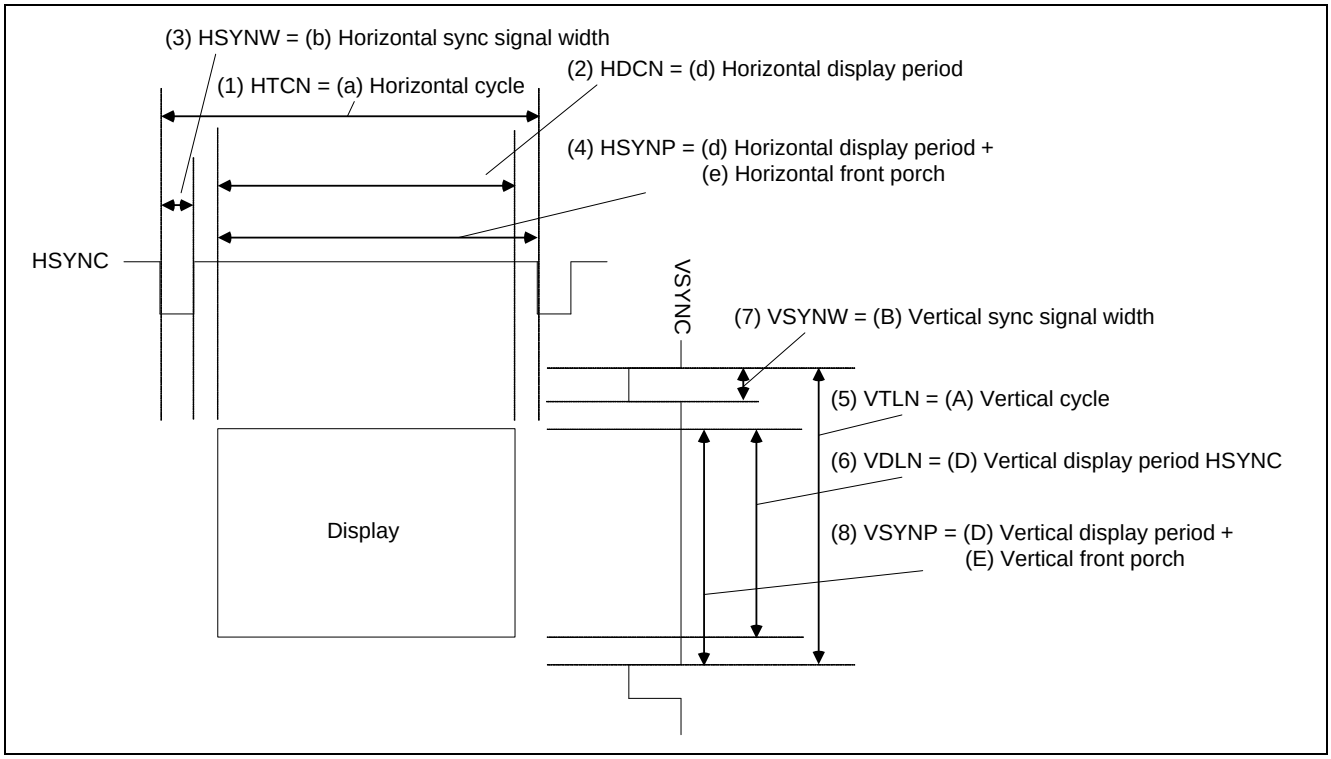

Figure 5 Sync Signal Configuration

(1) HTCN: Sets "horizontal cycle – 1" in units of characters.
(2) HDCN: Sets "horizontal display period – 1" in units of characters.
(3) HSYNW: Sets "horizontal sync signal width – 1" in units of characters.
(4) HSYNP: Sets "(horizontal display period + horizontal front porch width) – 1" in units of characters.
(5) VTLN: Sets "vertical cycle – 1" in units of horizontal sync signals.
(6) VDLN: Sets "vertical display period – 1" in units of horizontal sync signals.
(7) VSYNW: Sets "vertical sync signal width – 1" in units of horizontal sync signals.
(8) VSYNP: Sets "(vertical display period + vertical front porch width) – 2" in units of horizontal sync signals.

[Notes on Horizontal Direction Settings]

- 1 character = 8 pixels (8 dot clocks). Accordingly, each parameter in the horizontal direction can be set only in dot clock cycles as a multiple of 8. In some cases, a parameter in the horizontal direction needs to be set in dot clock cycles as a value other than a multiple of 8, depending on the LCD module used. However, in such a case, specify the nearest multiple of 8, convert that value into units of characters (change it to 1/8 of the value), and set the converted value. Confirm thoroughly that this setting does not cause trouble in the LCD module used. Confirm thoroughly that this setting does not cause trouble in the LCD module used. If the LCD module does not support the specified parameters, there may be an undisplayed range at either the left or right end.
- Make a setting to satisfy the expression of "HTCN ≥ HDCN".
- Make a setting to satisfy the expression of "HTCN ≥ HSYNP + HSYNW + 1".
- Make a setting to satisfy the expression of "HSYNP ≥ HDCN + 1".
- The HDCN setting has restrictions depending on the resolution of the panel used. For details, refer to the description of the corresponding registers in the hardware manual.

[Notes on Vertical Direction Settings]

- Make a setting to satisfy the expression of "VTLN ≥ VDLN" and "VTLN ≥ 1".

Table 6 shows the LCDC registers used for setting the sync signals.

Table 6 Sync Signal Setting

Function	Register
Sets the horizontal sync signal	LCDC horizontal character number register (LDHCNR)
	LCDC horizontal sync signal register (LDHSYNR)
Sets the vertical sync signal	LCDC vertical display line number register (LDVDLNR)
	LCDC vertical total line number register (LDVTLNR)
	LCDC vertical sync signal register (LDVSYNR)

2.3.6 Setting the Power Management

The LCDC has a function to operate, in accordance with the specified sequence, three control signals for managing the power supply of the LCD module. Using this function enables power control of the LCD module to be synchronized with the display start and display stop of the LCDC. The external pins that can be controlled by this function are the following three pins (hereafter expressed as power management pins).

- LCDVCPWC pin: First pin to become high at display start and last pin to become low at display stop.
- LCDVEPWC pin: Second pin to become high at display start and second pin to become low at display stop.
- LCDDON pin: Last pin to become high at display start and first pin to become low at display stop.

Table 7 shows the LCDC registers used for setting the power management.

Table 7 Power Management Setting

Function	Register
Sets the timing for the power management pins	LCDC power management mode register (LDPMMR)
	LCDC power-supply sequence period register (LDPSPR)

Transitions of the signal levels of the power management pins at LCDC activation and termination are shown in figure 6.

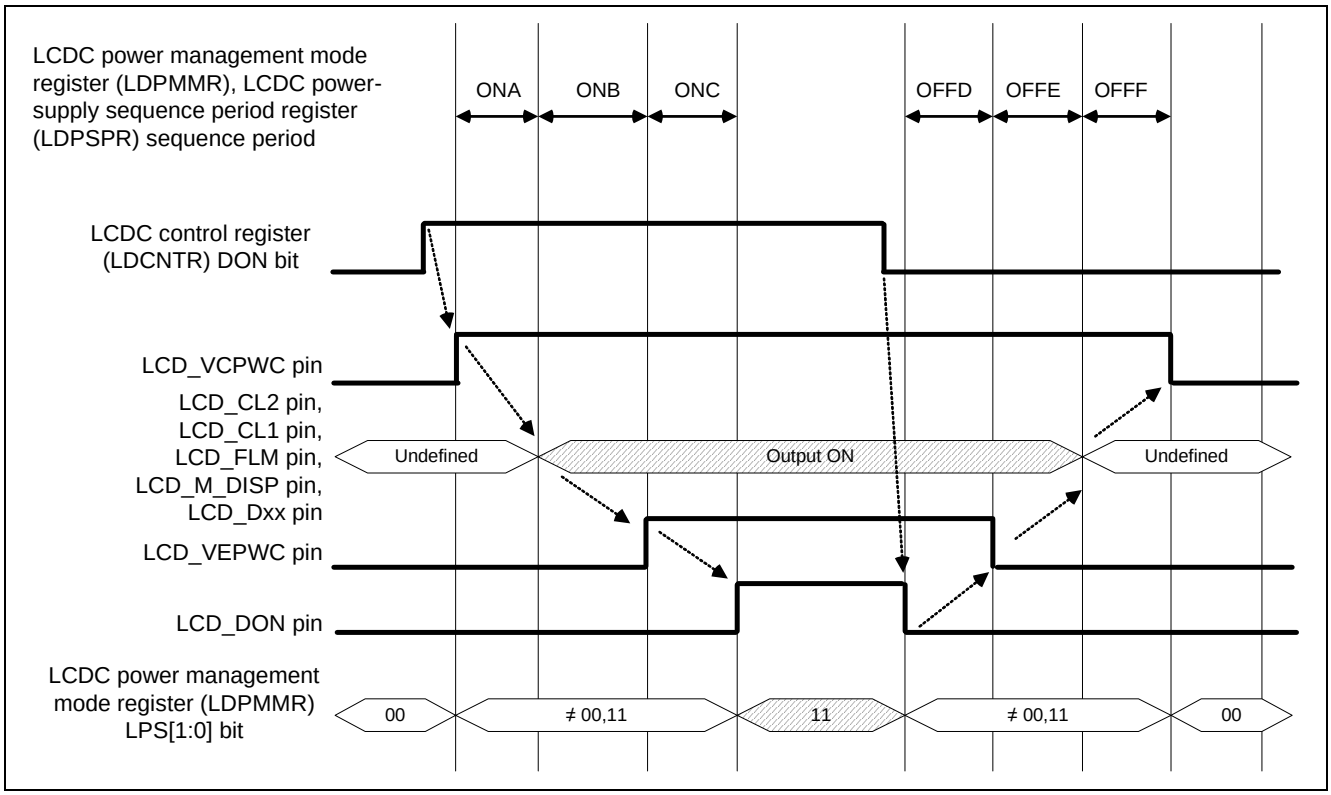

Figure 6 Transition Example of Power Management Pins

The delay between each signal is a number of frames equal to the value of the bits in LDPMMR and LDPSPR for setting the sequence interval. For details, please refer to the section 37.4.6 "Power-Supply Control Sequence" in the SH7763 Group Hardware Manual (REJ09B0256).

2.4 Activation and Termination of LCDC

Figure 7 shows a flowchart of activating the LCDC and starting display on the LCD module.

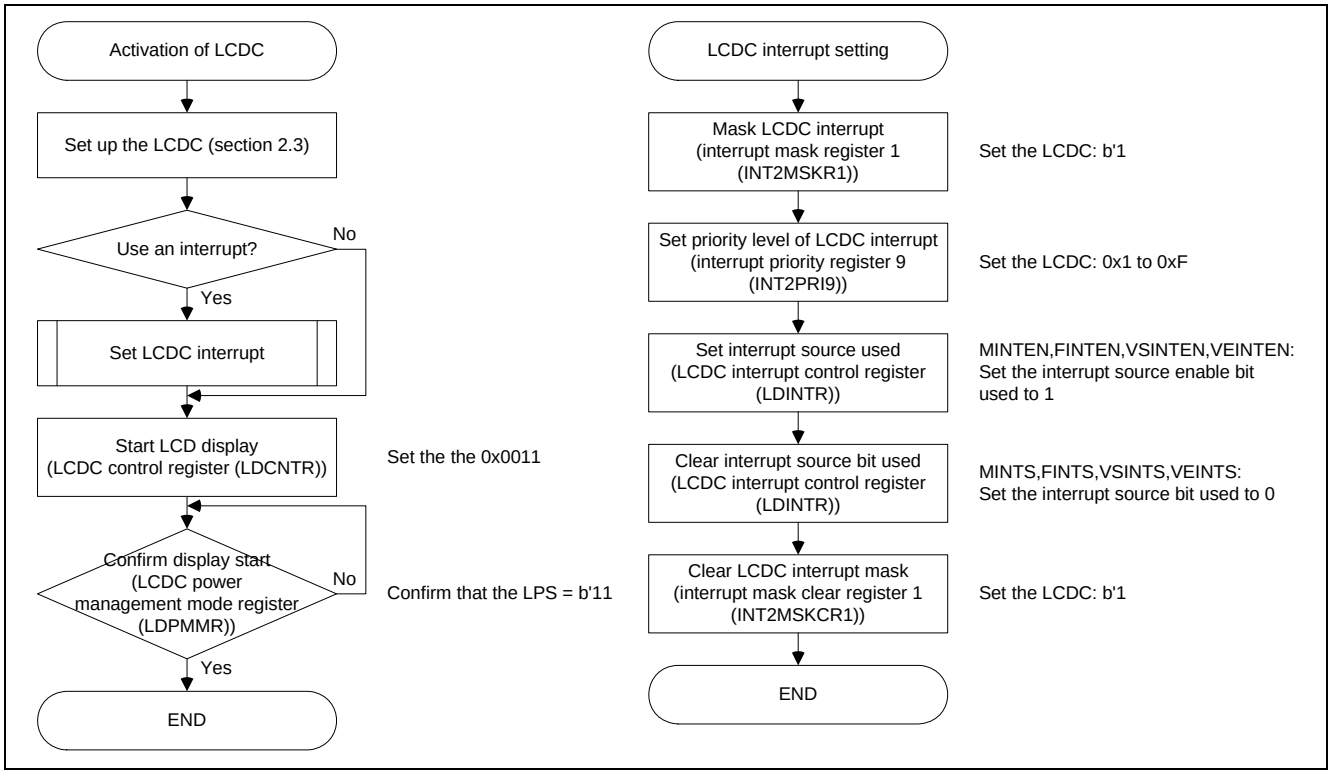

Figure 7 LCDC Activation Flow

Figure 8 shows a flowchart of terminating the LCDC and stopping display on the LCD module.

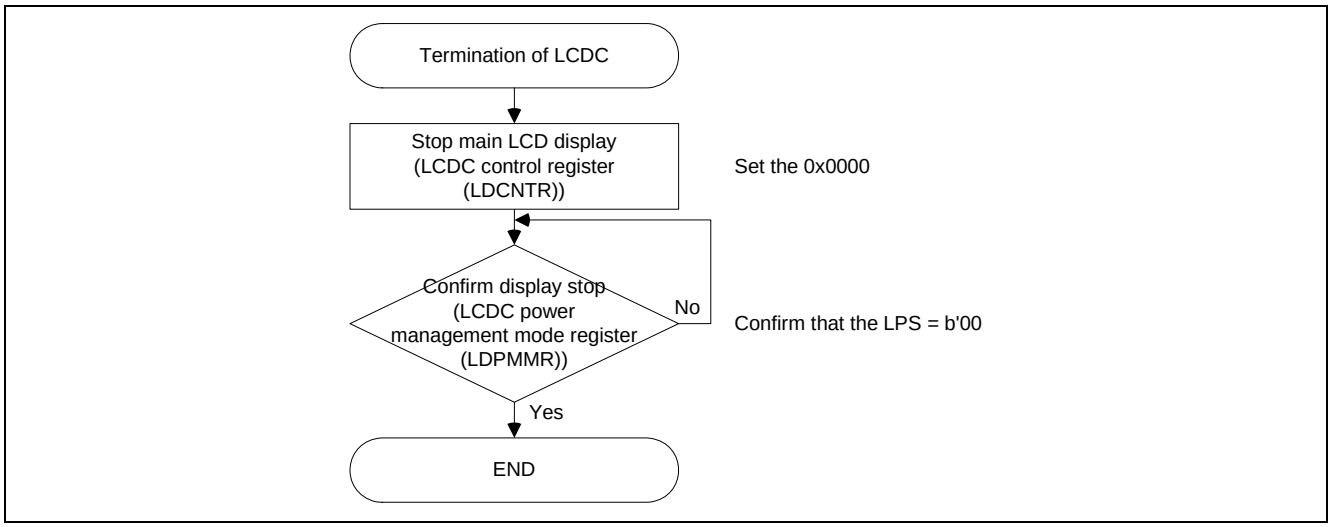

Figure 8 LCDC Termination Flow

- LCDC setup which is described in section 2.3 can be made in a random order. The setup can be started from any setting.
- When using an LCDC interrupt, start LCD display after enabling interrupts to be generated. If generation of an LCDC interrupt is enabled (interrupt mask is cleared, etc.) after display has already been started, an interrupt may occur at an undesired timing.
- To stop display, write 0x0000 to LDCNTR.
- Display start and display stop can be confirmed by the LPS bits in the LCDC power management mode register (LDPMMR), regardless of whether the power management function is used.

2.5 LCDC Synchronous Design

If there is only one frame buffer when the image data to be displayed by the LCDC is updated, while the LCDC is reading data from the frame buffer, new frame information is drawn to that same frame buffer. This causes the image to be distorted, such as, screen tearing. The necessary operations to avoid this are to prepare several frame buffers, and change the LCDC reading destination upon completion of drawing to the frame buffer whose contents are to be displayed next.

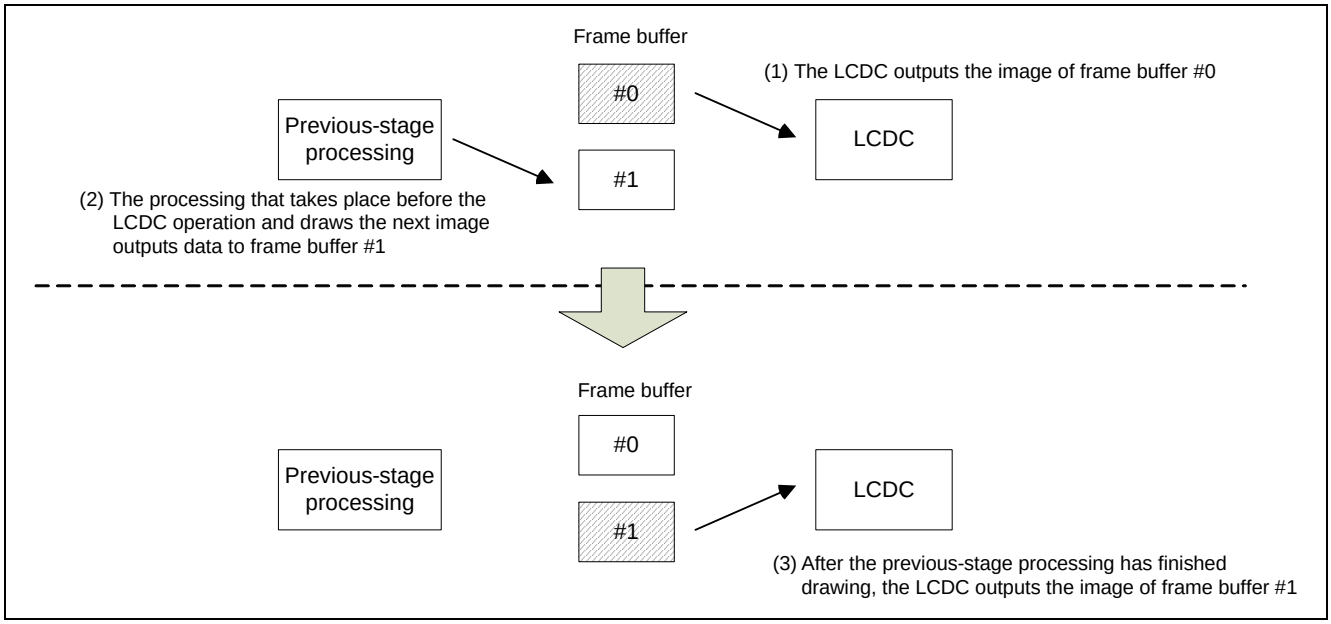

Figure 9 Overview of Plane Switching Operation

2.5.1 Multiple Buffer Switching by Changing the Fetch Start Address Register Setting

In this section, the plane being displayed is called the used plane and the plane not being displayed is called the unused plane. The information on the frame buffer to be displayed next is set to the unused plane, and upon completion of drawing to the frame buffer of the unused plane, the used plane and unused plane are switched and the new frame buffer is displayed.

[Plane Switching Method]

To switch the used plane, change the setting of the LCDC start address register for upper display data fetch (LDSARU) to the start address of the buffer of the unused plane within the interrupt handling routine with the LCDC interrupt timing.

- Figure 10 shows the timing chart for hardware switching. Shown here is an example of flag usage by software in order to achieve synchronization with the previous-stage processing.

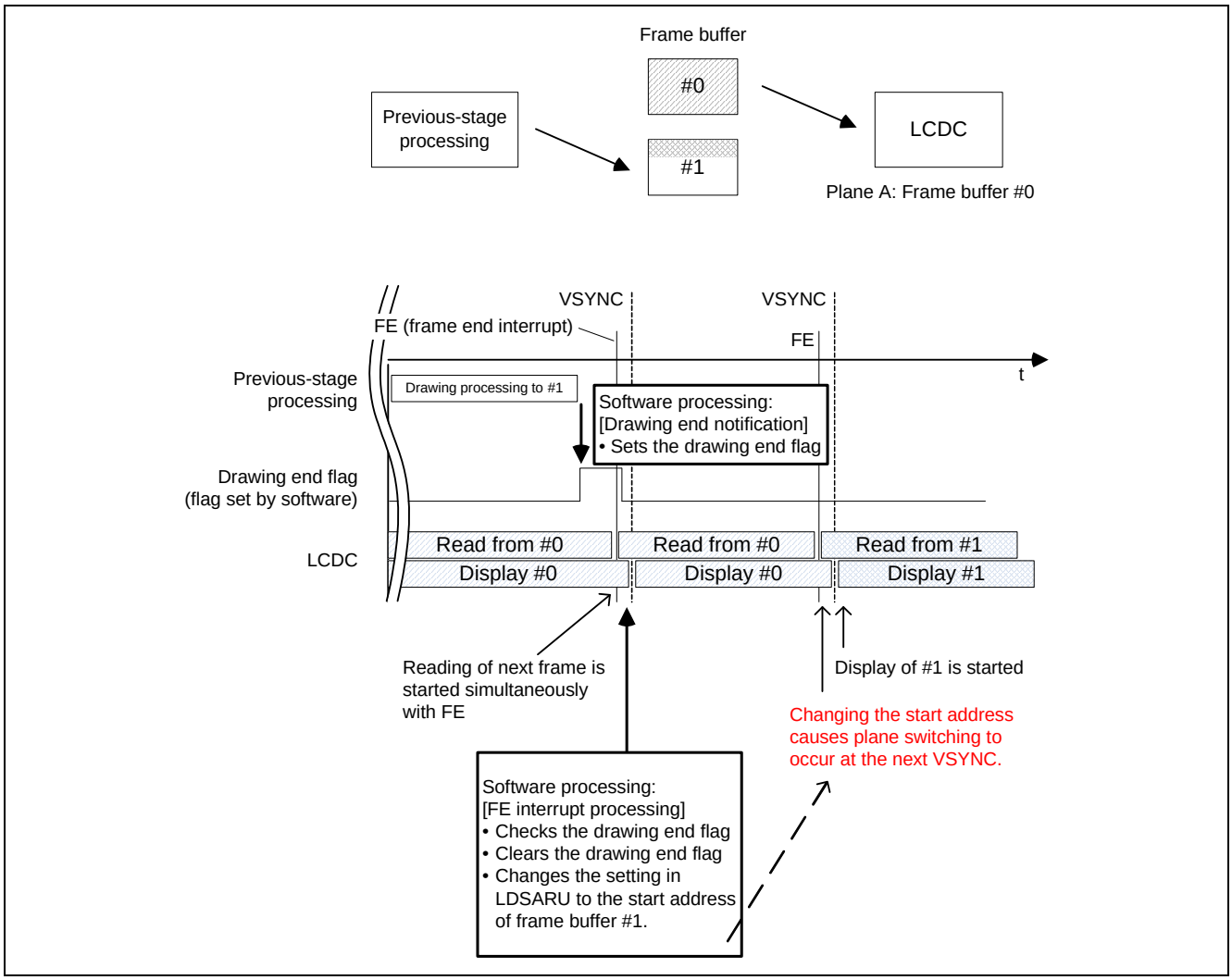

Figure 10 Timing of Software Switching Occurrence

The drawing end flag is set when the previous-stage processing has completed drawing. The LCDC monitors the drawing end flag by the frame end interrupt processing. If the flag is set, LDSARU is set to the start address of the unused-plane buffer. The LCDC updates the display image in the next frame after LDSARU is changed.

2.6 Usage Notes

2.6.1 Procedure for Halting Access to Display Data Storage VRAM

Follow the procedure below to halt access to VRAM for storing display data (DDR-SDRAM in area 3).

(1) Confirm that the LPS1 and LPS0 bits in LDPMMR are currently set to 1.
(2) Clear the DON bit in LDCNTR to 0 (display-off mode).
(3) Confirm that the LPS1 and LPS0 bits in LDPMMR have changed to 0.
(4) Wait for the display time for a single frame to elapse.

2.6.2 Writing to LDCNTR

Only 0x0011 and 0x0000 can be written to LDCNTR to start and stop display, respectively; do not write any other value to LDCNTR.

If 0x0011 or another value is overwritten to LDCNTR in any case other than when display is started, the LCDC will execute unstable and unexpected operations; correct operation is not guaranteed.

3. LCD Module Sizes Displayable in this LCDC

This LCDC is capable of controlling displays with up to 1024 × 1024 dots and 16 bpp. However, the image data for display is stored in the DDR-SDRAM connected to area 3, which is shared with the CPU and some peripheral functions. Accordingly, there may be some problems with the display when the CPU or other peripheral functions also access the DDR-SDRAM in area 3.

As a rough standard for the displayable LCD size, the bus occupation ratio shown below should not exceed 40%.

$$\text{Bus occupation rate (\%)} = \frac{\text{Overhead coefficient} \times \text{Total number of display pixels } ((\text{HDCN}+1) \times 8 \times (\text{VDLN}+1)) \times \text{Frame rate (Hz)} \times \text{Number of colors (bpp)}}{\text{CLKOUT (Hz)} \times \text{Bus width (bit)}} \times 100$$

Bus width (DDR-SDRAM in area 3, fixed): 32 bits
Overhead coefficient (fixed): 1.375

[Calculation Example]

Display size: 640 × 480 pixels
HDCN: 79
VDLN: 479
Frame rate: 60 Hz
Number of colors: 16 bpp
CLKOUT: 66 MHz

(1.375 × (79 + 1) × 8 × (479 + 1) × 60 × 16 × 100) / (66000000 × 32) = 19.2%

4. Description of the Sample Application

This section describes an example of pin connection and various settings as a sample application that uses the LCDC to display graphic images.

4.1 TFT-LCD Panel Specifications

The following shows the specifications of the TFT-LCD panel used in this sample application. As the details of the specifications differ depending on the TFT-LCD panel actually used in your system, please refer to the datasheet for the target LCD panel.

4.1.1 General Specifications

Table 8 lists the general specifications of the TFT-LCD panel used in this application.

Table 8 TFT-LCD Panel General Specifications (Excerpt from Datasheet)

Item	Specifications
Resolution	VGA or QVGA (VGA is used in this application)
Pixel format	H 480 × V 640 (Number of dots: H (480 × 3) × V640) * 1 pixel = R + G + B dots
Pixel configuration	R, G, B vertical stripe
Input signal	CMOS RGB (6 bits each, digital)

4.1.2 Pin Functions

Table 9 lists the pin functions of the TFT-LCD panel used in this application.

Table 9 TFT-LCD Panel Pin Functions (Excerpt from Datasheet)

Symbol	Description
RESB	Reset signal
INI	Power on control
DEN	Data enable signal
HSYNC	Horizontal synchronizing signal
VSYNC	Vertical synchronizing signal
CLKIN	System clock signal
R5-0	Red data signals (6 bits, MSB: R5, LSB: R0)
G5-0	Green data signals (6 bits, MSB: G5, LSB: G0)
B5-0	Blue data signals (6 bits, MSB: B5, LSB: B0)

4.1.3 Interface Timing

Table 10 lists the interface timing and characteristics of the TFT-LCD panel used in this application.

Table 10 TFT-LCD Panel Timing Characteristics (Excerpt from Datasheet)

Item		MODE	Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle time	VGA	t_{CLK}	38	39.7	41.7	ns
		QVGA		152	158.8	167	
HSYNC	Cycle time	VGA	t_{HS}	—	648	—	CLK
		QVGA		—	324	—	
	Horizontal back porch	VGA	t_{HBP}	28	78	166	
		QVGA		14	38	82	
	Horizontal front porch	VGA	t_{HFP}	0	88	138	
		QVGA		0	44	68	
	Valid display period	VGA	t_{HHW}	—	480	—	
		QVGA		—	240	—	
	Sync signal width		t_{HSW}	—	2	—	
VSYNC	Cycle time	VGA	t_{VS}	—	648	—	HSYNC
		QVGA		—	324	—	
	Vertical back porch	VGA	—	—	(1)	—	
		QVGA		—	(1)	—	
	Vertical front porch	VGA	—	—	(6)	—	
		QVGA		—	(2)	—	
	Valid display period	VGA	—	—	640	—	
		QVGA		—	320	—	
	Sync signal width		t_{VSW}	—	1	—	

Note: The vertical back porch and vertical front porch times are estimated from the timing chart because they are not specified in the AC characteristics table.

Table 11 shows an example of LCDC timing settings for VGA display calculated from the characteristics listed in table 10.

Table 11 Example of VGA Timing Settings

Function	Register	Bit Name	Number of Dot Clock	Setting Value Example
Horizontal timing settings	LCDC horizontal character number register (LDHCNR)	HTCN: Horizontal cycle – 1	648/8–1 = 80	0x50
		HDCN: Horizontal display period – 1	480/8–1 = 59	0x3B
	LCDC horizontal sync signal register (LDHSYNR)	HSYNW: Horizontal sync signal width – 1	8/8–1 = 0 *1	0x0
		HSYNP: (Horizontal display period + horizontal front porch) – 1	568/8–1 = 70	0x46
Vertical timing settings	LCDC vertical total line number register (LDVTLNR)	VTLN: Vertical cycle – 1	648–1 = 647	0x287
	LCDC vertical display line number register (LDVDLNR)	VDLN: Vertical display period – 1	640–1 = 639	0x27F
	LCDC vertical sync signal register (LDVSYNR)	VSYNW: Vertical sync signal width – 1	1–1	0x0
		VSYNP: (Vertical display period + vertical front porch) – 2 *2	648–1–2 = 645	0x285

Notes: *1 As the sync signal width for the TFT panel is 2, the minimum specifiable width (8) is used for this calculation.

*2 The vertical front porch width is calculated as (vertical period - vertical sync signal width) - 2 because it is not specified in the data sheet of the TFT panel.

4.2 TFT-LCD Panel Connection Circuit Example

4.2.1 Pin Connection Example

Figure 11 shows the TFT-LCD panel connection circuit example in this application.

In this example, five bits are connected for R, six bits for G, and five bits for B in the 18-bit bus of the TFT panel.

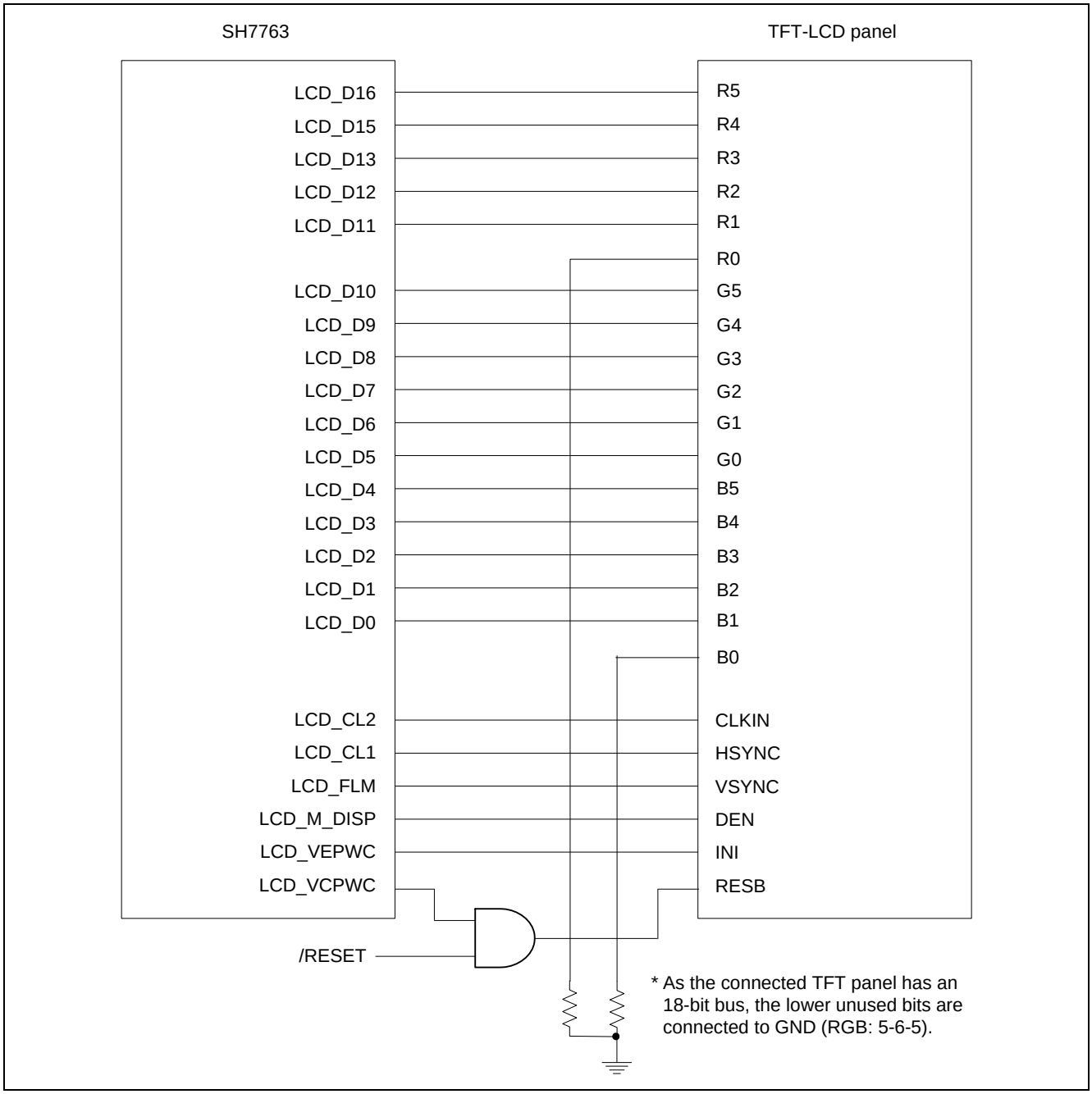

Figure 11 TFT-LCD Panel Connection Circuit Example

4.2.2 Power Management Setting

The LCDC power management function is specified as follows according to the power control timing requirements of the TFT-LCD panel used in this application.

[To Turn on the Power]

- Requirement (1): VCC (+3.3 V) should settle within a 2-frame period:
  → ONA is set to 1: The RESB timing is generated by the FPGA on the board, so this period should match the period used in the sample software provided with the board.
- Requirement (2): The sync signals and RGB data should be output before INI is driven high:
  → The RESB timing is generated by the FPGA on the board.
- Requirement (3): The RESB signal should be kept low for at least 20 µs after VCC (+3.3 V) has settled:
  → ONB is set to 6: The RESB timing is generated by the FPGA on the board, so this period should match the period used in the sample software provided with the board.
- Requirement (4): RESB should be driven high before INI:
  → The RESB timing is generated by the FPGA on the board.

[To Turn Off the Power]

- Requirement (5): The sync signal and RGB data output should be stopped and RESB should be driven low after 5-frame period has passed since INI is driven low:
  → OFFE is set to 6.
- Requirement (6): OFFF is set to 1 in this application although the TFT-LCD panel specifications do not prescribe such requirements.

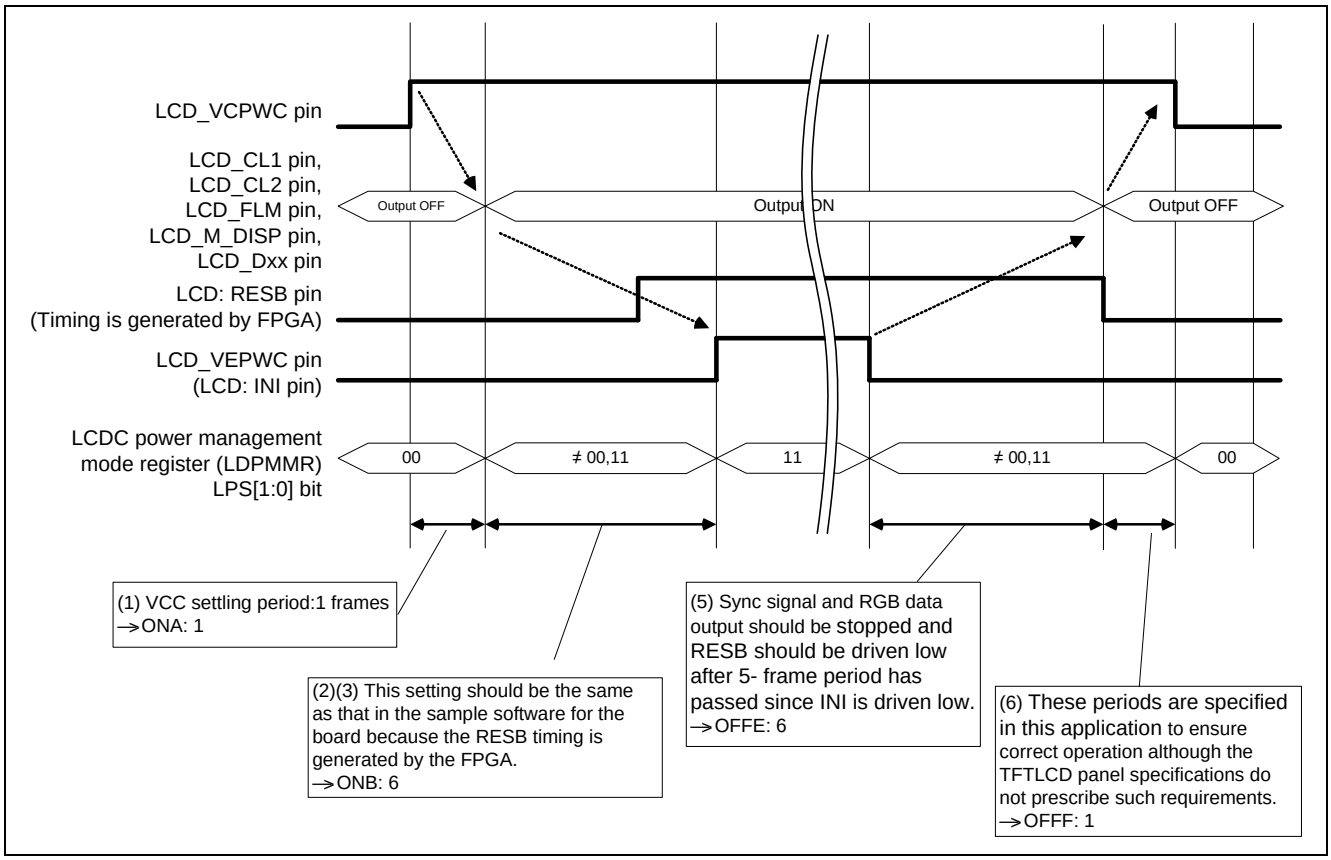

Figure 12 Example of Power Management Setting

4.3 Sample Program Specifications

This section describes the specifications of the sample program and shows the flowchart of each processing.

4.3.1 Specifications

(1) Displays in turn gradation images (gray-scale, red, green, and blue) drawn by the CPU on the VGA portrait (W480 × H640) TFT-LCD panel.
(2)Activates the LCDC, displays the images in turn with switching among four frame buffers, and then stops the LCDC.
(3) Repeats step (2) infinitely.
(4) Switches the planes by software.

4.3.2 Main Flowchart of the Sample Program

Figure 13 shows the main flowchart of the sample program.

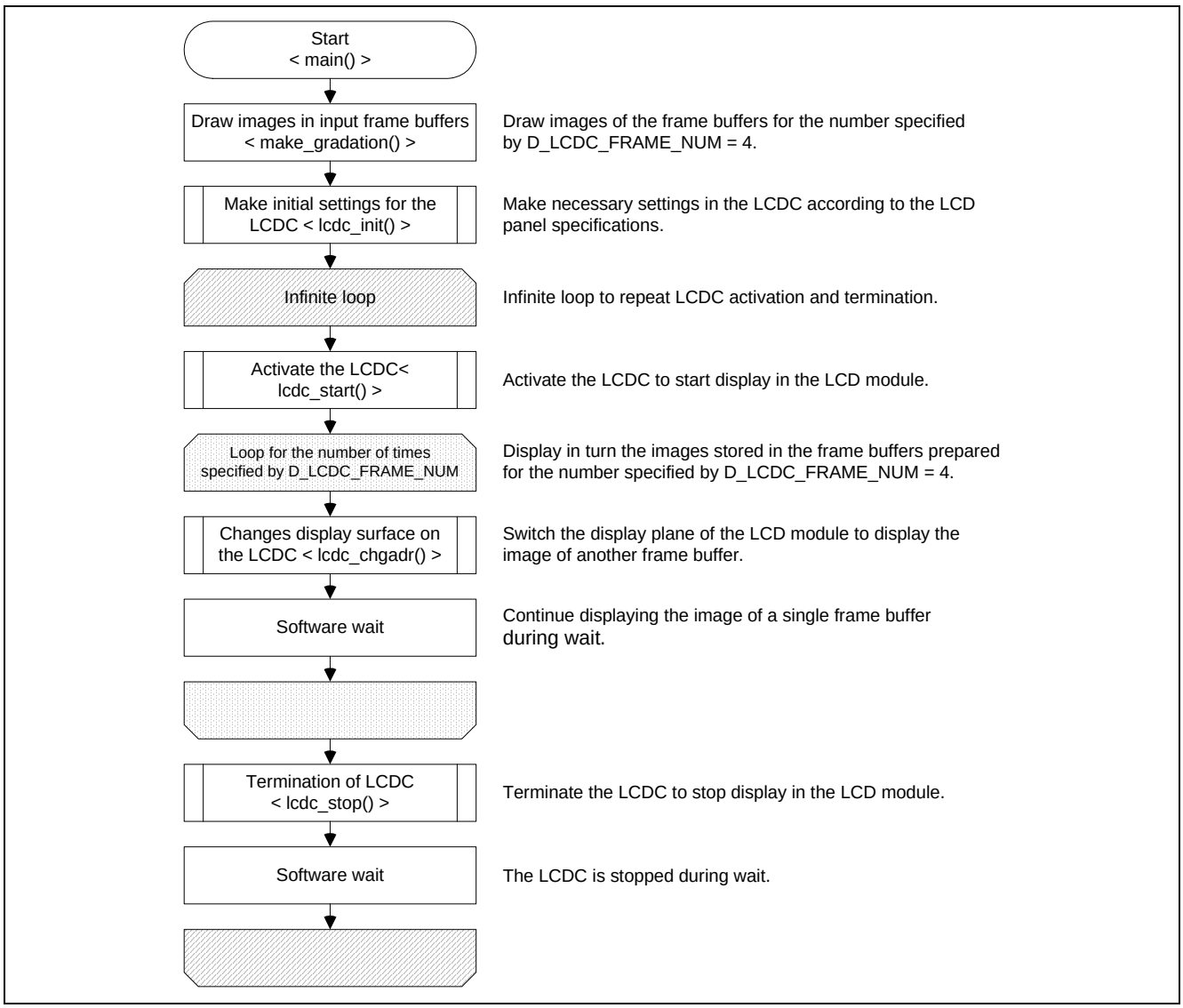

Figure 13 Main Flowchart of Sample Program

4.3.3 Initial Setting of the LCDC

Figure 14 to 16 shows the flowchart for initial setting of the LCDC.

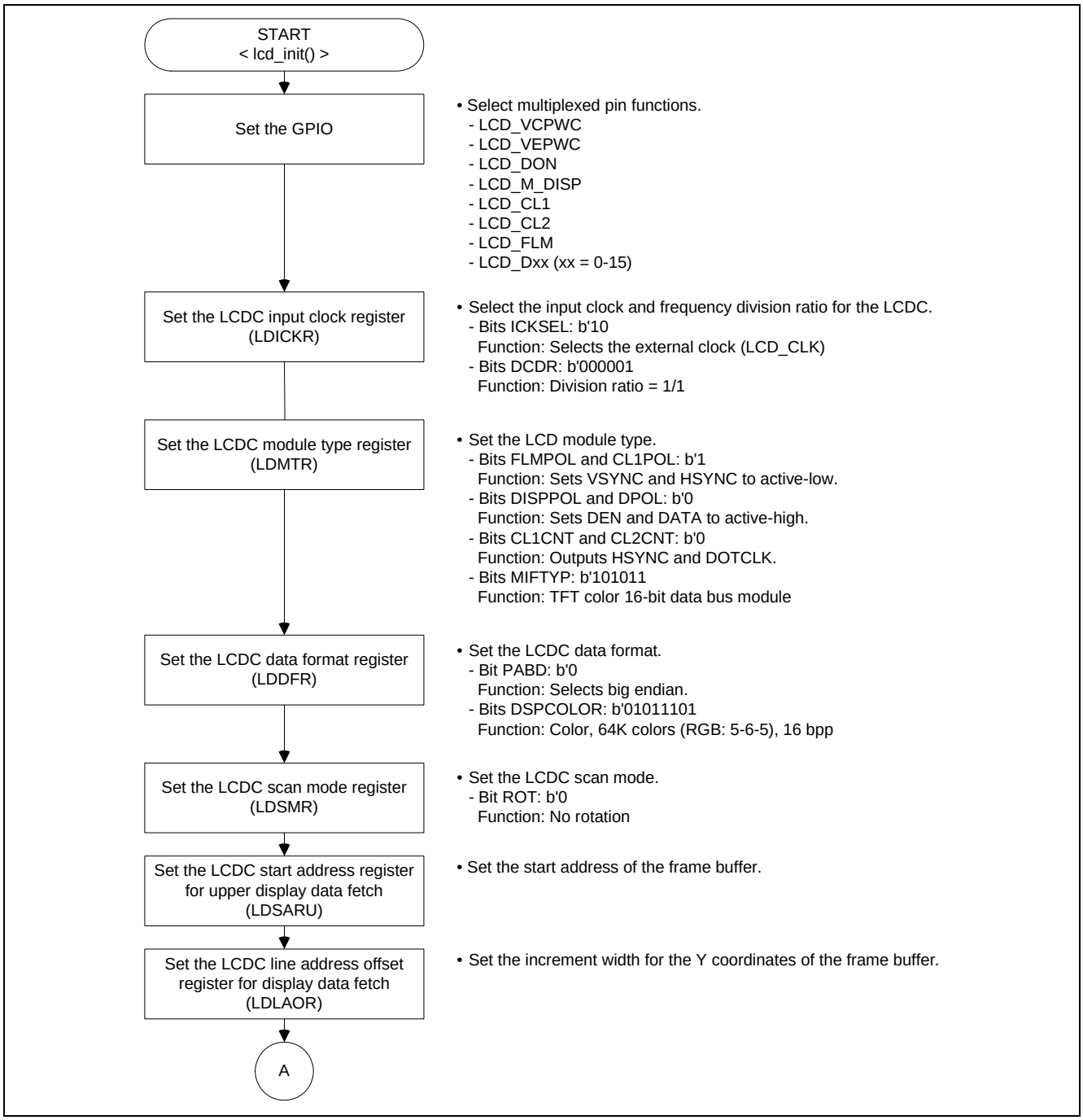

Figure 14 Flowchart for LCDC Initial Setting in Sample Program (1)

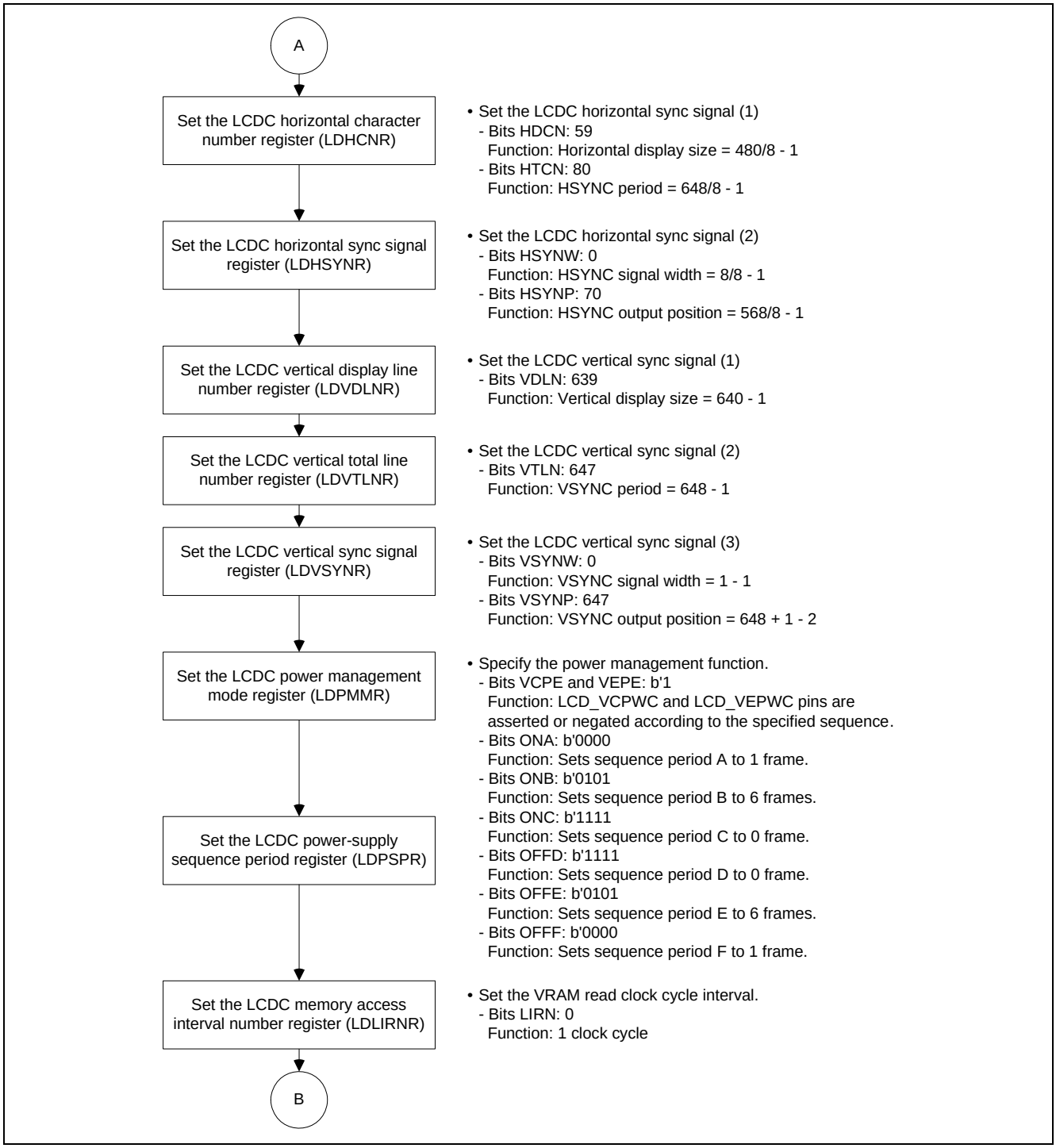

Figure 15 Flowchart for LCDC Initial Setting in Sample Program (2)

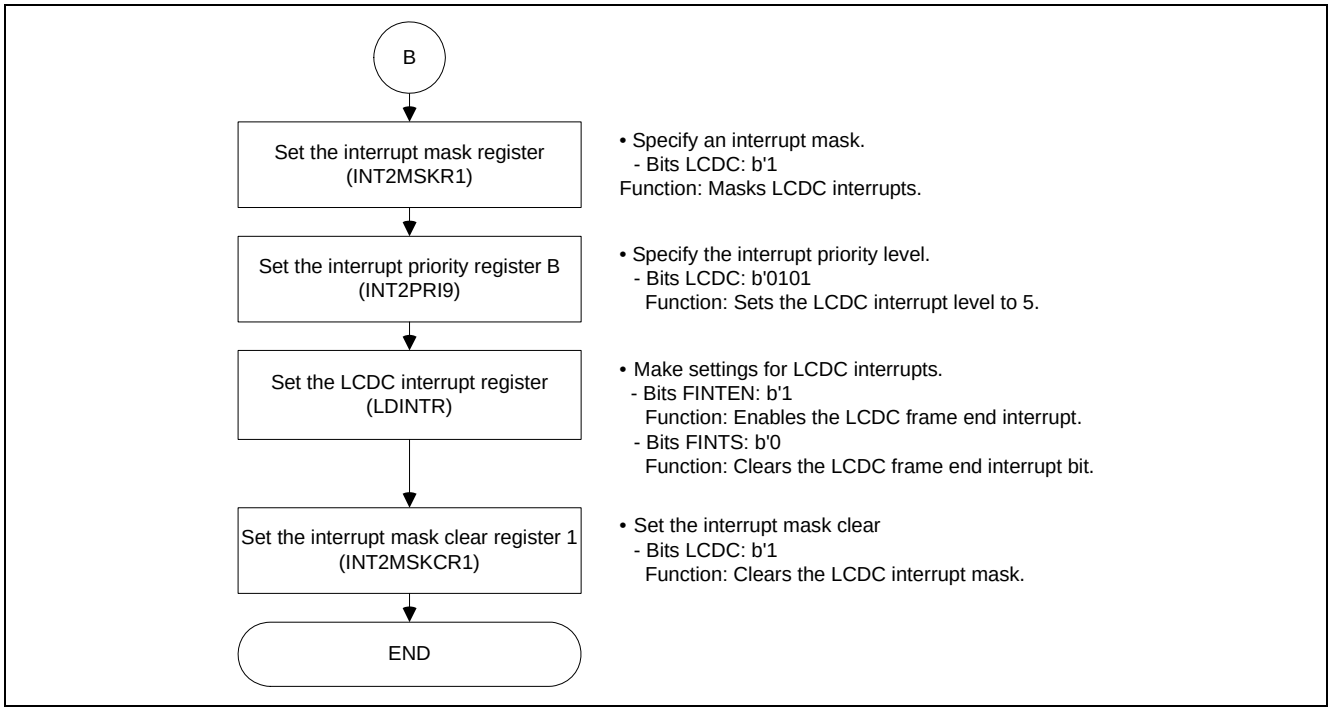

Figure 16 Flowchart for LCDC Initial Setting in Sample Program (3)

4.3.4 Starting and Stopping LCDC Display

Figure 17 shows the flowchart for starting LCDC display.

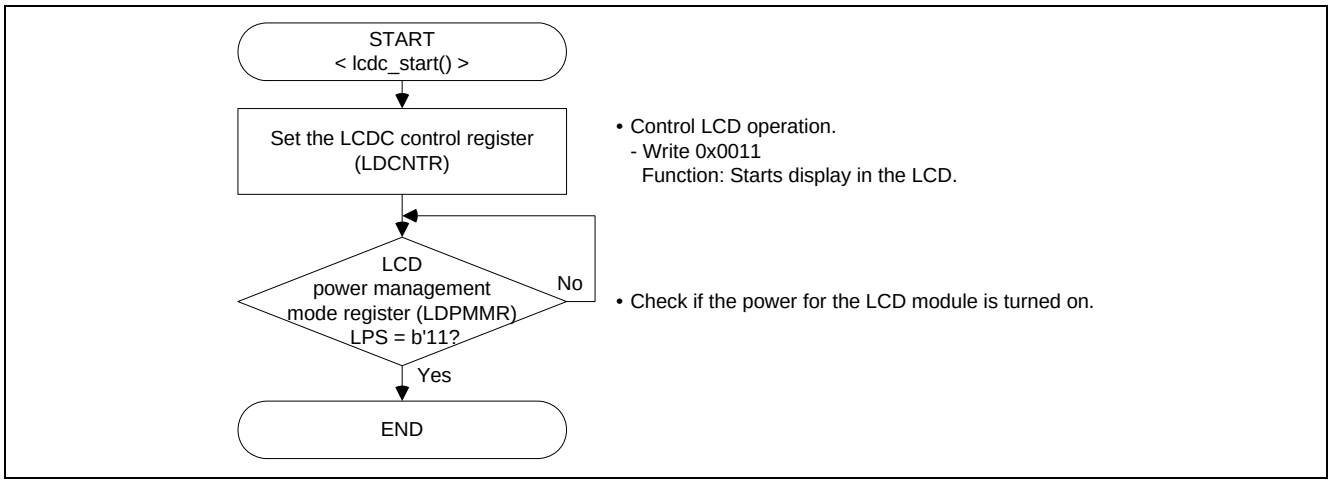

Figure 17 Flowchart for LCDC Activation in Sample Program

Figure 18 shows the flowchart for stopping LCDC display.

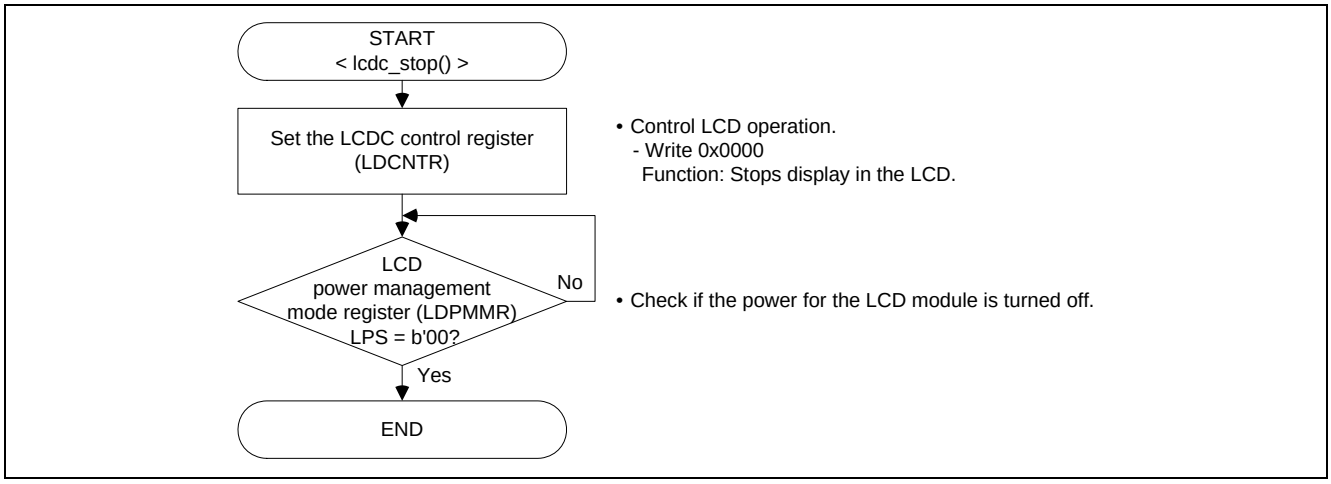

Figure 18 Flowchart for LCDC Termination in Sample Program

4.3.5 LCDC Plane Switching Settings

Figure 19 shows the flowchart for switching LCDC planes. This processing only sets the plane switching flag. The settings necessary for LCDC plane switching are made in the frame end interrupt processing.

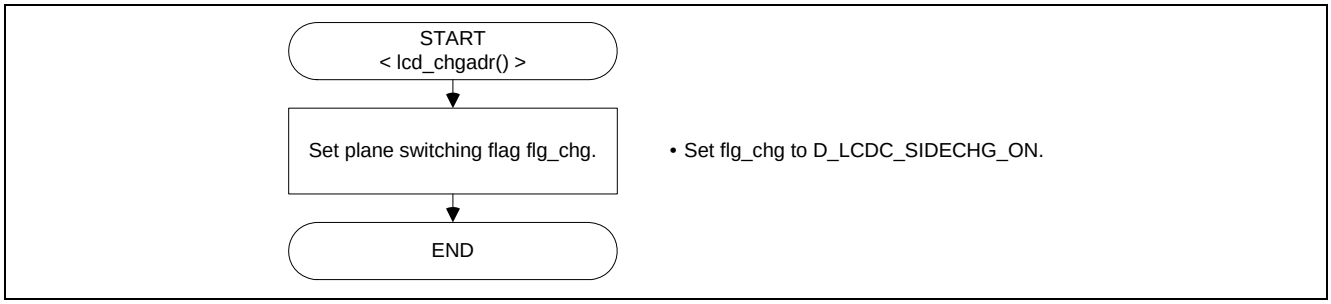

Figure 19 Flowchart for LCDC Plane Switching in Sample Program

4.3.6 LCDC Frame End Interrupt Settings

Figure 20 shows the flowchart for LCDC frame end interrupt processing. When the plane switching flag is set, this processing makes the necessary settings for plane switching in the LCDC. Plane switching is actually done at the end of the next frame. A wait is inserted for the INTC priority decision period (5 Pϕ clock cycles) so that clearing of end interrupt bit FINTS is reflected in the INTC.

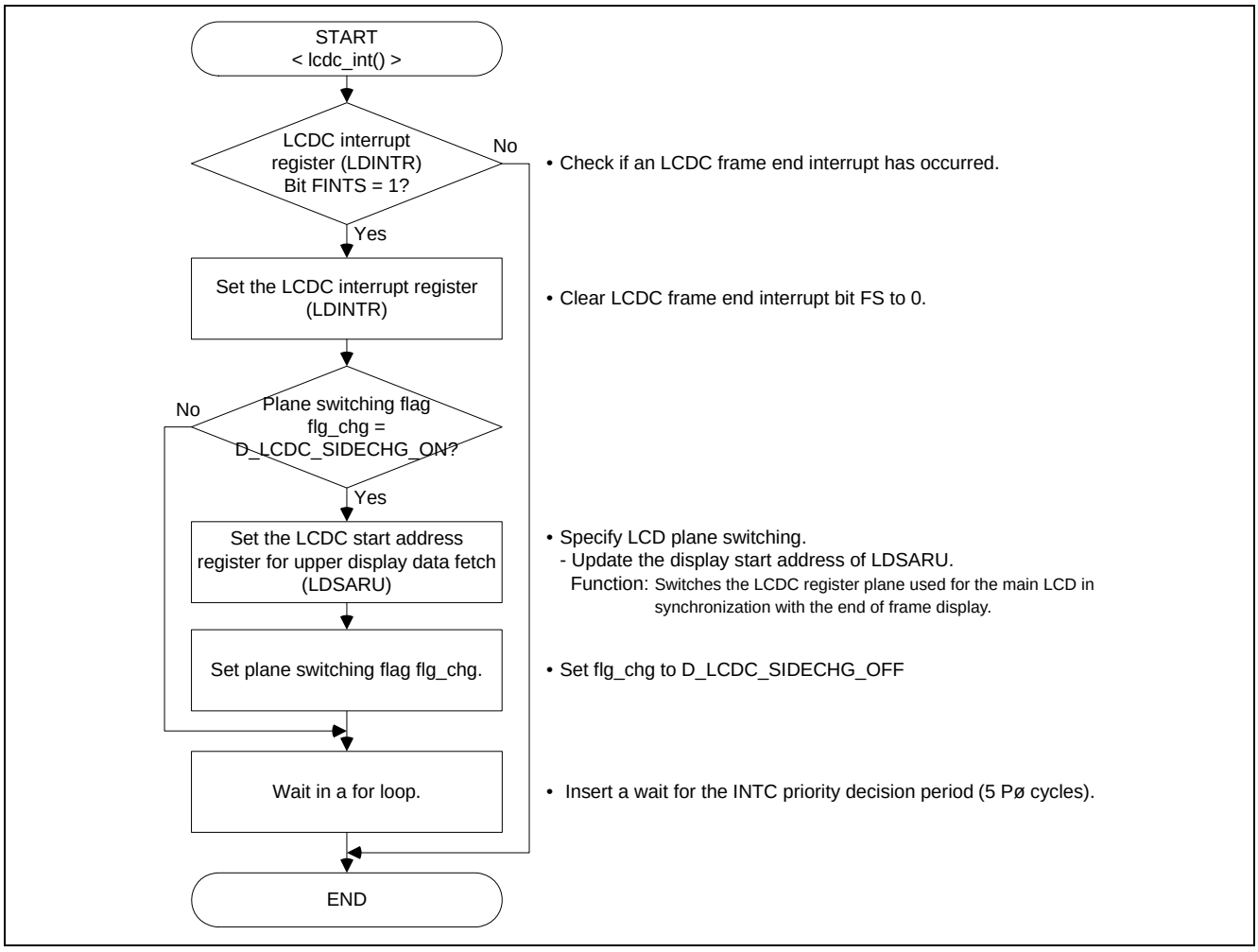

Figure 20 Flowchart for LCDC Frame End Interrupt in Sample Program

4.3.7 Section Allocation

Table 12 shows the allocation of the sections used in this application.

Table 12 Section Allocation

Section Name	Description	Area	Address (Virtual Address)	
P	Program area (with no specification)	ROM	0x00002000	P0 area (caching enabled and MMU address translation enabled)
C	Constant area	ROM		
C$BSEC	Structure for uninitialized data area addresses	ROM		
C$DSEC	Structure for initialized data area addresses	ROM		
D	Initialized data (initial values)	ROM		
B	Uninitialized data area	RAM	0x08000000	
R	Initialized data area	RAM		
S	Stack area	RAM	0x0FFFF9F0	
PINTHandler	Exception and interrupt handlers	ROM	0x80000400	P1 area (caching enabled and MMU address translation disabled)
VECTTBL	Reset vector table Interrupt vector table	ROM		
INTTBL	Interrupt mask table	ROM		
PIntPRG	Interrupt functions	ROM		
SP_S	Stack dedicated for TLB-miss handler	RAM	0x8FFFFDF0	
RSTHandler	Reset handlers	ROM	0xA0000000	P2 area (caching disabled and MMU address translation disabled)
PResetPRG	Reset programs	ROM		
PnonCACHE	Program area (cache-disabled access)	ROM		
B_LCD_BUFF	LCDC frame buffers	RAM	0xAE000000	

5. Listing of the Sample Program

(1) Sample Program Listing: "main.c"

```
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27    ***********************************************************************/
28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : main.c
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ***********************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*************************************************/
47
48    #include <machine.h>
49    #include "iodefine.h"
50    #include "lcdc.h"
51    #include "framebuf.h"
52
53    /* ==== Prototype declaration ==== */
54    void main(void);
55
56
57    /*""FUNC COMMENT""*****************************************************
58    * ID                    :
59    * Outline               : Sample program main
```

```
60    *                           : (Display by LCDC)
61    * Include                   :
62    * Declaration               : void main(void)
63    * Description               : Displays a VGA image on the main LCD. After a software
64    *                           : wait defined by LCDC_WAIT_CHGSIDE, repeats switching of
65    *                           : display planes, and then stops the display.
66    *                           : The display is restarted after a software wait defined
67    *                           : by LCDC_WAIT_STOP.
68    *                           :
69    * Limitation                :
70    *                           :
71    * Argument                  : None
72    * Return Value              : None
73    * Calling Functions         :
74    *""FUNC COMMENT END""*********************************************/
75    void main(void)
76    {
77        unsigned long j;
78
79        /* Draws an image in the frame buffer. */
80        make_gradation();
81
82        /* LCDC initialization : Displays a VGA image on the main LCD */
83        lcdc_init();
84
85        while(1)
86        {
87          /* LCDC activation : Starts display on the main LCD */
88            lcdc_start();
89
90          for(g_tbl_num=0;g_tbl_num<D_LCDC_FRAME_NUM;g_tbl_num++)
91            {
92
93                /* Switches LCDC display planes */
94              lcdc_chgadr();
95
96              /* Wait */
97              for(j=0;j<D_LCDC_WAIT_CHGSIDE;j++)
98                {
99
100               }
101           }
102           /* Stopping the LCDC : Stops display on the main LCD  */
103           lcdc_stop();
104
105         /* Wait */
106           for(j=0;j<D_LCDC_WAIT_STOP;j++)
107           {
108
109           }
110       }
111
112
113   }
114
115   /* End of File */
```

(2) Sample Program Listing: "framebuf.c"

```
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28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : framebuf.c
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ******************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*************************************************/
47
48
49    #include <machine.h>
50    #include "iodefine.h"
51    #include "framebuf.h"
52
53    unsigned long g_tbl_num  = 0;
54
55    /* ==== Frame buffer ==== */
56    #pragma section _LCD_BUFF
57    unsigned short lcdc_buf0[D_LCDC_HEIGHT][D_LCDC_WIDTH];
58    unsigned short lcdc_buf1[D_LCDC_HEIGHT][D_LCDC_WIDTH];
59    unsigned short lcdc_buf2[D_LCDC_HEIGHT][D_LCDC_WIDTH];
60    unsigned short lcdc_buf3[D_LCDC_HEIGHT][D_LCDC_WIDTH];
61    #pragma section
62
```

```
63    /* ==== Frame buffer table ==== */
64    void* tbl_lcdc_buf[4] = {
65        lcdc_buf0,
66        lcdc_buf1,
67        lcdc_buf2,
68        lcdc_buf3
69    };
70
71    /* ==== Prototype declaration ==== */
72    void make_gradation(void);
73
74
75    /*""FUNC COMMENT""*****************************************************
76    * ID                        :
77    * Outline                   : Sample program main
78    *                           : (Display by LCDC)
79    * Include                   :
80    * Declaration               : void make_gradation(void)
81    * Description               : Creates an image with gradation in RGB565 16-bpp format
82    *                           : in the frame buffer.
83    *                           :
84    * Limitation                :
85    *                           :
86    * Argument                  : None
87    * Return Value              : None
88    * Calling Functions         :
89    *""FUNC COMMENT END""*********************************************/
90    void make_gradation(void)
91    {
92        static unsigned long i;
93        static unsigned long j;
94        unsigned short pixel0 = 0;
95        unsigned short pixel1 = 0;
96        unsigned short pixel2 = 0;
97        unsigned short pixel3 = 0;
98
99        for(i=0;i<D_LCDC_HEIGHT;i++)
100       {
101           for(j=0;j<D_LCDC_WIDTH;j++)
102           {
103               lcdc_buf0[i][j] = pixel0;
104               lcdc_buf1[i][j] = pixel1;
105               lcdc_buf2[i][j] = pixel2;
106               lcdc_buf3[i][j] = pixel3;
107
108               if( ( j != 0 ) && ( (j%60) == 0 ) )
109               {
110                   pixel0 += D_LCDC_PATTERN0;
111                   pixel1 += D_LCDC_PATTERN1;
112                   pixel2 += D_LCDC_PATTERN2;
113                   pixel3 += D_LCDC_PATTERN3;
114               }
115           }
116           pixel0 = 0;
117           pixel1 = 0;
118           pixel2 = 0;
119           pixel3 = 0;
120       }
121   }
122
123
124   /* End of File */
```

(3) Sample Program Listing: "framebuf.h"

```
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27    ***********************************************************************/
28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : framebuf.h
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ********************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*************************************************/
47
48    #ifndef _FRAMEBUF_H_
49    #define _FRAMEBUF_H_
50
51    /* ==== Macro definition ==== */
52    #define  D_LCDC_FRAME_NUM        4
53
54    #define  D_LCDC_WIDTH        480 /* Width of the image */
55    #define  D_LCDC_HEIGHT       640 /* Height of the image */
56
57    #define D_LCDC_PATTERN0 0x2000
58    #define D_LCDC_PATTERN1 0x0100
59    #define D_LCDC_PATTERN2 0x0004
60    #define D_LCDC_PATTERN3 0x2104
61
```

```
62    /* ==== Frame buffer ==== */
63    extern void* tbl_lcdc_buf[D_LCDC_FRAME_NUM];
64
65    /* ==== Variable declaration ==== */
66    extern unsigned long g_tbl_num ;
67
68    #endif /* _FRAMEBUF_H_ */
69    /* End of File */
```

(4) Sample Program Listing: "lcdc.c"

```
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27    ***********************************************************************/
28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : lcdc.c
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ******************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*********************************************/
47
48
49    #include <machine.h>
50    #include "iodefine.h"
51    #include "lcdc.h"
52    #include "framebuf.h"
53
54
55
56    long g_flg_chg = D_LCDC_SIDECHG_OFF;
57
58    /*""FUNC COMMENT""*************************************************
59    * ID                      :
60    * Outline                 : Sample program main
61    *                         : (Display by LCDC)
```

```
62    * Include                 :
63    * Declaration             : void lcdc_init(void)
64    * Description             : Initializes the LCDC.
65    *                         : Makes necessary settings to enable display on the main LCD.
66    *                         :
67    *                         :
68    *                         :
69    * Limitation              :
70    *                         :
71    * Argument                : None
72    * Return Value            : None
73    * Calling Functions       :
74    *""FUNC COMMENT END""*********************************************/
75    void lcdc_init()
76    {
77        unsigned long dummy;
78
79        /* GPIO setting */
80        /* ---- Pin select registers ---- */
81        GPIO.PSEL2.BIT.PTSEL25 = 0;
82        GPIO.PSEL2.BIT.PTSEL24 = 0;
83        GPIO.PSEL2.BIT.PTSEL22 = 0;
84        GPIO.PSEL3.BIT.PTSEL33 = 0;
85        GPIO.PSEL3.BIT.PTSEL31 = 0;
86        GPIO.PSEL3.BIT.PTSEL30 = 0;
87
88        /* ---- Port control registers --- */
89        GPIO.PICR.BIT.PI5MD = 0;
90        GPIO.PJCR.WORD = 0x0000;
91        GPIO.PKCR.WORD = 0x0000;
92        GPIO.PLCR.WORD = 0x0000;
93
94        /* ---- Clock selection and division ratio setting ---- */
95        LCDC.LDICKR.WORD = 0x2101;
96          /* bits 13:12 (ICKSEL) = 01: Uses LCD_CLK (external pin). */
97          /* bits 5:0 (DCDR) = 000001: Specifies division ratio 1/1. */
98
99        /* ---- Pin polarity selection ---- */
100       LCDC.LDMTR.WORD = 0xC42B;
101         /* bit 15 (FLMPOL) = 1        Sets Vsync to active-low. */
102         /* bit 14 (CL1POL) = 1        Sets Hsync to active-low. */
103         /* bit 13 (DISPPOL) = 0           Sets DEN to active-high. */
104         /* bit 12 (DPOL) = 0          Sets DATA to active-high. */
105         /* bit 10 (MCNT) = 1          Does not output the M signal. */
106         /* bit 9 (CL1CNT) = 0         Outputs Hsync during vertical blanking period. */
107         /* bit 8 (CL2CNT) = 0         Outputs DotCLK during vertical blanking period. */
108         /* bits 5:0 (MIFTYP) = 101011     16-bit color TFT */
109
110       /* ---- Data format setting ---- */
111       LCDC.LDDFR.WORD = 0x002D;
112         /* bit 8 (PABD) = 0           Big endian */
113         /* bits 6:0 (DSPCOLOR) = 0101101  64k colors (RGB5-6-5) */
114
115       /* ---- Scan mode setting ---- */
116       LCDC.LDSMR.WORD = 0x0000;
117         /* No rotation */
118
119       /* Setting for reading image from external memory ----*/
120       LCDC.LDSARU = (void *)(unsigned long )tbl_lcdc_buf[0];
121
122       /* ---- Line offset setting ----*/
123       LCDC.LDLAOR = LINE_OFFSET * DATA_FORMAT;
124
```

```
125       /* ---- Horizontal display character and total character number setting ---- */
126       LCDC.LDHCNR.BIT.HDCN = (TFT_PANEL_CLOCK / 8) - 1;
127       LCDC.LDHCNR.BIT.HTCN = (TFT_TOTAL_CLOCK / 8) - 1;
128
129       /* ---- Vertical display line and total line number setting ---- */
130       LCDC.LDVDLNR.BIT.VDLN = TFT_PANEL_LINE - 1;
131       LCDC.LDVTLNR.BIT.VTLN = TFT_TOTAL_LINE - 1;
132
133       /* ---- Horizontal and vertical sync signal timing setting ---- */
134       LCDC.LDHSYNR.BIT.HSYNW = (TFT_HSYNC_WIDTH / 8) - 1;
135       LCDC.LDHSYNR.BIT.HSYNP = (TFT_HSYNC_START / 8) - 1;
136       LCDC.LDVSYNR.BIT.VSYNW = TFT_VSYNC_WIDTH - 1;
137       LCDC.LDVSYNR.BIT.VSYNP = (TFT_TOTAL_LINE - TFT_VSYNC_WIDTH) - 2;
138
139       /* ---- Power control pin setting ---- */
140       LCDC.LDPMMR.WORD = 0xFF60;
141         /* bits [15:12] (ONC) = 1111  ONC: 0xVSYNC */
142         /* bits [11:8] (OFFD) = 1111  OFFD: 0xVSYNC */
143         /* bit [6] (VCPE) = 1     Uses the LCD_VCPWC pin. */
144         /* bit [5] (VEPE) = 1     Uses the LCD_VEPWC pin. */
145       LCDC.LDPSPR.WORD = 0x0550;
146         /* bits [15:12] (ONA) = 0000  ONA: 1xVSYNC */
147         /* bits [11:8] (ONB) = 0101   ONB: 6xVSYNC */
148         /* bits [7:4] (OFFE) = 0101   OFFE: 6xVSYNC */
149         /* bits [3:0] (OFFF) = 0000   OFFF: 1xVSYNC */
150
151       /* ---- VRAM read clock cycle interval setting ---- */
152       LCDC.LDLIRNR.WORD = 0x0000;
153
154       /* Interrupt setting */
155       /* LCDC interrupt masking */
156       INTC.INT2MSKR1.BIT._LCDC= 1;
157       /* LCDC interrupt priority setting */
158       INTC.INT2PRI9.BIT._LCDC = 5;
159       /* LCDC module interrupt setting */
160       LCDC.LDINTR.WORD = D_LCDC_INT_ON;
161       /* LCDC module interrupt source clearing */
162       LCDC.LDINTR.WORD &= ~D_LCDC_INT_FLG;
163       /* LCDC interrupt mask clearing */
164       INTC.INT2MSKCR1.BIT._LCDC   = 1;
165
166   }
167
168   /*""FUNC COMMENT""************************************************
169   * ID                    :
170   * Outline               : Sample program main
171   *                       : (Display by LCDC)
172   * Include               :
173   * Declaration           : void lcdc_start(void)
174   * Description           : Activates the LCDC.
175   *                       :
176   * Limitation            :
177   *                       :
178   * Argument              : None
179   * Return Value          : None
180   * Calling Functions     :
181   *""FUNC COMMENT END""*****************************************/
182   void lcdc_start(void)
183   {
184       /* ---- Starting LCDC display ---- */
185       LCDC.LDCNTR = 0x0011;
186         /* bit [4] (DON2) = 1  Starts LCDC display operation. */
187         /* bit [0] (DON)  = 1  Display-on mode */
```

```
188
189       /* Waits until the status changes to "displaying". */
190       while( LCDC.LDPMMR.BIT.LPS != 3 )
191       {
192           /* DO NOTHING */
193       }
194   }
195
196   /*""FUNC COMMENT""************************************************
197   * ID                        :
198   * Outline                   : Sample program main
199   *                           : (Display by LCDC)
200   * Include                   :
201   * Declaration               : void lcdc_chgadr(void)
202   * Description               : Sets the LCDC plane switching flag.
203   *                           :
204   * Limitation                :
205   *                           :
206   * Argument                  : None
207   * Return Value              : None
208   * Calling Functions         :
209   *""FUNC COMMENT END""*******************************************/
210   void lcdc_chgadr(void)
211   {
212       /* Sets the display start address change timing flag. */
213       g_flg_chg = D_LCDC_SIDECHG_ON;
214   }
215
216   /*""FUNC COMMENT""************************************************
217   * ID                        :
218   * Outline                   : Sample program main
219   *                           : (Display by LCDC)
220   * Include                   :
221   * Declaration               : void lcdc_stop(void)
222   * Description               : Stops the LCDC.
223   *                           :
224   * Limitation                :
225   *                           :
226   * Argument                  : None
227   * Return Value              : None
228   * Calling Functions         :
229   *""FUNC COMMENT END""*******************************************/
230   void lcdc_stop(void)
231   {
232       /* ---- Stops LCDC display operation ---- */
233       LCDC.LDCNTR = 0x0000;
234         /* bit [0] (DON)  = 0   Display-off mode */
235
236       /* Waits until the status changes to "stopped". */
237       while( LCDC.LDPMMR.BIT.LPS != 0 )
238       {
239           /* DO NOTHING */
240       }
241   }
242
243   /* End of File */
```

(5) Sample Program Listing: "lcdc.h"

```
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27    ***********************************************************************/
28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : lcdc.h
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ***********************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*************************************************/
47
48    #ifndef _LCDC_H_
49    #define _LCDC_H_
50
51    /* ==== Macro definition ==== */
52    /* ---- TFT LCD module ---- */
53    #define      TFT_TOTAL_CLOCK    648     /* Width including blanking period        */
54    #define      TFT_TOTAL_LINE     648     /* Height including blanking period      */
55    #define      TFT_PANEL_CLOCK    480     /* Number of pixels in horizontal direction */
56    #define      TFT_PANEL_LINE     640     /* Number of pixels in vertical direction   */
57    #define      TFT_H_FRONT_PORCH  88      /* Horizontal front porch      */
58    #define      TFT_HSYNC_START    (TFT_PANEL_CLOCK + TFT_H_FRONT_PORCH)
59                                /* Horizontal display start position  */
60    #define      TFT_HSYNC_WIDTH    8       /* Hsync pulse width (8 dots min.) */
61    #define      TFT_VSYNC_WIDTH    1       /* Vsync pulse width */
```

```
62    #define      LINE_OFFSET        480 /* Line offset */
63    #define     DATA_FORMAT         2   /* Display data size (bytes) */
64
65    /* ---- Wait time setting ---- */
66    #define  D_LCDC_WAIT_CHGSIDE         (266000000/2*1) /* Frequency / (number of instructions
67                                          in the for loop) x seconds */
68    #define  D_LCDC_WAIT_STOP            (266000000/2*1) /* Frequency / (number of instructions
69                                          in the for loop) x seconds */
70
71    /* ---- LCDC interrupts ---- */
72    #define D_LCDC_INT_ON  0x4000
73    #define D_LCDC_INT_FLG  0x0400
74
75    enum {
76        D_LCDC_SIDECHG_OFF = 0,
77        D_LCDC_SIDECHG_ON,
78    };
79
80    /* ==== Function declaration ==== */
81    void lcdc_init(void);
82    void lcdc_start(void);
83    void lcdc_chgadr(void);
84    void lcdc_stop(void);
85    void lcdc_int(void);
86
87    /* ==== Variable declaration ==== */
88    extern long g_flg_chg;
89
90    #endif /* _LCDC_H_ */
91    /* End of File */
```

(6) Sample Program Listing: "intprg.c"

```
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27    ***********************************************************************/
28    /* Copyright (C) 2010. Renesas Electronics Corporation., All Rights Reserved.  */
29    /*""FILE COMMENT""************ Technical reference data ****************
30    * System Name  : SH7763 Sample Program
31    * File Name    : intprg.c
32    * Abstract     : Sample Program for SH7763 LCDC Display
33    * Version      : Ver 1.00
34    * Device       : SH7763
35    * Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36    *              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37    * OS           : None
38    * H/W Platform : MS7763SE02
39    * Description  : Sample Program for SH7763 LCDC Display
40    *              :
41    * Operation    :
42    * Limitation   :
43    *              :
44    ******************************************************************
45    * History      : 08.July.2010 Ver. 1.00 First Release
46    *""FILE COMMENT END""*********************************************/
47
48    #include <machine.h>
49    #include "iodefine.h"
50    #include "framebuf.h"
51    #include "lcdc.h"
52
53    #define I_DIV_P         4 /* Ick:Pck0 = 4:1 */
54    #define INST_NUM        2 /* instruction number of for loop */
55    #define PCLK_5CYC       ( 5 * I_DIV_P / 2)

      Omitted
```

```
255   /* H'620 LCDC */
256   /*""FUNC COMMENT""************************************************
257   * ID                    :
258   * Outline               : Sample program main
259   *                       : (Display by LCDC)
260   * Include               :
261   * Declaration           : void INT_LCDCI(void)
262   * Description           : Initializes the LCDC.
263   *                       : Makes necessary settings to enable display on the main LCD.
264   *                       :
265   *                       :
266   *                       :
267   * Limitation            :
268   *                       :
269   * Argument              : None
270   * Return Value          : None
271   * Calling Functions     :
272   *""FUNC COMMENT END""*****************************************/
273   void INT_LCDCI(void)
274   {
275       unsigned long i;
276
277
278       if( LCDC.LDINTR.WORD & D_LCDC_INT_FLG)
279       {
280           LCDC.LDINTR.WORD &= ~D_LCDC_INT_FLG;
281
282           if( g_flg_chg == D_LCDC_SIDECHG_ON )
283           {
284               LCDC.LDSARU = tbl_lcdc_buf[g_tbl_num]; /* Updates the display start address. */
285            g_flg_chg = D_LCDC_SIDECHG_OFF;
286           }
287
288         /* Waits for the INTC priority determination time. */
289         for(i=0;i<PCLK_5CYC;i++)
290         {
291             /* DO NOTHING */
292         }
293       }
294   }

      Omitted
```

6. Execution Results

When the above sample application is executed, the following processes will be repeated.

- The power for the LCD module is turned on.
- The red gradation pattern is displayed.
- The green gradation pattern is displayed.
- The blue gradation pattern is displayed.
- The gray gradation pattern is displayed.
- The power for the LCD module is turned off.
- The power for the LCD module is turned on (the above steps are repeated infinitely).

7. Documents for Reference

- Software Manual
  SH-4A Software Manual (REJ09B0003)
  (The most up-to-date versions of the documents are available on the Renesas Electronics Website.)
- Hardware Manual
  SH7763 Group Hardware Manual (REJ09B0256)
  (The most up-to-date versions of the documents are available on the Renesas Electronics Website.)

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct 27, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
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Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
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Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
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