

SH7734 Group

R01AN0898EJ0100

Rev.1.00

Example of Ethernet Receive Settings

Aug 30, 2012

Introduction

This application note presents a sample program for making Ethernet receive settings on the SH7734.

Positioning of This Document

This application note is based on the sample program in SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ) and presents a sample program for making settings for the Ethernet function. A description of the sample program for initial settings is omitted. Please refer to the application note SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ).

Target Device

SH7734 Group

In order to use the sample program described in this application note for a microcontroller other than the above, make changes as appropriate to match the microcontroller to be used and perform careful evaluation.

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1. Specifications

The sample program uses the media access control (MAC) function and Ethernet controller direct memory access controller (E-DMAC) function of the gigabit Ethernet controller (GETHER) module of the SH7734 to store in the DDR2-SDRAM memory, which is used as a receive buffer, the portions other than the preamble, SFD, and CRC of the Ethernet frames (see figure 1.2) received from another computer (the opposite host computer).

The SH7734 supports GMII (Gigabit Media Independent Interface), MII (Media Independent Interface), and RMII (Reduced Media Independent Interface), but the sample program is targeted at an evaluation board that supports RMII. For information on the different settings for each of the above interfaces, see the Gigabit Ethernet Controller (GETHER) section in SH7734 User’s Manual: Hardware (R01UH0233EJ).

The sample program makes settings for 10/100 Mbps transfer using the MAC and E-DMAC functions. It does not make use of the following functions of the GETHER:

- 1000 Mbps transfer function using GMII, 10/100 Mbps transfer function using MII
- TSU function
- CAM function
- Flow control
- Magic packet detection
- Checksum calculation function

Table 1.1 Peripheral Functions Used and Their Applications

Peripheral Function	Use
GETHER	Gigabit Ethernet controller: Uses the MAC function to resolve Ethernet frame data received from the physical layer chip (PHY-LSI) and the E-DMAC function to transfer data at high speed to and from the receive buffer in the memory. For details, see the Gigabit Ethernet Controller (GETHER) section in SH7734 User’s Manual: Hardware (R01UH0233EJ).

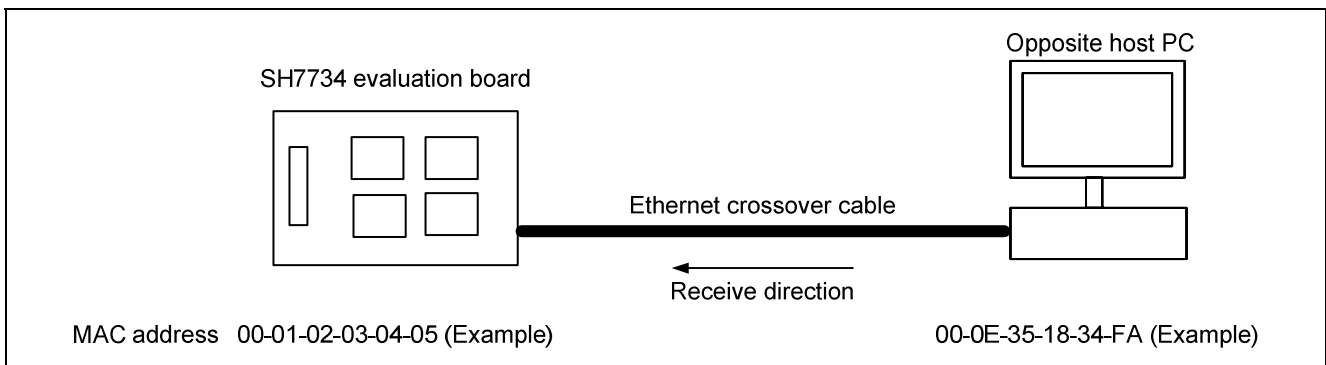


Figure 1.1 Operating Environment

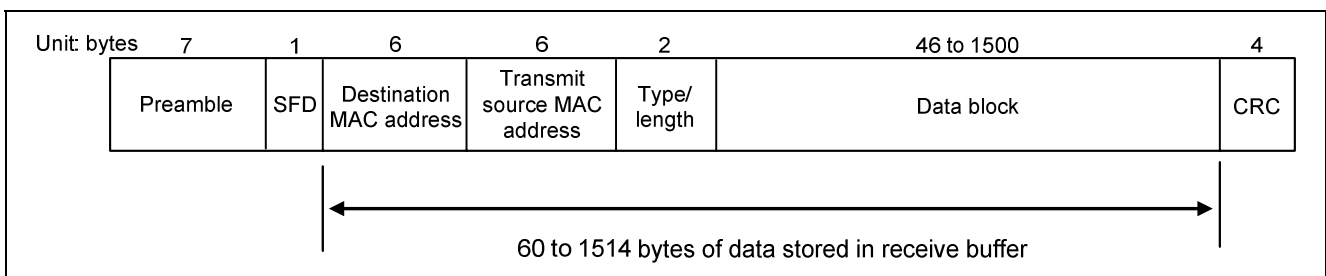


Figure 1.2 Ethernet Frame Format

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed to run normally under the operating conditions given below.

Table 2.1 Operating Conditions

Item	Description
Microcontroller used	SH7734 (R8A77343)
Operating frequency	EXTAL input frequency: 33.3333 MHz CPU clock (clki): 400 MHz SHwy clock (clks): 200 MHz SHwy clock (clks1): 100 MHz DDR clock (MCK0/MCK0#/MCK1/MCK1#): 200 MHz Bus clock (clkb): 50 MHz Peripheral clock (clkp): 50 MHz
Operating voltage	IO supply power (3.3 V) Core supply power (1.25 V)
Integrated development environment	Renesas Electronics High-performance Embedded Workshop (Version 4.08.00.011)
C compiler	Renesas Electronics C/C++ Compiler Package for SuperH Family (V.9.04 release00) Compiler options: -cpu=sh4a -endian=little -include="\$ (PROJDIR)¥inc" -change_message=warning -object="\$ (CONFIGDIR)¥\$(FILELEAF).obj" -debug -optimize=0 -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Version of the sample code	Ver. 1.00
Endian mode	Little endian
Processing mode	Operation in privileged mode only
Boot mode	CS0 boot mode
Address extension mode	29-bit
Memory management unit (MMU)	Disabled
Watchdog timer (WDT)	Disabled
Board used	Renesas Electronics Corporation SH7734 Evaluation Platform (R0P7734C00000RZ)

3. Related Application Notes

The following application notes are related to this document and should be referred to when using this application note.

- SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ)
- SH7734 Group: SH7734 Example of Ethernet Transmit Settings (R01AN0895EJ)

4. Hardware

4.1 Reference Circuit

Figure 4.1 is a connection diagram to an Ethernet PHY-LSI for the RMIIO interface used by the sample program. For details of connections to other peripheral circuits, etc., see the technical documentation of the SH7734 Evaluation Platform (ROP7734C00000RZ).

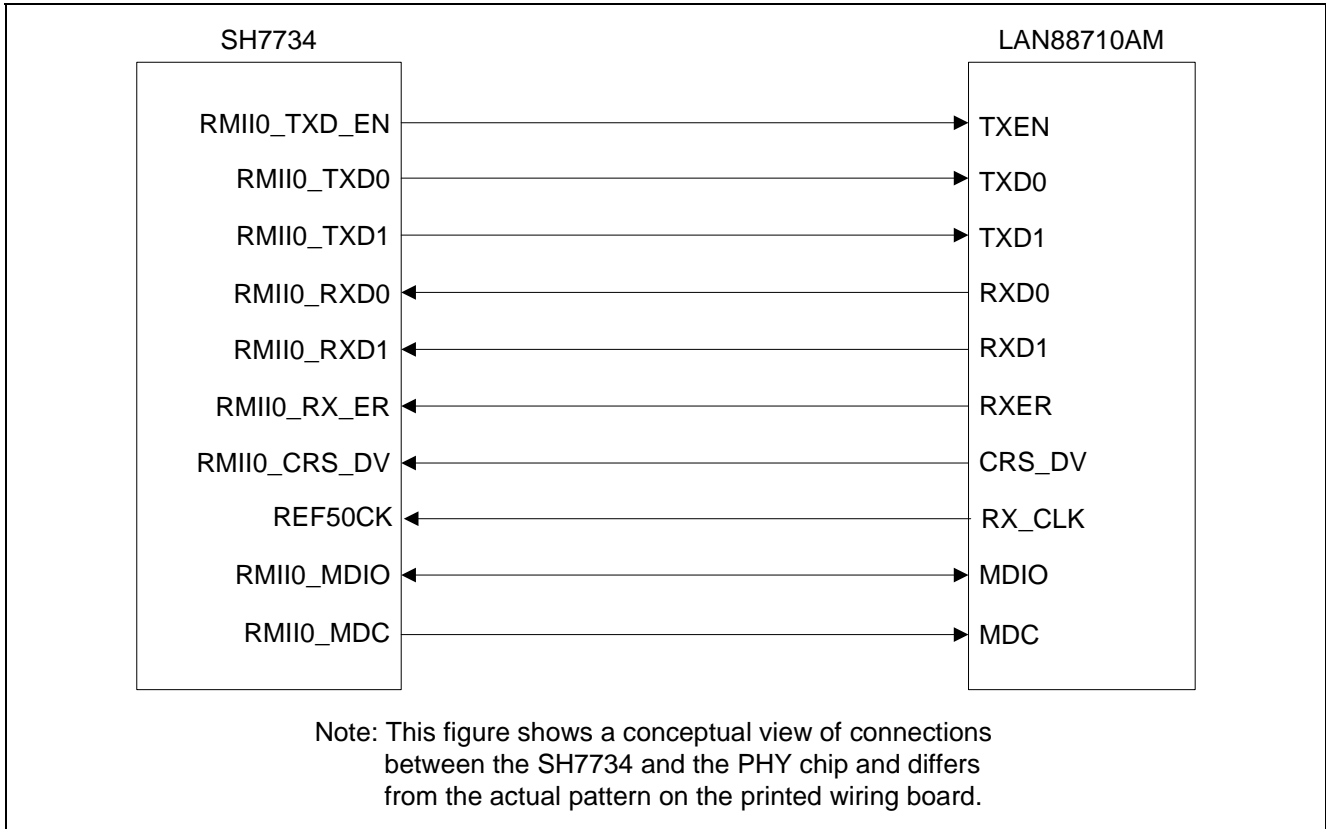


Figure 4.1 PHY-LSI Connection Example (RMII)

4.2 List of Pins Used

Table 4.1 lists the pins used by the sample program and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Description
RMII0_MDC	Output	RMII management data clock
RMII0_MDIO	I/O	RMII management data I/O
RMII0_CRS_DV	Input	RMII carrier detect
RMII0_RX_ER	Input	RMII receive error
RMII0_RXD0	Input	RMII receive data
RMII0_RXD1	Input	RMII receive data
RMII0_TXD_EN	Output	RMII transmit enable
RMII0_TXD0	Output	RMII transmit data
RMII0_TXD1	Output	RMII transmit data
REF50CK	Input	50 MHz reference clock

5. Software

5.1 Operation Overview

Figure 5.1 is a sequence diagram showing an overview of the operation of the sample program.

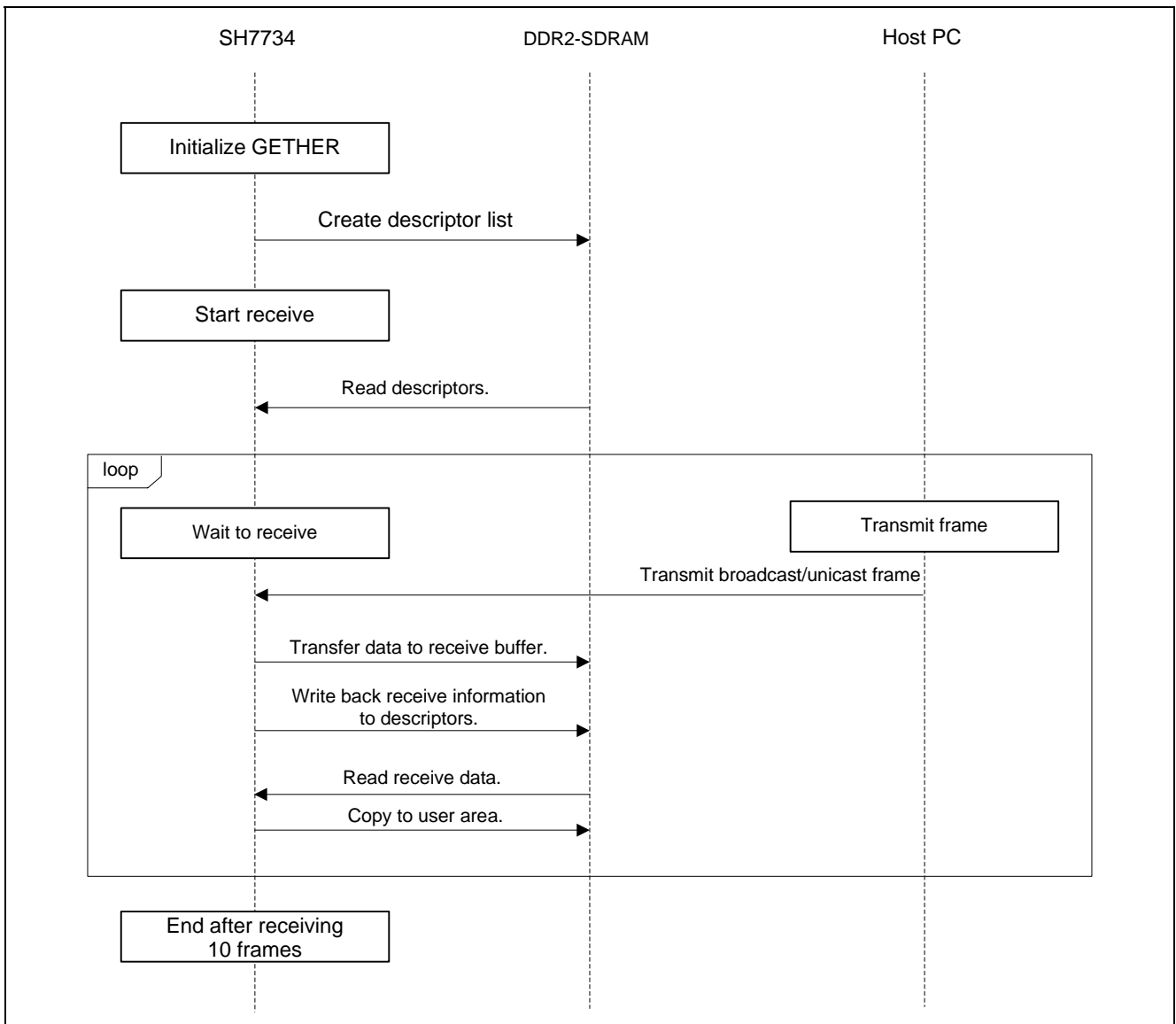


Figure 5.1 Sample Program Operation Overview Sequence Diagram

5.2 File Structure

Table 5.1 lists the files used for the sample code. Note that files generated automatically by the integrated development environment and files from SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ) that are used without modification are omitted.

Table 5.1 File Structure

File Name	Overview	Remarks
sh7734_main.c	Ethernet receive main processing module	
r_ether.c	Ethernet transmit/receive setting module	
r_phy.c	PHY-LSI automatic negotiation processing module	
dbstc.c	Memory initialization	
intprg.c	Definition of Ethernet transmit/receive interrupt handler	
r_ether.h	Include headers for externally referencing Ethernet transmit/receive setting module	
r_phy.h	Include headers for externally referencing PHY-LSI automatic negotiation processing module	
typedefine.h	Declaration headers for variable type names	
vecttbl.src	Exception (reset, general exception, interrupt) function table, interrupt level setting table during exception handling	

5.3 List of Constants

Table 5.2 lists the constants used in the sample code.

Table 5.2 Constants Used in Sample Code

Constant	Setting Value	Description
NUM_OF_USER_BUFFER	10	User data area
D_MOD_SEL	H'0000 0000	PFC MOD_SEL register setting value
D_IPSR4	H'0001 B6DB	PFC IPSR4 register setting value
D_IPSR5	H'0000 0000	PFC IPSR5 register setting value
D_IPSR11	H'0000 09B0	PFC IPSR11 register setting value
D_GPSR2	H'0000 7C2F	PFC GPSR2 register setting value
NUM_OF_TX_DESCRIPTOR	8	Transmit descriptor count
NUM_OF_RX_DESCRIPTOR	8	Receive descriptor count
NUM_OF_TX_BUFFER	8	Transmit buffer count
NUM_OF_RX_BUFFER	8	Receive buffer count
SIZE_OF_BUFFER	1600	Buffer size
MIN_FRAME_SIZE	60	Min. frame size
MAX_FRAME_SIZE	1514	Max. frame size
LOOP_100us	6700	100 μ s software wait
EDMAC_EESIPR_INI_SEND	H'2428 0700	GETHER EESIPR transmit setting Used in interrupt handler to identify transmit interrupt.
EDMAC_EESIPR_INI_RECV	H'0205 001F	GETHER EESIPR receive setting Used in interrupt handler to identify receive interrupt.
EDMAC_EESIPR_INI_EtherC	H'0040 0000	GETHER EESIPR E-MAC status interrupt enable Used in interrupt handler to identify E-MAC interrupt.
EtherC_ECSIPR_INI	H'0000 0004	GETHER ECSIPR setting

Constants related to register addresses, constants generated automatically by the integrated development environment, and constants described in SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ) are not listed in this document.

5.4 List of Structures and Unions

Figure 5.2 lists the structures and unions used in the sample code.

```

/* ==== Transmit descriptor ==== */
typedef union
{
    uint32_t LONG;
    struct{
        uint32_t TACT:1;           /* Transmit descriptor enabled */
        uint32_t TDLE:1;          /* End of transmit descriptor */
        uint32_t TFP :2;          /* Location 1, 0 within transmit frame */
        uint32_t TFE :1;          /* Transmit frame error */
        uint32_t TWBI :1;         /* Write-back completion interrupt notification */
        uint32_t reserved1 :16;   /* Reserved */
        uint32_t TFS9:1;          /* Transmit FIFO underflow (TCU bit in EESR) */
        uint32_t TFS8:1;          /* Transmit abort detect (TABT bit in EESR) */
        uint32_t reserved2 :8;    /* Reserved */
    }BIT;
} td0_t;

typedef struct
{
    #if defined(_BIG)
        uint16_t    TDL;           /* Transmit buffer data length (Big endian) */
        uint16_t    reserved;
    #else
        uint16_t    reserved;
        uint16_t    TDL;           /* Transmit buffer data length (Little endian) */
    #endif
} td1_t;

typedef struct
{
    uint8_t    *TBA;              /* Address of transmit buffer */
} td2_t;

typedef struct tag_edmac_send_desc
{
    td0_t    td0;
    td1_t    td1;
    td2_t    td2;
    struct    tag_edmac_send_desc *pNext;
} edmac_send_desc_t;

/* ==== Receive descriptor ==== */
typedef union
{
    uint32_t LONG;
    struct{
        uint32_t RACT:1;          /* Receive descriptor enabled */
        uint32_t RDLE:1;          /* End of receive descriptor */
        uint32_t RFP :2;          /* Location 1,0 within receive frame */
        uint32_t RFE :1;          /* Receive frame error */
        uint32_t PV :1;           /* Padding insertion */
        uint32_t reserved1:16;    /* Reserved */
        uint32_t RFS9:1;          /* Receive FIFO overflow (RFOF bit in EESR) */
        uint32_t RFS8:1;          /* Receive abort detect (RABT bit in EESR) */
        uint32_t RFS7:1;          /* Receive multicast frames (RMAF bit in EESR) */
        uint32_t RFS6:1;          /* Carrier extension error (CEEF bit in EESR) */
        uint32_t RFS5:1;          /* Carrier extension loss (CELF bit in EESR) */
    }

```

Note: Two versions of the structure are denoted, one for each endian setting, to enable the order of the members in the structure to be reversed to match the endian mode.

```

uint32_t RFS4:1;      /* Residual bits frame receive error (RFR bit in EESR) */
uint32_t RFS3:1;      /* Long frame receive error (RTLE bit in EESR) */
uint32_t RFS2:1;      /* Short frame receive error (RTSF bit in EESR) */
uint32_t RFS1:1;      /* PHY-LSI receive error (PRE bit in EESR) */
uint32_t RFS0:1;      /* Receive frame CRC error detected (CERF bit in EESR) */
}BIT;
} rd0_t;

typedef struct
{
#if defined(_BIG)
uint16_t RBL;          /* Receive buffer length (Big endian) */
uint16_t RDL;          /* Receive data length (Big endian) */
#else
uint16_t RDL;          /* Receive data length (Little endian) */
uint16_t RBL;          /* Receive buffer length (Little endian) */
#endif
} rd1_t;

typedef struct
{
uint8_t *RBA;          /* Receive buffer address */
} rd2_t;

typedef struct tag_edmac_rcv_desc
{
rd0_t rd0;
rd1_t rd1;
rd2_t rd2;
struct tag_edmac_rcv_desc *pNext;
} edmac_rcv_desc_t;

/* ==== The whole transmit/receive descriptors (must be allocated in 16-byte boundaries) ==== */
typedef struct
{
edmac_send_desc_t send[NUM_OF_TX_DESCRIPTOR];
edmac_rcv_desc_t rcv[NUM_OF_RX_DESCRIPTOR];
edmac_send_desc_t *pSend_top;      /* Registration location of transmit descriptors */
edmac_rcv_desc_t *pRcv_end;        /* Registration location and reception end of transmit descriptors */
} txrx_descriptor_set_t;

/* ==== Transmit/receive buffers (must be allocated in 32-byte boundaries) ==== */
/* ---- Definition of all transmit/receive buffer areas ---- */
typedef struct
{
uint8_t send[NUM_OF_TX_BUFFER][SIZE_OF_BUFFER];
uint8_t rcv[NUM_OF_RX_BUFFER][SIZE_OF_BUFFER];
} txrx_buffer_set_t;

typedef struct
{
uint8_t frame[SIZE_OF_BUFFER];
uint32_t len;
uint8_t wk[12];
} USER_BUFFER;

```

Note: Two versions of the structure are denoted, one for each endian setting, to enable the order of the members in the structure to be reversed to match the endian mode.

Figure 5.2 Structures and Unions Used in Sample Code

5.5 List of Variables

Table 5.3 lists the static variables.

Table 5.3 Static Variables

Type	Variable Name	Description	Used by Function
static uint8_t	mac_addr	MAC address	R_Ether_Open
static USER_BUFFER	recv	Receive data copy area	R_Ether_Read
static volatile txrx_descriptor_ set_t	eth_desc	Descriptor area	R_Ether_Read lan_desc_create
static volatile txrx_buffer_set_t	eth_buf	Receive buffer area	lan_desc_create

5.6 List of Functions

Table 5.4 lists the functions.

Table 5.4 FunctionsTable

Function Name	Description
R_Ether_Open	GETHER open function
R_Ether_Read	GETHER frame receive function
R_Ether_Close	GETHER close function

5.7 Function Specifications

The specifications of the functions of the sample code are listed below.

R_Ether_Open

Overview	Initializes the GETHER module.	
Header	r_ether.h	
Declaration	int R_Ether_Open(uint32_t ch, uint8_t mac_addr[])	
Description	Initializes the GETHER module.	
Arguments	<ul style="list-style-type: none"> uint32_t ch uint8_t mac_addr[] 	E-MAC channel number E-MAC MAC address
Return values	<ul style="list-style-type: none"> [R_ETHER_OK(0)]: Open successful [R_ETHER_ERROR(-1)]: Open failed 	
Notes	This function initializes the GETHER module, using the MAC address specified as an argument. When 0 is specified as the MAC address, an address is acquired from the system in EEPROM, etc. The implementation should match the usage conditions. Note that the SH7734 provides a single channel as an Ethernet port, so the argument specifying the E-MAC channel number should be set to 0.	

R_Ether_Read

Overview	Performs Ethernet frame receive processing.	
Header	r_ether.h	
Declaration	int R_Ether_Read(uint32_t ch, void *buf)	
Description	This function copies the Ethernet frame stored by the E-DMAC in the receive buffer to the user area and updates the descriptor information.	
Arguments	<ul style="list-style-type: none"> uint32_t ch void *buf 	E-MAC channel number Receive data pointer
Return values	<ul style="list-style-type: none"> Value other than (0): Number of bytes received [R_ETHER_ERROR(-1)]: Error generated [R_ETHER_HARD_ERROR(-3)]: Hardware error [R_ETHER_RECOVERABLE(-4)]: Recoverable error [R_ETHER_NODATA(-5)]: No receive data 	
Notes	Note that the Ethernet driver of the sample program does not use the return values R_ETHER_HARD_ERROR(-3) and R_ETHER_RECOVERABLE(-4). Also, the SH7734 provides a single channel as an Ethernet port, so the argument specifying the E-MAC channel number should be set to 0.	

R_Ether_Close

Overview	Resets and stops the GETHER module.	
Header	r_ether.h	
Declaration	int R_Ether_Close(uint32_t ch)	
Description	Resets and stops the GETHER module.	
Arguments	uint32_t ch	E-MAC channel number
Return values	<ul style="list-style-type: none"> [R_ETHER_OK(0)]: Close successful [R_ETHER_ERROR(-1)]: Close failed 	
Notes	Note that the Ethernet driver of the sample program does not use the R_ETHER_ERROR(-1) return value. Also, the SH7734 provides a single channel as an Ethernet port, so the argument specifying the E-MAC channel number should be set to 0.	

5.8 Flowcharts

5.8.1 Main Processing

Figure 5.3 is a flowchart of the main processing routine.

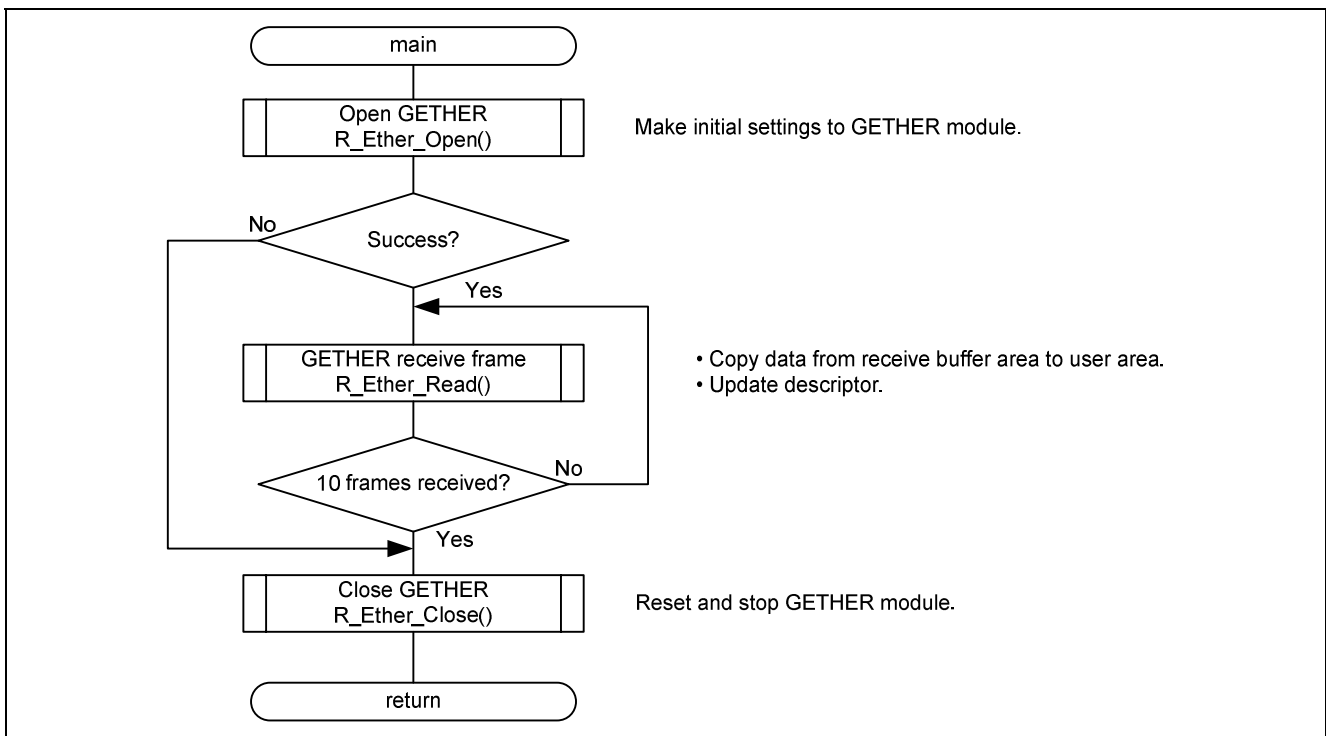


Figure 5.3 Main Processing

5.8.2 GETHER Open Processing

Figure 5.4 is a flowchart of the GETHER open processing.

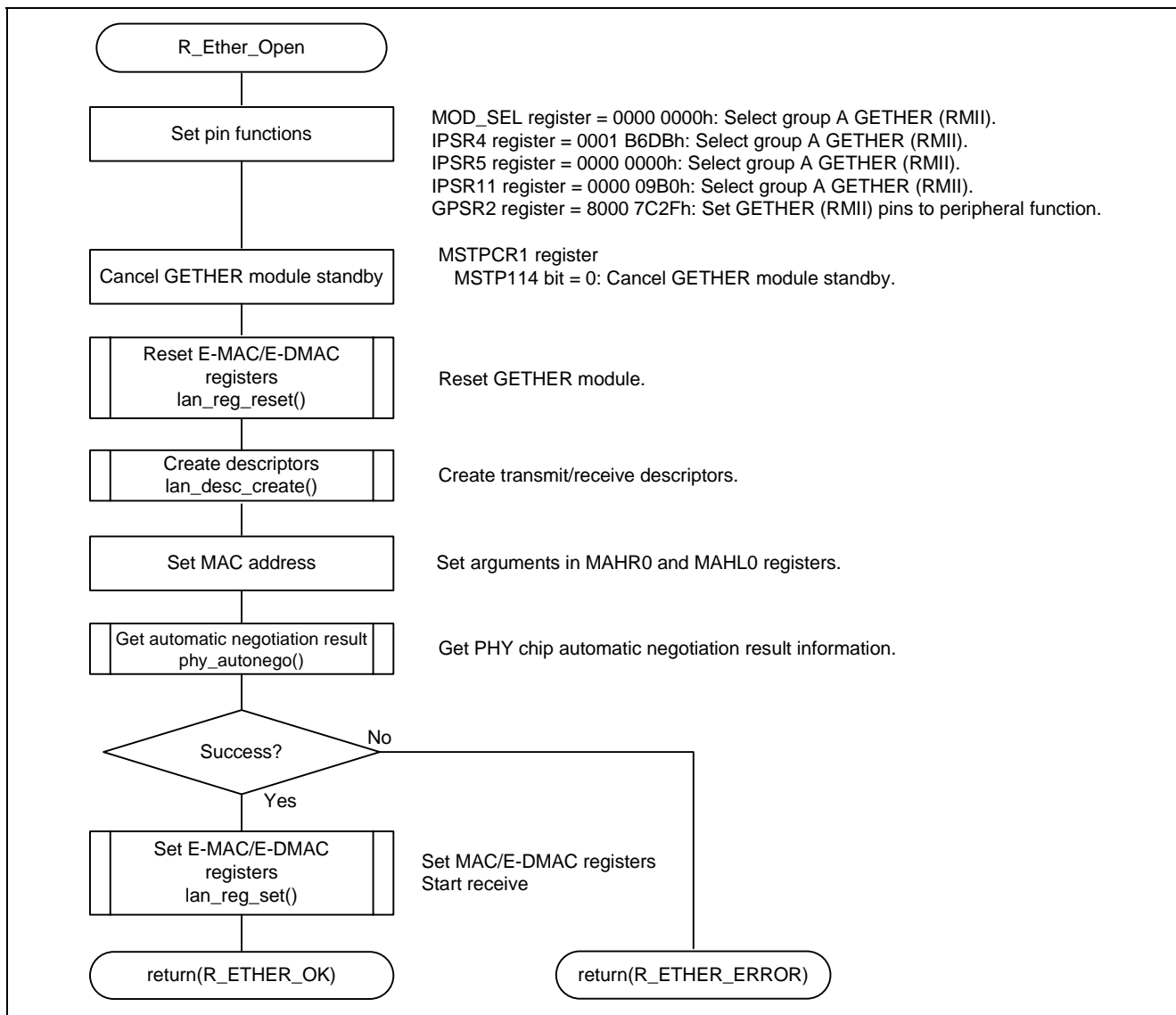


Figure 5.4 GETHER Open Processing

5.8.3 GETHER Close Processing

Figure 5.5 is a flowchart of the GETHER close processing routine.

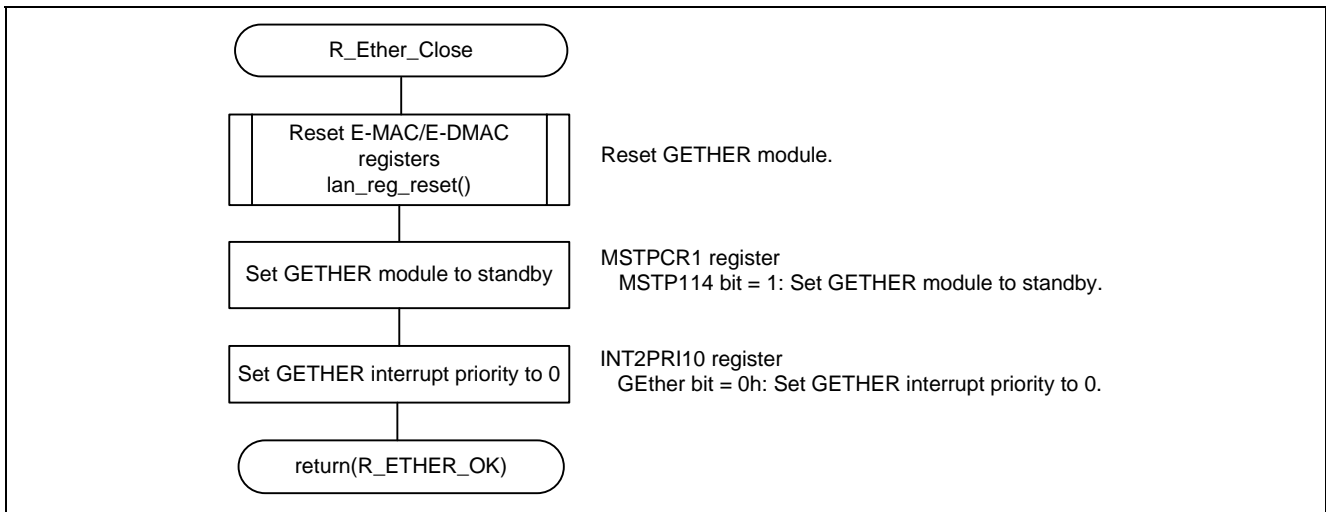


Figure 5.5 GETHER Close Processing

5.8.4 GETHER Frame Receive Processing

Figure 5.6 is a flowchart of the GETHER frame receive processing routine.

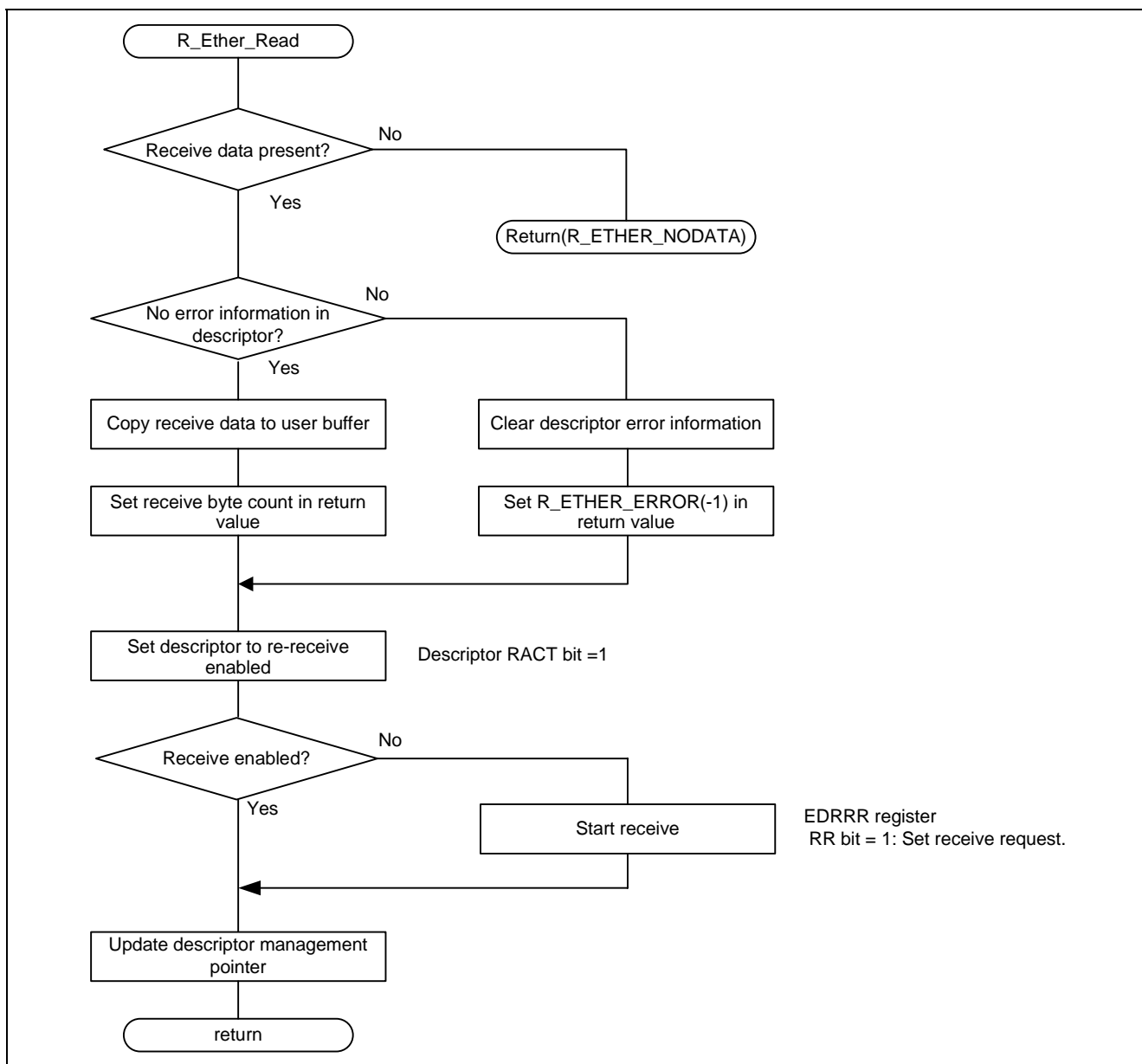


Figure 5.6 GETHER Frame Receive Processing

5.8.5 E-MAC/EDMAC Reset Function

Figure 5.7 is a flowchart of the E-MAC/EDMAC reset function.

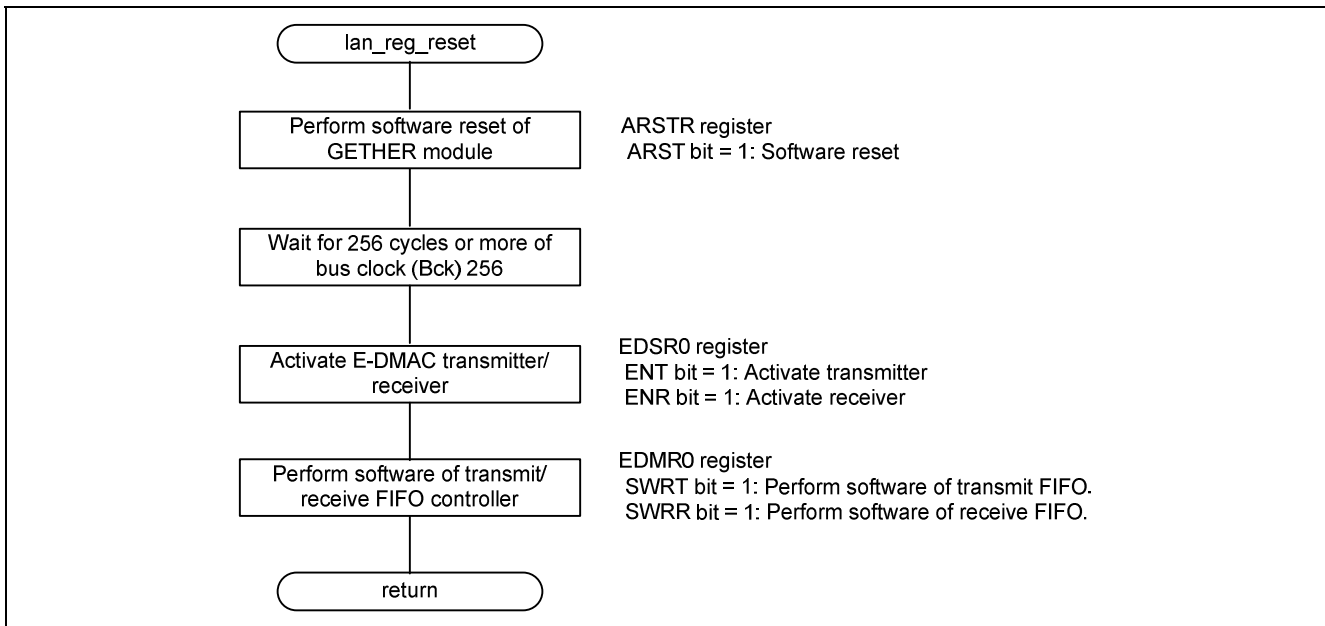


Figure 5.7 E-MAC/EDMAC Reset Function

5.8.6 Transmit/Receive Descriptor Initialization Function

Figure 5.8 is a flowchart of the transmit/receive descriptor initialization function.

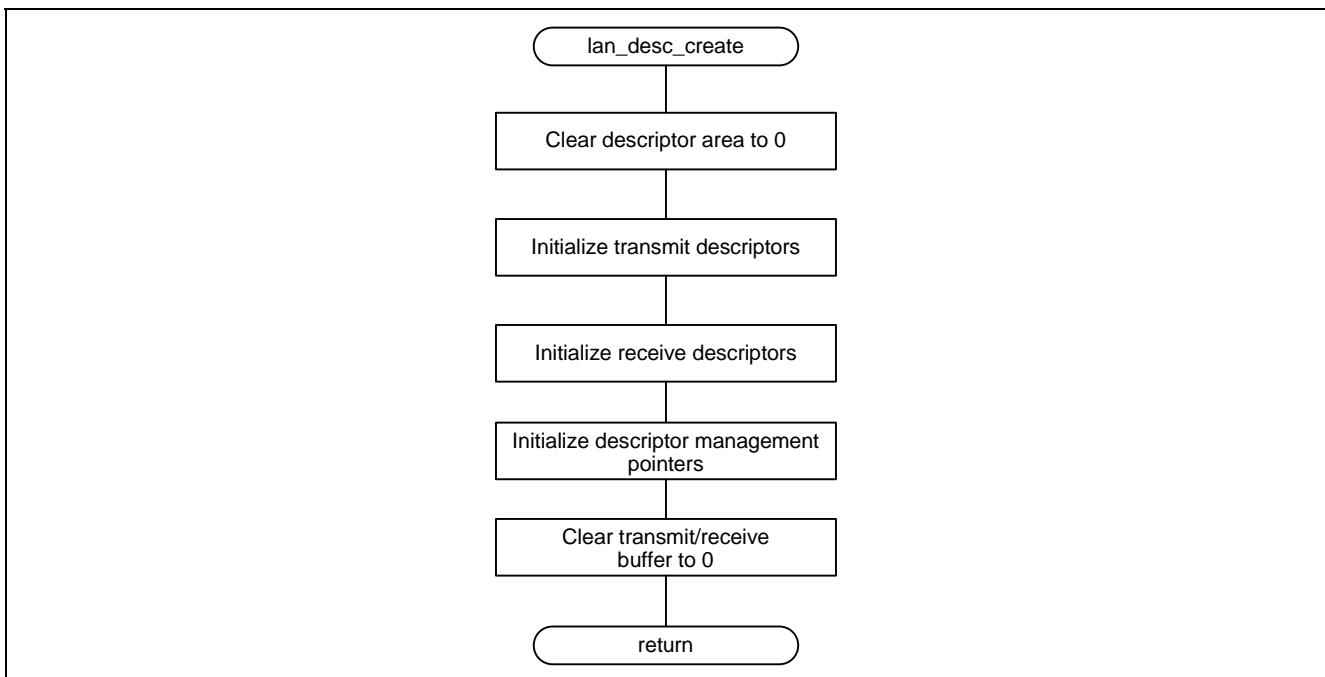


Figure 5.8 Transmit/Receive Descriptor Initialization Function

5.8.7 E-MAC/E-DMAC Register Setting Function

Figure 5.9 is a flowchart of the E-MAC/E-DMAC register setting function.

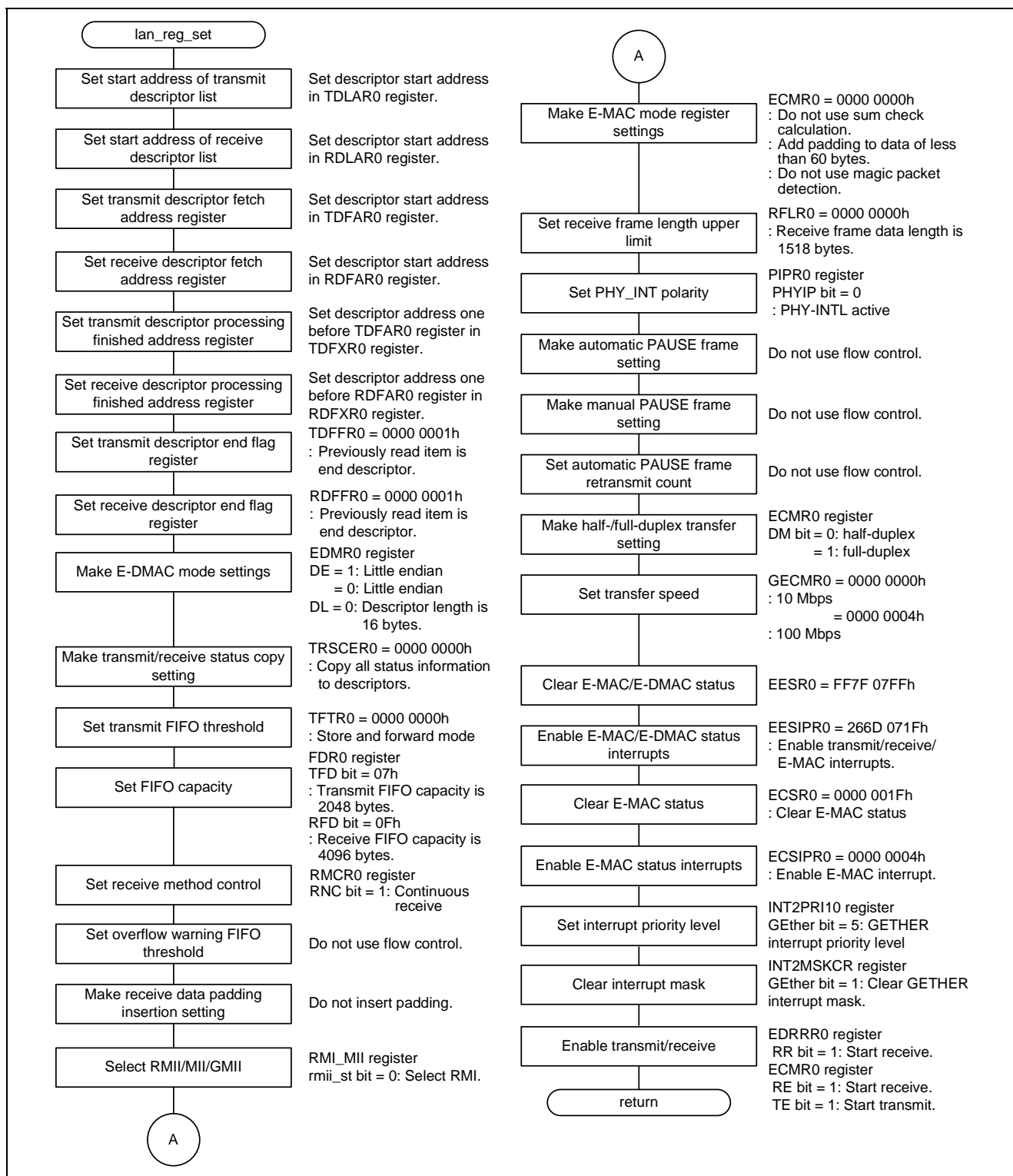


Figure 5.9 E-MAC/E-DMAC Register Setting Function

5.8.8 GETHER Interrupt Handler

Figure 5.10 is a flowchart of the GETHER interrupt handler.

In the sample program presented here, no particular processing is performed.

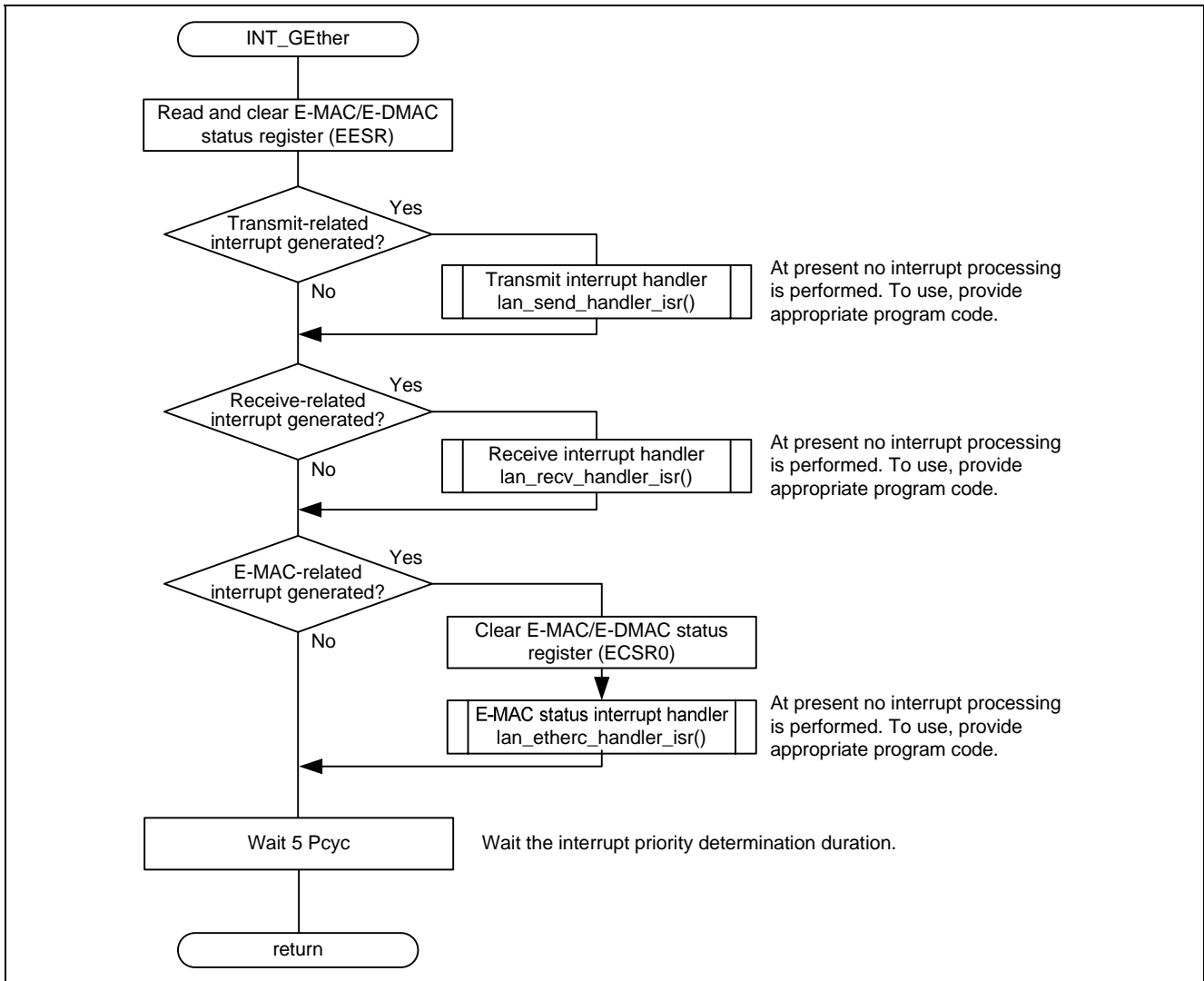


Figure 5.10 GETHER Interrupt Handler

5.8.9 PHY-LSI Automatic Negotiation Result Acquisition Processing

Figure 5.11 is a flowchart of the PHY-LSI automatic negotiation result acquisition processing routine.

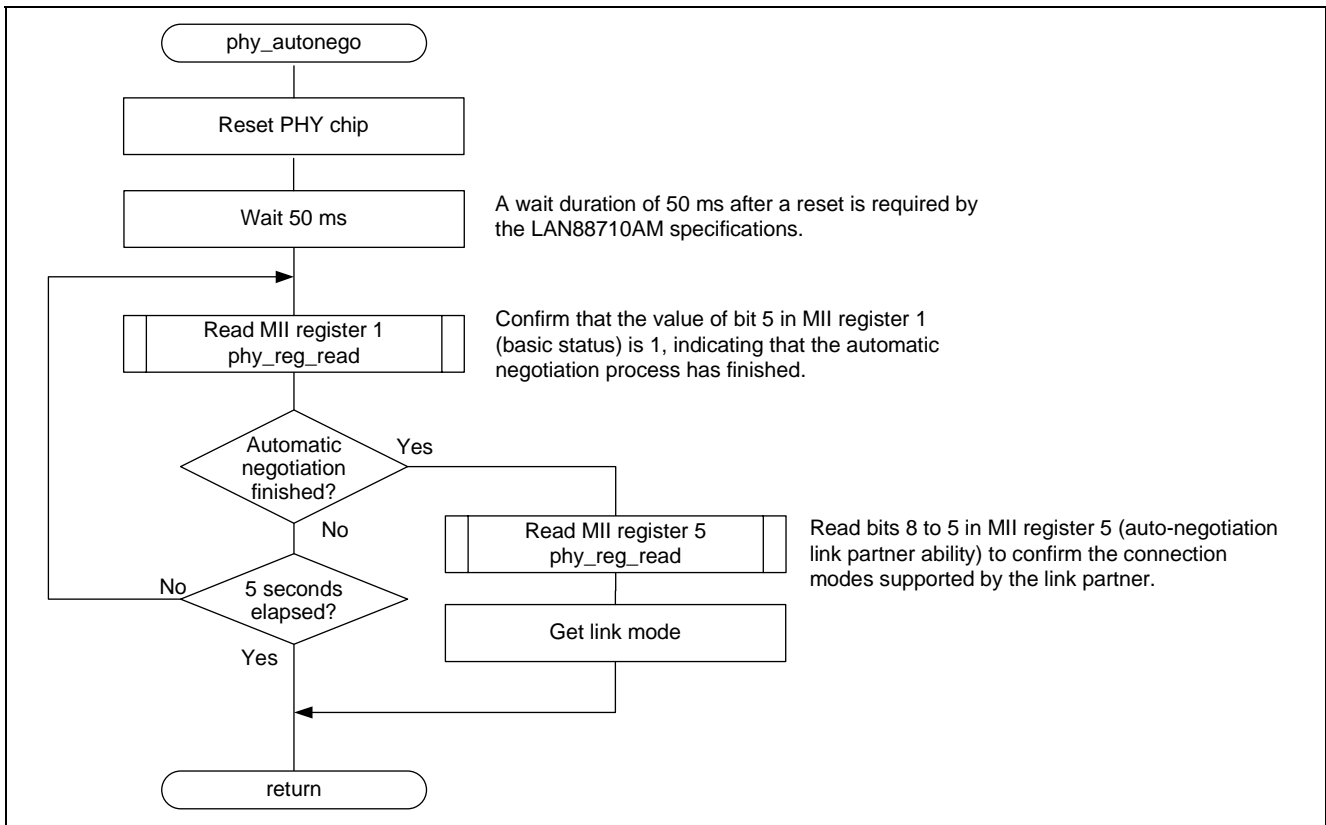


Figure 5.11 PHY-LSI Automatic Negotiation Result Acquisition Processing

5.8.10 Functions Related to PHY-LSI Automatic Negotiation Result Acquisition Processing

Figures 5.12 to 5.15 are flowcharts of the functions that perform PHY-LSI automatic negotiation result acquisition processing.

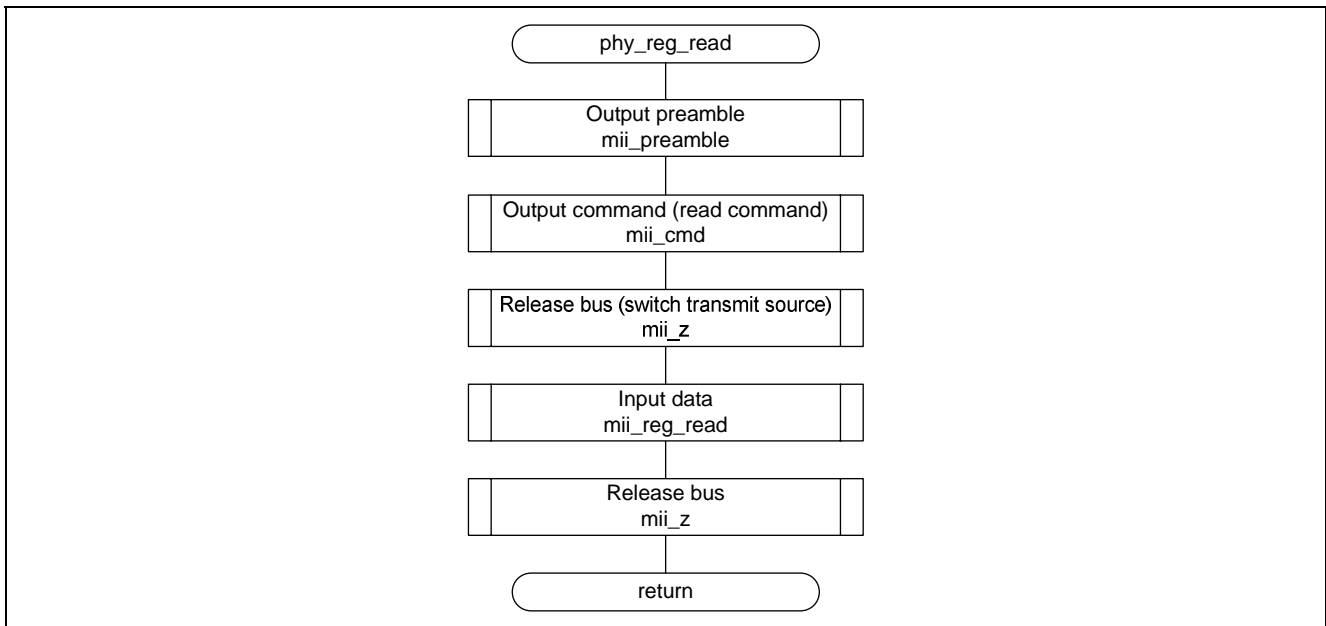


Figure 5.12 Functions Related to PHY-LSI Automatic Negotiation Result Acquisition Processing (1)

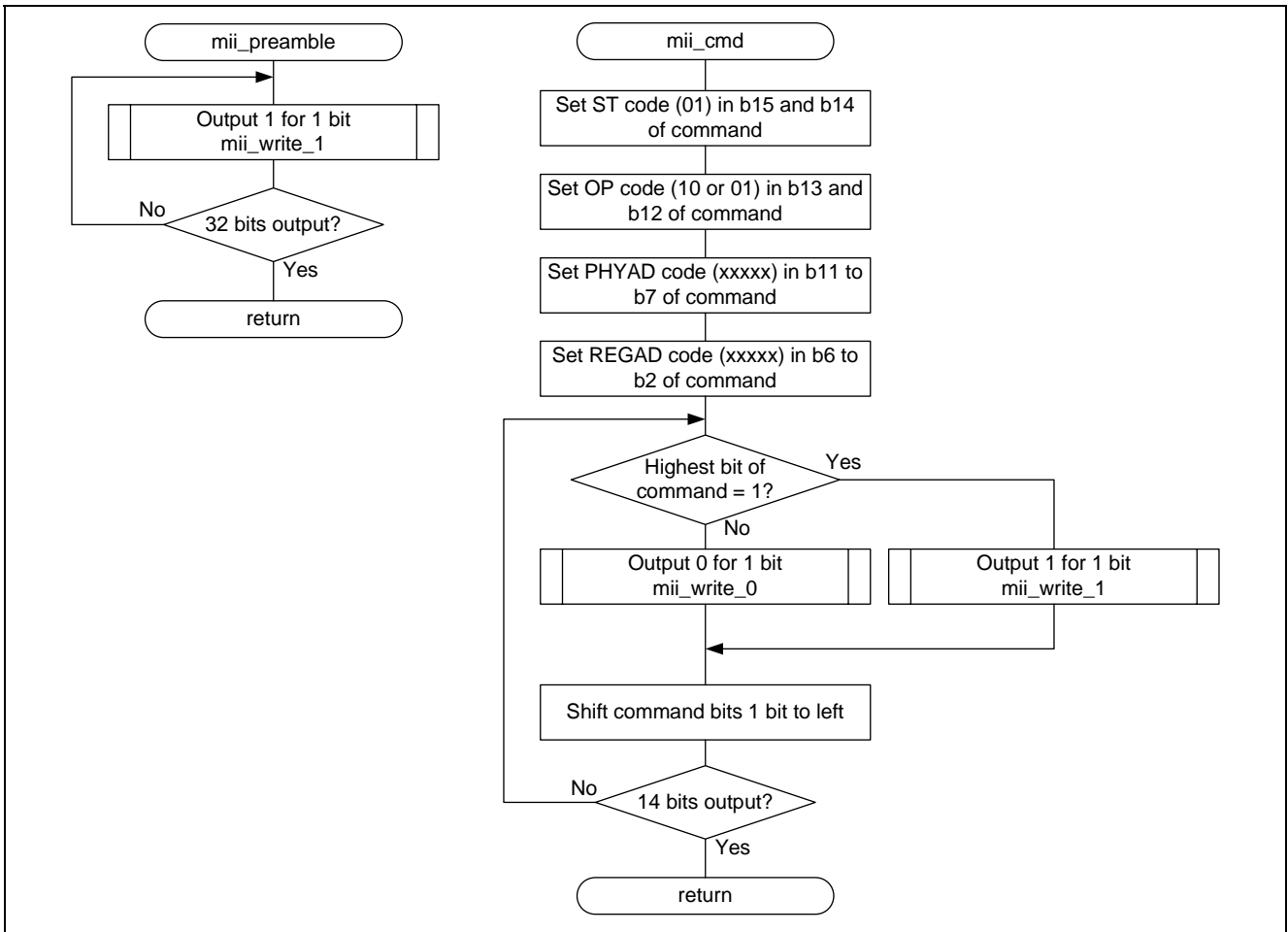


Figure 5.13 Functions Related to PHY-LSI Automatic Negotiation Result Acquisition Processing (2)

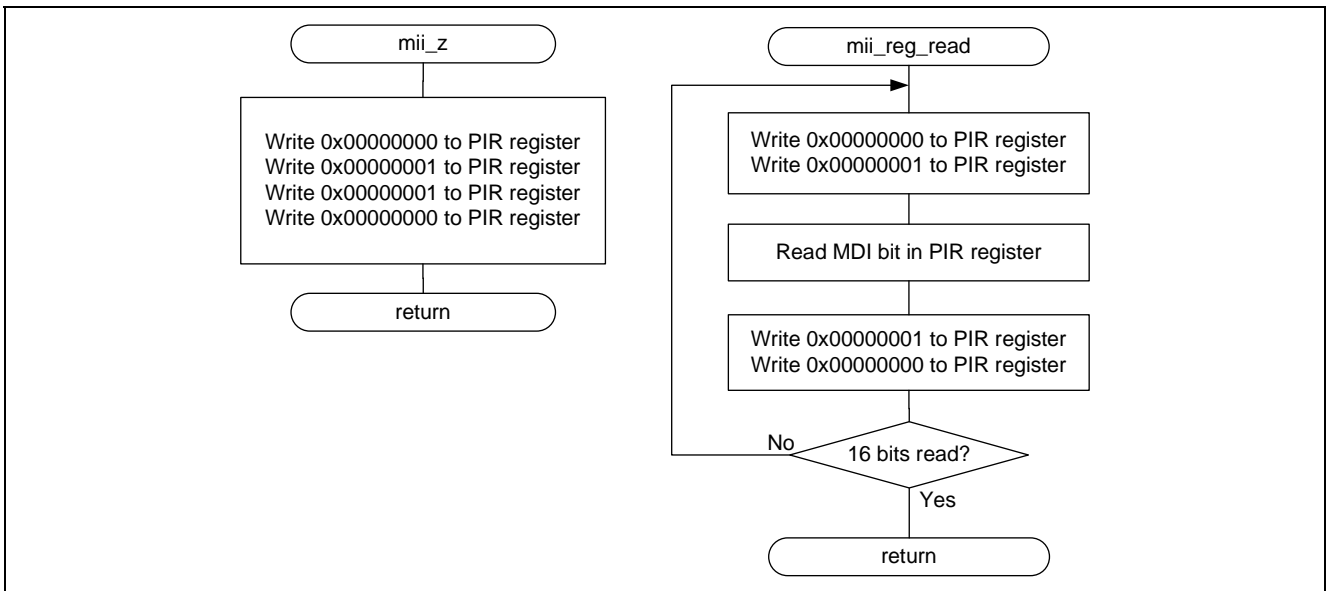


Figure 5.14 Functions Related to PHY-LSI Automatic Negotiation Result Acquisition Processing (3)

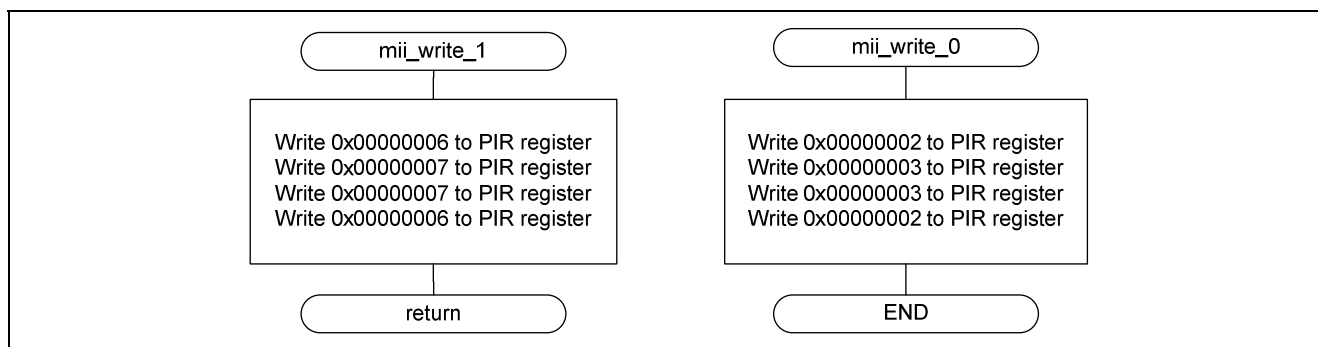


Figure 5.15 Functions Related to PHY-LSI Automatic Negotiation Result Acquisition Processing (4)

5.9 Section Assignments

Table 5.5 lists the assignments of the sections.

Table 5.5 Section Assignments

Section	Application	Area	Address assignment (virtual address)	
P	Program area (when not otherwise specified)	ROM	H'00003000	P0 area (cacheable, MMU address conversion supported)
C	Constant area	ROM		
P\$PSEC	Section initialization program area	ROM		
C\$BSEC	Address structure for uninitialized data	ROM		
C\$DSEC	Address structure for initialized data	ROM		
D	Initialized data (initial value)	ROM		
B	Uninitialized data area	RAM	H'0C000000	
R	Initialized data area	RAM		
PRAM	Target area for copying program (P) from ROM	RAM		
S	Stack area	RAM	0x0FFFF9F0	
PINTHandler	Exception/interrupt handler	ROM	H'80000800	P1 area (cacheable, MMU address conversion not supported)
VECTTBL	Reset vector table	ROM		
INTTBL	Interrupt vector table Interrupt mask table	ROM		
PIntPRG	Interrupt handler	ROM		
SP_S	Dedicated stack area for TLB miss handler	RAM	H'8FFFFDF0	
RSTHandler	Reset handler	ROM	H'A0000000	P2 area (not cacheable, MMU address conversion not supported)
PResetPRG	Reset program	ROM		
P_LBSC_ROM	ROM program area (for LBSC)	ROM		
P_DBSC3_ROM	ROM program area (for DBSC3)	ROM		
PnonCache	Program area (cache-disabled access)	ROM		
BETH_DESC	Ethernet descriptor area	RAM	H'AD000000	
BETH_BUFF	Ethernet buffer area	RAM	H'AD001000	
BETH_BUFF2	Ethernet data storage area	RAM	H'AD008000	
INTTBL_OL	Interrupt mask table copy area	RAM	H'E500E000	OL memory
PINTHandler_IL	Exception/interrupt handler copy area	RAM	H'E5200000	IL memory
PIntPRG_IL	Interrupt handler copy area	RAM		
P_LBSC_IL	ROM program copy area (for LBSC)	RAM		

Note: For information on the reasons for providing special sections, section copying specifications, etc., see *SH7734 Group: SH7734 Example of Initialization (R01AN0665EJ)*.

6. Sample Code

The sample code is available for download from the Renesas Electronics Web site.

7. Reference Documents

- SH7734 Group User's Manual: Hardware, (R01UH0233EJ) Rev.1.00
(The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates/Technical News
(The latest information can be downloaded from the Renesas Electronics Web site.)
- Integrated Development Environment User's Manual
Super H C/C++ Compiler Package V.9.04 User's Manual Rev.1.00
(The latest version can be downloaded from the Renesas Electronics Web site.)

Website and Support

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<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/inquiry>

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Aug.30.12	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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