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SH7705 Group, SH7720 Group

SDRAM Interface

1. Preface

The SuperH RISC engine microcomputers are new-generation RISC microcomputers that achieve superH arithmetic processing performance by adopting a RISC CPU. In addition, these microcomputers integrate on the same chip the peripheral functions required to implement application systems while at the same achieving the low-power operation indispensable in modern microcomputer application equipment.

The SH-3, SH3-DSP SDRAM Interface Application Note is organized for user reference during hardware design.

This application note collects examples of interfaces between the SH-3 and SH3-DSP microcomputers and external memory (SDRAM).

Note that while the operation of the task examples presented in this application note has been verified, these should only be used in an actual system after operational verification by the user.

Note: SuperH is a registered trademark of Renesas Technology Corp.

2. Using this Application Note

2.1 SDRAM Interface Document Structure

This SDRAM interface document has the following structure and describes methods for interfacing with SDRAM.

SDRAM Interface Document

- Bus state controller (BSC) documentation

  Describes the settings used when connected with SDRAM.

- Circuit Diagrams

  These circuit diagrams show the circuit used to interface with SDRAM.

This application note describes the interfaces between the following products and SDRAM.

Product	SDRAM*
SH7705	EDS6416AHTA (1 Mword × 16 bit × 4 bank)
	EDS1216AATA (2 Mword × 16 bit × 4 bank)
	EDS2516ADTA (4 Mword × 16 bit × 4 bank)
	EDS5116ABTA (8 Mword × 16 bit × 4 bank)
SH7720	EDS6416AHTA (1 Mword × 16 bit × 4 bank)
	EDS1216AATA (2 Mword × 16 bit × 4 bank)
	EDS2516ADTA (4 Mword × 16 bit × 4 bank)
	EDS5116ABTA (8 Mword × 16 bit × 4 bank)

Note: *These devices are products of Elpida Memory, Inc.

3. SDRAM Interface Examples

3.1 SH7705 SDRAM Interface Examples

3.1.1 SDRAM Direct Connection

Since synchronous DRAM can be selected by the $\overline{CS}$ signal, physical space areas 2 and 3 can be connected using $\overline{RAS}$ and other control signals in common. If the TYPE[2:0] bits in CSnBCR (n = 2 or 3) are set to 100, the synchronous DRAM interface can be selected. Do not set this value to CSnBCR unless n = 2 or 3, otherwise the operation of this LSI is not guaranteed.

The SDRAM that can be connected to this LSI is a product that has 11/12/13 bits of row address, 8/9/10 bits of column address, 4 or less banks, and uses the A10 pin for setting precharge mode in read and write command cycles. The control signals for direct connection of SDRAM are $\overline{RASU}$, $\overline{RASL}$, $\overline{CASU}$, $\overline{CASL}$, RD/$\overline{WR}$, DQMUU, DQMUL, DQMLU, DQMLL, CKE, $\overline{CS2}$, and $\overline{CS3}$. All the signals other than $\overline{CS2}$ and $\overline{CS3}$ are common to all areas, and signals other than CKE are valid when $\overline{CS2}$ or $\overline{CS3}$ is asserted. SDRAM can be connected to up to 2 spaces. The data bus width of the area that is connected to SDRAM can be set to 32 or 16 bits.

Burst read/single write (burst length 1) and burst read/burst write (burst length 1) are supported as the SDRAM operating mode.

Commands for SDRAM can be specified by $\overline{RASU}$, $\overline{RASL}$, $\overline{CASU}$, $\overline{CASL}$, RD/WR, and specific address signals. These commands are shown below.

- NOP
- Auto-refresh (REF)
- Self-refresh (SELF)
- All banks pre-charge (PALL)
- Specified bank pre-charge (PRE)
- Bank active (ACTV)
- Read (READ)
- Read with pre-charge (READA)
- Write (WRIT)
- Write with pre-charge (WRITA)
- Write mode register (MRS)

The byte to be accessed is specified by DQMUU, DQMUL, DQMLU, and DQMLL.

3.1.2 Power-On Sequence

In order to use synchronous DRAM, mode setting must first be performed after powering on. To perform synchronous DRAM initialization correctly, the bus state controller registers must first be set, followed by a write to the synchronous DRAM mode register. In synchronous DRAM mode register setting, the address signal value at that time is latched by a combination of the $\overline{\text{CSn}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and RD/$\overline{\text{WR}}$ signals. If the value to be set is X, the bus state controller provides for value X to be written to the synchronous DRAM mode register by performing a write to address H'A4FD4000 + X for area 2 synchronous DRAM, and to address H'A4FD5000 + X for area 3 synchronous DRAM. In this operation the data is ignored, but the mode write is performed as a word-size access. To set burst read/single write, CAS latency 2 to 3, wrap type = sequential, and burst length 1 supported by the LSI, arbitrary data is written in a word-size access to the addresses shown in tables 3.1(1) and 3.1(2). In this time 0 is output at the external address pins of A12 or later.

Table 3.1(1) SDRAM Mode Register Write Access Addresses (Area 2 Settings (SDMR2))

Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD4440	H'0000440
	3	H'A4FD4460	H'0000460
32 bits	2	H'A4FD4880	H'0000880
	3	H'A4FD48C0	H'00008C0

Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD4040	H'0000040
	3	H'A4FD4060	H'0000060
32 bits	2	H'A4FD4080	H'0000080
	3	H'A4FD40C0	H'00000C0

Table 3.1(2) SDRAM Mode Register Write Access Addresses (Area 3 Settings (SDMR3))

Burst read/single write (burst length 1)

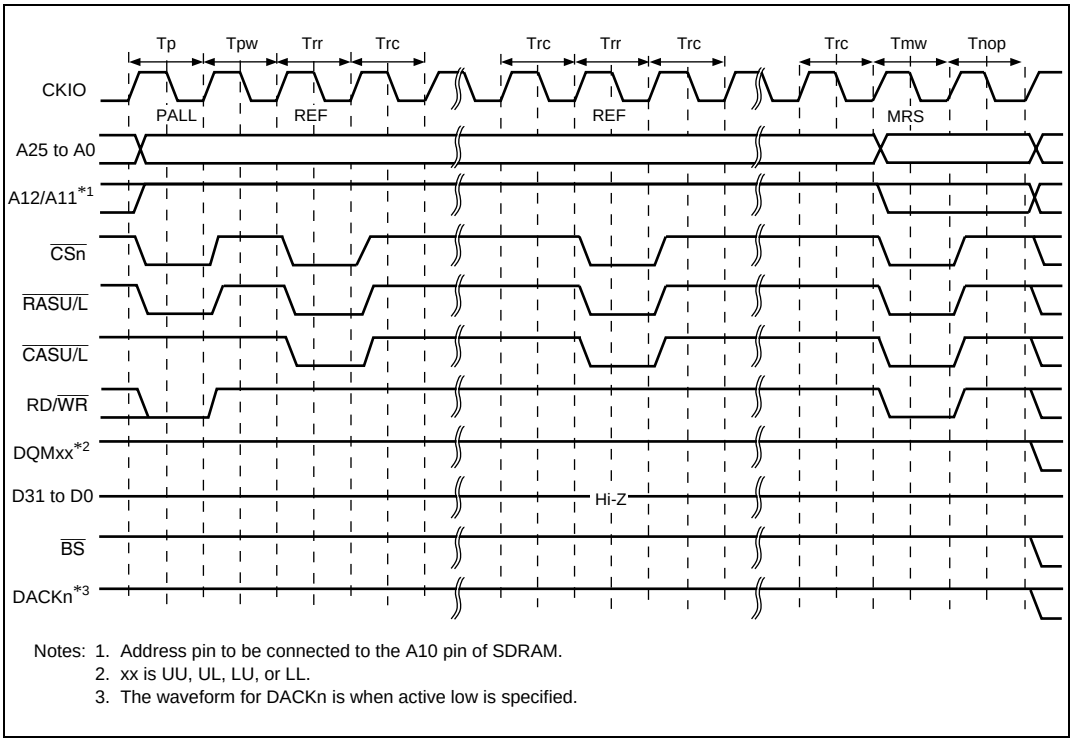
Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD5440	H'0000440
	3	H'A4FD5460	H'0000460
32 bits	2	H'A4FD5880	H'0000880
	3	H'A4FD58C0	H'00008C0

Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD5040	H'0000040
	3	H'A4FD5060	H'0000060
32 bits	2	H'A4FD5080	H'0000080
	3	H'A4FD50C0	H'00000C0

Mode register setting timing is shown in figure 3.1. A PALL command (all bank pre-charge command) is firstly issued. A REF command (auto refresh command) is then issued 8 times. An MRS command (mode register write command) is finally issued. Idle cycles, of which number is specified by the TRP[1:0] bits in CSnWCR, are inserted between the PALL and the first REF. Idle cycles, of which number is specified by the TRC[1:0] bits in CSnWCR, are inserted between REF and REF, and between the 8th REF and MRS. Idle cycles, of which number is one or more, are inserted between the MRS and a command to be issued next.

It is necessary to keep idle time of certain cycles for SDRAM before issuing PALL command after power-on. Refer the manual of the SDRAM for the idle time to be needed. When the pulse width of the reset signal is longer then the idle time, mode register setting can be started immediately after the reset, but care should be taken when the pulse width of the reset signal is shorter than the idle time.



Notes: 1. Address pin to be connected to the A10 pin of SDRAM.
2. xx is UU, UL, LU, or LL.
3. The waveform for DACKn is when active low is specified.

Figure 3.1 Synchronous DRAM Mode Write Timing (Based on JEDEC)

3.1.3 EDS6416AHTA (1 Mword × 16 bits × 4 banks) 64-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS6416AHTA) is connected to the SH7705's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.2 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.2 BSC Settings (EDS6416AHTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0808
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.2 shows the circuit diagram for connecting a single 64-Mbit (1 Mword × 16 bits × 4 banks) SDRAM to area 3.

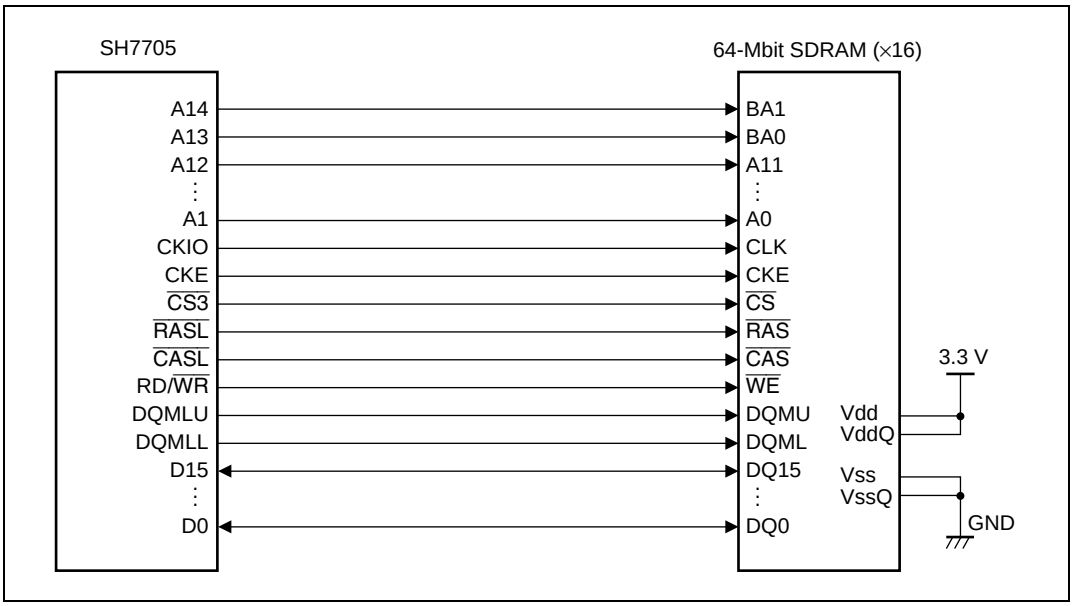


Figure 3.2 Block Diagram

3.1.4 EDS6416AHTA (1 Mword × 16 bits × 4 banks) 64-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS6416AHTA) are connected to the SH7705's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.3 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.3 BSC Settings (EDS6416AHTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0808
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.3 shows the circuit diagram for connecting two 64-Mbit (1 Mword × 16 bits × 4 banks) SDRAMs to area 3.

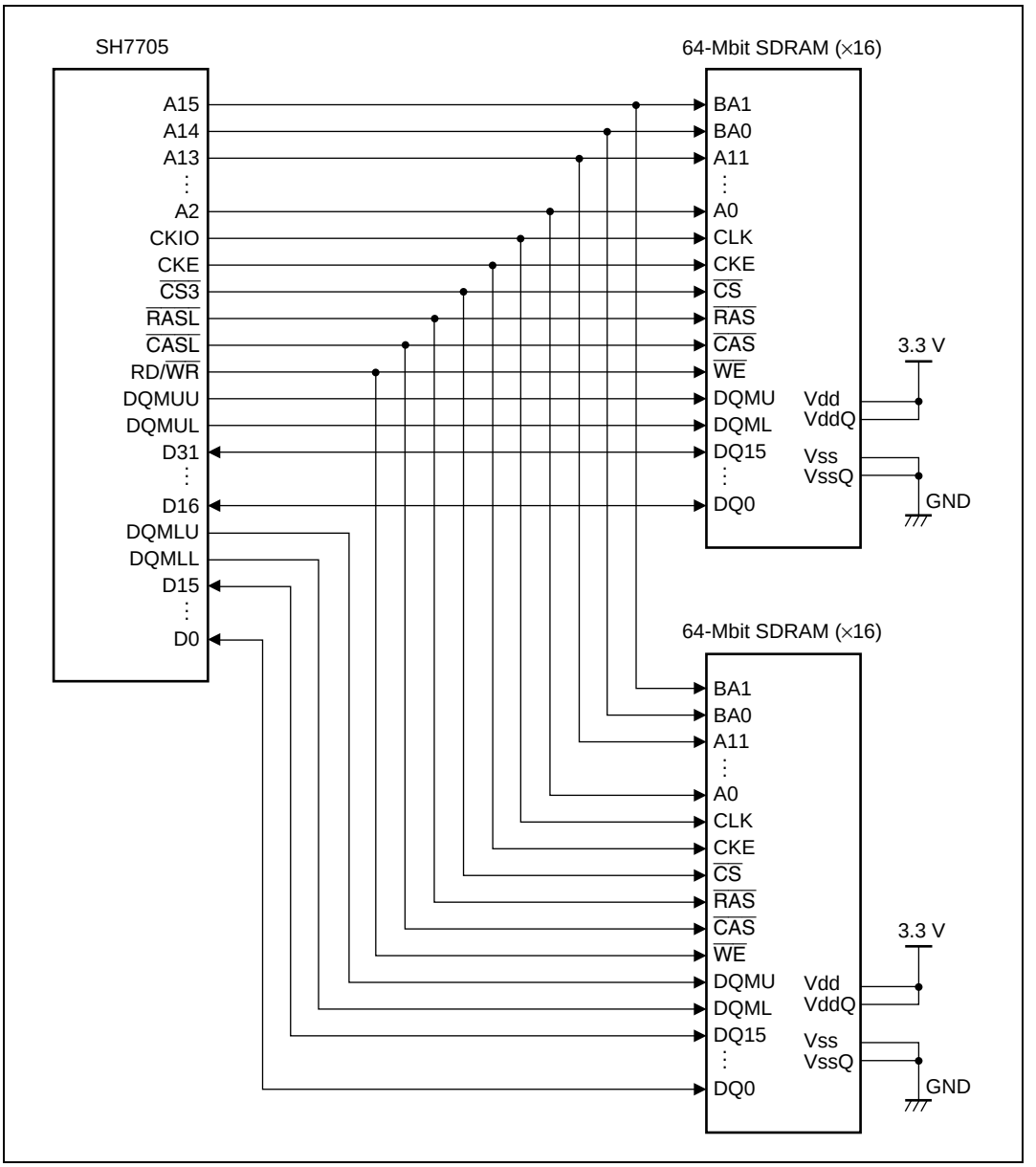


Figure 3.3 Block Diagram

3.1.5 EDS1216AATA (2 Mwords × 16 bits × 4 banks) 128-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS1216AATA) is connected to the SH7705's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.4 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.4 BSC Settings (EDS1216AATA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0809
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.4 shows the circuit diagram for connecting a single 128-Mbit (2 Mwords × 16 bits × 4 banks) SDRAM to area 3.

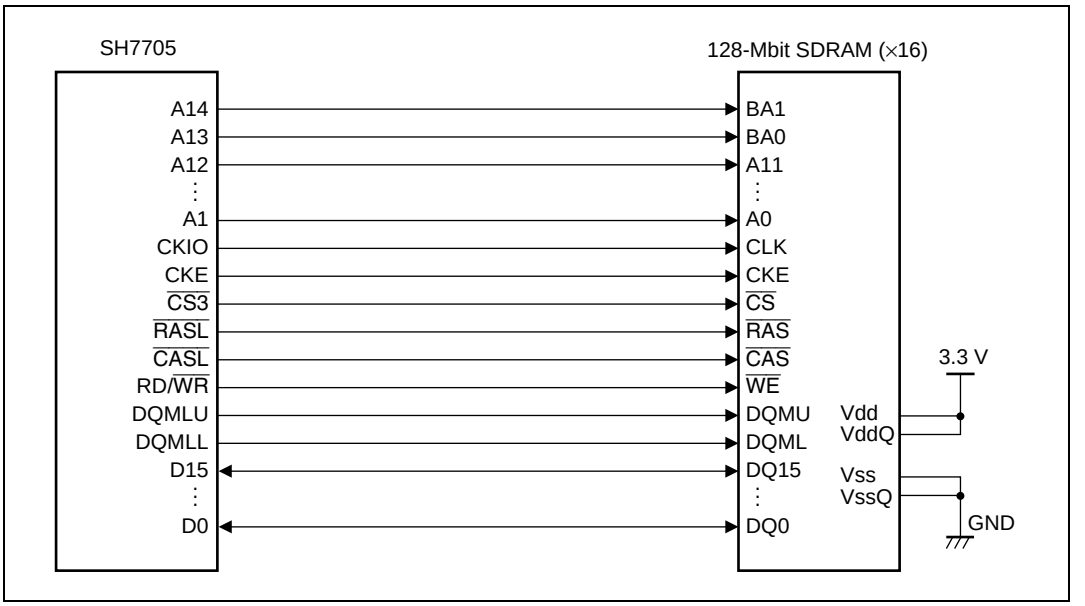


Figure 3.4 Block Diagram

3.1.6 EDS1216AATA (2 Mwords × 16 bits × 4 banks) 128-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS1216AATA) are connected to the SH7705's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.5 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.5 BSC Settings (EDS1216AATA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0809
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.5 shows the circuit diagram for connecting two 128-Mbit (2 Mwords × 16 bits × 4 banks) SDRAMs to area 3.

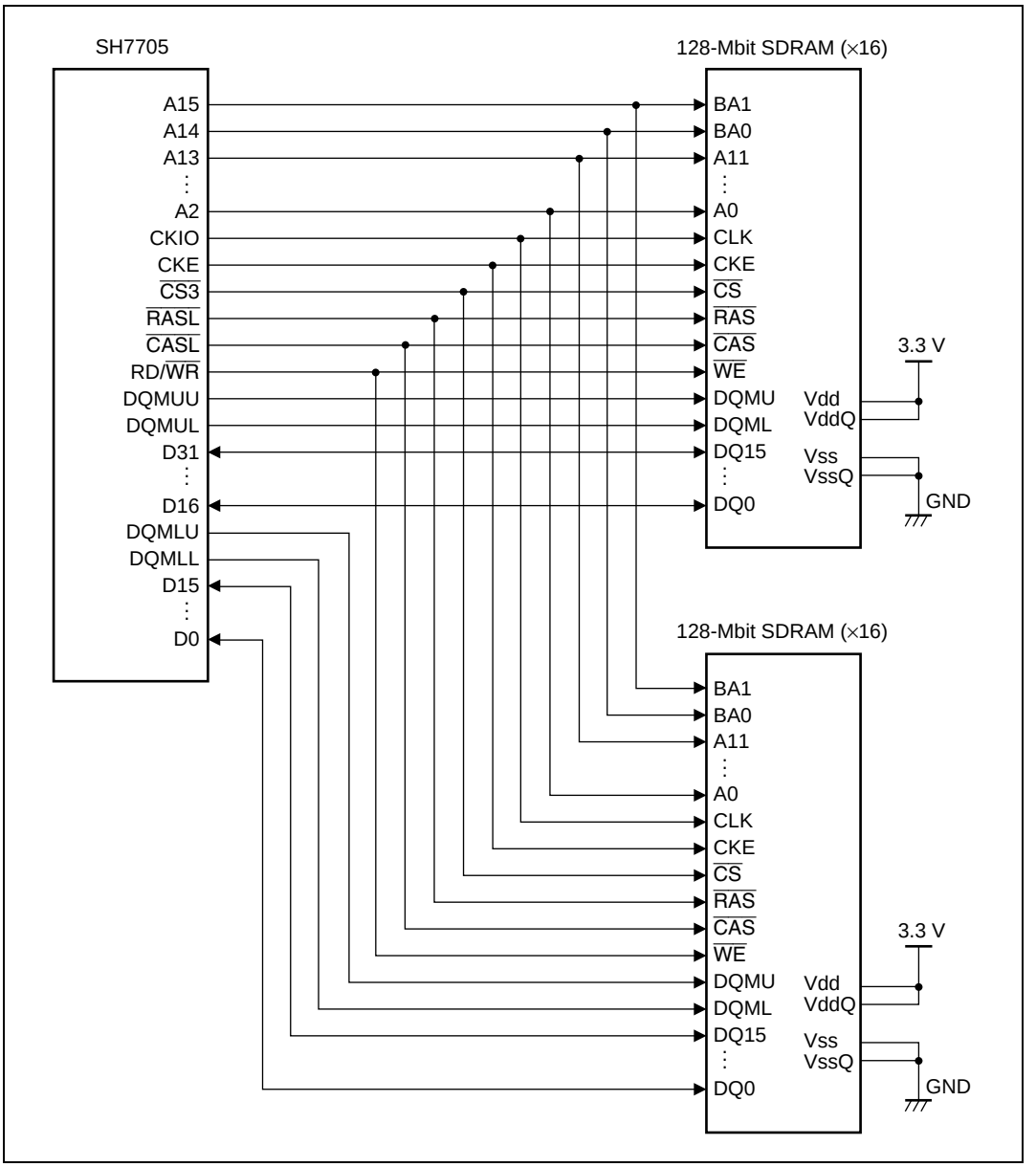


Figure 3.5 Block Diagram

3.1.7 EDS2516ADTA (4 Mwords × 16 bits × 4 banks) 256-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS2516ADTA) is connected to the SH7705's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.6 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.6 BSC Settings (EDS2516ADTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0811
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.6 shows the circuit diagram for connecting a single 256-Mbit (4 Mwords × 16 bits × 4 banks) SDRAM to area 3.

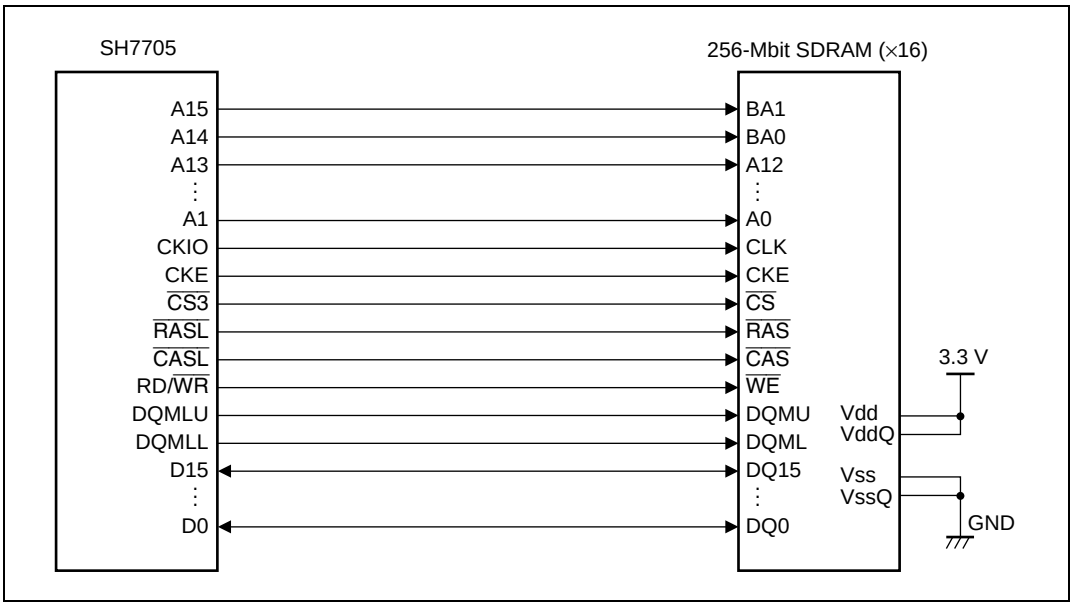


Figure 3.6 Block Diagram

3.1.8 EDS2516ADTA (4 Mwords × 16 bits × 4 banks) 256-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS2516ADTA) are connected to the SH7705's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.7 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.7 BSC Settings (EDS2516ADTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0811
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.7 shows the circuit diagram for connecting two 256-Mbit (4 Mwords × 16 bits × 4 banks) SDRAMs to area 3.

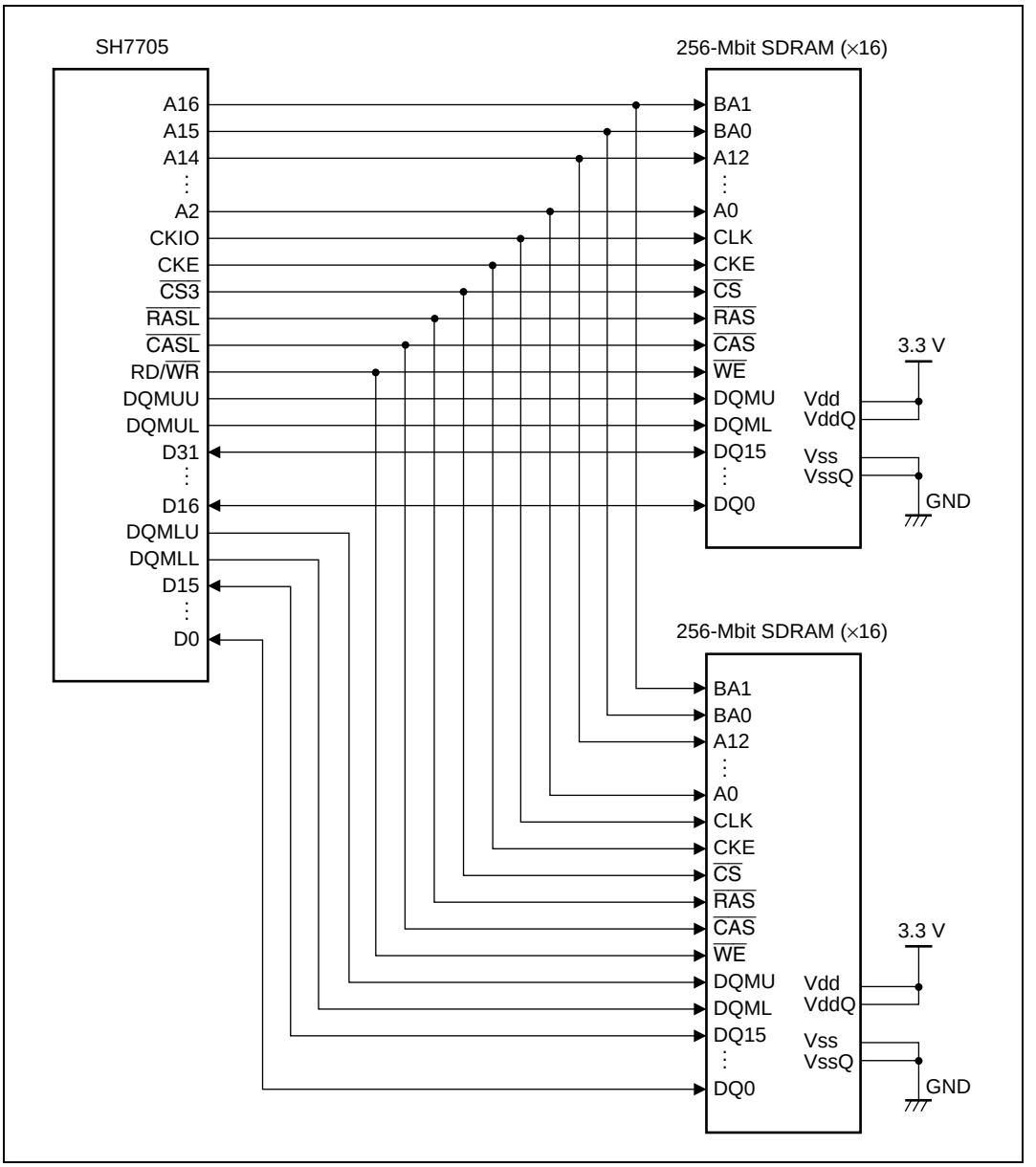


Figure 3.7 Block Diagram

3.1.9 EDS5116ABTA (8 Mwords × 16 bits × 4 banks) 512-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS5116ABTA) is connected to the SH7705's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.8 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 4 cycles, TRCD = 3 cycles, TRWL = 2 cycles, TRC = 6 cycles.

Table 3.8 BSC Settings (EDS5116ABTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 6892
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0812
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.8 shows the circuit diagram for connecting a single 512-Mbit (8 Mwords × 16 bits × 4 banks) SDRAM to area 3.

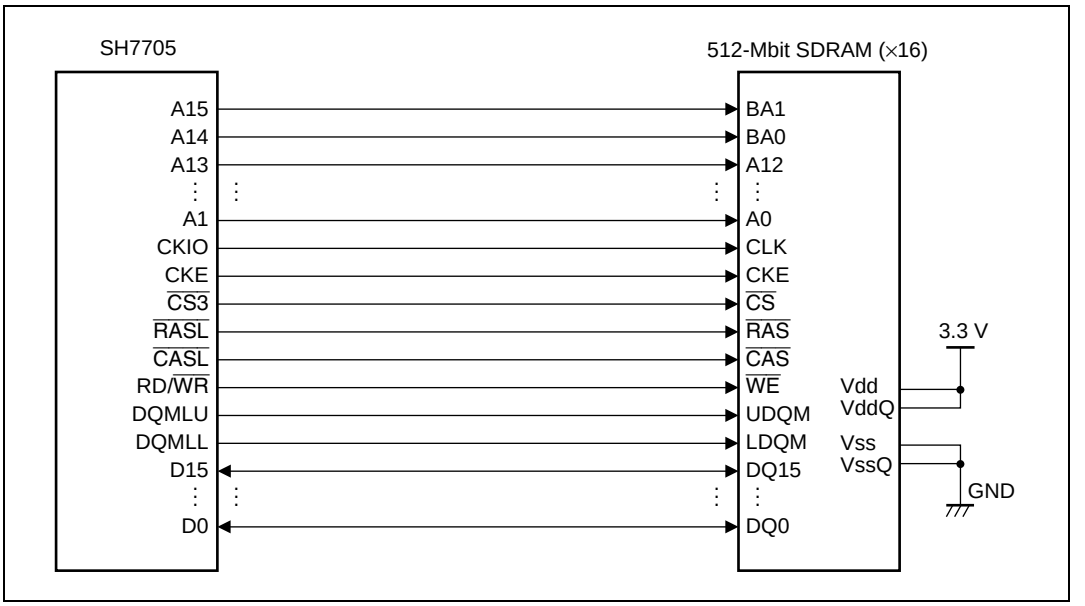


Figure 3.8 Block Diagram

3.2 SH7720 SDRAM Interface Examples

3.2.1 SDRAM Interface

SDRAM Direct Connection: The SDRAM that can be connected to this LSI is a product that has 11/12/13 bits of row address, 8/9/10 bits of column address, 4 or less banks, and uses the A10 pin for setting precharge mode in read and write command cycles.

The control signals for direct connection of SDRAM are $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, DQMUU, DQMUL, DQMLU, DQMLL, CKE, $\overline{CS2}$, and $\overline{CS3}$. All the signals other than $\overline{CS2}$ and $\overline{CS3}$ are common to all areas, and signals other than CKE are valid when $\overline{CS2}$ or $\overline{CS3}$ is asserted. SDRAM can be connected to up to 2 spaces. The data bus width of the area that is connected to SDRAM can be set to 32 or 16 bits.

Burst read/single write (burst length 1) and burst read/burst write (burst length 1) are supported as the SDRAM operating mode.

Commands for SDRAM can be specified by $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, and specific address signals. These commands are shown below.

- NOP
- Auto-refresh (REF)
- Self-refresh (SELF)
- All banks precharge (PALL)
- Specified bank precharge (PRE)
- Bank active (ACTV)
- Read (READ)
- Read with precharge (READA)
- Write (WRIT)
- Write with precharge (WRITA)
- Write mode register (MRS)

The byte to be accessed is specified by DQMUU, DQMUL, DQMLU, and DQMLL. Reading or writing is performed for a byte whose corresponding DQMxx is low.

The power supply pin VccQ1 can be set either to 1.65 to 1.95 V or to 2.7 to 3.6 V. If VccQ1 is set to 1.65 to 1.95 V, we recommend setting the 1.8/3.3 V shared I/O buffers to high drive capacity (DRV = 0), and if VccQ1 is set to 2.7 to 3.6 V, we recommend setting the 1.8/3.3 V shared I/O buffers to low drive capacity (DRV = 1).

UTRCTL register bit 8 (I/O buffer drive control bit)
0: 1.8/3.3 V shared I/O buffers high drive capacity state
1: 1.8/3.3 V shared I/O buffers low drive capacity state

3.2.2 Power On Sequence

In order to use SDRAM, mode setting must first be performed after powering on. To perform SDRAM initialization correctly, the bus state controller registers must first be set, followed by a write to the SDRAM mode register. In SDRAM mode register setting, the address signal value at that time is latched by a combination of the $\overline{CS}$n, $\overline{RAS}$, $\overline{CAS}$, and RD/$\overline{WR}$ signals. If the value to be set is X, the bus state controller provides for value X to be written to the SDRAM mode register by performing a write to address H'A4FD4000 + X for area 2 SDRAM, and to address H'A4FD5000 + X for area 3 SDRAM. In this operation the data is ignored, but the mode write is performed as a byte-size access. To set burst read/single write, CAS latency 2 to 3, wrap type = sequential, and burst length 1 supported by the LSI, arbitrary data is written in a byte-size access to the addresses shown in tables 3.9(1) and 3.9(2). In this time 0 is output at the external address pins of A12 or later.

Table 3.9(1) SDRAM Mode Register Write Access Addresses (Area 2 Settings (SDMR2))

Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD4440	H'0000440
	3	H'A4FD4460	H'0000460
32 bits	2	H'A4FD4880	H'0000880
	3	H'A4FD48C0	H'00008C0

Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD4040	H'0000040
	3	H'A4FD4060	H'0000060
32 bits	2	H'A4FD4080	H'0000080
	3	H'A4FD40C0	H'00000C0

Table 3.9(2) SDRAM Mode Register Write Access Addresses (Area 3 Settings (SDMR3))

Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD5440	H'0000440
	3	H'A4FD5460	H'0000460
32 bits	2	H'A4FD5880	H'0000880
	3	H'A4FD58C0	H'00008C0

Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pins
16 bits	2	H'A4FD5040	H'0000040
	3	H'A4FD5060	H'0000060
32 bits	2	H'A4FD5080	H'0000080
	3	H'A4FD50C0	H'00000C0

Mode register setting timing is shown in figure 3.9. A PALL command (all bank precharge command) is firstly issued. A REF command (auto-refresh command) is then issued 8 times. An MRS command (mode register write command) is finally issued. Idle cycles, of which number is specified by the TRP[1:0] bits in CSnWCR, are inserted between the PALL and the first REF. Idle cycles, of which number is specified by the TRC[1:0]bits in CSnWCR, are inserted between REF and REF, and between the 8th REF and MRS. Idle cycles, of which number is one or more, are inserted between the MRS and a command to be issued next.

It is necessary to keep idle time of certain cycles for SDRAM before issuing PALL command after power-on. Refer the manual of the SDRAM for the idle time to be needed. When the pulse width of the reset signal is longer then the idle time, mode register setting can be started immediately after the reset, but care should be taken when the pulse width of the reset signal is shorter than the idle time.

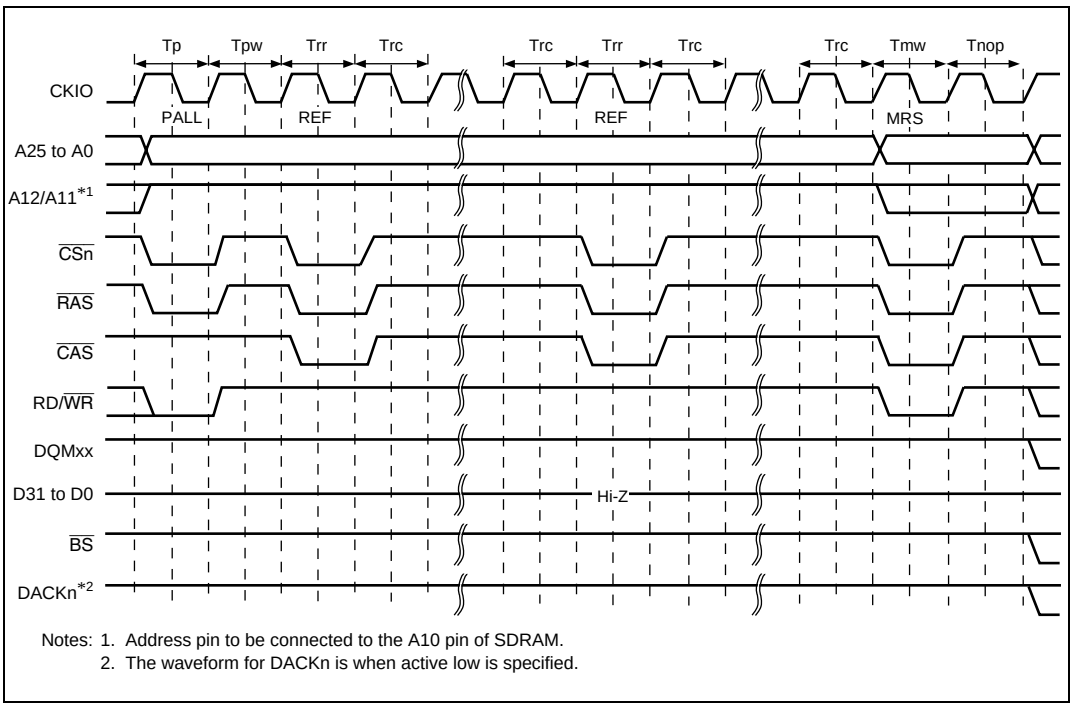


Figure 3.9 Synchronous DRAM Mode Write Timing (Based on JEDEC)

3.2.3 EDS6416AHTA (1 Mword × 16 bits × 4 banks) 64-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS6416AHTA) is connected to the SH7720's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.10 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.10 BSC Settings (EDS6416AHTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0808
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.10 shows the circuit diagram for connecting a single 64-Mbit (1 Mword × 16 bits × 4 banks) SDRAM to area 3.

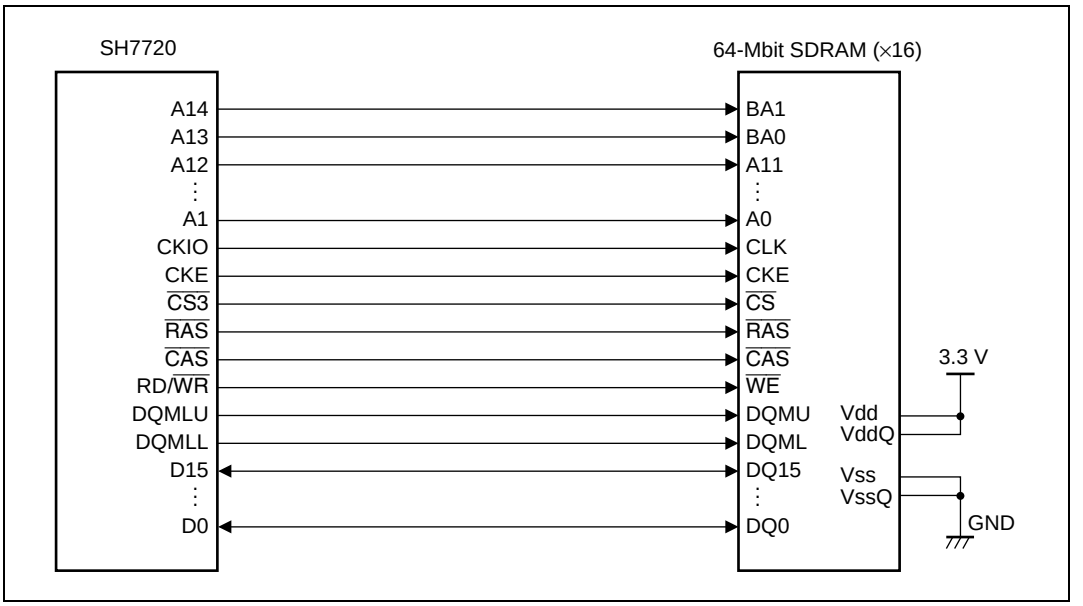


Figure 3.10 Block Diagram

3.2.4 EDS6416AHTA (1 Mword × 16 bits × 4 banks) 64-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS6416AHTA) are connected to the SH7720's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.11 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.11 BSC Settings (EDS6416AHTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0808
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.11 shows the circuit diagram for connecting two 64-Mbit (1 Mword × 16 bits × 4 banks) SDRAMs to area 3.

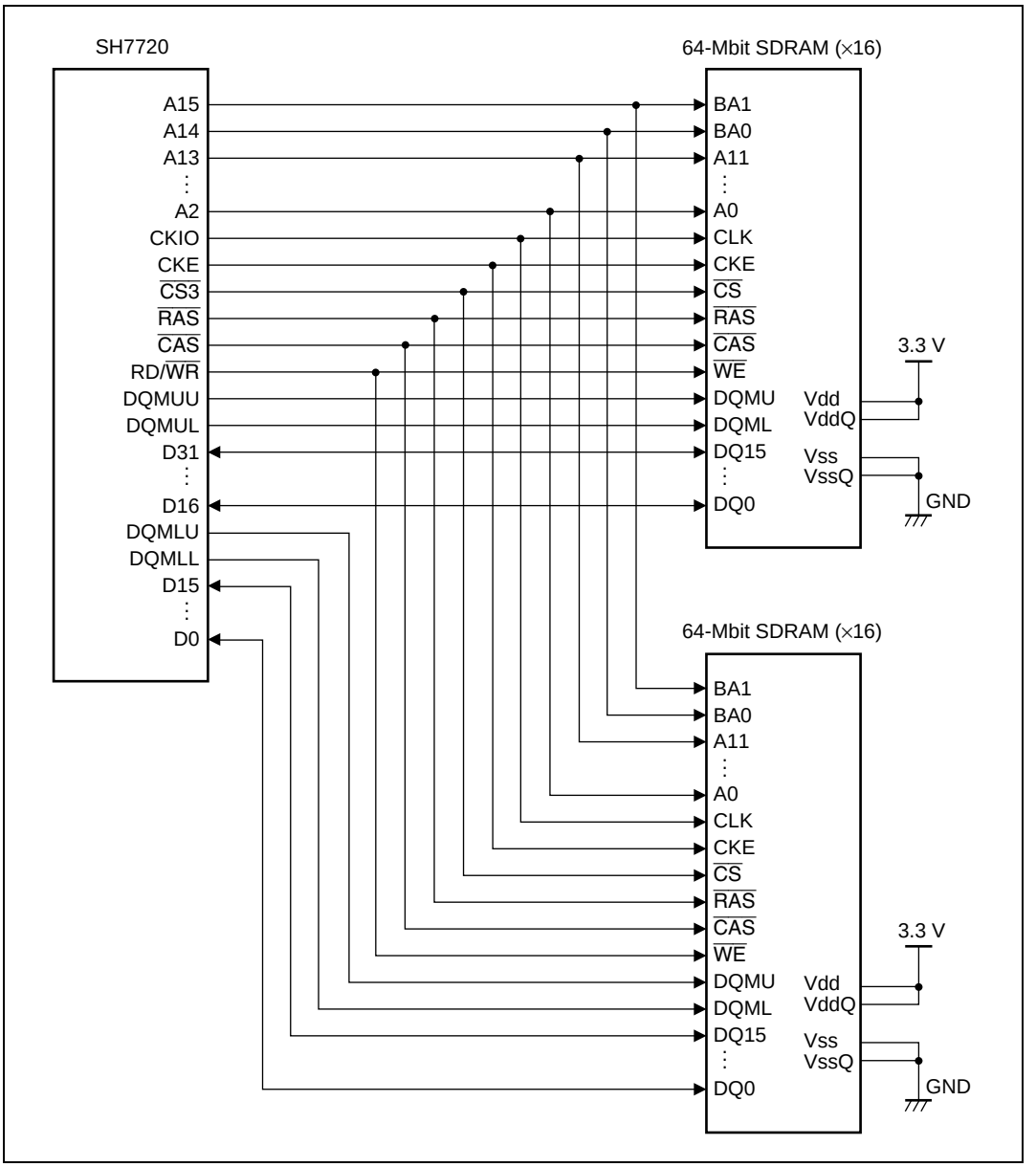


Figure 3.11 Block Diagram

3.2.5 EDS1216AATA (2 Mwords × 16 bits × 4 banks) 128-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS1216AATA) is connected to the SH7720's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.12 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.12 BSC Settings (EDS1216AATA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0809
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.12 shows the circuit diagram for connecting a single 128-Mbit (2 Mwords × 16 bits × 4 banks) SDRAM to area 3.

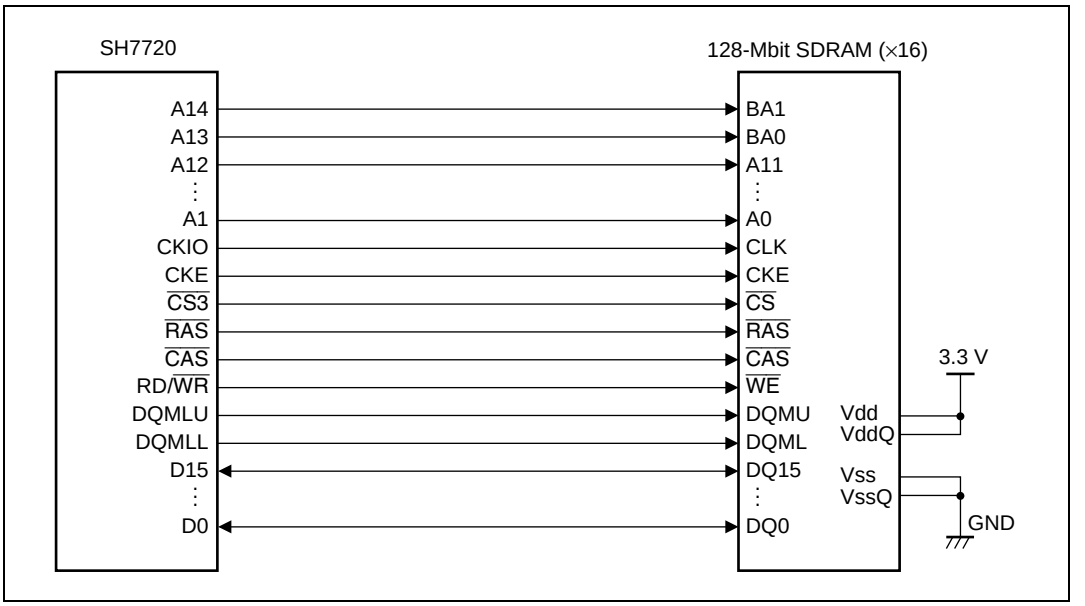


Figure 3.12 Block Diagram

3.2.6 EDS1216AATA (2 Mwords × 16 bits × 4 banks) 128-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS1216AATA) are connected to the SH7720's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.13 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.13 BSC Settings (EDS1216AATA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0809
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 00F8
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.13 shows the circuit diagram for connecting two 128-Mbit (2 Mwords × 16 bits × 4 banks) SDRAMs to area 3.

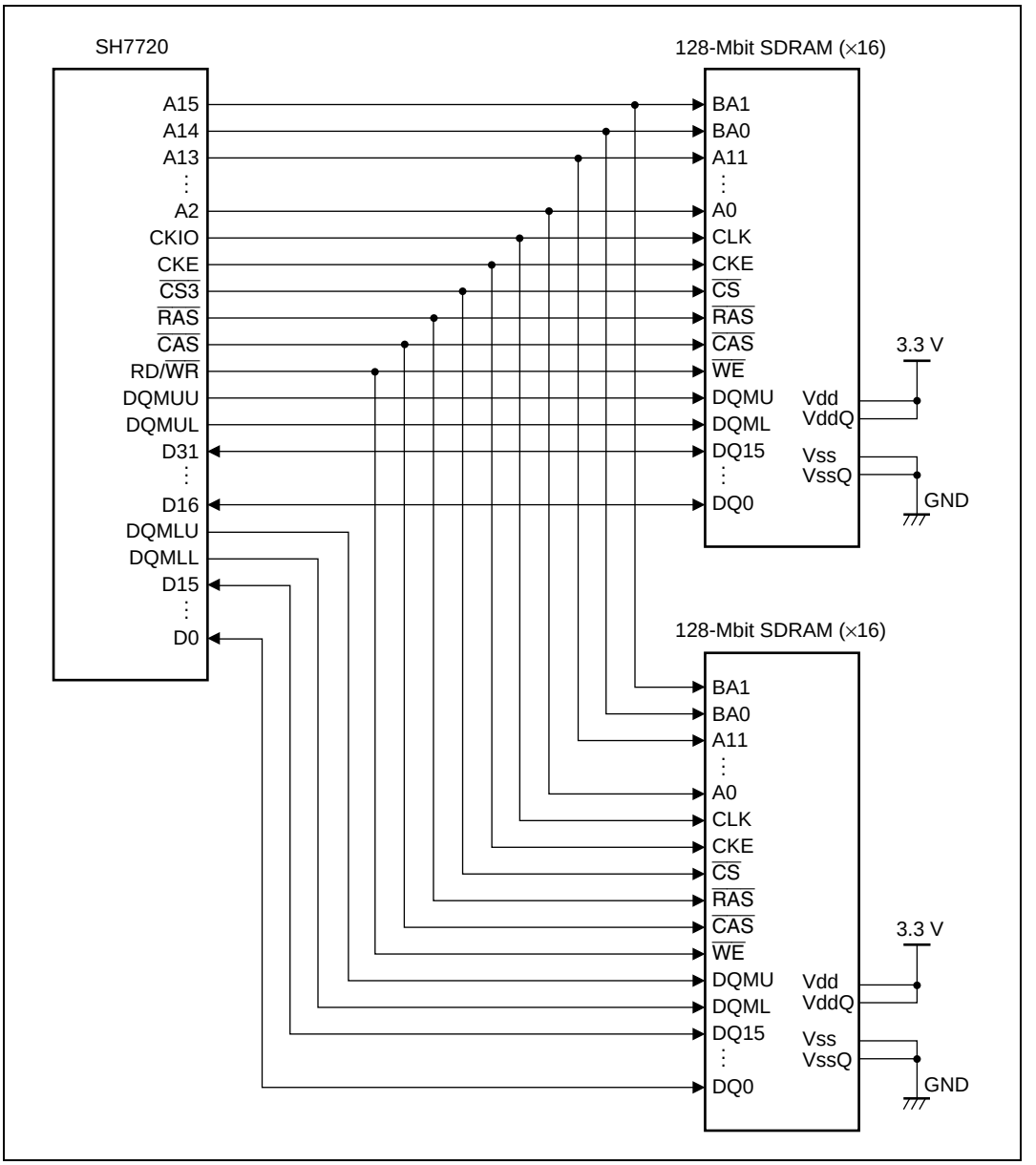


Figure 3.13 Block Diagram

3.2.7 EDS2516ADTA (4 Mwords × 16 bits × 4 banks) 256-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS2516ADTA) is connected to the SH7720's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.14 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.14 BSC Settings (EDS2516ADTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0811
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.14 shows the circuit diagram for connecting a single 256-Mbit (4 Mwords × 16 bits × 4 banks) SDRAM to area 3.

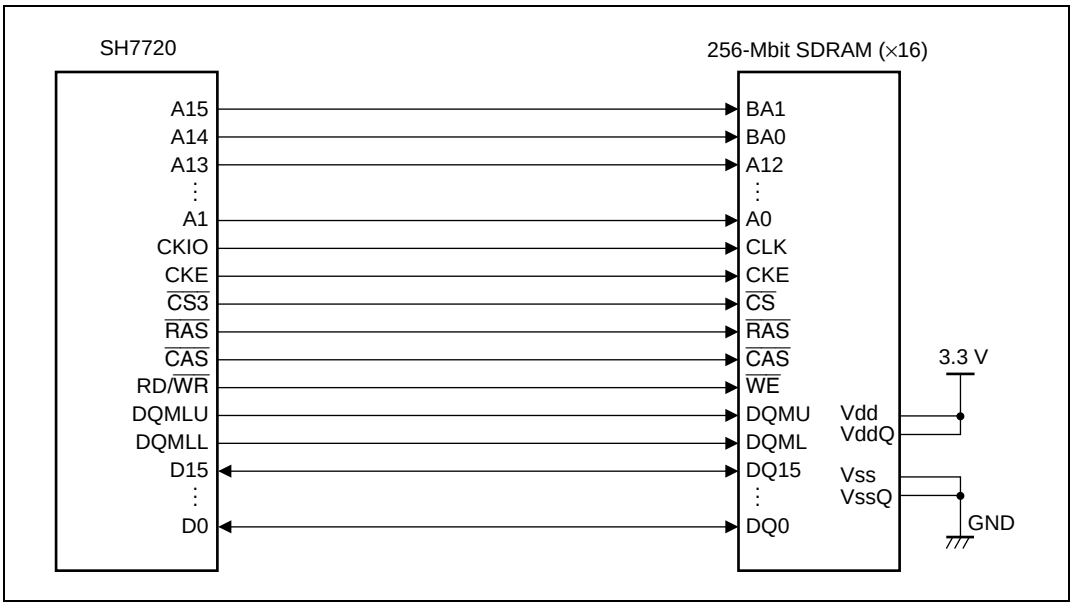


Figure 3.14 Block Diagram

3.2.8 EDS2516ADTA (4 Mwords × 16 bits × 4 banks) 256-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When two SDRAMs (EDS2516ADTA) are connected to the SH7720's area 3 with a 32-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.15 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 2 cycles, TRCD = 2 cycles, TRWL = 2 cycles, TRC = 4 cycles.

Table 3.15 BSC Settings (EDS2516ADTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4600
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 2491
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0811
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5880 CAS latency: 2). External address pins: H'00000880. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5080 CAS latency: 2). External address pins: H'00000080. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.15 shows the circuit diagram for connecting two 256-Mbit (4 Mwords × 16 bits × 4 banks) SDRAMs to area 3.

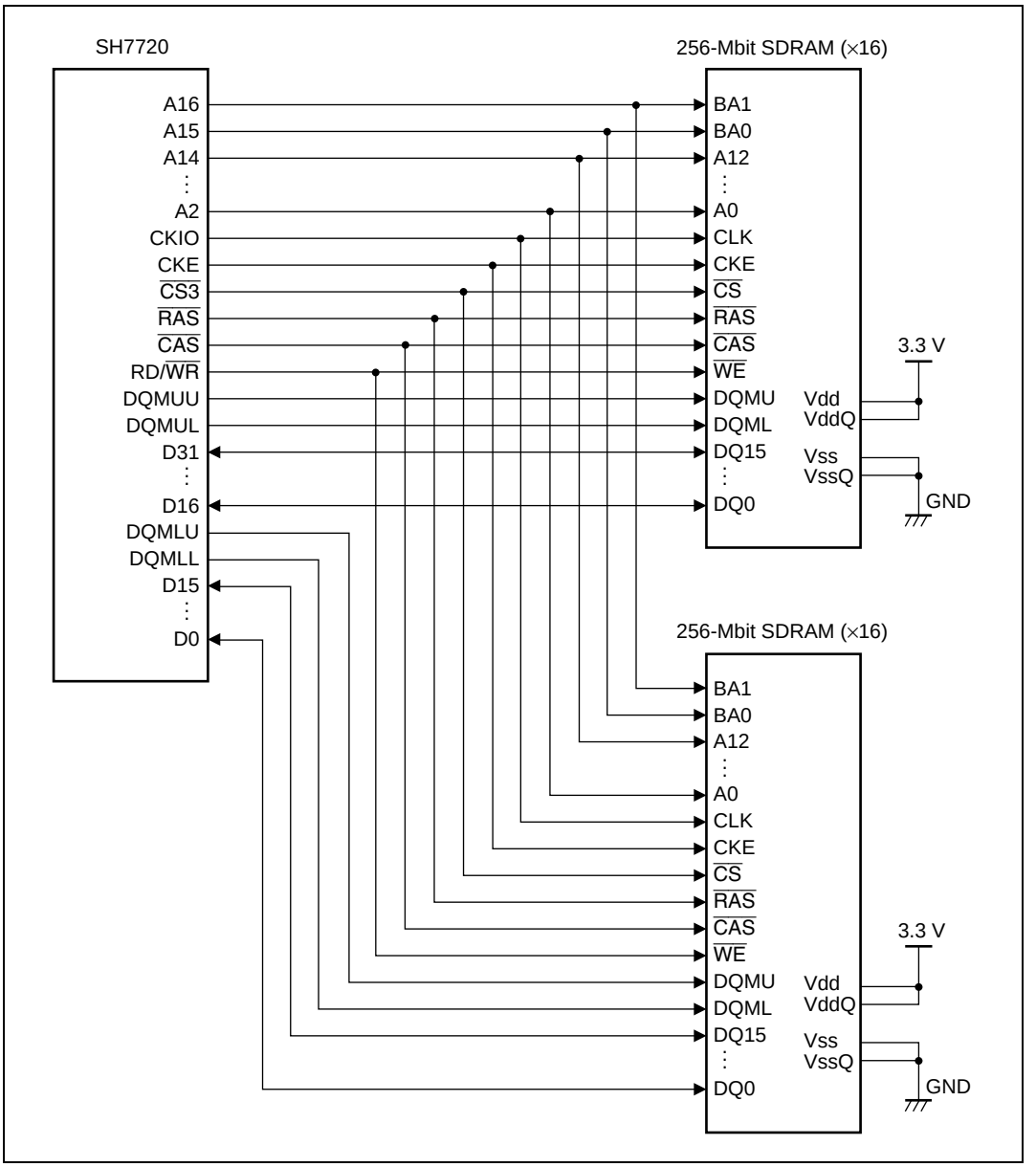


Figure 3.15 Block Diagram

3.2.9 EDS5116ABTA (8 Mwords × 16 bits × 4 banks) 512-Mbit Product Example

(1) Bus State Controller (BSC) Settings

When a single SDRAM (EDS5116ABTA) is connected to the SH7720's area 3 with a 16-bit bus width, the bus state controller (BSC) requires the settings described here. Table 3.16 shows these BSC register setting values.

Note that this SDRAM is connected with the following conditions: bus clock = 66 MHz, CAS latency = 2, TRP = 4 cycles, TRCD = 3 cycles, TRWL = 2 cycles, TRC = 6 cycles.

Table 3.16 BSC Settings (EDS5116ABTA)

Item	Abbreviation	Initial value	Address	Access size	Setting value
Area 2 bus control register	CS2BCR	H'36DB 0600	H'A4FD 0008	32	Arbitrary for area 2
Area 3 bus control register	CS3BCR	H'36DB 0600	H'A4FD 000C	32	H'36DB 4400
Area 2 wait control register	CS2WCR	H'0000 0500	H'A4FD 0028	32	Arbitrary for area 2
Area 3 wait control register	CS3WCR	H'0000 0500	H'A4FD 002C	32	H'0000 6892
SDRAM control register	SDCR	H'0000 0000	H'A4FD 0044	32	H'0000 0812
Refresh timer control register/status register	RTCSR	H'0000 0000	H'A4FD 0048	32	H'A55A 0008
Refresh timer counter	RTCNT	H'0000 0000	H'A4FD 004C	32	H'A55A 0000
Refresh time constant register	RTCOR	H'0000 0000	H'A4FD 0050	32	H'A55A 007C
CS2 space SDRAM mode register	SDMR2	—	H'A4FD 4xxx	16	—
CS3 space SDRAM mode register	SDMR3	—	H'A4FD 5xxx	16	*1

Note: If the value to be written is X, for area 3 the value X can be written to the SDRAM mode register by performing a word write to location X + H'A4FD5000. The data written in this operation is ignored.

1. Write an arbitrary value to H'A4FD5440 CAS latency: 2). External address pins: H'00000440. For burst read/single write (burst length 1).

   Or write an arbitrary value to H'A4FD5040 CAS latency: 2). External address pins: H'00000040. For burst read/burst write (burst length 1).

Note: In this example we assume that the initial values are used for bits unrelated to the external SDRAM connection. All register settings should be reviewed according to the application system.

Figure 3.16 shows the circuit diagram for connecting a single 512-Mbit (8 Mwords × 16 bits × 4 banks) SDRAM to area 3.

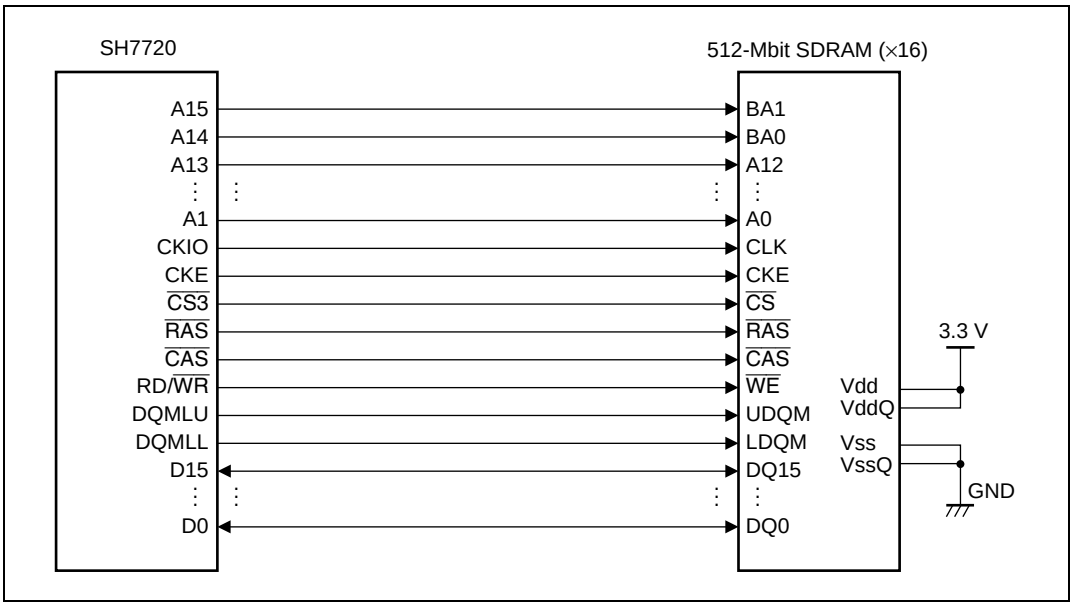


Figure 3.16 Block Diagram

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