SH7670 Group

Example of Cache Memory Setting

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Summary

This application note describes an example of cache-function settings for the SH7670/SH7671/SH7672/SH7673.

Target Device

SH7670 MCU

Contents

1. Introduction

1.1 Specifications

- The instruction cache and the operand cache are enabled and placed in the write-back mode.

1.2 Module Used

- Bus state controller (BSC)
- Cache

1.3 Applicable Conditions

MCU	SH7670
Operating Frequency	Internal clock: 200 MHz Bus clock: 66.6 MHz Peripheral clock: 33.3 MHz
Integrated Development Environment	Renesas Electronics High-performance Embedded Workshop Ver.4.03.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 01
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7670 Group Example of Initialization

2. Description of the Sample Application

This sample application employs the instruction cache and operand cache.

2.1 Summary of MCU Functions Used

If the instruction cache and operand cache are enabled (respectively, when the ICE and OCE bits in register CCR1 are set to 1), whenever an instruction or data in a cacheable area is accessed, the cache is searched to see if it contains the desired instruction or data. The cache is searched according to the following procedure.

1. A single entry is selected by using bits 10 to 4 of the address used to access memory from CPU and the tag addresses at the corresponding entry number in all four ways are read out. At this time, the highest-order three bits of the tag addresses are always cleared to 0.
2. Bits 31 to 11 of the address used to access memory are compared with the tag addresses that have been read out. Address comparison is with the tag addresses read out from the entries in all four ways.
3. When the result of comparison is a match with a tag address and the selected entry is valid (V = 1), a cache hit is said to have occurred. When the comparison does not show a match or the selected entry is not valid (V = 0), a cache miss is said to have occurred.
4. In the case of a cache hit, the long-word (LW) of data at the position in the data array defined by bits 3 and 2 of the accessed address is read or written.

Table 1 Overview of Caches

Item	Description
Capacity	Instruction cache: 8 KB Operand cache: 8 KB
Structure	Instructions and data are separated; each cache is 4-way set associative
Cache lock function	Ways 2 and 3 can be locked (only in the operand cache)
Line size	16 bytes
Number of entries	128
Write system	Write-back and write-through methods are selectable
Replacement method	Least-recently-used (LRU) algorithm

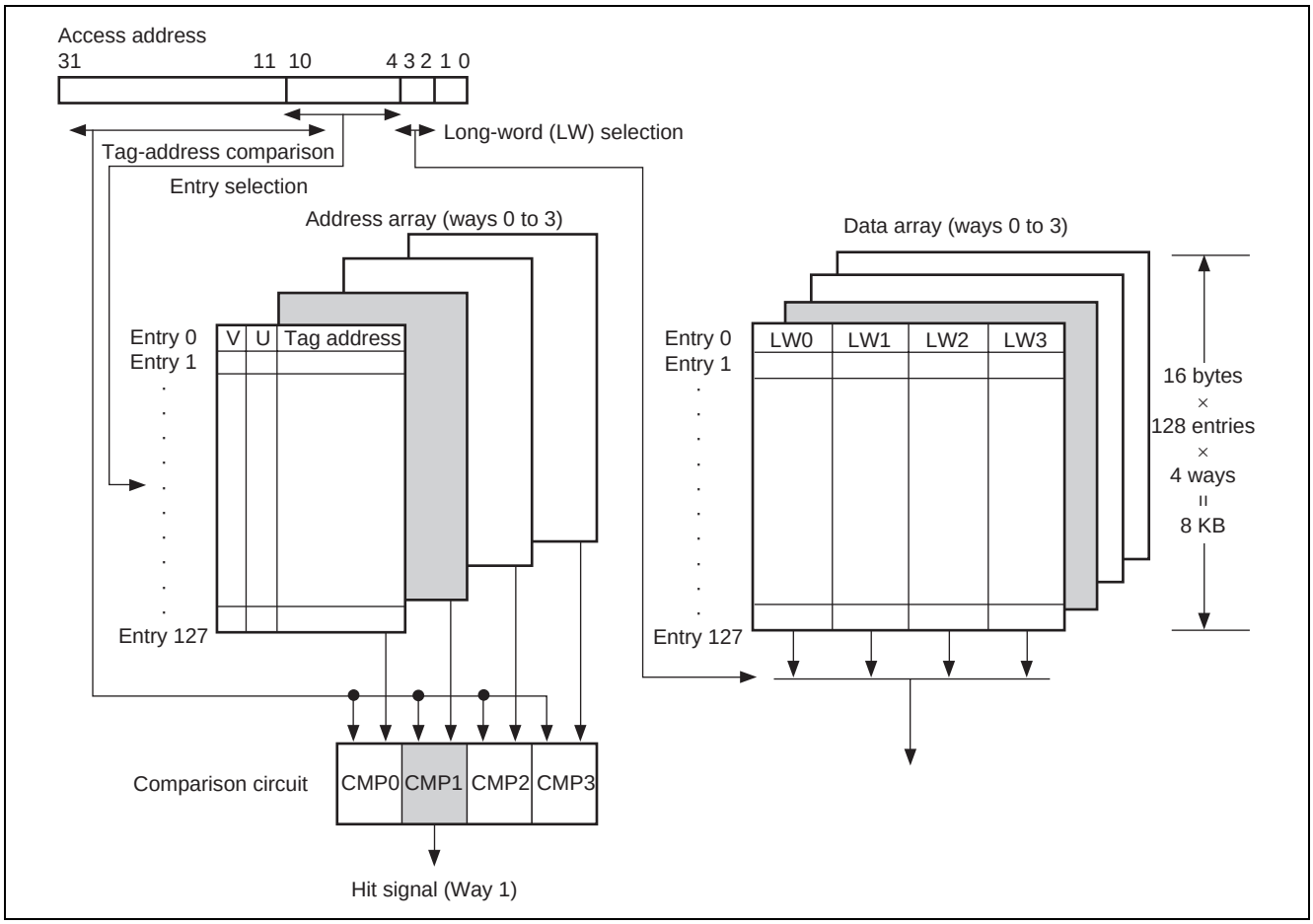

Figure 1 Overview of the Cache-Search Scheme

2.2 Procedure for Setting the Module Used

The procedure for setting up the caches is described below.

Cache control register 1 (CCR1) is used to set up the cache. Program code that manipulates the cache control registers must be executed from an area for which caching is disabled. Also, access to areas for which caching has been enabled must only proceed after the CCR1 register has been read.

This sample application also changes the interrupt mask to prevent the acceptance of interrupt processing that might include access to the cache-enabled spaces while the cache mode is being updated.

Figure 2 is a flow chart showing an example of the procedure used to enable both the instruction cache and operand cache.

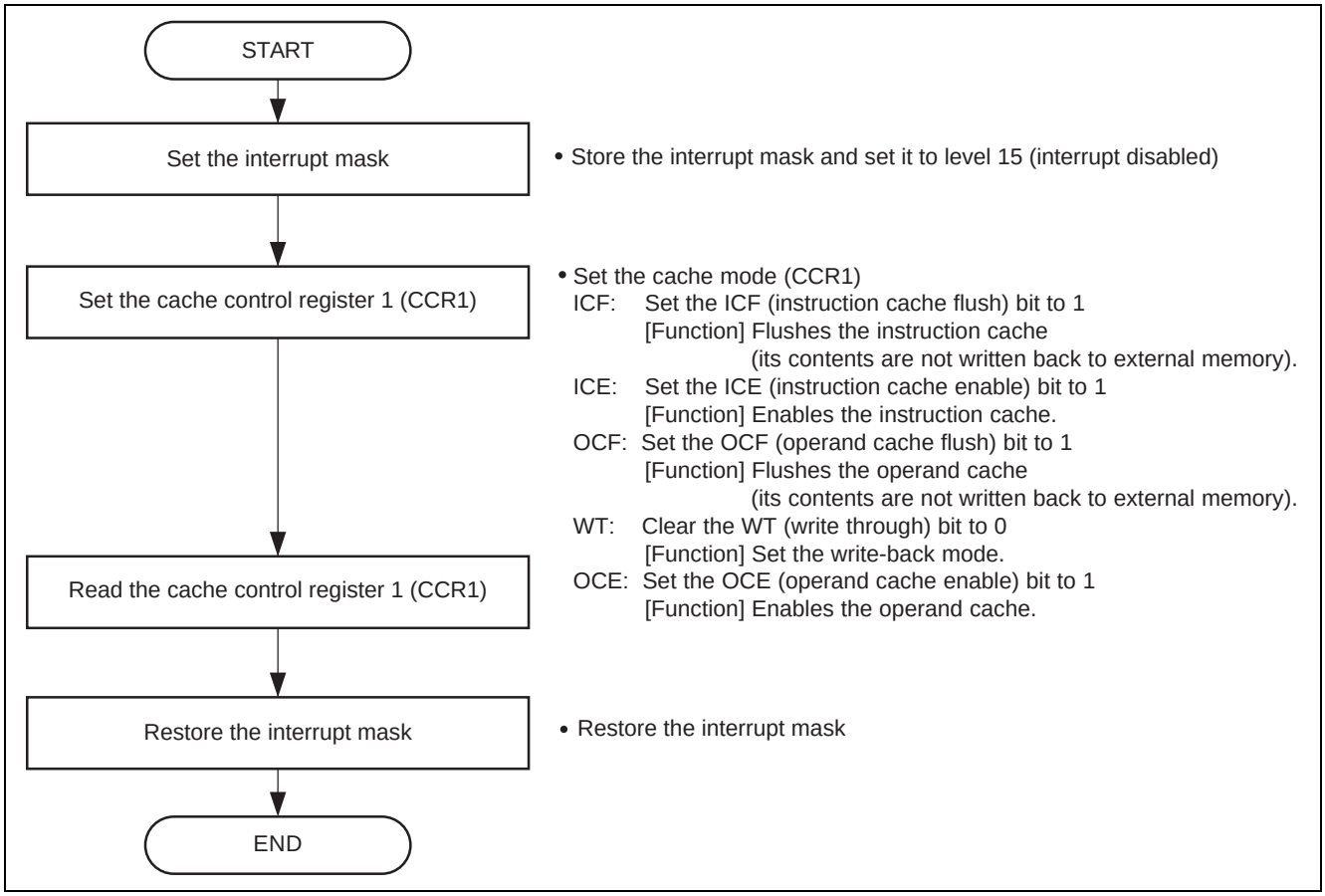

Figure 2 Example Flow for Settings Up the Cache

2.3 Description of the Sample Program

In the sample program, the instruction cache and operand cache are enabled, and then data equivalent to a single cache line (16 bytes) are written to external memory (SDRAM) in write-back mode. In this case, the data are actually written to the cache and not reflected in external memory (SDRAM) until the cache entry (line) is replaced. Contents of external memory (SDRAM) are read out from a cache-disabled space after the fill operation, and compared with the contents of the cache.

The section name for the cache manipulation function is adjusted so that the function is placed in a cache-disabled space.

2.4 Procedure for Processing by the Sample Program

Table 2 describes how the cache is set up by the sample program. Figure 3 shows a flow of processing by the sample program.

Table 2 Cache Settings

Register Name	Address	Setting	Description	
Cache control register1 (CCR1)	H'FFFC 1000	H'0000 0109	ICE = "1":	Enables the instruction cache
			OCF = "1":	Flushes the operand cache
			WT = "0":	Write-back mode
			OCE = "1":	Enables the operand cache

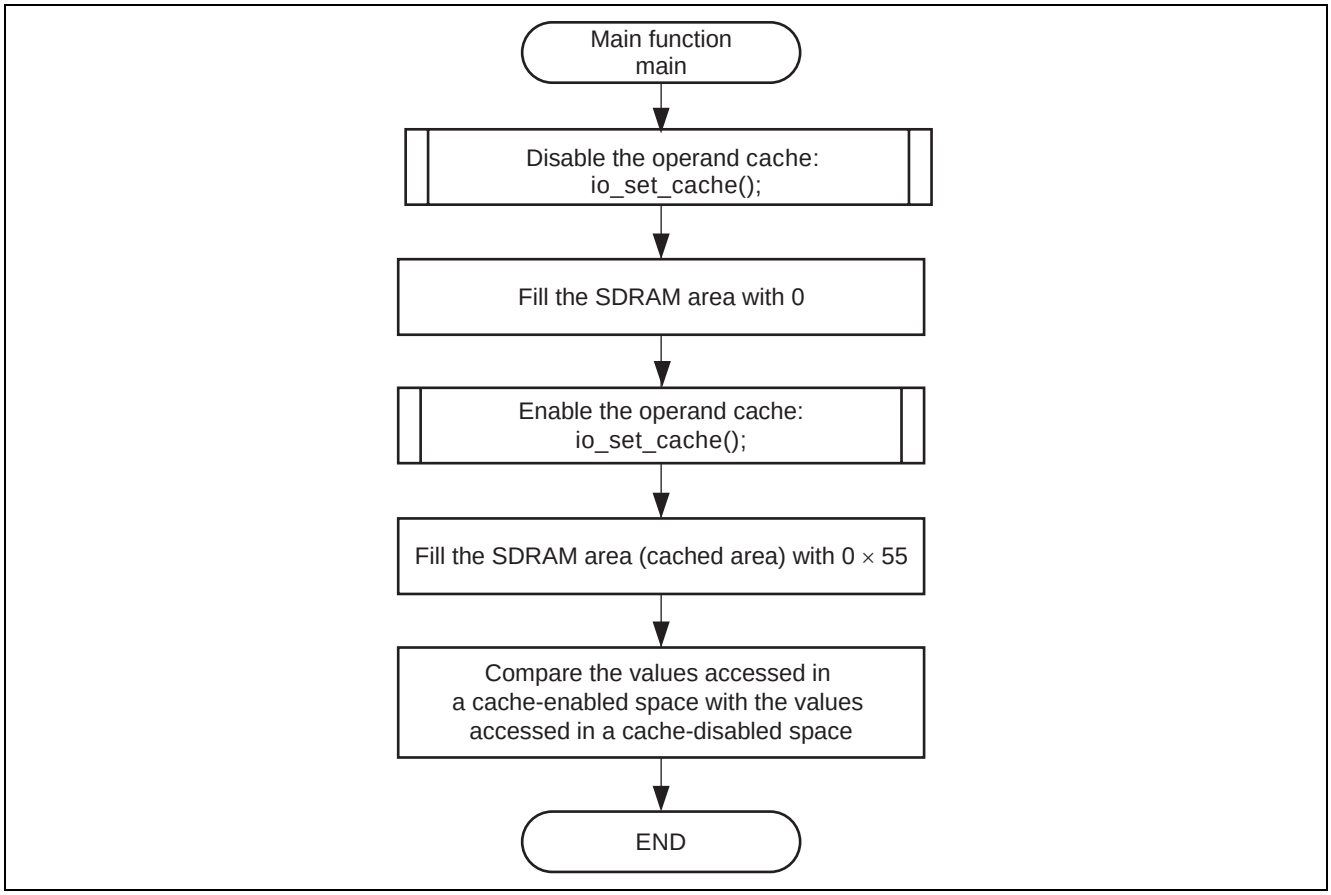

Figure 3 Flow of Processing of the Main Function

2.5 Allocation of Sections in the Sample Program

The cache manipulation function must be placed in a cache-disabled space.

In this sample program, an extended compiler function (the #pragma section directive) is used to place the function that manipulates the cache control registers (io_set_cache) in a specific section (the PCACHE section) separately from the rest of the program. Linkage editor options are then specified so that only this PCACHE section is allocated to a cache-disabled space. That is, the rest of the program is allocated to a cache-enabled space (the P section).

Figure 4 is a memory map for the sample program.

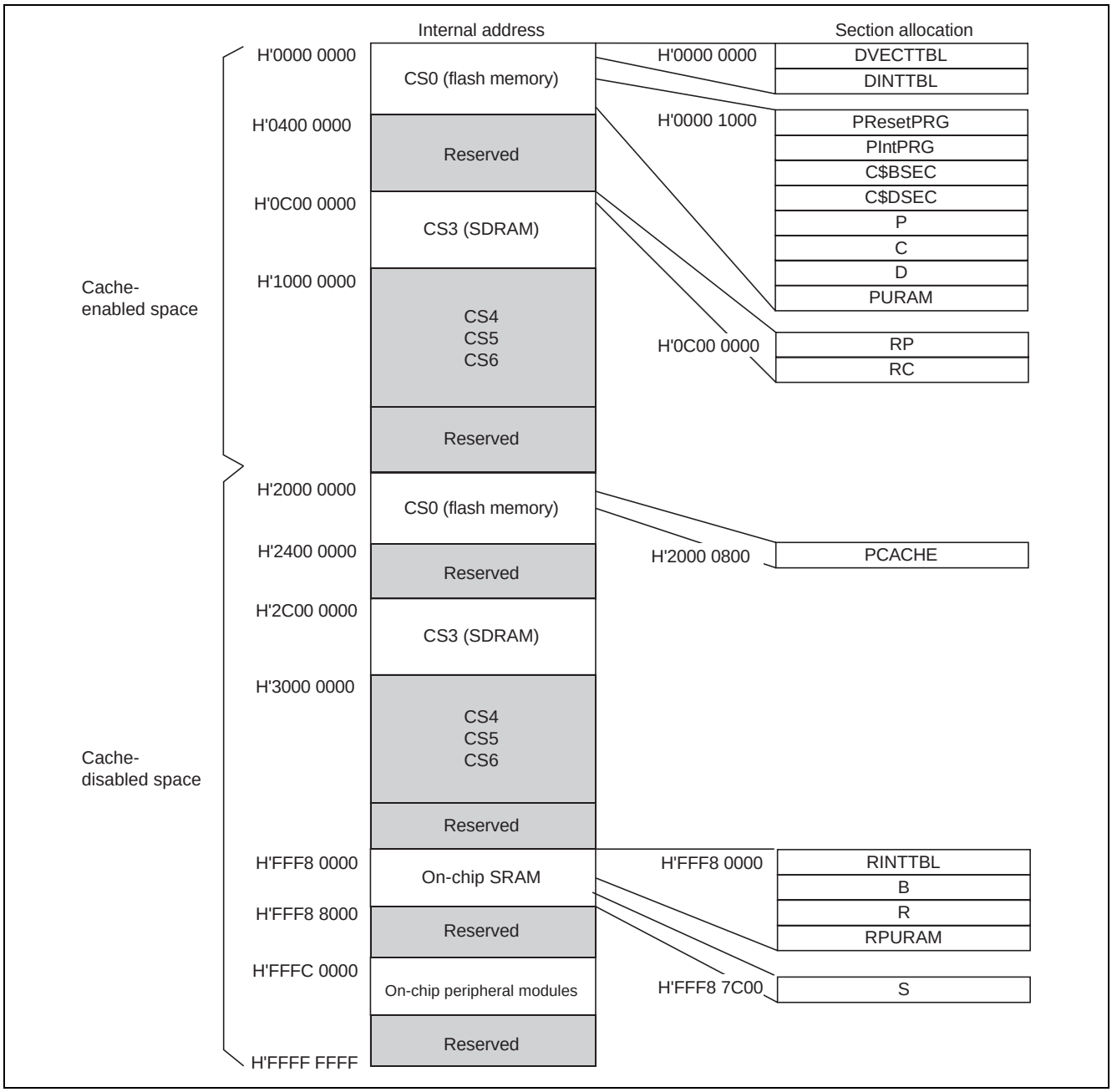

Figure 4 Memory Map of the Sample Program

3. Sample Program Listing

3.1 Sample program list "main.c" (1)

```
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***********************************************************************
* Copyright (C) 2007(2010) Renesas Electronics Corporation. All rights reserved.
*""FILE COMMENT""*********** Technical reference data *************************
*   System Name : SH7671 Sample Program
*   File Name   : main.c
*   Abstract    : sample of cache memory setting
*   Version     : 1.01.03
*   Device      : SH7671
*   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
*               : C/C++ compiler package for the SuperH RISC engine family
*               :                               (Ver.9.01 Release01).
*   OS          : None
*   H/W Platform: M3A-HS71(CPU board)
*   Description :
***********************************************************************
*   History     : Jul.05,2007 ver.1.00.00
*               : Jul.09,2007 ver.1.01.00 Revision of the section allocation
*               : Jan.17,2008 ver.1.01.01 Revision of comment
*               : Feb.28,2008 ver.1.01.02 Revision of a macro name
*               : May 10,2010 ver.1.01.03 Changed the company name and device name
*""FILE COMMENT END""*************************************************/
#include <machine.h>
#include "iodefine.h"  /* iodefine.h is a file automatically generated by the
                          High-performance Embedded Workshop */
#include "defs.h"
```

3.2 Sample program list "main.c" (2)

```
52
53    /* ==== Prototype declaration  ==== */
54    void main(void);
55
56    /* ==== Macro definition ==== */
57    #define SDRAM_ADDR_CACHABLE       (volatile unsigned char *)(0x0C100000)
58    #define SDRAM_ADDR_NON_CACHABLE   (volatile unsigned char *)(0x2C100000)
59
60    /*""FUNC COMMENT""*****************************************************************
61     * ID          :
62     * Outline     : Sample Program main
63     *-------------------------------------------------------------------------------
64     * Include     : #include "iodefine.h"
65     *-------------------------------------------------------------------------------
66     * Declaration : void main(void)
67     *-------------------------------------------------------------------------------
68     * Function    : Example of enabling / disabling cache memory.
69     *             : After the SDRAM area has been initialized with the operand cache OFF,
70     *             : a fill operation is performed with the operand cache ON,
71     *             : and the cached area is compared with its shadow in the cache-disabled
       space.
72     *            : The operand cache is to be controlled.
73     *-------------------------------------------------------------------------------
74     * Argument    : void
75     *-------------------------------------------------------------------------------
76     * ReturnValue : void
77     *-------------------------------------------------------------------------------
78     * Notice      : In this sample program, the cache is flushed. Therefore,
79     *             : a program for initialization that enables the cache will invalidate
80     *             : the contents of the cache.
81     *""FUNC COMMENT END""*************************************************************/
82    void main(void)
83    {
84      int i;
85      unsigned char *ptr1, *ptr2;
86
87      /* ==== Disabling operand cache ==== */
88      io_set_cache( 0x00000108 );         /* Instruction cache enable           *
89                                       * Operand cache flush *
90                                       * Write-back mode            *
91                                       * Operand cache disable      */
92      /* ---- Initializing SDRAM ---- */
93      ptr1 = SDRAM_ADDR_CACHABLE;         /* Cache-enabled space            */
94      for(i=0; i<16; i++){            /*  Written to actual memory */
95        *ptr1++ = 0;                  /*  as caching is disabled               */
96      }
97      /* ==== Enabling operand cache  ==== */
98      io_set_cache( 0x00000109 );         /* Instruction cache enable           *
99                                       * Operand cache flush *
100                                      * Write-back mode        *
101                                      * Operand cache enable       */
```

3.3 Sample program list "main.c" (3)

```
102      /* ---- Filling SDRAM area  ---- */
103      ptr1 = SDRAM_ADDR_CACHABLE;         /* Cache-enabled space            */
104      for(i=0; i<16; i++){            /*  Only written to the cache */
105        *ptr1++ = 0x55;               /*  in write-back mode    */
106      }
107      /* ==== Comparing cache-enabled and cache-disabled spaces ==== */
108      ptr1 = SDRAM_ADDR_CACHABLE;         /* Cache-enabled space        */
109      ptr2 = SDRAM_ADDR_NON_CACHABLE;     /* Cache-disabled space       */
110
111      for(i=0; i<16; i++){
112        if(*ptr1++ == *ptr2++ ){
113            while(1){
114                /* Error in cache setting  */
115            }
116        }
117      }
118      while(1){
119        /* Program end */
120      }
121    }
122
123    #pragma section CACHE                /* Allocated to a non-cacheable area */
124    /*""FUNC COMMENT""*****************************************************************
125     * ID          :
126     * Outline     : Cache setting
127     *-------------------------------------------------------------------------------
128     * Include     : #include <machine.h>
129     *             : #include "iodefine.h"
130     *-------------------------------------------------------------------------------
131     * Declaration : int io_set_cache(unsigned int mode)
132     *-------------------------------------------------------------------------------
133     * Function    : Cache is placed in the mode specified by the argument "mode".
134     *-------------------------------------------------------------------------------
135     * Argument    : unsigned int mode  : I : Set the value of cache control register 1
136     *-------------------------------------------------------------------------------
137     * ReturnValue : 0 : Normally finished
138     *-------------------------------------------------------------------------------
139     * Notice      : This function must be allocated in the CSO non-cacheable area.
140     *             : Interrupts are disabled during cache operation.
141     *""FUNC COMMENT END""*************************************************************/
142    int io_set_cache(unsigned int mode)
143    {
144      int mask;
145
146      mask = get_imask();                /* ↓↓↓ interrupts disabled  ↓↓↓ */
147      set_imask(15);
148
149      /* ==== Setting cache register ==== */
150      CCNT.CCR1.LONG = mode;
151
152      set_imask(mask);                /* ↑↑↑ interrupts disabled  ↑↑↑ */
153
154      return 0;
155    }
156    /* End of file */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas Electronics website.

- Hardware Manual
  SH7670 Group Hardware Manual Rev. 2.00
  The latest version of the hardware user's manual can be downloaded from the Renesas Electronics website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Oct.31.08	—	First edition issued
1.01	Oct.15.10	—	Changed the sample program (AC Switching Characteristics are removed)

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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
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Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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