SH7670 Group

Example of BSC SDRAM Interface Connection (32-Bit Data Bus)

REJ06B0782-0101
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May 07, 2010

Introduction

This application note introduces the synchronous DRAM (SDRAM) interface of the bus state controller (BSC) of SH7670/SH7671/SH7672/SH7673 products and includes a sample application.

Target Device

SH7670

Contents

1. Preface

1.1 Specifications

- Two 256-Mbit (4 Mwords × 16 bits × 4 banks) SDRAM modules are connected to the SH7670 with a 32-bit data bus width.
- SDRAM is initialized by using the SDRAM interface function of the SH7670.

1.2 Module Used

- Bus state controller (BSC)

1.3 Applicable Conditions

• MCU	SH7670/SH7671/SH7672/SH7673 (R5S76700/R5S76710/R5S76720/R5S76730)
• Operating frequency	Internal clock: 200 MHz Bus clock: 66.67 MHz Peripheral clock: 33.33 MHz
• Integrated development environement	High-performance Embedded Workshop Ver.4.03.00 from Renesas Electronics
• C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Electronics
• Compiler options	Default settings of High-performance Embedded Workshop (-cpu = sh2afpu -fpu = single -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1 -nologo)

1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the *SH7670 Group Application Note: Example of Initialization* (REJ06B0799). Please refer to that document in combination with this one.

2. Description of Sample Application

2.1 Operational Overview of Module Used

The bus state controller (BSC) of the SH7670 supports an SDRAM interface that is directly connectable to SDRAM units that have 11, 12, or 13 bits of row address, 8, 9, or 10 bits of column address, 4 or fewer banks, and in which the A10 pin is used to set pre-charge mode in read and write command cycles. Burst reading/single writing (burst length 1) and burst reading/burst writing (burst length 1) are supported as SDRAM operating modes.

Table 1 provides the specifications of SDRAM used in this sample application.

Table 1 Specifications of SDRAM Used in This Sample Application

Item	Specification
Clock frequency	Up to 133 MHz
Capacity	256 Mbits (32 MB) × 2
Configuration	4 banks × 4 Mwords × 16 bits
CAS latency	2 or 3 (programmable)
Refresh cycle	8192 refresh cycles per 64 ms
Burst length	1, 2, 4 or 8 full pages (programmable)
Row address	A12 to A0
Column address	A8 to A0
Pre-charge	Auto pre-charge/all bank pre-charge controlled via A10

Figure 1 shows a memory map.

SDRAM can be connected to the CS3 space of the SH7670. The value of bit A29 in internal addresses can control enabling and disabling of the cache.

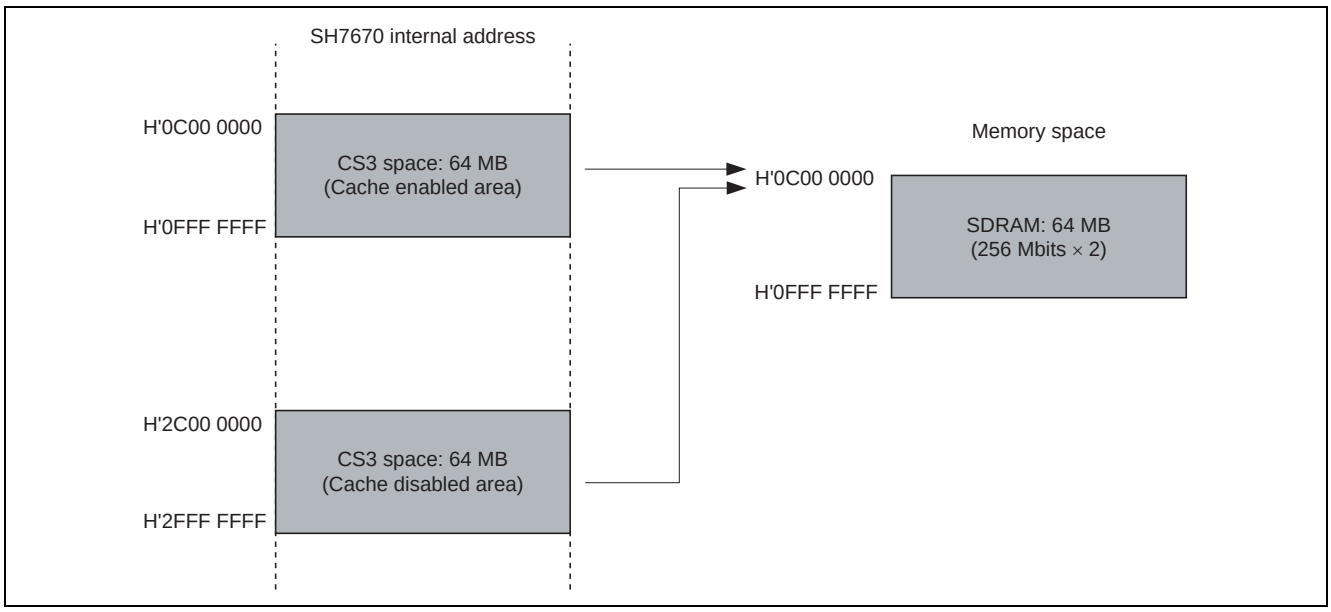


Figure 1 Memory Map in Relation to SDRAM

Figure 2 shows an example of circuitry for SDRAM connection.

Table 2 gives a list of the address-multiplexing output pins in the case of 256-Mbit SDRAM.

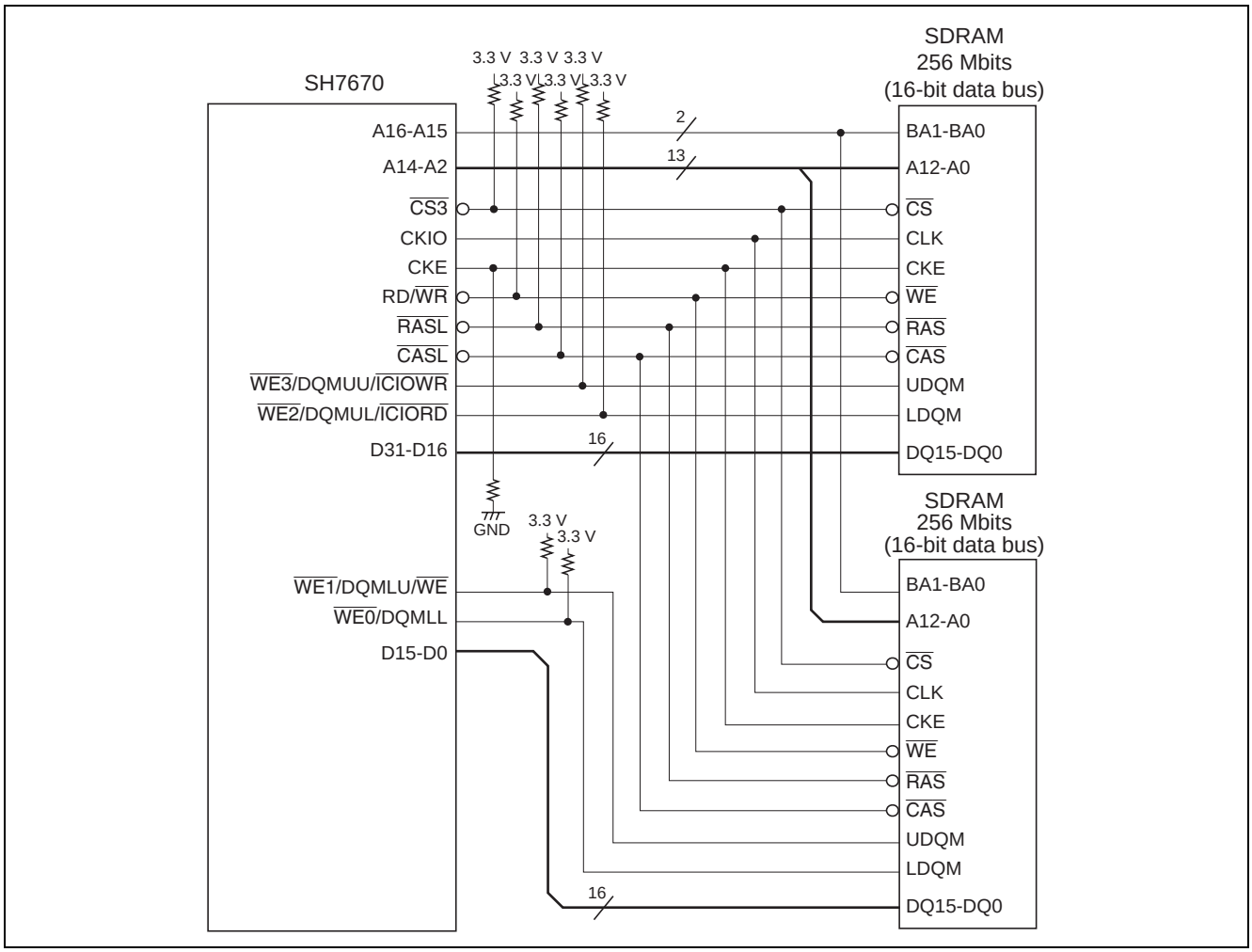


Figure 2 Example of Circuitry for SDRAM Connection (256-Mbit SDRAM × 2 and 32-Bit Bus)

Note: Handling of control signal pins with external pull-up or pull-down resistors
In general, the criterion for whether control pins should be pulled up or down is stability of operation. We thus recommend that the CS, RAS, CAS, WE, DQMU, and DQML pins be pulled up (set to the high level) by external resistors.
The CKE pin is pulled down (set to the low level) by an external resistor for a reason other than that stated above. In this case, the intention is to continue the self-refresh state so that data in the SDRAM are protected even after signals from the MCU have stopped.

Table 2 Connections between SH7670 Pin Functions and SDRAM

SH7670 Pin (32 bits)	Row Address (13 bits)	Column Address (9 bits)	SDRAM Pin	Function
A17	A26	A17		Not in use
A16	A25*[2]	A25*[2]	A14 (BA1)	Specifies bank
A15	A24*[2]	A24*[2]	A13 (BA0)	
A14	A23	A14	A12	Address
A13	A22	A13	A11	
A12	A21	L/H*[1]	A10/AP	Specifies address/pre-charge
A11	A20	A11	A9	Address
A10	A19	A10	A8	
A9	A18	A9	A7	
A8	A17	A8	A6	
A7	A16	A7	A5	
A6	A15	A6	A4	
A5	A14	A5	A3	
A4	A13	A4	A2	
A3	A12	A3	A1	
A2	A11	A2	A0	
A1	A10	A1		Not in use
A0	A9	A0		

Notes: 1. The L/H bit is used in command specification; it is fixed at low or high according to the access mode.
2. Bank address specification

2.2 Procedure for Setting Module Used

2.2.1 Example of the Initialization Procedure for SDRAM

Figure 3 gives an example of the initialization procedure to place SDRAM in the CS3 space.

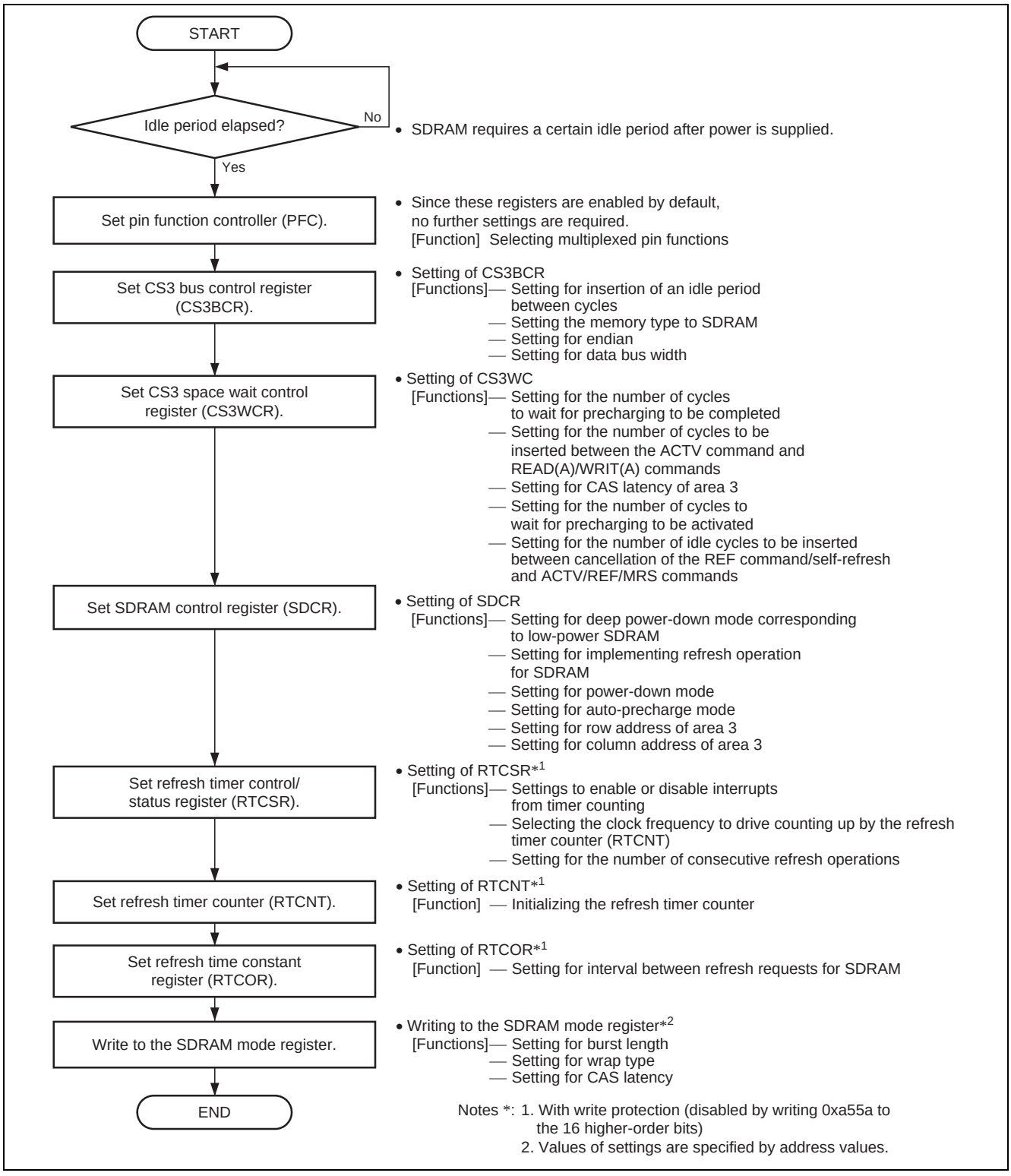


Figure 3 Example of the Procedure for Initial Settings to Place SDRAM in the CS3 Space

2.2.2 Power-On Sequence

To perform SDRAM initialization, registers of the bus state controller must first be set, followed by a write to the SDRAM mode register. Burst length, wrap type, CAS latency, etc. can be set in the mode register. SDRAM requires a certain idle period after power is supplied, and this period differs with the SDRAM specifications. Please confirm the specifications of the SDRAM to be used, and make settings after the idle period has elapsed.

Settings are written to the SDRAM mode register by writing a word (16 bits) with any value to the addresses shown in table 3. Select the address for access in accord with the settings.

Table 3 Addresses for Access to Write Values to the SDRAM Mode Register

Data Bus Width	CAS Latency	Burst Read/Single Write (Burst Length 1)		Burst Read/Burst Write (Burst Length 1)	
		Access Address	External Address Pin	Access Address	External Address Pin
16 bits	2	H'FFFC 5440	H'0000 0440	H'FFFC 5040	H'0000 0040
	3	H'FFFC 5460	H'0000 0460	H'FFFC 5060	H'0000 0060
32 bits	2	H'FFFC 5880	H'0000 0880	H'FFFC 5080	H'0000 0080
	3	H'FFFC 58C0	H'0000 08C0	H'FFFC 50C0	H'0000 00C0

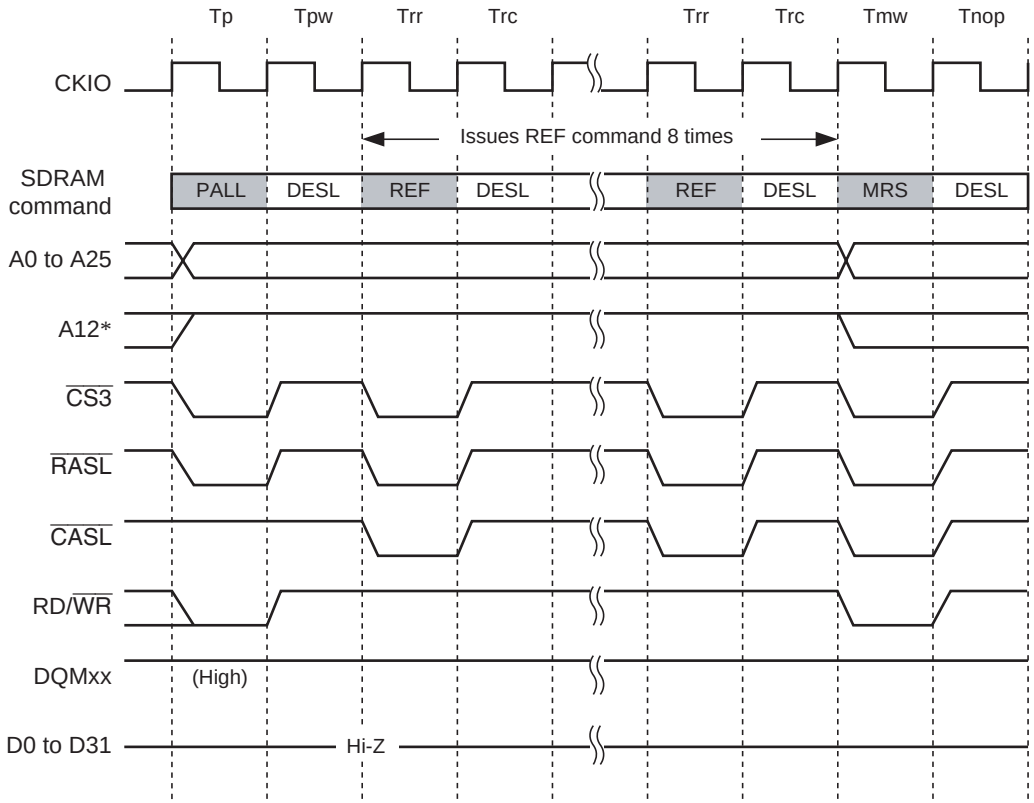
Writing a word to an access address writes the corresponding settings to the SDRAM mode register. Writing is executed by the following commands being issued in sequence. Figure 5 shows an example of timing for writing to the SDRAM mode register.

1. All bank pre-charge command (PALL)
   Idle cycles (Tpw) as specified by the WTRP[1:0] bits in CS3WCR are inserted between the PALL and the first REF.

2. Auto-refresh command (REF, eight times)
   The REF command is issued and is followed by the number of idle cycles (Trc) specified by the WTRC[1:0] bits in CS3WCR. This is repeated eight times.

3. Mode-register setting command (MRS)
   The mode-register setting command is issued in combination with CS3, RAS, CAS, and RD/WR. The combination of levels on the external address pins determines the value of the setting written to the SDRAM.

Furthermore, the burst length is always set to 1 for the SH7670. Accordingly, burst operations to transfer more data than the width of the data bus, for example to transfer 16 bytes of data, are realized by issuing consecutive commands. This is efficient because unnecessary bus cycles are not generated even when the access size is small. Selection of burst read/single write (burst length 1) or burst read/burst write (burst length 1) as given in table 3 does not affect the operation of the SH7670.



PALL: All banks pre-charge command (idle cycles (Tpw) as set by the WTRP bits in CS3WCR are inserted.)
REF: Auto-refresh command (idle cycles (Trc) as set by the WTRC bits in CS3WCR are inserted.)
MRS: Mode register write command
DESL: Deselect command
Note *: This address pin is connected to the A10 pin of the SDRAM.

Figure 5 Example of Timing for Writing to the SDRAM Mode Register

2.3 Operation of the Sample Program

SDRAM read and write operations for sample program are described as follows:

1. Read operation
   Figure 6 shows an example of SDRAM single-read timing in operation with the bus clock running at 66.67 MHz. The operations below are performed on successive cycles of the SH7670.

   — Tr : An ACTV command is issued, activating the relevant rows and banks.
   — Trw1, Trw2 : Wait cycles are inserted between the ACTV command and READ(A)/WRIT(A) commands. The number of wait cycles (two) for insertion is set by the WTRCD bits in CS3WCR.
   — Tcl : A READ(A) command is issued; a read command with auto-precharge is issued.
   — Tcw : Wait cycles are inserted between the Tcl and Tdl cycles. The wait cycles are equivalent to the number set for the CAS latency –1; the number of wait cycles (one) for insertion is set by the A3CL bits in CS3WCR.
   — Td1 : Read data are retrieved. In the case of burst reading, consecutive READ(A) commands are issued to read the data in sequence.
   — Tde : This is an idle cycle that is necessary for transfer of the read data within this LSI. One cycle must be allowed without fail for both burst-read and single-read operations.
   — Tap : This is a cycle of waiting for completion of auto-precharge. The number of wait cycles (one) for insertion is set by the WTRP bits in CS3WCR.

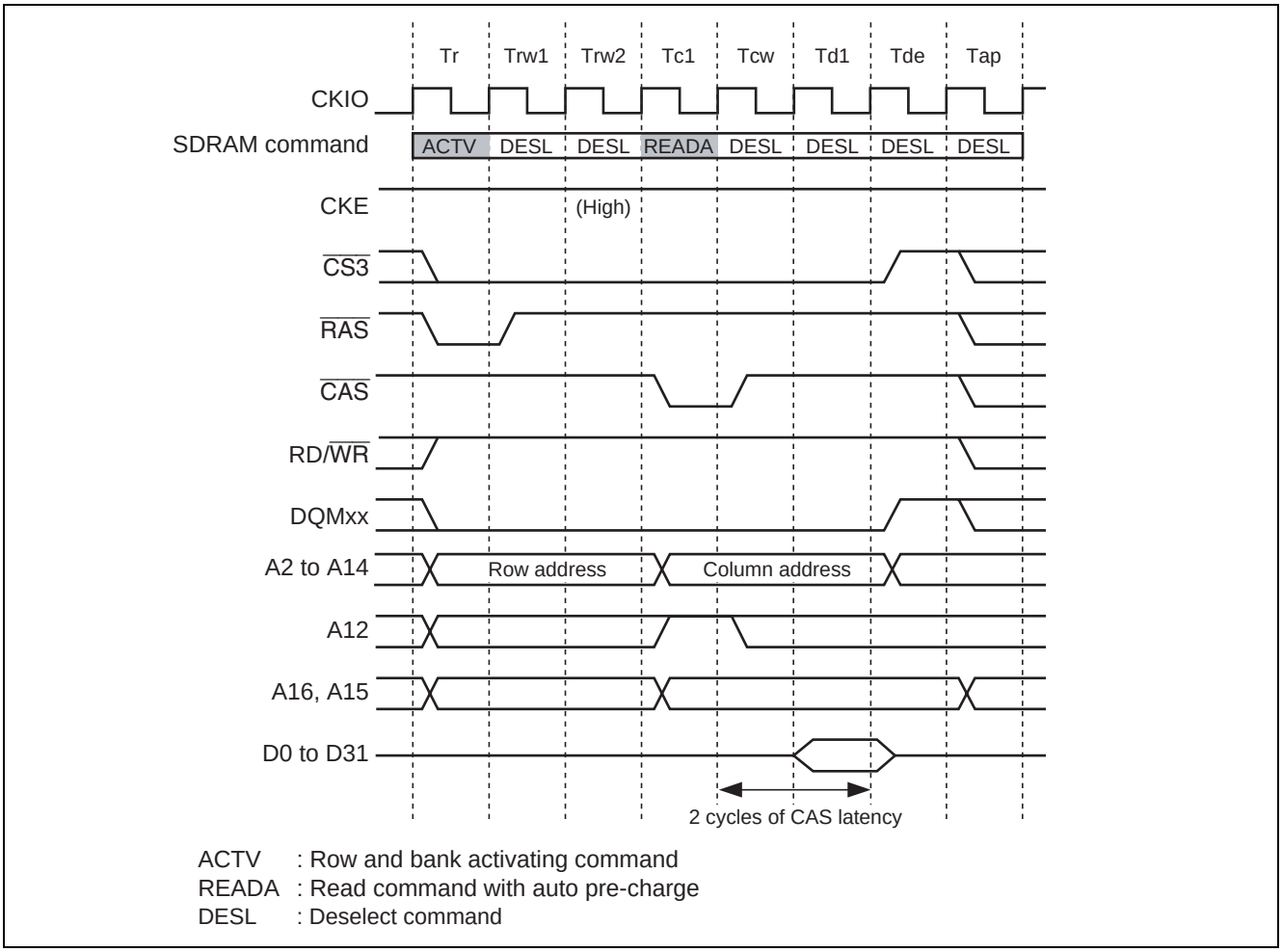


Figure 6 Example of SDRAM Single-Read Timing (Auto-Precharge)

2. Write operation
   Figure 7 shows an example of SDRAM single-write timing in operation with the bus clock running at 66.67 MHz. The operations below are performed on successive cycles of the SH7670.

   — Tr : An ACTV command is issued, activating the relevant rows and banks.
   — Trw1, Trw2 : Wait cycles are inserted between the ACTV command and READ(A)/WRIT(A) commands. The number of wait cycles (two) for insertion is set by the WTRCD bits in CS3WCR.
   — Tcl : A WRIT(A) command is issued; a write command with auto-precharge is issued. In case of burst writing, a WRIT(A) command is consecutively issued.
   — Trw1, Trw2 : These are cycles of waiting for activation of auto-precharge. The number of wait cycles (two) for insertion is set by the TRWL bits in CS3WCR.
   — Tap : This is a cycle of waiting for completion of auto-precharge. The number of wait cycles (one) for insertion is set by the WTRP bits in CS3WCR.

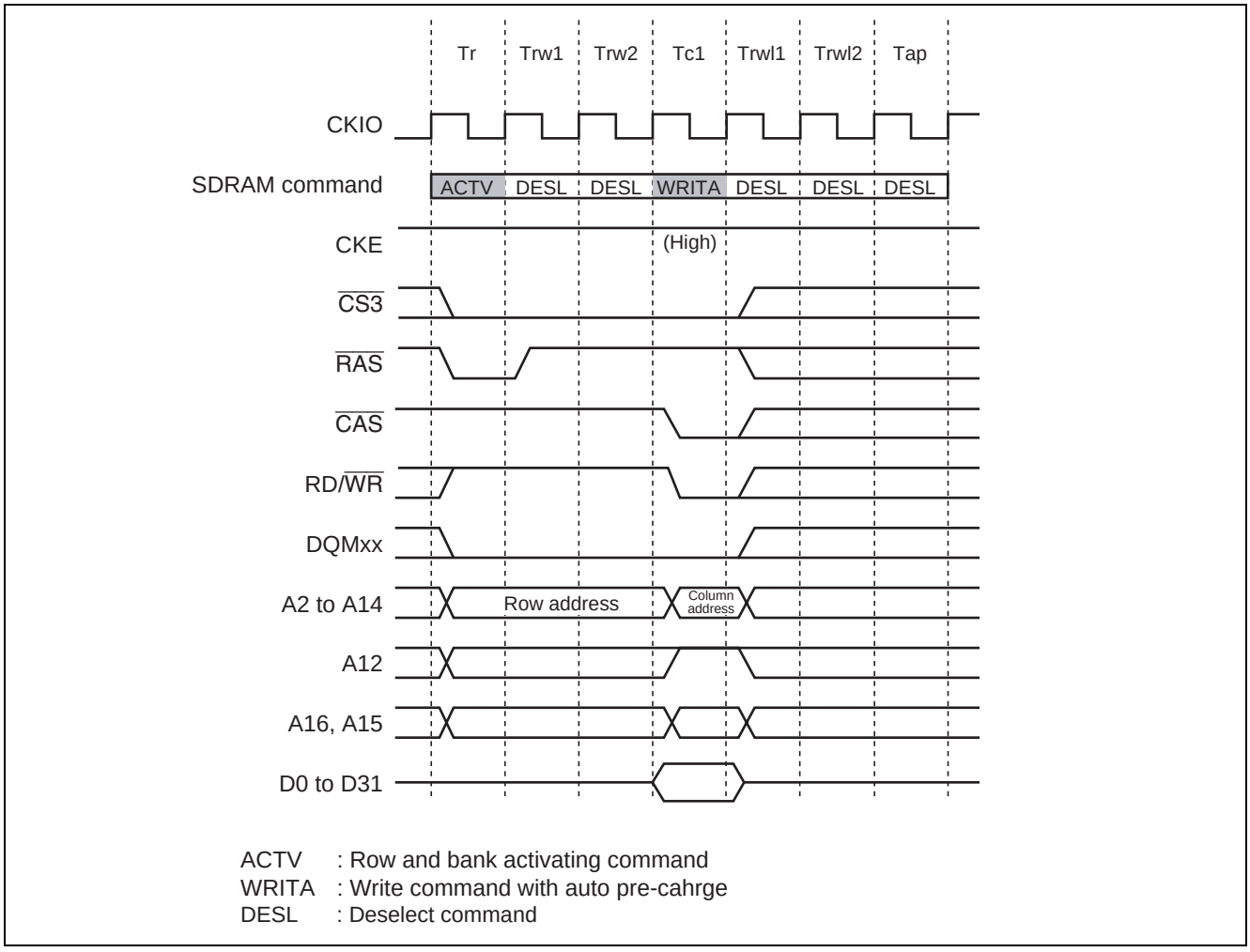


Figure 7 Example of Timing for Single-Writing to SDRAM (Auto Pre-charge)

2.4 Sample Settings of Bus State Controller

Table 4 provides sample settings of the BSC in operation with the SH7670 bus clock running at 66.67 MHz. For details on individual registers, please refer to the section on the bus state controller in the *SH7670 Group hardware manual* (REJ09B0437).

Table 4 Sample Settings of the BSC

Name of Register	Address	Setting Value	Description
CS3 space bus control register (CS3BCR)	H'FFFC 0010	H'0000 4600	• IWW[2:0], IWRWD[2:0], IWRWS[2:0], IWRRD[2:0], IWRRS[2:0] = B'000: No idle cycles are inserted. • TYPE[2:0] = B'100: SDRAM • ENDIAN = 0: Arranged in big endian • BSZ[1:0] = B'11: 32-bit data bus width
CS3 space wait control register (CS3WCR)	H'FFFC 0034	H'0000 2892	• WTRP[1:0] = B'01: Number of cycles to wait for completion of precharging is 1. • WTRCD[1:0] = B'10: Number of wait cycles inserted between ACTV command and READ(A)/WRIT(A) commands is 2. • A3CL[1:0] = B'01: CAS latency of area 3 is 2 cycles. • TRWL[1:0] = B'10: Number of cycles to wait for activation of precharging is 2. • WTRC[1:0] = B'10: Number of idle cycles inserted between cancellation of REF command/self-refresh and ACTV/REF/MRS commands is 5.
SDRAM control register (SDCR)	H'FFFC 004C	H'0000 0811	• DEEP = 0: Deep power-down mode is not in use. • RFSH = 1: Refresh • RMODE = 0: Auto-refresh • PDOWN = 0: Power-down mode is not in use. • BACTV = 0: Auto pre-charge mode • A3ROW[1:0] = B'10: Row address of area 3 is 13 bits. • A3COL[1:0] = B'01: Column address of area 3 is 9 bits.
Refresh timer control register/status register (RTCSR)	H'FFFC 0050	H'A55A 0010*	• CKS[2:0] = B'010: Bϕ/16 is selected. • RRC[2:0] = B'000: Refresh count is once.
Refresh time constant register (RTCOR)	H'FFFC 0058	H'A55A 0020*	• Interval between refresh requests for SDRAM = H'20 Request interval: 8192 cycles/64 ms = 7.8125 μs/time, 1 cycle: 1/(Bϕ (66.67 MHz)/16) = 240 ns, 7.8125 μs/240 ns > 32 = H'20
Refresh timer counter (RTCNT)	H'FFFC 0054	H'A55A 0000*	• Initialization of counter

Note: When writing, set the upper 16 bits to H'A55A to disable write protection.

3. Listing of Sample Program

3.1 Sample Program Listing: "bscsdram.c" (1)

```
1         /***********************************************************************
2         *   DISCLAIMER
3         *
4         *   This software is supplied by Renesas Electronics Corp. and is only
5         *   intended for use with Renesas products. No other uses are authorized.
6         *
7         *   This software is owned by Renesas Electronics Corp. and is protected under
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26        *   http://www.renesas.com/disclaimer
27        ***********************************************************************
28        * (C) 2007(2010) Renesas Electronics Corporation. All rights reserved.
29        *""FILE COMMENT""*********** Technical reference data *************************
30        *   System Name : SH7671 Sample Program
31        *   File Name   : bscsdram.c
32        *   Abstract    : SH7671 Initial Settings
33        *   Version     : 1.02.02
34        *   Device      : SH7671
35        *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.03.00).
36        *               : C/C++ compiler package for the SuperH RISC engine family
37        *               :                               (Ver.9.01 Release01).
38        *   OS          : None
39        *   H/W Platform: M3A-HS71(CPU board)
40        *   Description :
41        ***********************************************************************
42        *   History     : Jul.04,2007 ver.1.00.00
43        *             : Oct.29,2007 ver.1.00.01 Modification due to change of iodefine.h(v1.00.00)
44        *               : Jan.17,2008 ver.1.00.02 Wait change
45        *               : Feb.07,2008 ver.1.01.00 Changed to be after refresh start mode setting
46        *               : Mar.03,2008 ver.1.02.00 Setting procedure is unified
47        *               : Dec.18,2009 ver.1.02.01 Updated header comments
48        *               : Apr.07,2010 ver.1.02.02 Changed the company name and device name
49        *""FILE COMMENT END""*************************************************************/
```

3.2 Sample Program Listing: "bscsdram.c" (2)

```
50        #include "iodefine.h"
51        #include "defs.h"
52
53        /* ==== Macro name definition ==== */
54
55        /* The address when writing in a SDRAM mode register */
56        #define SDRAM_MODE      (*(volatile unsigned short *)(0xfffc5080))
57
58        /* ==== Prototype Declaration ==== */
59        void io_init_sdram(void);
60
61        #pragma section ResetPRG
62        /*""FUNC COMMENT""*****************************************************************
63         * ID            :
64         * Outline       : SDRAM 16 bit bus width connection settings
65         *-------------------------------------------------------------------------------
66         * Include       : "iodefine.h", "defs.h"
67         *-------------------------------------------------------------------------------
68         * Declaration   : void io_init_sdram(void);
69         *-------------------------------------------------------------------------------
70         * Description   : A connection setup to SDRAM of CS3 space.
71         *-------------------------------------------------------------------------------
72         * Argument      : void
73         *-------------------------------------------------------------------------------
74         * Return Value  : void
75         *-------------------------------------------------------------------------------
76         * Note          :
77         *""FUNC COMMENT END""*************************************************************/
78        void io_init_sdram(void)
79        {
80
81            volatile int j = LOOP_100us*2;          /* 200usec wait */
82
83            /* ==== 200us interval elapsed ? ==== */
84            while(j-- > 0){
85                /* wait */
86            }
87
88            /* ==== CS3BCR settings ==== */
89            BSC.CS3BCR.LONG = 0x00004600ul; /* Idle Cycles between Write-read Cycles
90                                               and Write-write Cycles :2idle cycles */
91                                            /* Memory type :SDRAM */
92                                            /* Data Bus Size :32-bit size */
93
```

3.3 Sample Program: Listing of "bscsdram.c" (3)

```
94
95            /* ==== CS3WCR settings ==== */
96            BSC.CS3WCR_SDRAM.LONG = 0x00002892ul;
97                                          /* Precharge completion wait cycles
98                                             :1cycles */
99                                          /* Wait cycles between ACTV command
100                                            and READ(A)/WRITE(A) command :2cycles */
101                                         /* CAS latency for Area 3 :2cycles */
102                                         /* Auto-precharge startup wait cycles
103                                            :2cycles */
104                                         /* Idle cycles from REF command/self-refresh
105                                            Release to ACTV/REF/MRS command
106                                            :5cycles */
107
108           /* ==== SDCR settings ==== */
109           BSC.SDCR.LONG = 0x00000811ul;   /*
110                                               Refresh Control :Refresh start
111                                               RMODE :Auto-refresh is performed
112                                               BACTV :Auto-precharge mode
113                                               Row address for Area3 :13-bits
114                                               Column Address for Area3 :9-bits
115                                         */
116
117           /* ==== RTCOR settings ==== */
118           BSC.RTCOR.LONG = 0xa55a0020ul;  /*
119                                               7.8usec /240nsec
120                                               >= 32(0x20)cycles per refresh
121                                         */
122
123           /* ==== RTCSR settings ==== */
124           BSC.RTCSR.LONG = 0xa55a0010ul;
125                                         /*
126                                               Initialization sequence start
127                                               Clock select B-phy/16 = 240nsec
128                                               Refresh count :Once
129                                         */
130           /* ==== Written in SDRAM Mode Register ==== */
131           SDRAM_MODE = 0;                 /*
132                                             SDRAM mode register setting(CS3 area)
133                                             dummy write
134                                             burst read / burst write (burst length 1)
135                                       */
136       }
137       /* End of File */
138
```

4. Documents for Reference

- Software manual
  SH-2A/SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-data version of this document is available on the Renesas Electronics Website.
- Hardware manual
  SH7670 Group Hardware Manual (REJ09B0437)
  The most up-to-data version of this document is available on the Renesas Electronics Website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Nov.19.08	—	First edition issued
1.01	May 07.10	—	AC Switching Characteristics are removed Format is changed

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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