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SH7262/SH7264 Group

Serial Communication Interface with FIFO, Configuration to Transmit Strings in Asynchronous Mode

Summary

This application note describes the configuration example to transmit strings using the SH7264 Serial Communication Interface with FIFO (SCIF) in asynchronous mode.

Target Device

SH7262/7264 MCU (In this document, SH7262/SH7264 are described as "SH7264".)

Contents

1. Introduction

1.1 Specifications

- Uses the Serial Communication Interface with FIFO (SCIF) channel 0
- Initializes the SH7264 MCU as the transmitter in asynchronous mode, and transmits character strings

1.2 Modules Used

- Serial Communication Interface with FIFO (SCIF)

1.3 Applicable Conditions

MCU	SH7262/SH7264
Operating Frequencies	Internal clock: 144 MHz Bus clock: 72 MHz Peripheral clock: 36 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Technology SuperH RISC engine Family C/C++ Compiler Package Ver.9.03 Release 00
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

For more information, refer to the following application notes:

- SH7262/SH7264 Example of Initialization
- SH7262/SH7264 Group Serial Communication Interface with FIFO, Configuration to Receive Strings in Asynchronous Mode
- SH7262/SH7264 Group Serial Communication Interface with FIFO, Configuring the Serial Communication in Clock Synchronous Mode (Full-duplex)

1.5 About Active-low Pins (Signals)

The symbol "#" suffixed to the pin (or signal) names indicates that the pins (or signals) are active-low.

2. Applications

This application note uses the Serial Communication Interface with FIFO (SCIF).

2.1 SCIF Overview

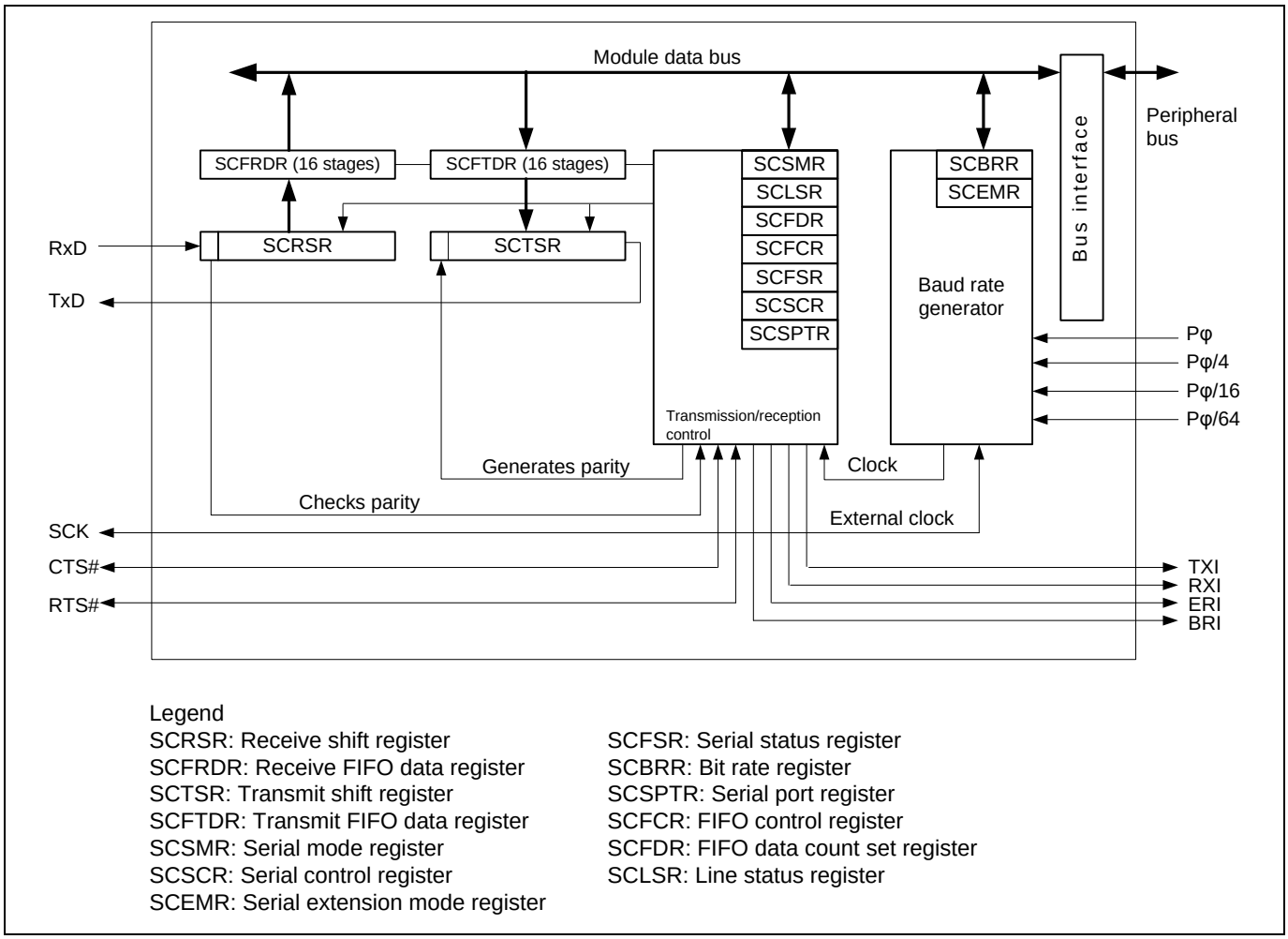
The SH7264 SCIF transmits or receives a "character", appending a start bit which indicates the initiation of the communication, and a stop bit which indicates the end of the communication to data. Then, the SH7264 SCIF handles communication in sync per character. The internal clock or external clock from the SCK pin can be specified as the clock source. Transfer data format and baud rate can be set in the SCIF.

Table 1 lists the overview of the asynchronous mode. Figure 1 shows the SCIF block diagram.

Table 1 SCIF (Asynchronous mode) Overview

Item	Description
Number of channels	8 (SCIF0 to SCIF7)
Clock source	Internal clock: Pφ, Pφ/4, Pφ/16, Pφ/64 Pφ: internal peripheral clock External clock: SCK0 to SCK3 pin input clock (The pin input divided by 16 or 8 is selected as the SCIF operating clock.)
Data format	Transfer data length: 7-bit or 8-bit Order of transfer: LSB first fixed Start bit: 1-bit fixed Stop bit: 1-bit or 2-bit Parity bit: even parity, odd parity, or no parity
Baud rate	When specifying the internal clock: 68.66 bps to 4500 kbps (Pφ is at 36 MHz) When specifying the external clock: up to 1125 kbps (Pφ is at 36 MHz, external clock is at 9 MHz)
Error detection	Parity error, framing error, overrun error
Interrupt request	Transmit-FIFO-data-empty interrupt (TXI) by the transmit FIFO data empty (TDFE) Break interrupt (BRI) by the break (BRK) or overrun error (ORER) Receive FIFO data full (RXI) by the Receive FIFO data full (RDF) or data ready (DR) Receive-error interrupt (ERI) by the receive error (ER)
Other	• Break can be detected • Supplying clock unused channels can be stopped to reduce power consumption • Includes the modem control functions (RTS and CTS), (Only channels 1 and 3. Only channel 1 for the SH7262) • The number of valid data stored in the Transmit and Receive FIFO data registers, and the number of receive errors stored in the Receive FIFO data register can be detected • Time out error (DR) on reception can be detected • Base clock frequency can be either 16 or 8 times the bit rate • Double-speed mode can be specified for the baud rate generator (When not using the SCK pin)

Note: For more information about the SCIF, refer to the Serial Communication Interface with FIFO chapter in the SH7262 Group, SH7264 Group Hardware Manual.



Legend

SCRSR: Receive shift register
SCFRDR: Receive FIFO data register
SCTSR: Transmit shift register
SCFTDR: Transmit FIFO data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCEMR: Serial extension mode register
SCFSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCFCR: FIFO control register
SCFDR: FIFO data count set register
SCLSR: Line status register

Figure 1 SCIF Block Diagram

2.2 Configuration Procedure

This section describes how to configure the communication in the SH7264 SCIF asynchronous mode. Figure 2 and Figure 3 show flow charts of configuring the transmission in asynchronous mode. Figure 4 shows the flow chart of transmission in asynchronous mode.

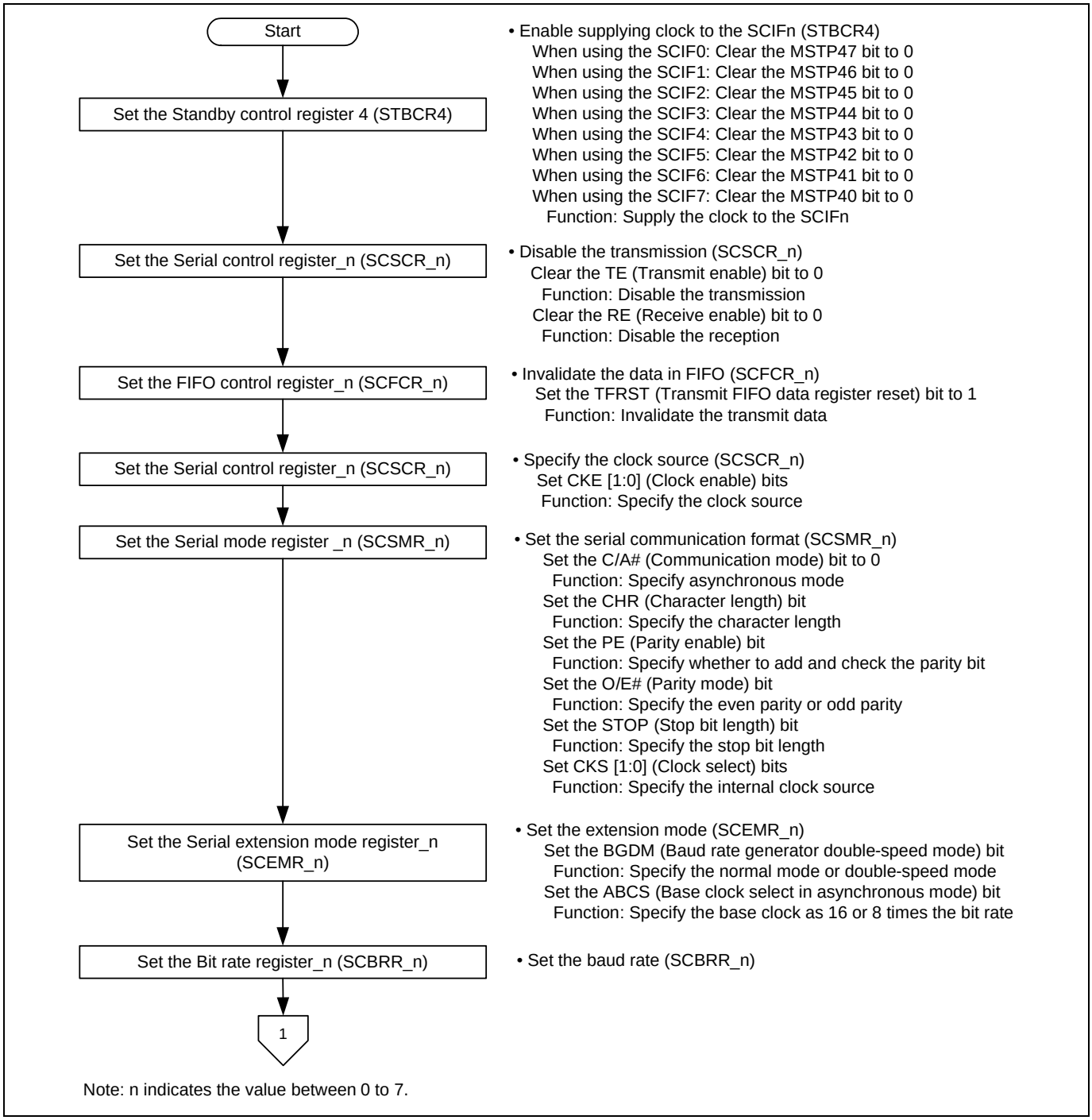
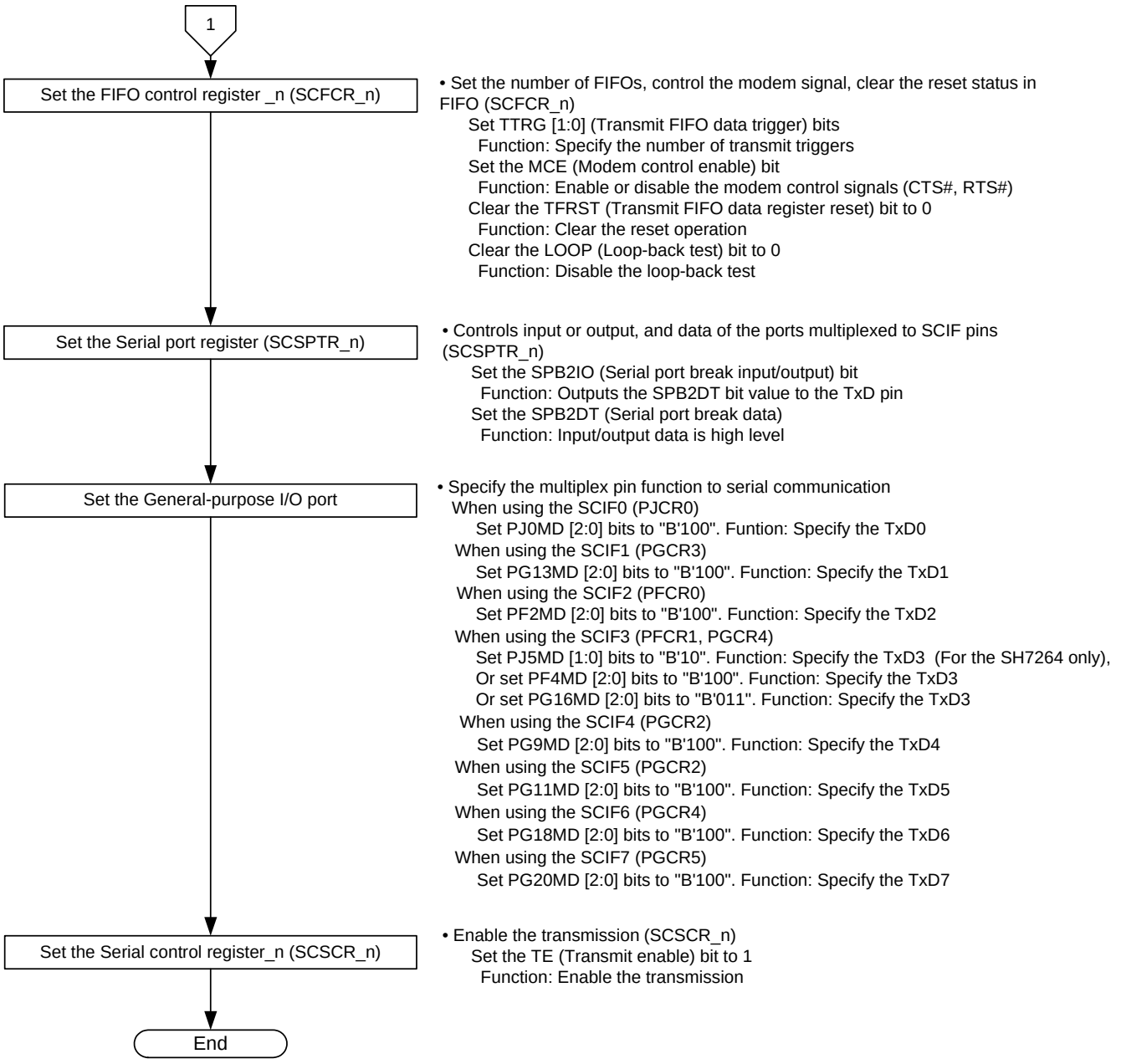


Figure 2 Flow Chart for Configuring the Transmission in Asynchronous Mode (1/2)



Note: n indicates the value between 0 to 7.

Figure 3 Flow Chart for Configuring the Transmission in Asynchronous Mode (2/2)

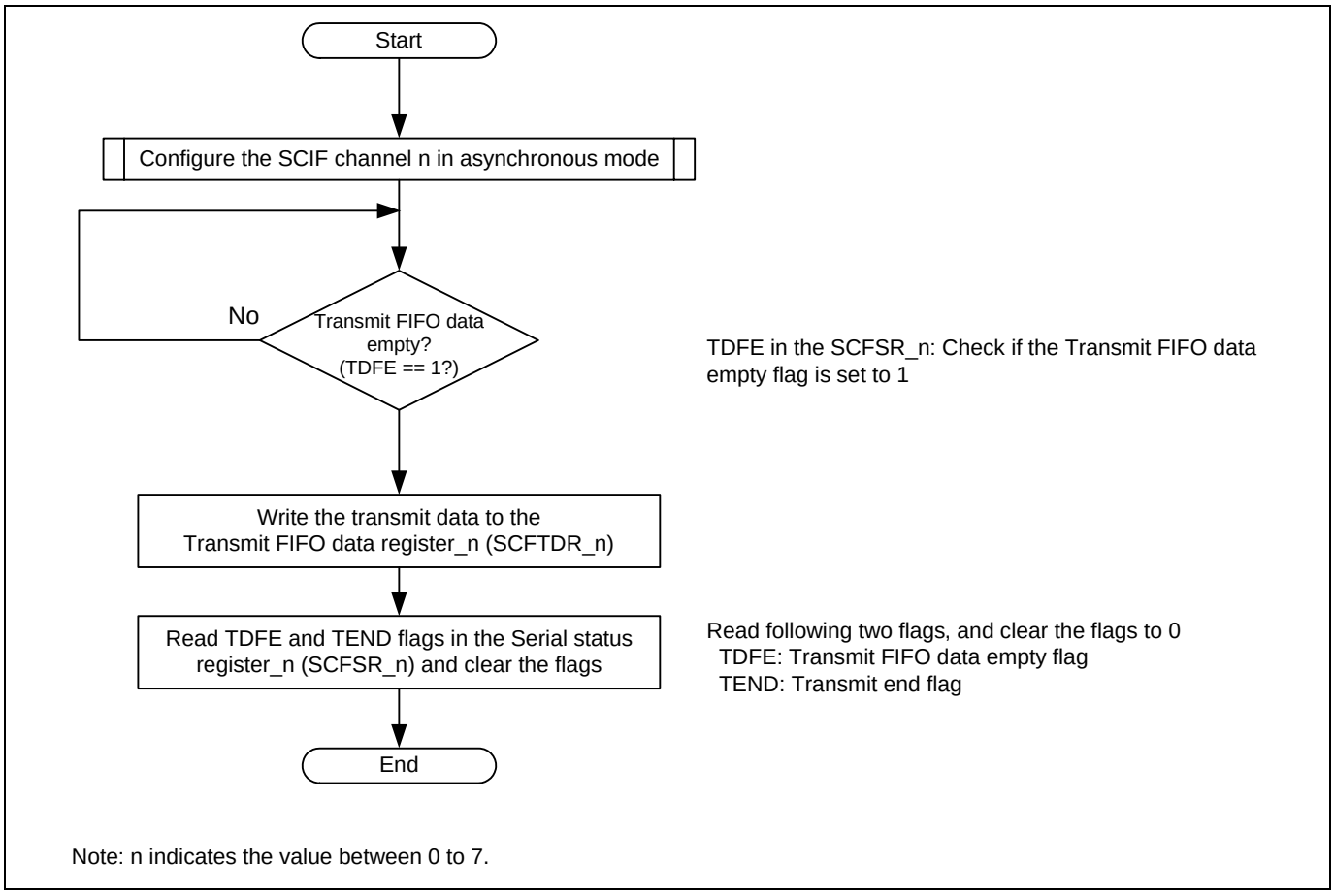


Figure 4 Flow Chart of the Transmission in Asynchronous Mode

2.3 Sample Program Operation

This sample program uses the SCIF channel 0 in asynchronous mode, and transmits character strings. It checks the Transmit FIFO data empty flag, and writes 1-byte data when the flag indicates "empty". After writing data, it clears both the Transmit end flag and the Transmit FIFO data empty flag.

Table 2 lists the transmission settings for the sample program. Figure 5 shows the operation timing of the sample program.

Table 2 Sample Program Transmission Settings

Communication Format	Setting
Communication mode	Asynchronous mode
Number of channel to use	Channel 0
Interrupt	Not used
Baud rate	19,200 bps
Data length	8-bit
Parity	No parity
Stop bit	1 stop bit
Modem control	RTS/CTS functions are disabled
Bit order	LSB first
Number of FIFO data triggers	0

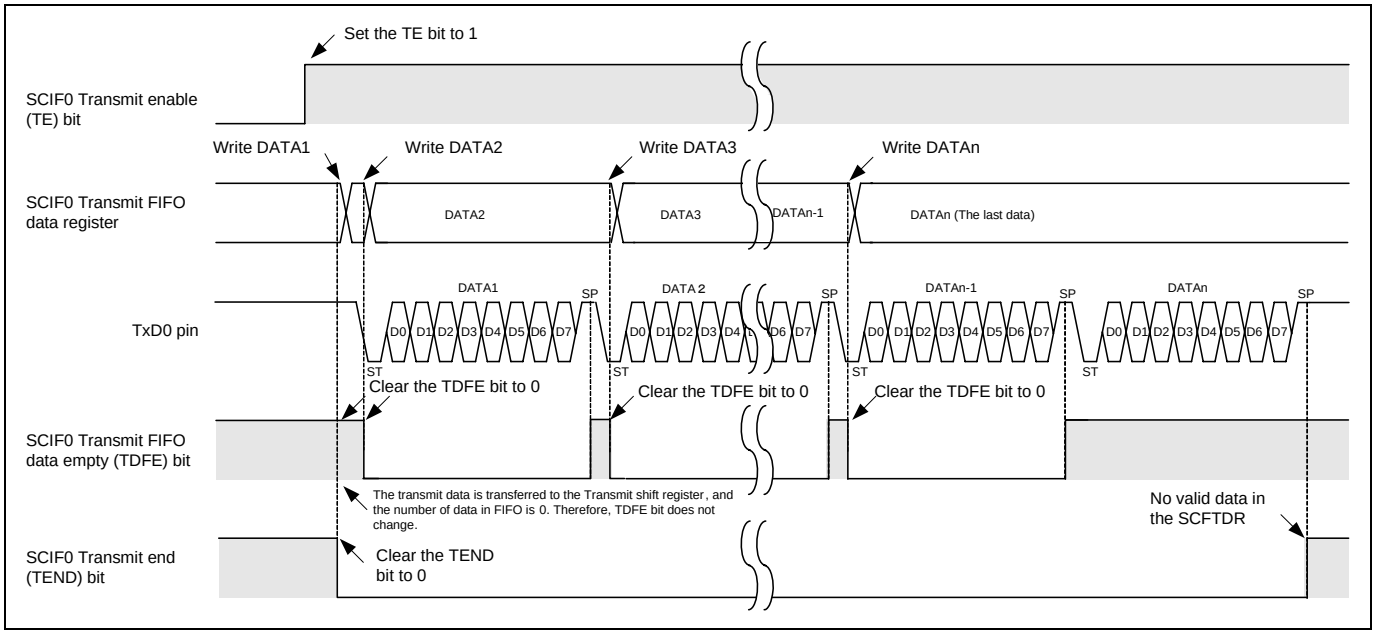


Figure 5 Sample Program Operation Timing

2.4 Sample Program Procedure

The sample program initializes the SCIF channel 0 in asynchronous mode, and transmits 1-byte character string data.

Table 3 lists register settings related to the SCIF channel 0 in the sample program. Figure 6 shows the flow chart of the sample program.

Table 3 Sample Program Register Settings

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE 040C	H'7F	• MSTP47 = "0": SCIF0 is operating (Supplies the clock)
Port J control register 0 (PJCR0)	H'FFFE 390E	H'0004	• PJ0MD [2:0] = "B'100": TxD0 output (SCIF0)
Serial mode register_0 (SCSMR_0)	H'FFFE 8000	H'0000	• C/A# = "0": Asynchronous mode • CHR = "0": 8-bit data • PE = "0": Disable to add the parity bit • STOP = "0": 1 stop bit • CKS [1:0] = "0": Peripheral clock
Serial control register (SCSCR_0)	H'FFFE 8008	H'0000	• TE = "0": Disable the transmission • RE = "0": Disable the reception • CKE [1:0] = "B'00": Internal clock/SCK pin is an input pin
		H'0020	• TE = "1": Enable the transmission
FIFO control register_0 (SCFCR_0)	H'FFFE 8018	H'0004	• TFRST = "1": Enable to reset the Transmit FIFO data register
		H'0030	• TFRST = "0": Disable to reset the Transmit FIFO data register • TTRG [1:0] = "B'11": Set the TDFE flag when the number of data in the Transmit FIFO is equal to or less than 0
Serial extension mode register_0 (SCEMR_0)	H'FFFF 8028	H'0000	• BGDM = "0": Normal mode • ABCS = "0": Base clock is 16 times the bit rate
Bit rate register_0 (SCBRR_0)	H'FFFE 8004	H'3A	Specifies the bit rate as 19,200 bps (Error: −0.69% when Pφ is at 36 MHz)
Serial port register_0 (SCSPTR_0)	H'FFFE 8020	H'0053	• SPB2IO = "1": Output the SPB2DT bit value to the TxD pin • SPB2DT = "1": Input/output data is high level

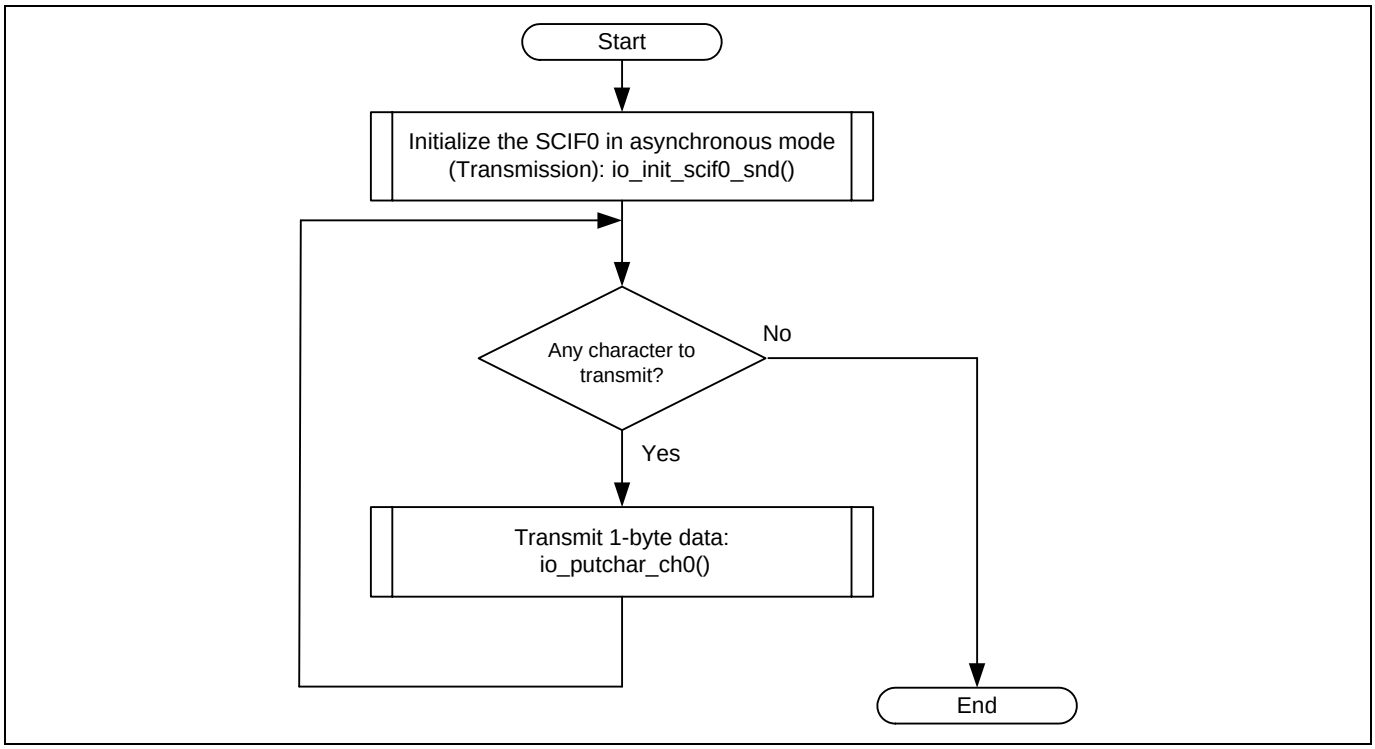


Figure 6 Sample Program Flow Chart

3. Sample Program Listing

3.1 Supplement to the Sample Program

As the capacity of the SH7264 large-capacity internal RAM varies as 1 MB or 640 KB, depending on the MCU type, the section alignment and register setting must be partly altered. To support both MCU types, this application note provides two types of sample programs (workspaces) for 1-MB RAM and 640-KB RAM.

As the MCU with 640-KB RAM must be write-enabled before writing data in the data-retention RAM, the System control register 5 (SYSCR5) is set to write-enable the RAM in the sample program for 640-KB RAM.

Review your product and use the appropriate workspace.

3.2 Sample Program Listing "main.c" (1/6)

```
1       /***********************************************************************
2       *   DISCLAIMER
3       *
4       *   This software is supplied by Renesas Technology Corp. and is only
5       *   intended for use with Renesas products. No other uses are authorized.
6       *
7       *   This software is owned by Renesas Technology Corp. and is protected under
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25      *   conditions found by accessing the following link:
26      *   http://www.renesas.com/disclaimer
27      ***********************************************************************
28      *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29      *""FILE COMMENT""*********** Technical reference data *************************
30      *   System Name : SH7264 Sample Program
31      *   File Name   : main.c
32      *   Abstract    : Serial communication interface with FIFO (SCIF).
33      *               : Transmission in asynchronous mode sample program
34      *   Version     : 1.00.00
35      *   Device      : SH7262/SH7264
36      *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
37      *               : C/C++ compiler package for the SuperH RISC engine family
38      *               :                              (Ver.9.03 Release00).
39      *   OS          : None
40      *   H/W Platform: M3A-HS64G50 (CPU board)
41      *   Description :
42      ***********************************************************************
43      *   History     : Dec.03,2009 ver.1.00.00
44      *""FILE COMMENT END""*****************************************************/
45      #include "iodefine.h"       /* SH7264 iodefine  */
46
```

3.3 Sample Program Listing "main.c" (2/6)

```
47    /* ==== Prototype declaration ==== */
48    void main(void);
49    void io_init_scif0_snd(int);
50    void io_putchar_ch0(unsigned char) ;
51
52    /* ==== Type definition ==== */
53    /* SCIF baud rate setting */
54    typedef struct  {
55      unsigned char scbrr;     /* SCBRR register setting */
56      unsigned short scsmr;       /* SCSMR register setting */
57    } SH7264_BAUD_SET;
58
59    /* ---- Baud rate specified value ---- */
60    enum{
61      CBR_1200,
62      CBR_2400,
63      CBR_4800,
64      CBR_9600,
65      CBR_19200,
66      CBR_31250,
67      CBR_38400,
68      CBR_57600,
69      CBR_115200
70    };
71
72    /* ==== Register setting table (P clock = 36 MHz) ==== */
73    static SH7264_BAUD_SET scif_baud[] = {
74      {233, 1},    /*  1200 bps (error: 0.16%) */
75      {116, 1},    /*  2400 bps (error: 0.16%) */
76      {233, 0},    /*  4800 bps (error: 0.16%) */
77      {116, 0},    /*  9600 bps (error: 0.16%) */
78      { 58, 0},    /* 19200 bps (error: -0.69%) */
79      { 35, 0},    /* 31250 bps (error: 0.00%) */
80      { 28, 0},    /* 38400 bps (error: 1.02%) */
81      { 19, 0},    /* 57600 bps (error: -2.34%) */
82      {  9, 0}     /*115200 bps (error: -2.34%) */
83    };
84
85
```

3.4 Sample Program Listing "main.c" (3/6)

```
86    /*""FUNC COMMENT""*****************************************************************
87     * ID            :
88     * Outline       : Sample program main (Asynchronous serial I/O transmission).
89     *-------------------------------------------------------------------------------
90     * Include       : "iodefine.h"
91     *-------------------------------------------------------------------------------
92     * Declaration   : void main(void);
93     *-------------------------------------------------------------------------------
94     * Description   : Initializes the SCIF0 in predefined communication format and
95     *               : operating mode, and transmits character one by one.
96     *-------------------------------------------------------------------------------
97     * Argument      : void
98     *-------------------------------------------------------------------------------
99     * Return Value  : void
100    *-------------------------------------------------------------------------------
101    * Note          :
102    *""FUNC COMMENT END""*************************************************************/
103   void main(void)
104   {
105     const unsigned char data[] = "SCIF sample\r\nHello\r\n";  /* Character string to
106   transmit */
107     const unsigned char *ptr;
108
109     /* ==== Initializes the SCIF0 in asynchronous mode (transmission) ==== */
110     io_init_scif0_snd(CBR_19200);       /* Specifies the bit rate as 19200 bps */
111
112     ptr = data;
113     /* ==== Any character to transmit? ==== */
114     while(*ptr != 0) {
115       /* ==== Transmits 1-byte data ==== */
116       io_putchar_ch0 (*ptr++);
117     }
118
119     while (1) {
120       /* Program end */
121     }
122   }
```

3.5 Sample Program Listing "main.c" (4/6)

```
123   /*""FUNC COMMENT""*****************************************************************
124    * ID            :
125    * Outline       : Configure the SCIF0 as the transmitter in asynchronous mode
126    *-------------------------------------------------------------------------------
127    * Include       : "iodefine.h"
128    *-------------------------------------------------------------------------------
129    * Declaration   : void io_init_scif0_snd(int bps);
130    *-------------------------------------------------------------------------------
131    * Description   : Configures the SCIF0 as the transmitter in asynchronous mode.
132    *               : Sets it in asynchronous mode, 8-bit, no parity,
133    *               : 1 stop bit, and RTS/CTS disabled.
134    *               : Specify the baud rate by the argument "bps".
135    *-------------------------------------------------------------------------------
136    * Argument      : int bps ; I : Baud rate specified value (Table index)
137    *-------------------------------------------------------------------------------
138    * Return Value  : void
139    *-------------------------------------------------------------------------------
140    * Note          : The above baud rate specified value is applicable when using
141    *               : the peripheral clock (operating frequency for the peripheral
142    *               : module using the internal clock) is 36 MHz. Alter the baud rate
143    *               : setting when using other clocks.
144    *""FUNC COMMENT END""*************************************************************/
145   void io_init_scif0_snd(int bps)
146   {
147     /* ==== Wakes up the MCU from power-down mode ==== */
148     /* ---- Sets the Standby control register 4 (STBCR4) ---- */
149     CPG.STBCR4.BIT.MSTP47 = 0;      /* Starts to supplying clock to the SCIF0 */
150
151     /* ==== Configures the SCIF0 ==== */
152     /* ---- Sets the Serial control register (SCSCRi) ---- */
153     SCIF0.SCSCR.WORD = 0x0000;      /* SCIF0 stops transmission/reception */
154
155     /* ---- Sets the FIFO control register (SCFCRi) ---- */
156     SCIF0.SCFCR.BIT.TFRST = 1;      /* Resets the transmit FIFO */
157
158     /* ---- Sets the Serial control register (SCSCRi) ---- */
159     SCIF0.SCSCR.BIT.CKE = 0x0;      /* B'00: internal clock */
160
161     /* ---- Sets the Serial mode register (SCSMRi) ---- */
162     SCIF0.SCSMR.WORD = scif_baud[bps].scsmr;
163                                /*  Communication mode, 0: Asynchronous mode  */
164                                /*  Character length, 0: 8-bit data   */
165                                /*  Parity enable, 0: Disables to add and check parity */
166                                /*  Parity mode, 0: Even parity */
167                                /*  Stop bit length, 0: 1 stop bit */
168                                /*  Clock select: Setting in table */
169
```

3.6 Sample Program Listing "main.c" (5/6)

```
170     /* ---- Sets the Serial extension mode register (SCEMRi) ---- */
171     SCIF0.SCEMR.WORD = 0x0000;      /* Baud rate generator double-speed mode, 0: Normal mode */
172                                 /* Base clock select in asynchronous mode, */
173                                 /*   0: Base clock is 16 times the bit rate */
174
175     /* ---- Sets the Bit rate register (SCBRRi) ---- */
176     SCIF0.SCBRR.BYTE = scif_baud[bps].scbrr;
177
178     /* ---- Sets the FIFO control register (SCFCRi) ---- */
179     SCIF0.SCFCR.WORD = 0x0030;      /* Number of the transmit FIFO data trigger: Zero */
180                                 /* Modem control enable: Disabled */
181                                 /* Transmit FIFO data register reset: Disabled */
182                                 /* Loop-back test: Disabled */
183
184     /* ---- Sets the Serial port register (SCSPTRi) ---- */
185     SCIF0.SCSPTR.WORD = 0x0053;     /* Serial port break input/output, 1: Outputs the SPB2DT
186                                                                 value to the TxD pin */
187                                 /* Serial port break data, 1: Input/output data is high level */
188
189     /* ==== Sets the General-purpose I/O port ==== */
190     PORT.PJCR0.BIT.PJ0MD = 4;       /* Specifies the TxD0 pin */
191
192     /* ---- Sets the Serial control register (SCSCRi) ---- */
193     SCIF0.SCSCR.BIT.TE = 1;         /* Enables the SCIF0 to transmit data */
194   }
195
```

3.7 Sample Program Listing "main.c" (6/6)

```
196   /*""FUNC COMMENT""*****************************************************************
197    * ID            :
198    * Outline       : SCIF0 1 character transmission
199    *-------------------------------------------------------------------------------
200    * Include       : "iodefine.h"
201    *-------------------------------------------------------------------------------
202    * Declaration   : void io_putchar_ch0(unsigned char c);
203    *-------------------------------------------------------------------------------
204    * Description   : Checks if the Transmit FIFO data empty flag in the SCIF0 serial
205    *               : status register (SCFSR0) is set as transmit-enabled (empty),
206    *               : and transmits 1-byte data in the argument.
207    *-------------------------------------------------------------------------------
208    * Argument      : unsigned char c : Transmit data
209    *-------------------------------------------------------------------------------
210    * Return Value  : void
211    *-------------------------------------------------------------------------------
212    * Note          :
213    *""FUNC COMMENT END""*************************************************************/
214   void io_putchar_ch0 (unsigned char c)
215   {
216     /* ==== Checks the Transmit FIFO data empty flag (TDFE flag) in the Serial
217         status register (SCFSR0) ==== */
218     while(SCIF0.SCFSR.BIT.TDFE == 0){
219       /* Waits until the TDFE flag is set */
220     }
221
222     /* ==== Writes the transmit data in the Transmit FIFO data register (SCFTDR0) ==== */
223     SCIF0.SCFTDR.BYTE = c;
224
225     /* ==== Reads bits TDFE and TEND in the Serial status register (SCFSR0)
226                                       before clearing these bits ==== */
227     SCIF0.SCFSR.WORD &= ~0x0060u ;
228   }
229   /* End of File */
```

4. References

- Software Manual
  SH-2A/SH2A-FPU Software Manual Rev. 3.00
  The latest version of the software manual can be downloaded from the Renesas website.

- Hardware Manual
  SH7262 Group, SH7264 Group Hardware Manual Rev. 2.00
  The latest version of the hardware manual can be downloaded from the Renesas website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
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