

# SH7239 Group

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## Reading/Writing EEPROM

### Using the Renesas Serial Peripheral Interface

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#### Summary

This application note describes examples of reading/writing EEPROM using the SH7239 Microcomputers (MCUs) Renesas Serial Peripheral Interface (RSPI).

#### Target Device

SH7239 MCU

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## 1. Introduction

### 1.1 Specifications

- Use an EEPROM of 64 KB (512 Kbit) to connect with the SH7239 MCU

### 1.2 Modules Used

- Renesas Serial Peripheral Interface (RSPI)
- General-purpose I/O ports

### 1.3 Applicable Conditions

MCU	SH7239 (R5F72395ADFP)
Power Supply Voltage	3.3 V
Operating Frequency	Internal clock: 160 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
Integrated Development Environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.07.00
C Compiler	Renesas Electronics SuperH RISC engine Family C/C++ compiler package Ver.9.03 Release 02
Compiler Options	Default setting in the High-performance Embedded Workshop (-cpu=sh2afpu -fpu=single -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

## 2. Applications

Connect the SH7239 MCU (Master) with the SPI-compatible EEPROM (Slave) for read/write access using the Renesas Serial Peripheral Interface (RSPI). This chapter describes the pin connection example and flow charts of the sample program.

### 2.1 RSPI Operation

SH7239 RSPI allows full-duplex, synchronous, serial communications with peripheral devices in SPI operation using MOSI (Master Out Slave In), MISO (Master In Slave Out), SSL (Slave Select), and RSPCK (SPI Clock) pins.

The RSPI has the following features to support SPI-compliant devices:

- Master/slave modes
- Serial transfer clock with programmable polarity and phase (change SPI modes)
- Transfer bit length selectable (8- to 16-bit, 20-, 24-, and 32-bit)

### 2.2 EEPROM Pin Connection

The following table lists the specifications of the SPI-compliant EEPROM (R1EX25512ATA00A, Renesas Electronics) used in this application.

**Table 1 EEPROM Specifications**

Item	Description
Power Supply Voltage	Single supply 1.8 V to 5.5 V
SPI Modes	Supports SPI modes 0 and 3
Clock Frequency	5 MHz (2.5 to 5.5 V), 3 MHz (1.8 to 5.5 V)
Capacity	64 KB (512 Kbit)
Page Write	128 bytes/page
Write Cycle Time	5 ms (max.)
Endurance	1,000,000 Erase/Write cycles

The figure below shows an example of EEPROM. Set the SH7239 pin functions as shown in Table 2.

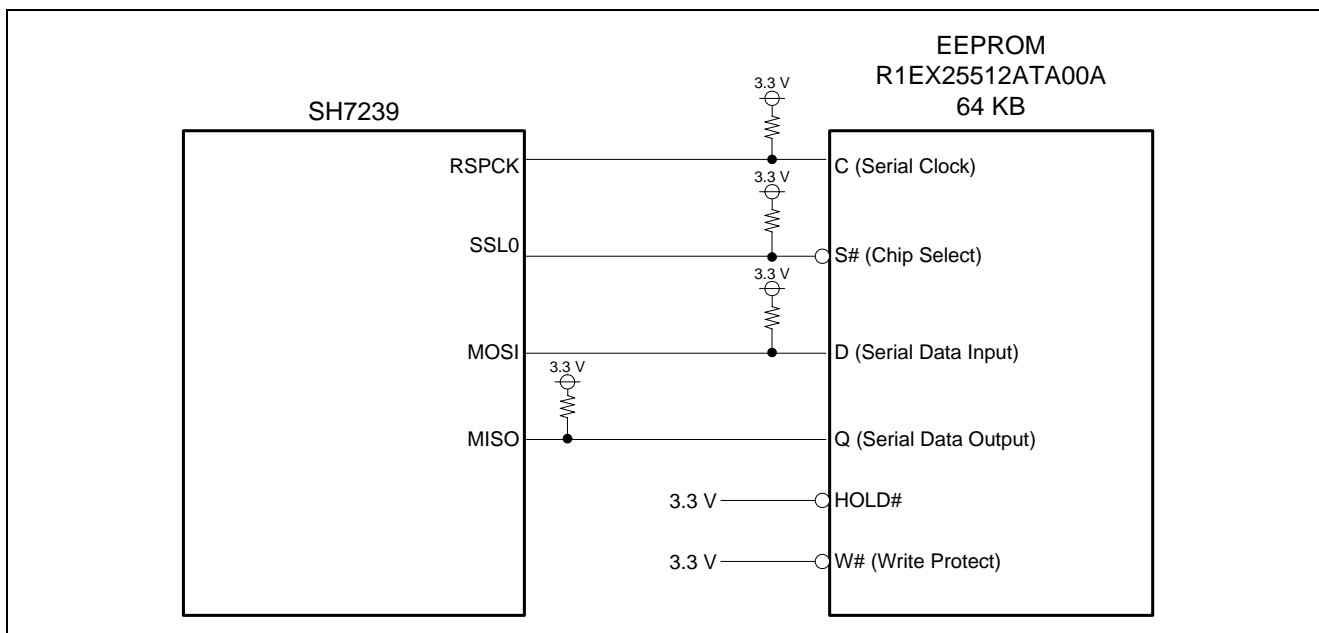


Figure 1 EEPROM Circuit

Note: Pull up or pull down the control signal pins using the external resistors

To pull up or pull down the control signal pins, determine the signal line level not to cause the external device malfunction when the MCU pin status is high-impedance. SSL0 pin is pulled up by an external resistor to high level. Pull up or down the RSPCK and MOSI pins. As the MISO pin is configured as input, pull-up or pull-down is recommended to avoid floating to the midpoint voltage.

Table 2 Multiplexed Output

Peripheral Functions	Pin Name	SH7239 Port Control Register		SH7239 Multiplexed Pin Name
		Register Name	MD bit Setting	
RSPI	RSPCK	PACRL2	PA6MD[2:0] = B'101	PA6/IRQ6/TCLKA/CS6#/RSPCK/SCK1
	MOSI	PACRL2	PA7MD[2:0] = B'101	PA7/IRQ5/TCLKB/CS5#/MOSI/TXD1
	MISO	PACRL3	PA8MD[2:0] = B'101	PA8/IRQ4/TCLKC/CS4#/MISO/RXD1
	SSL0	PACRL3	PA9MD[2:0] = B'101	PA9/IRQ3/TCLKD/CS3#/SSL0/SCK0

Note: SH7239 Multiplexed pins

RSPCK, MOSI, MISO, and SSL0 pins are multiplexed, and set to general-purpose I/O ports by default. Before accessing EEPROM, use the general-purpose I/O port control register to set the multiplexed pins to RSPI pins.

### 2.3 Interface Timing Example

This section describes an example of the interface timing between the SH7239 and EEPROM. Initialize the RSPI and the clock frequency according to the EEPROM, which is used as a slave device.

Figure 2 shows an example of the data transfer timing. As the EEPROM used in this application latches data at the rising edge of the clock, and outputs data at the falling edge of the clock, specify 1 to the CPOL and CPHA bits in the RSPI command register (SPCMD). By this setting, RSPCK is specified to 1 when it is idling, and the timing to vary the data in the RSPI can be set to the odd edge (falling edge). Initialize the RSPI to satisfy the timing conditions listed in Table 3 and Table 4.

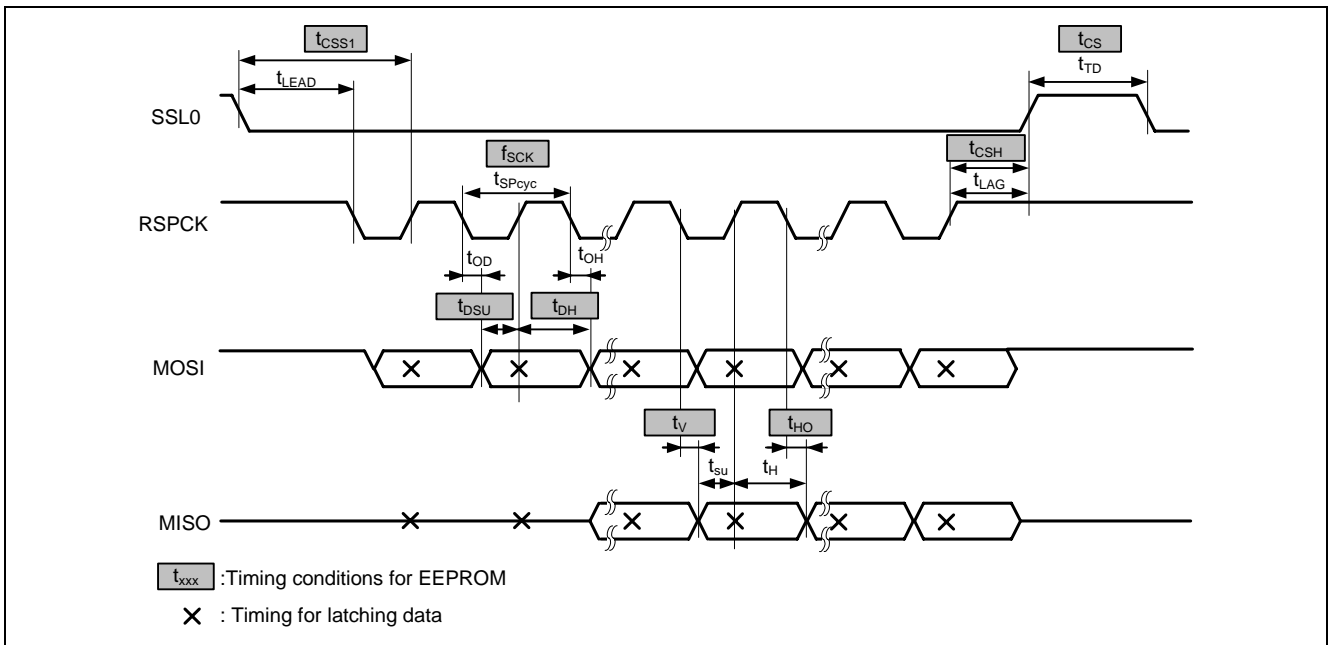


Figure 2 Data Transfer Timing Example (CPOL = 1, CPHA = 1)

Table 3 Timing Conditions for EEPROM when Transferring Data

Symbol	Item	Description	Related registers
$t_{CSS1}$	Chip Select Low Setup Time	Time required for the slave device to latch data from asserting SSL to the RSPCK rising. The following formula must be fulfilled: $t_{LEAD} (= RSPCK \text{ delay}) + 1/2 \times t_{SPCyc} \geq t_{CSS1} \text{ (min.)}$	SPCKD register SPCMD register SPBR register
$t_{CS}$	Chip Select High Time	Time required for SSL negation. The following formula must be fulfilled: $t_{TD} (= \text{next-access delay}) \geq t_{CS} \text{ (min.)}$	SPND register SPCMD register
$f_{SCK}$	Serial Clock Frequency	The maximum operating frequency supported by the slave device. The following formula must be fulfilled: $f_{SCK} \text{ (max.)} \geq 1/t_{SPCyc}$	SPBR register SPCMD register
$t_{CSH}$	Chip select Low Hold Time	Hold time required from the last RSPCK rising to the SSL negation. The following formula must be fulfilled: $t_{LAG} (= \text{SSL negation delay}) \geq t_{CSH} \text{ (min.)}$	SSLND register SPCMD register
$t_{DSU}$	Data Input Setup Time	Time required for the master device from outputting data to latching data. The following formula must be fulfilled: $1/2 \times t_{SPCyc} - t_{OD} \text{ (max.)} \geq t_{DSU} \text{ (min.)}$	SPBR register SPCMD register
$t_{DH}$	Data Input Hold Time	Time required for the master device to remain the data output. The following formula must be fulfilled: $t_{OH} \text{ (min.)} + 1/2 \times t_{SPCyc} \geq t_{DH} \text{ (min.)}$	SPBR register SPCMD register

Table 4 Timing Conditions for the SH7239 MCU when Transferring Data

Symbol	Item	Description	Related registers
$t_{SU}$	Data Input Setup Time	Time required for the slave device from outputting data to latching data. The following formula must be fulfilled: $1/2 \times t_{SPCyc} - t_W \text{ (max.)} \geq t_{SU} \text{ (min.)}$	SPBR register SPCMD register
$t_H$	Data Input Hold Time	Time required for the slave device from latching data to stop the data output. The following formula must be fulfilled: $t_{HO} \text{ (min.)} + 1/2 \times t_{SPCyc} \geq t_H \text{ (min.)}$	SPBR register SPCMD register

## 2.4 Sample Program Operation

### 2.4.1 RSPI Initialization Example

Figure 3 and Figure 4 show flow charts of initializing the RSPI in the sample program. This setting enables the SPI operation in master mode.

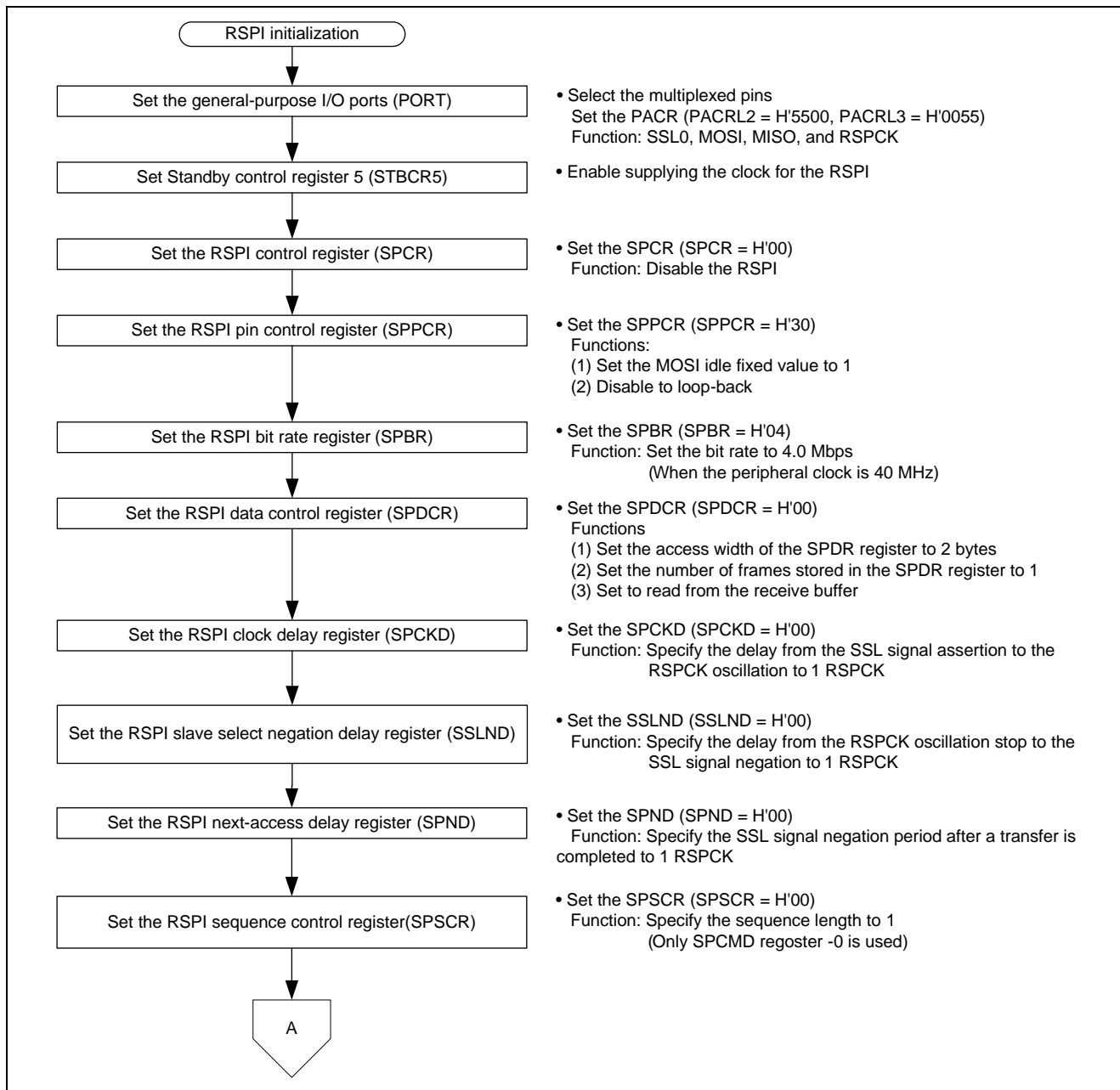


Figure 3 Flow Chart for Initializing the RSPI (1/2)

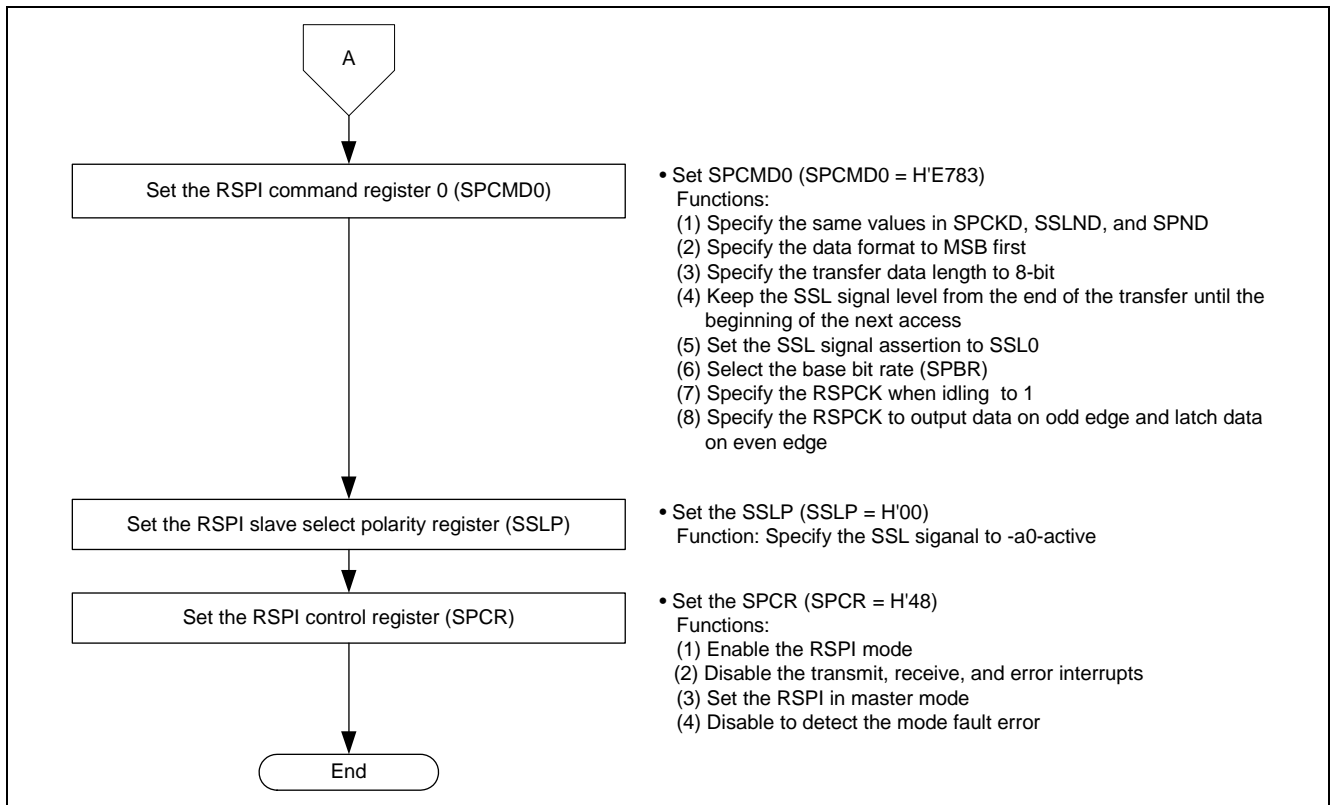


Figure 4 Flow Chart for Initializing the RSPI (2/2)



### 2.4.2 Command Transfer Example

Use commands to access EEPROM. This section describes the major commands and command sequence example, and shows flow charts in the sample program.

This application refers to the commands of the Renesas Electronics R1EX25512ATA00A. For details on commands, refer to the datasheet provided by the EEPROM manufacturer.

#### A. Major Commands

The following table lists the major commands for the R1EX25512ATA00A.

**Table 5 R1EX25512ATA00A Commands**

Command Name	Opcode	Address Bytes	Data Bytes	Description
WREN	H'06	0	0	Write Enable
WRDI	H'04	0	0	Write Disable
RDSR	H'05	0	1	Reads the status
WRSR	H'01	0	1	Writes the status
READ	H'03	2	1 or more <sup>(1)</sup>	Reads data from the memory
WRITE	H'02	2	1 to 128 <sup>(2)</sup>	Writes data to the memory

Notes 1. Reads the address incremented from the specified address (When the last byte of the memory array has been read, the device will continue reading back at the beginning of the array).

2. Writes the data in the incremented in the same page (When the device goes beyond the end of the page, it will wrap around back to the beginning of the same page).

B. Command Sequence Example

Figure 5 shows the sequence example of the READ command.

When issuing the READ command, the master device transfers the opcode (H'03) and three address bytes after the SSL signal is asserted. Then, the slave device transfers the read data in every falling edge of the RSPCK.

Although commands can be sequentially issued by repeating to transfer the data in the specified access width, pay special attention to the SSL signal level. Do not negate the SSL signal between the assertion of the SSL signal at the beginning of the command and the transfer end of the last byte of the command. The sample program sets the SSLKP bit in the SPCMD register to 1 to keep the SSL signal. SSL signal is negated by clearing the SPE bit in the SPCR register to 0 after all data transfer is completed.

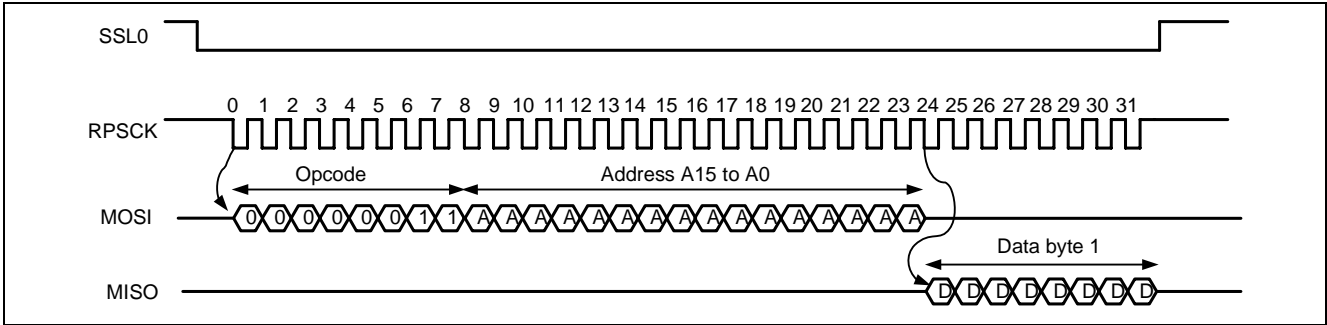


Figure 5 Read Command Sequence (Opcode: H'03)

C. Command Transfer Example in the Sample Program

The Read command that uses both master output and slave output, and the Write command that uses the master output are supported by the sample program. Figure 6 shows the flow chart of the read/write commands transfer. Figure 7 shows the flow chart of the data transfer.

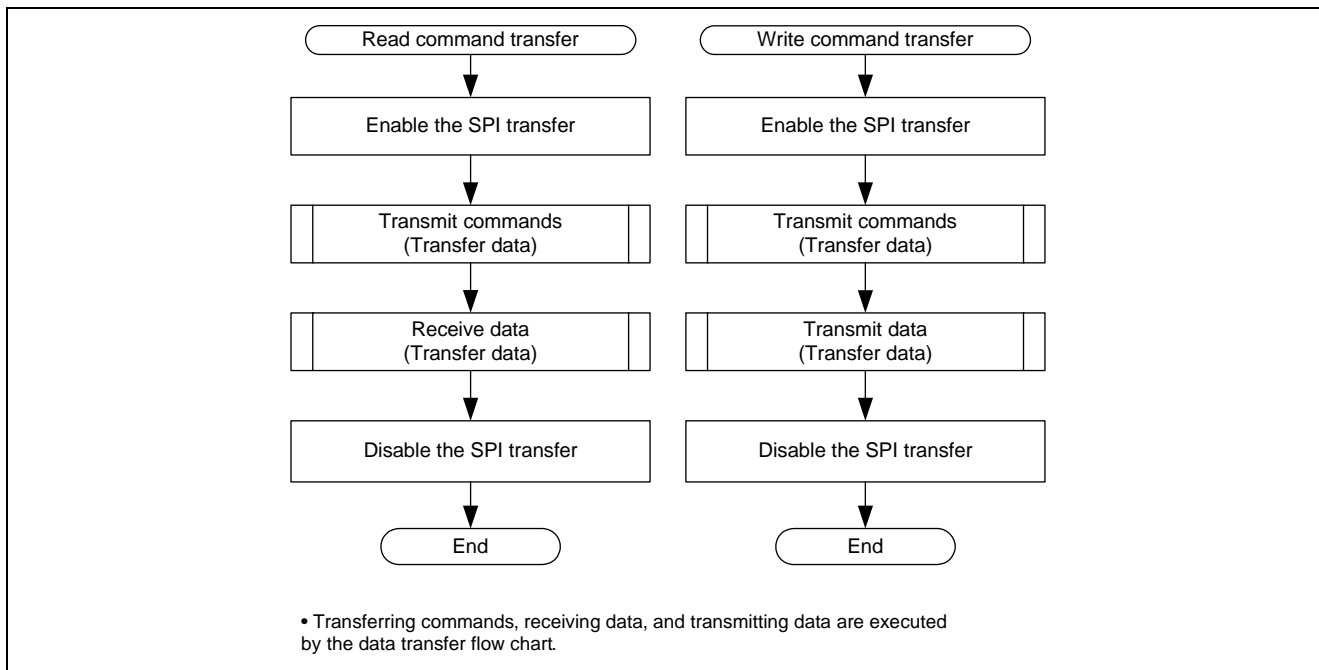


Figure 6 Flow Chart of Read/Write Commands Transfer

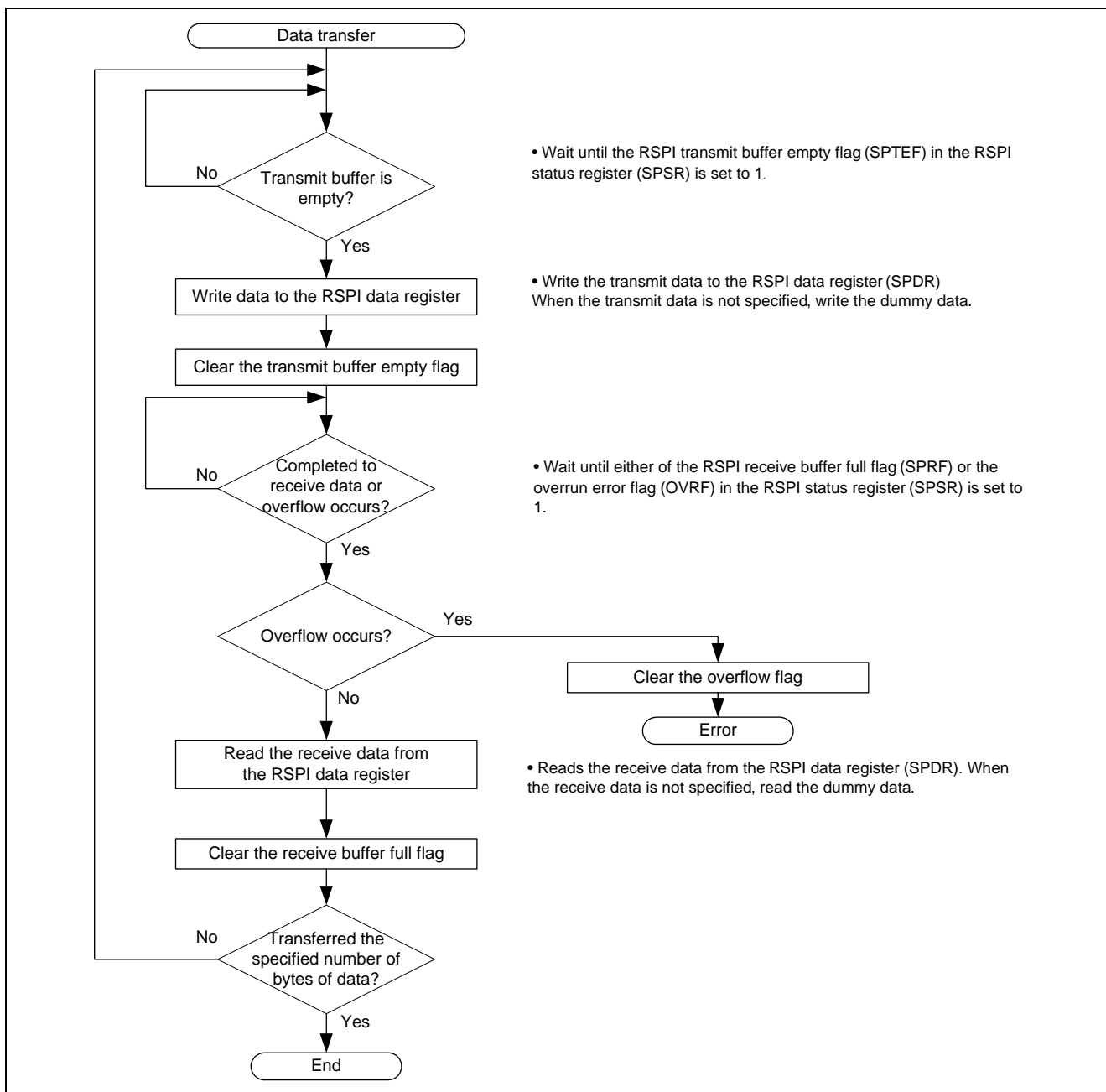


Figure 7 Flow Chart of the Data Transfer

2.4.3 Main Function

Figure 8 shows the flow chart of the main function in the sample program. The sample program writes data in the entire memory array, and compares the written value to the read value.

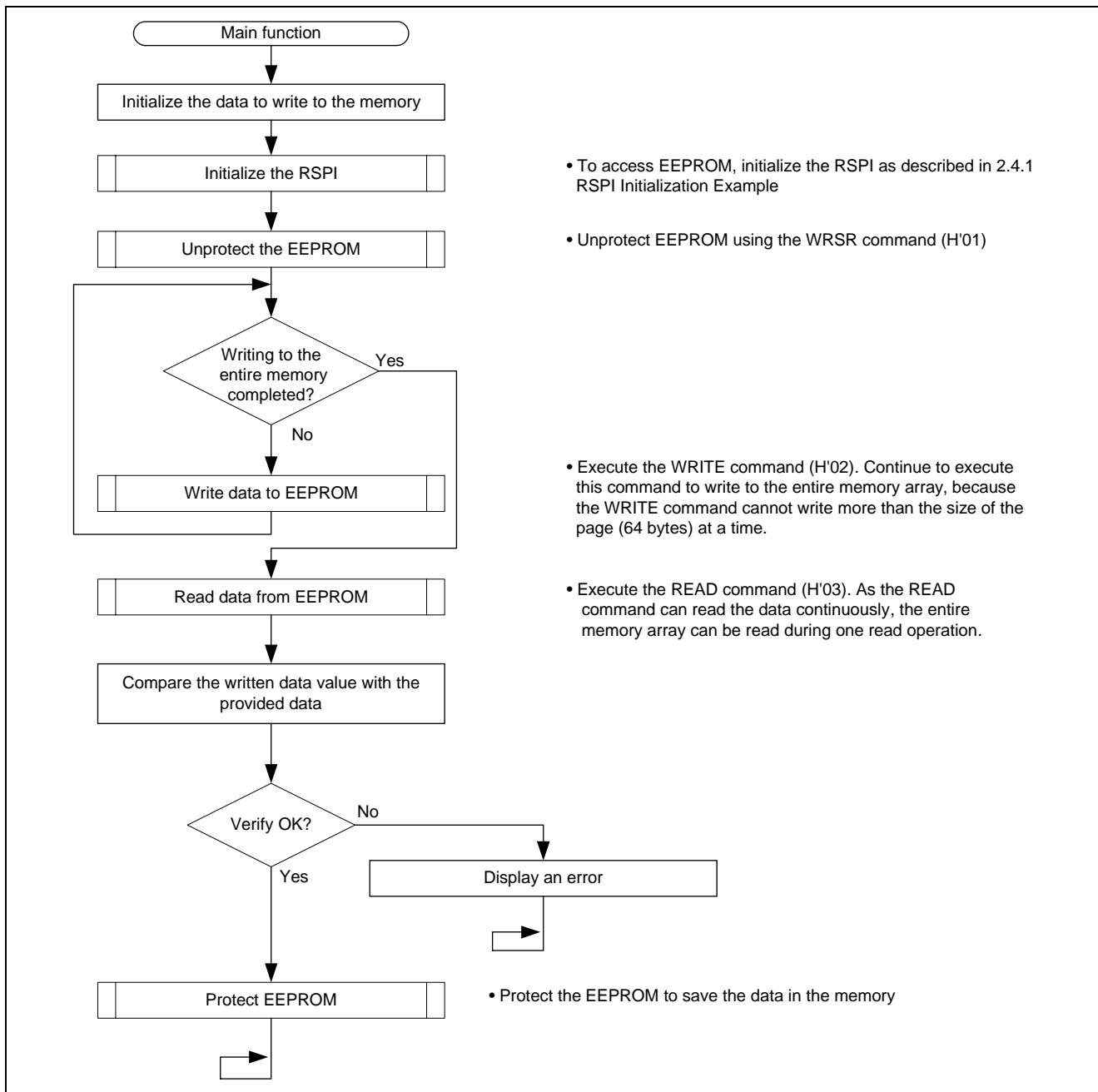


Figure 8 Main Function Flow Chart

### 3. Sample Program Listing

#### 3.1 Sample Program Listing "main.c" (1/3)

```
1  /*****
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3  *
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5  *   intended for use with Renesas products.  No other uses are authorized.
6  *
7  *   This software is owned by Renesas Electronics Corporation and is protected under
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10 *   THIS SOFTWARE IS PROVIDED "AS IS" AND RENESAS MAKES NO WARRANTIES
11 *   REGARDING THIS SOFTWARE, WHETHER EXPRESS, IMPLIED OR STATUTORY,
12 *   INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, FITNESS FOR A
13 *   PARTICULAR PURPOSE AND NON-INFRINGEMENT.  ALL SUCH WARRANTIES ARE EXPRESSLY
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26 *   http://www.renesas.com/disclaimer
27 *****/
28 *   Copyright (C) 2010 Renesas Electronics Corporation. All Rights Reserved.
29 *"FILE COMMENT"***** Technical reference data *****
30 *   System Name : SH7239 Sample Program
31 *   File Name   : main.c
32 *   Abstract    : Reading/Writing EEPROM Using the Renesas Serial
33 *               : Peripheral Interface
34 *   Version     : 1.00.00
35 *   Device      : SH7239
36 *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.07.00).
37 *               : C/C++ compiler package for the SuperH RISC engine family
38 *               :                               (Ver.9.03 Release02).
39 *   OS          : None
40 *   H/W Platform: R0K572390 (CPU board)
41 *   Description : Connects the EEPROM with the MCU using the Renesas Serial
42 *               : Peripheral Interface.
43 *****/
44 *   History     : Aug.20,2010 Ver.1.00.00
45 *"FILE COMMENT END"*****/
46 #include <stdio.h>
47 #include "eeprom.h"
48
```

## 3.2 Sample Program Listing "main.c" (2/3)

```

49  /* ==== Macro definition ==== */
50  #define TOP_ADDRESS    0                /* Start address of EEPROM */
51
52  /* ==== Function prototype declaration ==== */
53  void main(void);
54
55  /* ==== Variable definition ==== */
56  #pragma section DEBUG_BUFFER
57  static unsigned char data[EEP_BUFF_SIZE];
58  static unsigned char rbuf[EEP_BUFF_SIZE];
59  #pragma section
60
61  /*"FUNC COMMENT"*****
62  * ID          :
63  * Outline     : Accessing EEPROM main
64  *-----
65  * Include     :
66  *-----
67  * Declaration : void main(void);
68  *-----
69  * Description : Writes or reads EEPROM.
70  *             : Initializes the RSPI, and then writes data to the entire memory
71  *             : array from the beginning. Then, it reads and verifies the data.
72  *-----
73  * Argument    : void
74  *-----
75  * Return Value : void
76  *-----
77  * Note        : None
78  *"FUNC COMMENT END"*****/
79  void main(void)
80  {
81      int i,j;
82      static unsigned long addr;
83
84      /* ==== Initializes the RSPI ==== */
85      eep_init_eeprom();
86
87      /* ==== Unprotects EEPROM ==== */
88      eep_protect_ctrl( EEP_REQ_UNPROTECT );
89

```

### 3.3 Sample Program Listing "main.c" (3/3)

```
90      /* ==== Writes data (64 KB) ==== */
91      addr = TOP_ADDRESS;
92      /* ---- Initializes the data (16 KB) ---- */
93      for(i = 0; i < EEP_BUFF_SIZE; i++){
94          data[i] = i % 100;
95          rbuf[i] = 0;
96      }
97      /* ---- Writes one memory (64 KB) data ---- */
98      for(j = 0; j < EEP_MEM_SIZE/EEP_BUFF_SIZE; j++){
99          /* ---- Writes one buffer (4 KB) data ---- */
100         for(i = 0; i < ( EEP_BUFF_SIZE / EEP_PAGE_SIZE ); i++){
101             /* ---- Writes one page (128 bytes) data ---- */
102             eep_byte_write( addr, data+(i*EEP_PAGE_SIZE), EEP_PAGE_SIZE );
103             addr += EEP_PAGE_SIZE;          /* Updates the destination address to write */
104         }
105     }
106     /* ==== Reads data (64 KB) ==== */
107     addr = TOP_ADDRESS;
108     /* ---- Reads one memory (64 KB) data ---- */
109     for(j = 0; j < EEP_MEM_SIZE/EEP_BUFF_SIZE; j++){
110         /* ---- Reads one buffer (4 KB) data ---- */
111         eep_byte_read( addr, rbuf, EEP_BUFF_SIZE );
112         addr += EEP_BUFF_SIZE;          /* Updates the destination address to read */
113         /* ---- Verifies data ---- */
114         for(i = 0; i < EEP_BUFF_SIZE; i++){
115             data[i] = i % 100;          /* Outputs the written data */
116             if( data[i] != rbuf[i] ){
117                 puts("Error: verify error\n");
118                 fflush(stdout);
119                 while(1);
120             }
121         }
122     }
123     /* ==== Protects EEPROM ==== */
124     eep_protect_ctrl( EEP_REQ_PROTECT );
125
126     while(1){
127         /* loop */
128     }
129 }
130
131 /* End of File */
```



## 3.4 Sample Program Listing "eeprom.c" (1/12)

```

1  /*****
2  *   DISCLAIMER
3  *
4  *   This software is supplied by Renesas Electronics Corporation and is only
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24 *   By using this software, you agree to the additional terms and
25 *   conditions found by accessing the following link:
26 *   http://www.renesas.com/disclaimer
27 *****/
28 *   Copyright (C) 2010 Renesas Electronics Corporation. All Rights Reserved.
29 *   "FILE COMMENT"***** Technical reference data *****
30 *   System Name   : SH7239 Sample Program
31 *   File Name    : eeprom.c
32 *   Abstract     : Reading/Writing EEPROM Using the Renesas Serial
33 *                : Peripheral Interface
34 *   Version      : 1.00.00
35 *   Device       : SH7239
36 *   Tool-Chain   : High-performance Embedded Workshop (Ver.4.07.00).
37 *                : C/C++ compiler package for the SuperH RISC engine family
38 *                :                               (Ver.9.03 Release02).
39 *   OS           : None
40 *   H/W Platform: R0K572390 (CPU board)
41 *   Description  : Connects the EEPROM with the MCU using the Renesas Serial
42 *                : Peripheral Interface.
43 *****/
44 *   History      : Aug.20,2010 Ver.1.00.00
45 *   "FILE COMMENT END"*****/
46 #include <stdio.h>
47 #include <machine.h>
48 #include "iodefine.h"
49 #include "eeprom.h"
50

```

## 3.5 Sample Program Listing "eeprom.c" (2/12)

```

51  /* ==== Macro definition ==== */
52  #define EEPROMCMD_WRITE_ENABLE 0x06
53  #define EEPROMCMD_WRITE_DISABLE 0x04
54  #define EEPROMCMD_READ_STATUS 0x05
55  #define EEPROMCMD_WRITE_STATUS 0x01
56  #define EEPROMCMD_READ_ARRAY 0x03
57  #define EEPROMCMD_WRITE_ARRAY 0x02
58  #define UNPROTECT_WR_STATUS 0x00
59  #define PROTECT_WR_STATUS 0x0C
60  #define EEP_BUSY_BIT 0x01
61
62  /* ==== Function prototype declaration ==== */
63  /** Local function **/
64  static void write_enable(void);
65  static void write_disable(void);
66  static void busy_wait(void);
67  static unsigned char read_status(void);
68  static void write_status(unsigned char status);
69  static void io_init_rspi(void);
70  static void io_cmd_exe(unsigned char *ope, int ope_sz, unsigned char *data, int data_sz);
71  static void io_cmd_exe_rdmode(unsigned char *ope, int ope_sz, unsigned char *rd, int rd_sz);
72  static int io_rspi_transfer(unsigned char *write_data, unsigned char *read_data, int data_sz);
73
74  /* ==== Variable definition ==== */
75
76  /*"FUNC COMMENT"*****
77  * ID :
78  * Outline : EEPROM initialization
79  *-----
80  * Include :
81  *-----
82  * Declaration : void eep_init_eeprom(void);
83  *-----
84  * Description : Initializes EEPROM for being accessed.
85  * : Initializes the Renesas Serial Peripheral Interface (RSPI).
86  *-----
87  * Argument : void
88  *-----
89  * Return Value : void
90  *-----
91  * Note : None
92  *"FUNC COMMENT END"*****/
93  void eep_init_eeprom(void)
94  {
95  /* ==== Initializes RSPI0 ==== */
96  io_init_rspi();
97  }

```

## 3.6 Sample Program Listing "eeprom.c" (3/12)

```

98  /*"FUNC COMMENT"*****
99  * ID      :
100 * Outline   : Protect/unprotect operation
101 *-----
102 * Include   :
103 *-----
104 * Declaration : void eep_protect_ctrl(enum eep_req req);
105 *-----
106 * Description : Protects or unprotects EEPROM. Use the argument req to specify.
107 *             : Default setting and unprotecting method depends on the
108 *             : specifications of EEPROM.
109 *-----
110 * Argument   : enum eep_req req ; I : EEP_REQ_UNPROTECT -> Write-enable entire memory array
111 *             :                   EEP_REQ_PROTECT   -> Write-protect entire memory array
112 *-----
113 * Return Value : void
114 *-----
115 * Note       : None
116 *"FUNC COMMENT END"*****/
117 void eep_protect_ctrl(enum eep_req req)
118 {
119     if( req == EEP_REQ_UNPROTECT ){
120         write_status( UNPROTECT_WR_STATUS);      /* Unprotects the entire memory area */
121     }
122     else{
123         write_status( PROTECT_WR_STATUS );      /* Protects the entire memory area */
124     }
125 }
126 /*"FUNC COMMENT"*****
127 * ID      :
128 * Outline   : Write data
129 *-----
130 * Include   :
131 *-----
132 * Declaration : void eep_byte_write(unsigned long addr, unsigned char *buf, int size);
133 *-----
134 * Description : Writes the specified data to EEPROM.
135 *             : Issue the Write Enable command before writing. After writing,
136 *             : make sure to check the status of EEPROM if it is not busy.
137 *             : The maximum write data size depends on the type of the device.
138 *-----
139 * Argument   : unsigned long addr ; I : Address in EEPROM to write
140 *             : unsigned char *buf ; I : Buffer address to store the write data
141 *             : int size ; I : Number of bytes to write
142 *-----
143 * Return Value : void
144 *-----
145 * Note       : None
146 *"FUNC COMMENT END"*****/
147 void eep_byte_write(unsigned long addr, unsigned char *buf, int size)

```

## 3.7 Sample Program Listing "eeprom.c" (4/12)

```

148  {
149      unsigned char cmd[3];
150
151      cmd[0] = EEPROMCMD_WRITE_ARRAY;
152      cmd[1] = (unsigned char)((addr >> 8) & 0xff);
153      cmd[2] = (unsigned char)( addr          & 0xff);
154      write_enable();
155      io_cmd_exe(cmd, 3, buf, size);
156      busy_wait();
157  }
158  /*"FUNC COMMENT"*****
159  * ID          :
160  * Outline     : Read data
161  *-----
162  * Include     :
163  *-----
164  * Declaration : void eep_byte_read(unsigned long addr, unsigned char *buf, int size);
165  *-----
166  * Description : Reads the specified number of bytes from EEPROM.
167  *-----
168  * Argument    : unsigned long addr ; I : Address in EEPROM to read
169  *              : unsigned char *buf ; I : Buffer address to store the read data
170  *              : int size           ; I : Number of bytes to read
171  *-----
172  * Return Value : void
173  *-----
174  * Note        : None
175  *"FUNC COMMENT END"*****/
176  void eep_byte_read(unsigned long addr, unsigned char *buf, int size)
177  {
178      unsigned char cmd[3];
179
180      cmd[0] = EEPROMCMD_READ_ARRAY;
181      cmd[1] = (unsigned char)((addr >> 8) & 0xff);
182      cmd[2] = (unsigned char)( addr          & 0xff);
183      io_cmd_exe_rdmode(cmd, 3, buf, size);
184  }

```

### 3.8 Sample Program Listing "eeprom.c" (5/12)

```
185  /*"FUNC COMMENT"*****
186  * ID      :
187  * Outline : Write enable
188  *-----
189  * Include :
190  *-----
191  * Declaration : static void write_enable(void);
192  *-----
193  * Description : Issues the Write Enable command to enable writing data to
194  *             : EEPROM.
195  *-----
196  * Argument  : void
197  *-----
198  * Return Value : void
199  *-----
200  * Note      : None
201  *"FUNC COMMENT END"*****/
202  static void write_enable(void)
203  {
204      unsigned char cmd[1];
205      cmd[0] = EEPROMCMD_WRITE_ENABLE;
206      io_cmd_exe(cmd, 1, NULL, 0);
207  }
208  /*"FUNC COMMENT"*****
209  * ID      :
210  * Outline : Write disable
211  *-----
212  * Include :
213  *-----
214  * Declaration : static void write_disable(void);
215  *-----
216  * Description : Issues the Write Disable command to disable writing data to
217  *             : EEPROM.
218  *-----
219  * Argument  : void
220  *-----
221  * Return Value : void
222  *-----
223  * Note      : None
224  *"FUNC COMMENT END"*****/
225  static void write_disable(void)
226  {
227      unsigned char cmd[1];
228      cmd[0] = EEPROMCMD_WRITE_DISABLE;
229      io_cmd_exe(cmd, 1, NULL, 0);
230  }
```

## 3.9 Sample Program Listing "eeprom.c" (6/12)

```

231  /*"FUNC COMMENT"*****
232  * ID      :
233  * Outline : Busy waiting
234  *-----
235  * Include :
236  *-----
237  * Declaration : static void busy_wait(void);
238  *-----
239  * Description : Loops internally when the EEPROM status is busy.
240  *-----
241  * Argument   : void
242  *-----
243  * Return Value : void
244  *-----
245  * Note       : None
246  *"FUNC COMMENT END"*****/
247  static void busy_wait(void)
248  {
249      while ((read_status() & EEP_BUSY_BIT) != 0) { /* RDY/BSY */
250          /* EEPROM is busy */
251      }
252  }
253  /*"FUNC COMMENT"*****
254  * ID      :
255  * Outline : Read status
256  *-----
257  * Include :
258  *-----
259  * Declaration : static unsigned char read_status(void);
260  *-----
261  * Description : Reads the status of EEPROM.
262  *-----
263  * Argument   : void
264  *-----
265  * Return Value : Status register value
266  *-----
267  * Note       : None
268  *"FUNC COMMENT END"*****/
269  static unsigned char read_status(void)
270  {
271      unsigned char buf;
272      unsigned char cmd[1];
273
274      cmd[0] = EEPROMCMD_READ_STATUS;
275      io_cmd_exe_rdmode(cmd, 1, &buf, 1);
276      return buf;
277  }

```

### 3.10 Sample Program Listing "eeprom.c" (7/12)

```
278  /*"FUNC COMMENT"*****
279  * ID      :
280  * Outline : Write status
281  *-----
282  * Include :
283  *-----
284  * Declaration : static void write_status(unsigned char status);
285  *-----
286  * Description : Writes the status of EEPROM.
287  *-----
288  * Argument    : unsigned char status ; I : status register value
289  *-----
290  * Return Value : void
291  *-----
292  * Note        : None
293  *"FUNC COMMENT END"*****/
294  static void write_status(unsigned char status)
295  {
296      unsigned char cmd[2];
297
298      cmd[0] = EEPROMCMD_WRITE_STATUS;
299      cmd[1] = status;
300
301      write_enable();
302      io_cmd_exe(cmd, 2, NULL, 0);
303      busy_wait();
304  }
```

## 3.11 Sample Program Listing "eeprom.c" (8/12)

```

305  /*"FUNC COMMENT"*****
306  * ID      :
307  * Outline : RSPI initialization
308  *-----
309  * Include :
310  *-----
311  * Declaration : static void io_init_rsipi(void);
312  *-----
313  * Description : Initializes the RSPI.
314  *             : Sets the RSPI in master mode to set parameters required to transfer
315  *             : according to the specifications of EEPROM.
316  *-----
317  * Argument  : void
318  *-----
319  * Return Value : void
320  *-----
321  * Note      : None
322  *"FUNC COMMENT END"*****/
323  static void io_init_rsipi(void)
324  {
325      /* ==== PFC ==== */
326      PFC.PACRL3.BIT.PA9MD = 5; /* SSL0 */
327      PFC.PACRL3.BIT.PA8MD = 5; /* MISO */
328      PFC.PACRL2.BIT.PA7MD = 5; /* MOSI */
329      PFC.PACRL2.BIT.PA6MD = 5; /* RSPCK */
330
331      /* ==== CPG ==== */
332      STB.CR5.BIT._RSPI = 0; /* RSPI active */
333
334      /* ==== RSPI ==== */
335      RSPI.SPCCR.BYTE = 0x00; /* Disables the RSPI */
336      RSPI.SPPCR.BYTE = 0x30; /* MOSI idle fixed value = 1 */
337      RSPI.SPBR.BYTE = 0x04; /* Specifies the base bit rate as 4.0 MHz
338                          /* (P clock = 40 MHz) */
339      RSPI.SPDCR.BYTE = 0x00; /* Access width of the SPDR register: 16-bit */
340      RSPI.SPCKD.BYTE = 0x00; /* RSPCK delay: 1 RSPCK */
341      RSPI.SSLND.BYTE = 0x00; /* SSL negation delay: 1 RSPCK */
342      RSPI.SPND.BYTE = 0x00; /* Next-access delay: 1 RSPCK */
343      RSPI.SPSCR.BYTE = 0x00; /* Sequence length: 1 (Only SPCMD0 is used) */
344      RSPI.SPCMD0.WORD = 0xE783; /* MSB first */
345                          /* Data length: 8-bit */
346                          /* Keeps the SSL signal level after a transfer */
347                          /* is completed */
348                          /* Bit rate: Base bit rate is not divided */
349                          /* RSPCK when idling is 1 */
350                          /* Outputs data on odd edge, latches data on even edge */
351      RSPI.SSLP.BYTE = 0x00; /* SSLP = b'0 SSL signal 0-active */
352      RSPI.SPCCR.BYTE = 0x48; /* Master mode */
353                          /* Disables interrupts */
354                          /* Enables the RSPI */
355  }

```



## 3.12 Sample Program Listing "eeprom.c" (9/12)

```

356  /*"FUNC COMMENT"*****
357  * ID      :
358  * Outline : Execute command (No read data).
359  *-----
360  * Include :
361  *-----
362  * Declaration : static int io_cmd_exe(unsigned char *ope, int ope_sz,
363  *      :      unsigned char *data,int data_sz)
364  *-----
365  * Description : Executes the specified command.
366  *      : Transmits the argument ope, and then transmits the argument
367  *      : data. Discards the received data.
368  *      : Set one of the values between 0 and 8 to the ope_sz.
369  *      : Set one of the values between 0 to 256 to the data_sz.
370  *-----
371  * Argument   : unsigned char *ope ; I : Start address of the opcode block and
372  *      :      : address block to transmit
373  *      : int ope_sz      ; I : Number of bytes in the opcode block and
374  *      :      : address block
375  *      : unsigned char *data; I : Start address of the data block to transmit
376  *      : int data_sz    ; I : NUmber of bytes in the data block
377  *-----
378  * Return Value : void
379  *-----
380  * Note      : None
381  /*"FUNC COMMENT END"*****/
382  static void io_cmd_exe(unsigned char *ope, int ope_sz, unsigned char *data, int data_sz)
383  {
384  /* ---- Enables the SPI transfer ---- */
385  RSPI.SPCR.BIT.SPE = 1;
386
387  /* ---- MOSI ---- */
388  io_rsapi_transfer(ope, NULL, ope_sz);
389  io_rsapi_transfer(data, NULL, data_sz);
390
391  /* ---- SPI transfer is completed (SSL negation) ---- */
392  RSPI.SPCR.BIT.SPE = 0;
393  }

```

## 3.13 Sample Program Listing "eeprom.c" (10/12)

```

394  /*"FUNC COMMENT"*****
395  * ID      :
396  * Outline : Execute command (With read data).
397  *-----
398  * Include :
399  *-----
400  * Declaration : static void io_cmd_exe_rdmode(unsigned char *ope, int ope_sz,
401  *      :      unsigned char *rd, int rd_sz)
402  *-----
403  * Description : Executes the specified command.
404  *      : Transmits the argument ope, and then receives data in the
405  *      : argument rd. Set one of the values between 0 and 8 to the ope_sz.
406  *      : More than 0 can be set to the rd_sz.
407  *-----
408  * Argument : unsigned char *ope ; I : Start address of the opcode block and
409  *      :      : address block to transmit
410  *      : int ope_sz      ; I : Number of bytes in the opcode block and
411  *      :      : address block
412  *      : unsigned char *rd ; I : Buffer address to store the received data
413  *      : int rd_sz      ; I : Number of bytes in the data block
414  *-----
415  * Return Value : void
416  *-----
417  * Note      : None
418  *"FUNC COMMENT END"*****/
419  static void io_cmd_exe_rdmode(unsigned char *ope, int ope_sz, unsigned char *rd, int rd_sz)
420  {
421  /* ---- Enables the SPI transfer ---- */
422  RSPI.SPCR.BIT.SPE = 1;
423
424  /* ---- MISO ---- */
425  io_rspi_transfer(ope, NULL, ope_sz);
426  io_rspi_transfer(NULL, rd, rd_sz);
427
428  /* ---- SPI transfer is completed (SSL negation) ---- */
429  RSPI.SPCR.BIT.SPE = 0;
430  }

```

## 3.14 Sample Program Listing "eeprom.c" (11/12)

```

431  /*"FUNC COMMENT"*****
432  * ID      :
433  * Outline : RSPI data transfer
434  *-----
435  * Include :
436  *-----
437  * Declaration : int io_rspi_transfer(unsigned char *write_data,
438  *      :      unsigned char *read_data, int data_sz);
439  *-----
440  * Description : Transfers commands and data in bytes. Transmits the opcode or
441  *      : data from the argument write_data, and receives the data in the
442  *      : argument read_data.
443  *      : When the argument write_data is NULL, this function transmits
444  *      : the dummy data (0xff). WHEN the argument read_data is NULL,
445  *      : this function does not receive the data.
446  *-----
447  * Argument   : unsigned char *write_data : I : Start address of the transmit data
448  *      : unsigned char *read_data : O : Buffer address to store the
449  *      :                          : received data
450  *      : int data_sz : I : Number of bytes of the transmit and received data
451  *-----
452  * Return Value : 0 : Succeeded to transfer data
453  *      : -1: Overrun error occurs
454  *-----
455  * Note        : None
456  *"FUNC COMMENT END"*****/
457  static int io_rspi_transfer(unsigned char *write_data, unsigned char *read_data, int data_sz)
458  {
459      unsigned short tmp;
460
461      while(data_sz--){
462          while(RSPI.SPSR.BIT.SPTEF == 0){
463              /* wait */
464          }
465          /* Writes the transmit data to the data register */
466          if(write_data != (unsigned char *)0){
467              tmp = (unsigned short)*write_data++;
468          }
469          else{
470              tmp = 0x00ff; /* Dummy write data */
471          }
472      }
473
474      RSPI.SPDR.WORD = 0x00ff & tmp;
475
476      RSPI.SPSR.BIT.SPTEF = 0; /* Clears the bit to 0 to transmit data */
477

```

**3.15 Sample Program Listing "eeprom.c" (12/12)**

```
478     /* Waits until the reception is completed */
479     while((RSPI.SPSR.BYTE & 0x81) == 0x00){
480         /* Waits until the receive buffer is full or an overrun error occurs */
481     }
482
483     /* Overrun error occurs? */
484     if(RSPI.SPSR.BIT.OVRF == 1){
485         RSPI.SPSR.BIT.OVRF = 0;
486         return -1; /* Overrun error occurred */
487     }
488
489     /* Reads the received data */
490     tmp = RSPI.SPDR.WORD;
491     if(read_data != (unsigned char *)0){
492         *read_data++ = (unsigned char)tmp;
493     }
494     RSPI.SPSR.BIT.SPRF = 0;
495 }
496
497     return 0;
498 }
499
500     /* End of File */
```

## 3.16 Sample Program Listing "eeprom.h" (1/2)

```

1  /*****
2  *   DISCLAIMER
3  *
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25 *   conditions found by accessing the following link:
26 *   http://www.renesas.com/disclaimer
27 *****/
28 *   Copyright (C) 2010 Renesas Electronics Corporation. All Rights Reserved.
29 *   "FILE COMMENT"***** Technical reference data *****
30 *   System Name   : SH7239 Sample Program
31 *   File Name    : eeprom.h
32 *   Abstract     : Reading/Writing EEPROM Using the Renesas Serial
33 *                : Peripheral Interface
34 *   Version      : 1.00.00
35 *   Device       : SH7239
36 *   Tool-Chain   : High-performance Embedded Workshop (Ver.4.07.00).
37 *                : C/C++ compiler package for the SuperH RISC engine family
38 *                :                               (Ver.9.03 Release02).
39 *   OS           : None
40 *   H/W Platform: R0K572390 (CPU board)
41 *   Description  : Connects the EEPROM with the MCU using the Renesas Serial
42 *                : Peripheral Interface.
43 *****/
44 *   History      : Aug.20,2010 Ver.1.00.00
45 *   "FILE COMMENT END"*****/
46 #ifndef _EEPROM_H_
47 #define _EEPROM_H_
48

```

### 3.17 Sample Program Listing "eeprom.h" (2/2)

```
49  /* ==== Macro definition ==== */
50  #define EEP_PAGE_SIZE      128      /* Page size of EEPROM */
51  #define EEP_MEM_SIZE      0x10000  /* EEPROM size (64 KB) */
52  #define EEP_BUFF_SIZE     0x1000   /* Buffer area to verify the EEPROM data */
53                                     /* = 4 KB */
54  enum eep_req{
55      EEP_REQ_PROTECT = 0,          /* Requests to protect */
56      EEP_REQ_UNPROTECT          /* Requests to unprotect */
57  };
58  /* ==== Function prototype declaration ==== */
59  void eep_init_serial_flash(void);
60  void eep_protect_ctrl(enum eep_req req);
61  void eep_byte_write(unsigned long addr, unsigned char *buf, int size);
62  void eep_byte_read(unsigned long addr, unsigned char *buf, int size);
63
64  /* ==== Variable definition ==== */
65
66  #endif /* _EEPROM_H_ */
67
68  /* End of File */
```

#### **4. References**

- Software Manual  
SH-2A/SH2A-FPU Software Manual Rev. 3.00  
The latest version of the software manual can be downloaded from the Renesas Electronics website.
- Hardware Manual  
SH7239 Group, SH7237 Group Hardware User's Manual Rev. 1.00
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## Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Nov.24.10	—	First edition issued

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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