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# SH7211 Group

## Sample Settings at CPG Operation Frequency Change

### Introduction

This application note presents sample settings for changing the operating frequency of the clock pulse generator (CPG) of the SH7211.

### Target Devices

SH7211

### Contents

# 1. Preface

## 1.1 Specifications

- The clock pulse generator (CPG) settings are changed to change the operating frequency.
- The watchdog timer is used to provide the necessary PLL settling time when changing the multiplication ratio of the PLL circuit.

## 1.2 Functions Used

- Clock pulse generator (CPG)
- Watchdog timer (WDT)

## 1.3 Application Conditions

- MCU: SH7211
- Operating frequencies: Internal clock = 160 MHz
  Bus clock = 40 MHz
  Peripheral clock = 40 MHz
  MTU2S clock = 80 MHz
  AD clock = 40 MHz
- C compiler: Renesas Technology SuperH RISC Engine Family C/C++ Compiler Package, Ver. 9.01, Release 01
- Compile options: HEW default settings (-cpu=sh2a -debug -gbr=auto -chgincpath -global_volatile=0 -opt_range=all -infinite_loop=0 -struct_alloc=1 -nologo)

## 1.4 Related Application Notes

The reference program code provided in this application note has been confirmed to work under the setting conditions described in the SH7211 application note “Example of Initialization.”

## 2. The Application Example

In this application example, the watchdog timer (WDT) is used to count the clock oscillation settling time when the operating frequency is changed.

### 2.1 Operational Overview of the Functions Used

When the multiplication ratio of the PLL circuit of the clock pulse generator (CPG) is changed, it is necessary to provide time for the PLL to settle following the change. The on-chip WDT is used to ensure the proper PLL settling time.

When the timer enable (TME) bit is cleared to 0 and the CPG's frequency control register (FRQCR) is overwritten to change the PLL multiplication ratio, CPU internal operation stops temporarily and the WDT starts counting. When the WDT overflows, the CPG starts to supply the clock and CPU operation resumed.

Tables 1 and 2 provide an overview of the CPG and WDT. Figures 1 and 2 show a visual overview of the CPG and WDT.

**Table 1 Overview of CPG**

| Item | Description |
|---|---|
| Clock operating modes | 4 |
| Clocks generated | Internal clock (Iϕ) : Used by CPU<br>Peripheral clock (Pϕ) : Used by on-chip peripheral modules<br>Bus clock (Bϕ) : Used by external bus interface |
| Frequency change function | The frequencies of the internal clock and peripheral clock can be changed independently by means of the CPG's internal PLL circuit and peripheral circuits. |
| Control of low-power modes | The clock can be stopped in sleep mode, software standby mode, and deep standby mode, and the operation of specific modules can be stopped by using the module standby function. |

**Table 2 Overview of WDT**

| Item | Description |
|---|---|
| Channels | 1 |
| Counter | 8-bit counter (up-counter only) |
| Timer modes | Watchdog timer mode, interval timer mode |
| Pin functions | WDTOVF: Counter overflow signal output in watchdog timer mode |
| Clock sources | Pϕ, Pϕ/64, Pϕ/128, Pϕ/256, Pϕ/512, Pϕ/1024, Pϕ/4096, Pϕ/16384<br>Pϕ: On-chip peripheral clock |
| Activation methods | Watchdog timer/interval timer: Activated by software<br>At frequency change: Activated by software<br>At cancelation of software standby mode: Activated by interrupt detection |

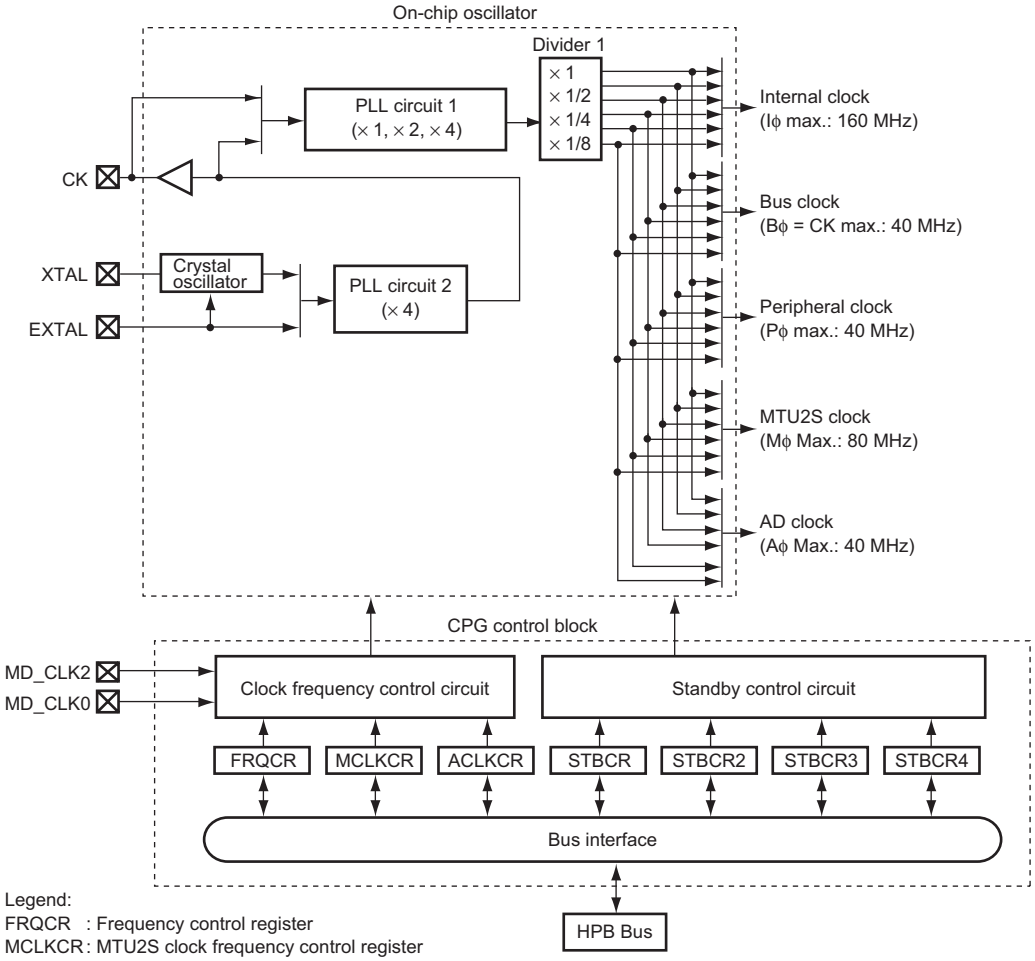


**Figure 1 Overview of CPG**

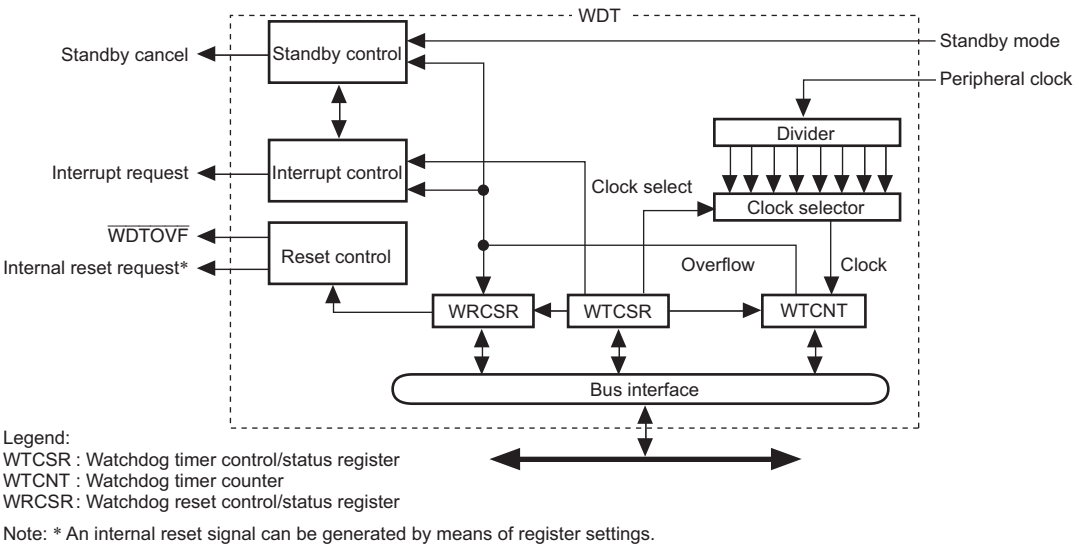


**Figure 2 Overview of WDT**

## 2.2 Setup Procedure for the Functions Used

Figure 3 shows an example settings sequence for changing the operating frequency.

For details on the register settings, see the SH7211 Group Hardware Manual.

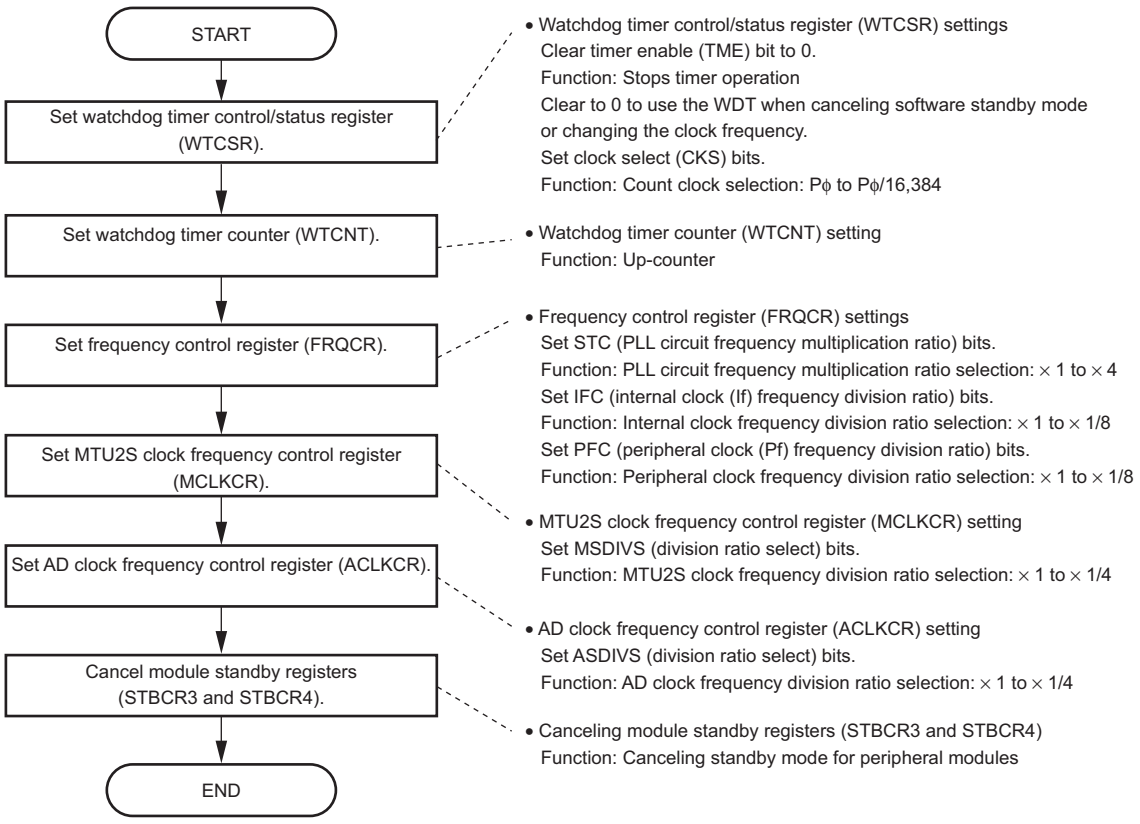


**Figure 3 Example Settings Sequence for Changing Operating Frequency**

## 2.3 Operation of Reference Program

Table 3 lists the register settings for changing the operating frequency, and table 4 lists the operating frequencies used in the reference program.

The peripheral functions are in module standby mode after a reset. The reference program makes CPG settings and then cancels module standby mode.

**Table 3 Register Settings for Changing Operating Frequency**

| Register Name | Address | Setting Value | Function |
|---|---|---|---|
| Watchdog timer control/status register (WTCSR) | H'FFFE 0000 | H'A51E | TME = 0: Timer disabled<br>CKS[2:0] = B'110: 1/4096 × Pϕ<br>Overflow period: 26.21 ms (when Pϕ = 40 MHz) |
| Watchdog timer counter (WTCNT) | H'FFFE 0002 | H'5A9E | Set count value so oscillation settling time is 10 msec. or more.<br>(H'100 – H'9E) × (1/4,096 × Pϕ) = 10.04 ms |
| Frequency control register (FRQCR) | H'FFFE 0010 | H'1303 | STC[1:0] = B'11<br>PLL circuit 1 frequency multiplication ratio = ×4<br>IFC[2:0] = B'000<br>Internal clock frequency division ratio = ×1<br>PFC[2:0] = B'011<br>Peripheral clock frequency division ratio = ×1/4 |
| MTU2S clock frequency control register (MCLKCR) | H'FFFE0410 | H'41 | MSDIVS[1:0] = B'01<br>Division ratio select = ×1/2 |
| AD clock frequency control register (ACLKCR) | H'FFFE0414 | H'43 | ASDIVS[1:0] = B'11<br>Division ratio select = ×1/4 |

**Table 4 Operating Frequencies Used in Reference Program**

| | FRQCR Setting Value | Clock Ratio (I: B: P) | Operating Frequencies (I: B: P) |
|---|---|---|---|
| Operating frequency with initial settings | H'1003 | 4: 4: 1 | 40 MHz: 40 MHz: 10 MHz |
| Operating frequency after change | H'1303 | 16: 4: 4 | 160 MHz: 40 MHz: 40 MHz |

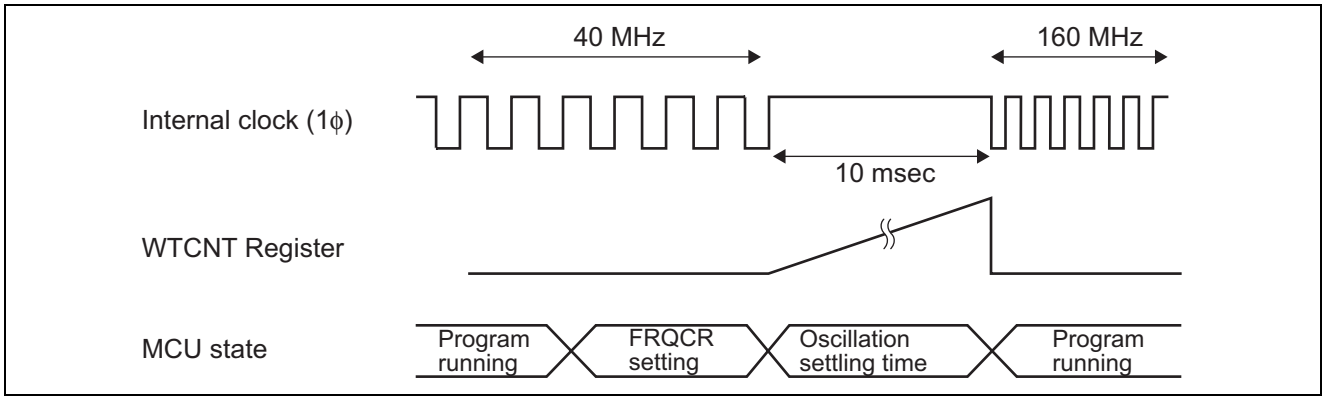


**Figure 4 Conceptual View of Reference Program Operation Timing**

## 3. Sample Program

```
1       /*""FILE COMMENT""*****************************************************************
2       *
3       *       System Name : SH7211 Sample Program
4       *       File Name   : cpg.c
5       *       Version     : 1.01.00
6       *       Contents    : CPG Setting Processing
7       *       Model       : M3A-HS11
8       *       CPU         : SH7211
9       *       Compiler    : SHC9.1.1.0
10      *       OS          : none
11      *
12      *       note        :
13      *                   : <Notes>
14      *                     This sample program is provided for reference
15      *                     purposes; its operation is not guaranteed.
16      *                     This sample program may be used for reference
17      *                     purposes when developing user applications.
18      *
19      *                     <Caution>
20      *                     This sample programs are all reference,
21      *                     and no one to guarantee the operation.
22      *                     Please use this sample program for the technical
23      *                     reference when customers develop softwares.
24      *
25      *       Copyright (C) 2006(2007) Renesas Technology Corp. All Rights Reserved
26      *       AND Renesas Solutions Corp. All Rights Reserved
27      *
28      *       history   : 2006.02.23 ver.1.00.00
29      *                 : 2007.04.03 ver.1.01.00
30      *""FILE COMMENT END""*************************************************************/
31      #include "iodefine.h"
32
33      /* ==== Prototype declaration ==== */
34      void io_set_cpg(void);
35
```

**Figure 5 Sample Program Listing: cpg.c (1)**

```
/*""FUNC COMMENT""*************************************************************
* ID             :
* Module outline : CPG setting
*-----------------------------------------------------------------------------
* Include        : #include "iodefine.h"
*-----------------------------------------------------------------------------
* Declaration    : void io_set_cpg(void)
*-----------------------------------------------------------------------------
* Function       : The clock pulse generator (CPG) setting are as follows.
*                : Clock pulse generator (CPG) is set as follows.
*                :
*                : I Clock = 160MHz, B Clock = 40MHz, P Clock = 40MHz
*                : MTU2S = 80MHz, A/D = 40MHz
*-----------------------------------------------------------------------------
* Argument       : None
*-----------------------------------------------------------------------------
* Return value   : None
*-----------------------------------------------------------------------------
* Note     : This function is a setting example using an input clock frequency of 10 MHz.
*          : This function is the setting example when the input clock 10MHz.
*""FUNC COMMENT END""*********************************************************/
void io_set_cpg(void)
{
  /* ==== CPG Set ==== */
  WDT.WRITE.WTCSR = 0xa51e;       /* WDT stop, WDT count clock setting */
                                  /* 1/4096 xP-clock  40MHz;26.2ms  */
  WDT.WRITE.WTCNT = 0x5a9e;       /* Counter initial setting 10mS */
  CPG.FRQCR.WORD = 0x1303;        /* PLL1(x4),PLL2(x4),I:B:P=16:4:4
                                  * Clockin = 10MHz, CKIO = 40MHz
                                  * I Clock = 160MHz, B Clock = 40MHz,
                                  * P Clock = 40MHz
                                  */
  CPG.MCLKCR.BYTE = 0x41;         /* MTU2S =80MHz */
  CPG.ACLKCR.BYTE = 0x43;         /* AD = 40MHz */

  /* ==== Enable module clock ==== */
  STB.CR3.BYTE = 0x00;               /* Module Standby Clear
                                     * MTU2S,MTU2,POE2,IIC3,ADC,DAC */

  STB.CR4.BYTE = 0x00;               /* Module Standby Clear
                                     * SCIF0-3,CMT,WAVE */
}

/* End of File */
```

**Figure 6 Sample Program Listing: cpg.c (2)**

## 4. Reference Documents

- Software Manual
  SH-2A, SH2A-FPU Software Manual, Rev. 3.00
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Hardware Manual
  SH7211 Group Hardware Manual, Rev. 2.00
  (The latest version can be downloaded from the Renesas Technology Web site.)

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|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
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