To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

SH7211 Group

MTU2 Positive Phase/Antiphase Three-Phase PWM Output Function (Reset-Synchronized PWM Mode)

Introduction

This application note presents sample settings for producing three-phase PWM waveform output using the reset-synchronized PWM mode of multi-function timer pulse unit 2 (MTU2) of the SH7211.

Target Device

SH7211

Contents

1. Preface

1.1 Specifications

This application note describes how to use the reset-synchronized PWM mode of channels 3 and 4 of multi-function timer pulse unit 2 (MTU2) to output three-phase (positive phase, antiphase) PWM waveforms. Figure 1 shows the configuration.

- Channels 3 and 4 of MTU2 are set to reset-synchronized PWM mode.
- The positive phase PWM output pins are TIOC3B, TIOC4A, and TIOC4B. The antiphase output pins corresponding to these positive phase output pins are TIOC3D, TIOC4C, and TIOC4D.
- The PWM output signal is high-active.
- The PWM carrier cycle is set to 400 µm.
- The three-phase PWM duty is updated by the interrupt handler that is executed each PWM cycle. The register buffer function is used to update the PWM duty.
- A toggle waveform synchronized with the PWM carrier cycle is output by pin TIOC3A.

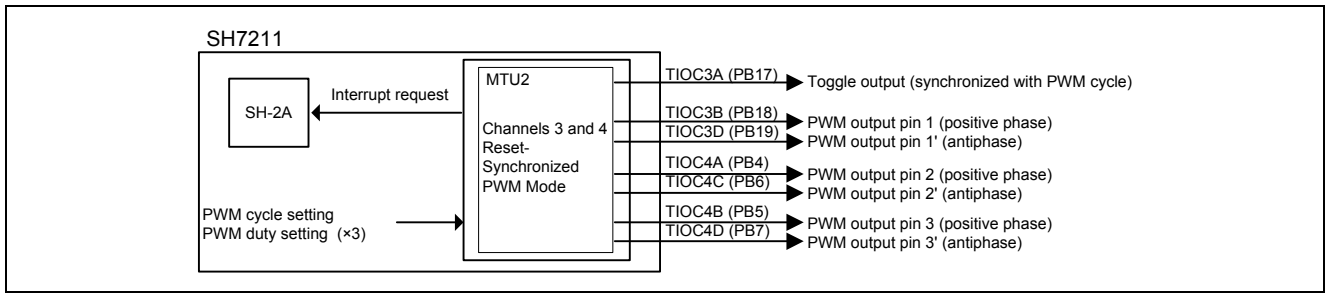


Figure 1 Three-Phase PWM Output (Reset-Synchronized PWM Mode)

1.2 Module Used

In this application note, the reset-synchronized PWM mode function of multi-function timer pulse unit 2 (MTU2) is used.

1.3 Applicable Conditions

MCU:	SH7211 [R5F7211]
Operating frequencies:	Internal clock (Iϕ) = 160 MHz
	Bus clock (Bϕ) = 40 MHz
	Peripheral clock (Pϕ) = 40 MHz
	MTU2S clock (Mϕ) = 80 MHz
	AD clock (Aϕ) = 40 MHz
MCU operating mode:	Single-chip mode
Integrated development environment:	Renesas Technology High-performance Embedded Workshop, Ver. 4.05.01.001
C compiler:	Renesas Technology SuperH RISC engine Family C/C++ Compiler Package, Ver. 9.03, Release 00
Compile options:	High-performance Embedded Workshop default settings
	(-cpu=sh2a -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo)

2. Description of the Sample Application

In reset-synchronized PWM mode, channel 3 and channel 4 are combined to produce three-phase PWM waveform output (positive phase, antiphase) with common waveform change points.

2.1 Operation at Overview of Module Used

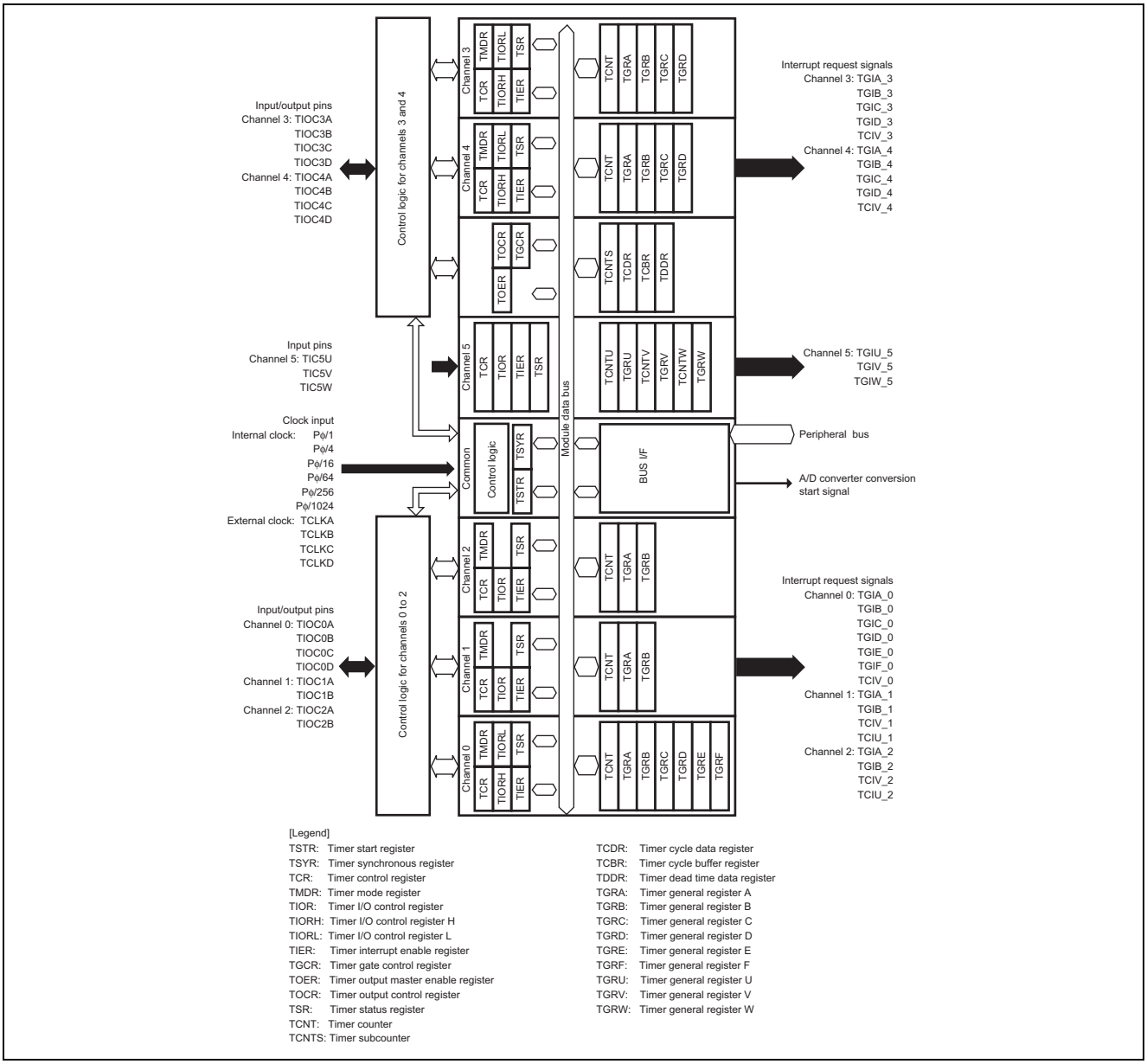
2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

When operation is set to reset-synchronized PWM mode, pins TIOC3B, TIOC4A, and TIOC4B are used for positive phase PWM output. The antiphase PWM output corresponding to the positive phase output is on pins TIOC3D, TIOC4C, and TIOC4D. Timer counter 3 (TCNT_3) functions as an up-counter. When a compare match occurs between TCNT_3 and the TGRA_3 register (cycle), the counter is cleared and up-counting restarts from H'0000. The output of the PWM output pins is toggled by compare matches with registers TGRB_3, TGRA_4, and TGRB_4, and when the counter is cleared.

Table 1 is an overview of multi-function timer pulse unit 2 (MTU2). Figure 2 is a block diagram of MTU2.

Table 1 Overview of MTU2

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clock	Each channel selectable among eight counter input clocks (four counter input clocks for channel 5)
Operation of channels 0 to 5	• Waveform output at compare match, input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clear at compare match or input capture • Synchronous register I/O using counter-synchronous operation, max. 12-phase PWM output through combination with synchronous operation
Triggers for A/D converter	• Ability to generate conversion start trigger for A/D converter • Ability to generate interrupt at counter peak/trough and to skip conversion start triggers for A/D converter in complementary PWM mode
Buffered operation	• Ability to specify register buffer operation for channels 0, 3, and 4
Operating modes	• Ability to specify PWM mode for channels 0 to 4 • Ability to specify phase counting mode independently for channels 1 and 2 • Ability to specify 3-phase positive and negative PWM waveform output (total 6 lines) in complementary PWM mode or reset synchronous PWM mode, using linked operation of channels 3 and 4
Interrupt requests	• 28 interrupt sources (compare match, input capture, etc.)
Others	• Cascade connection operation • High-speed access via internal 16-bit bus • Support for automatic transfer of register data • Ability to specify module standby mode • Support for dead time compensation counter function using channel 5



[Legend]

TSTR: Timer start register
TSYR: Timer synchronous register
TCR: Timer control register
TMDR: Timer mode register
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TGCR: Timer gate control register
TOER: Timer output master enable register
TOCR: Timer output control register
TSR: Timer status register
TCNT: Timer counter
TCNTS: Timer subcounter
TCDR: Timer cycle data register
TCBR: Timer cycle buffer register
TDDR: Timer dead time data register
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W

Figure 2 Block Diagram of MTU2

2.1.2 Reset-Synchronized PWM Mode

In reset-synchronized PWM mode, channel 3 and channel 4 are combined to produce three-phase PWM waveform output (positive phase, antiphase) with common waveform change points.

When operation is set to reset-synchronized PWM mode, pins TIOC3B, TIOC4A, and TIOC4B are used for positive phase PWM output. The antiphase PWM output corresponding to the positive phase output is on pins TIOC3D, TIOC4C, and TIOC4D. Timer counter 3 (TCNT_3) functions as an up-counter. When a compare match occurs between TCNT_3 and the TGRA_3 register (cycle), the counter is cleared and up-counting restarts from H'0000. The output of the PWM output pins is toggled by compare matches with registers TGRB_3, TGRA_4, and TGRB_4, and when the counter is cleared.

Figure 3 shows an example of operation in reset-synchronized PWM mode. In this operation example, both the positive phase and the antiphase PWM output are high-active.

Table 2 lists the PWM output pins used in reset-synchronized PWM mode. Table 3 lists the register functions.

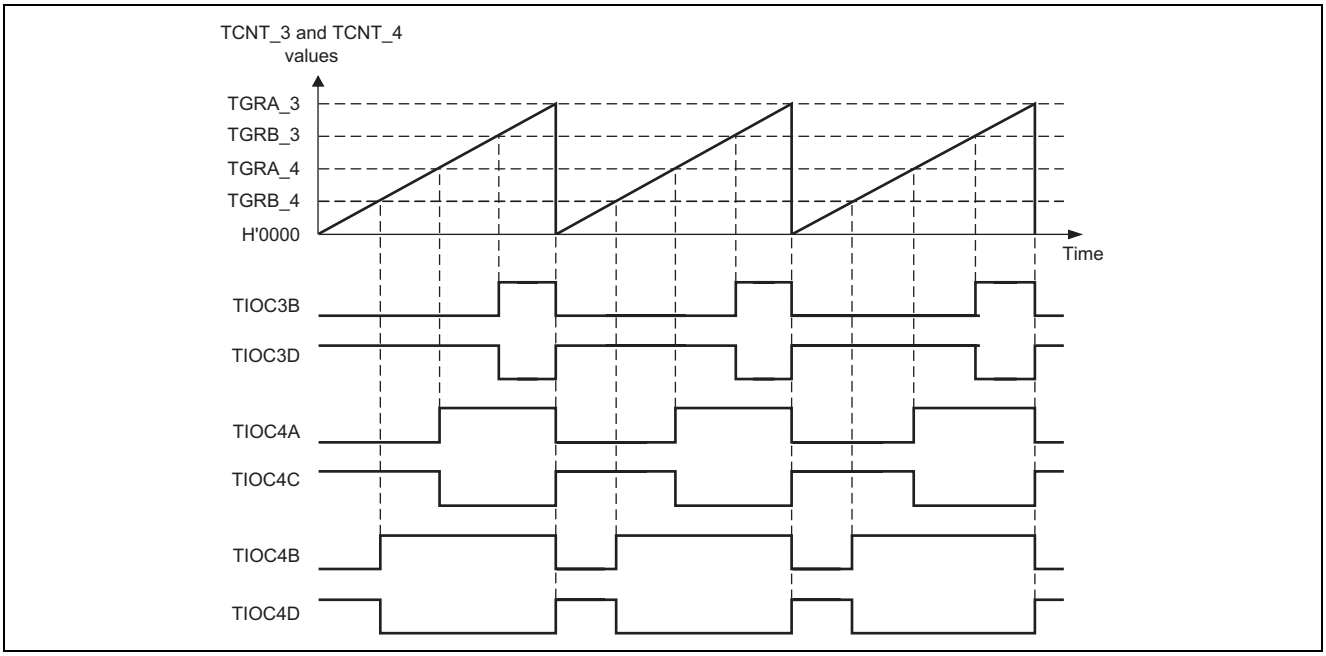


Figure 3 Sample Timing of Operation in Reset-Synchronized PWM Mode (In TOCR, OLSN = 1 and OLSP = 1)

Table 2 Output Pins in Reset-Synchronized PWM Mode

Channel	Output Pin	Description
Channel 3	TIOC3A	Toggle output synchronized with PWM cycle (Can be used as an I/O port when not used as toggle output.)
	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (PWM output 1 antiphase waveform)
Channel 4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (PWM output 2 antiphase waveform)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (PWM output 3 antiphase waveform)

Table 3 Registers Used in Reset-Synchronized PWM Mode

Register	Description
TCNT_3	Channel 3 timer counter This is initially set to H'0000.
TCNT_4	Channel 4 timer counter This is initially set to H'0000.
TGRA_3	TCNT_3 count cycle setting (PWM cycle) When updating the PWM cycle, the new value is set in the buffer register.
TGRB_3	Compare match register Sets the change point (duty) for PWM waveforms output from pins TIOC3B and TIOC3D. When updating the duty, the new value is set in the buffer register.
TGRA_4	Compare match register Sets the change point (duty) for PWM waveforms output from pins TIOC4A and TIOC4C. When updating the duty, the new value is set in the buffer register.
TGRB_4	Compare match register Sets the change point (duty) for PWM waveforms output from pins TIOC4B and TIOC4D. When updating the duty, the new value is set in the buffer register.
TGRC_3	TGRA_3 buffer register (When using the buffer function.)
TGRD_3	TGRB_3 buffer register (When using the buffer function.)
TGRC_4	TGRA_4 buffer register (When using the buffer function.)
TGRD_4	TGRB_4 buffer register (When using the buffer function.)

2.2 Operation of the Sample Program

2.2.1 Settings for Operation of the Sample Program

In this application note, channels 3 and 4 of the multi-function timer pulse unit 2 (MTU2) are set to reset-synchronized PWM mode and three-phase PWM waveforms are output.

Table 4 lists the setting conditions for reset-synchronized PWM mode.

Table 4 Settings for Reset-Synchronized PWM Mode Operation

Item	Description
Channels in use	Channels 3 and 4
Operating mode	Reset-synchronized PWM mode
Functions of pins	• TIOC3A pin: Toggle output synchronized to PWM cycle • TIOC3B pin: PWM output 1 (positive phase waveform) • TIOC3D pin: PWM output 1' (PWM output 1 antiphase waveform) • TIOC4A pin: PWM output 2 (positive phase waveform) • TIOC4C pin: PWM output 2' (PWM output 2 antiphase waveform) • TIOC4B pin: PWM output 3 (positive phase waveform) • TIOC4D pin: PWM output 4' (PWM output 3 antiphase waveform)
Active level	• Positive phase output: High-active output • Antiphase output: High-active output
Counter clock	10 MHz (4 cycles of Pϕ clock)
PWM carrier cycle	400 µm (carrier frequency: 2.5 kHz)
PWM duty	• For PWM outputs 1, 2, and 3, the initial PWM duty is 50%. • The PWM duty is updated by during interrupt handling at every compare match with TGRA_3. (The setting value is incremented or decremented.)
Interrupt	• TGRA_3 compare match interrupt TGRA_3 interrupt occurs every PWM carrier cycle.

2.2.2 Description of Operation by the Sample Program

Figure 4 illustrates the operation of the reference program. Channels 3 and 4 of multi-function timer pulse unit 2 (MTU2) are set to reset-synchronized PWM mode. The cycle and PWM duty setting registers are set by means of buffer operation. Buffer operation is enabled in reset-synchronized PWM mode by setting bits BFA and BFB in the TMDR_3 register. When bits BFA and BFB in the TMDR_3 register are set to 1, TGRC_3 functions as the buffer register of TGRA_3 and TGRD_3 as the buffer register of TGRB_3 for channel 3. At the same time, TGRC_4 functions as the buffer register of TGRA_4 and TGRD_4 as the buffer register of TGRB_4 for channel 4.

Updating of the three-phase PWM duty takes place as part of the handling routine for the TGRA_3 compare match interrupt, which is generated every PWM carrier cycle. The PWM duty update values are set in the buffer registers (TGRD_3, TGRC_4, and TGRD_4). The buffer register values are transferred to the compare registers at each TGRA_3 compare match, which is once each cycle. Using buffer operation makes it possible to update the registers according to a user-defined timing.

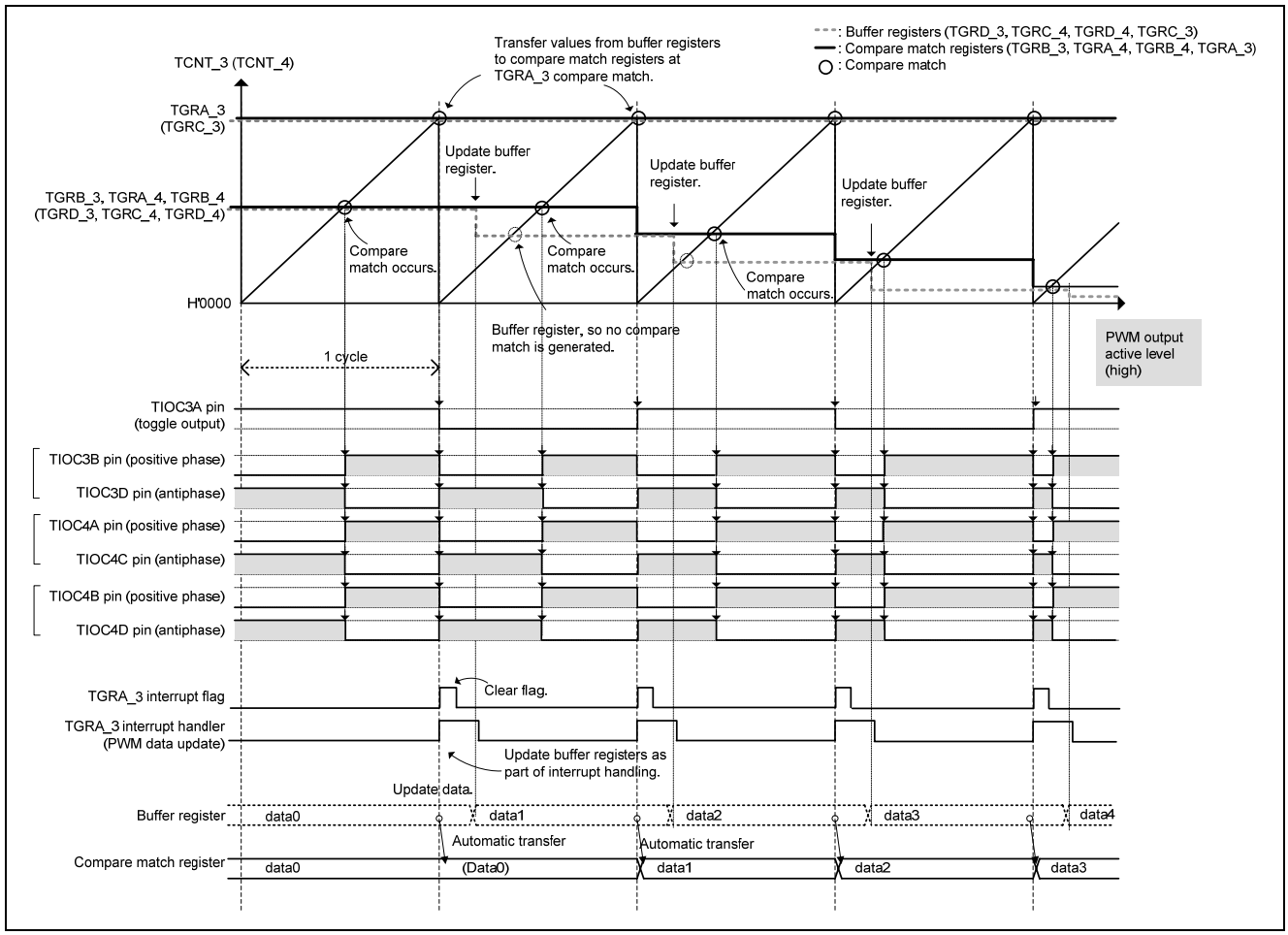


Figure 4 Operation (Buffered Operation) in Reset-Synchronized PWM Mode

(1) Cycle Register Setting Value

When the counter is set to be cleared by a compare match with cycle register TGRA_3, timer counter TCNT is cleared at the last state of the match with the value of TGR (the point in time at which the count value matching TCNT is updated). Therefore, the following equation can be used to obtain the setting value of the cycle register (TGRA_3 register):

TGRA_3 register setting value = (PWM cycle duration / 1 count duration) – 1

- PWM cycle duration: Desired PWM carrier cycle duration setting
- 1 count duration: Duration of 1 count of timer counter TCNT

If the PWM carrier cycle is 400 [µs], the following value should be set in the cycle register (TGRA_3 register):

TGRA_3 register setting value = 400 [µs] / 100 [ns] – 1

= D'3999

- Timer counter TCNT count clock: 10 MHz (Pϕ / 4: Pϕ is the on-chip peripheral clock.)
- 1 count duration: 100 [ns]

(2) Setting PWM Duty to 100% or 0%

Figure 5 shows the PWM output waveforms in reset-synchronized PWM mode when the setting value of PWM duty register TGRB_3 is H'0000 or when it matches the setting of cycle register TGRA_3.

When the setting value of PWM duty register TGRB_3 is H'0000 in reset-synchronized PWM mode, the PWM output is a pulse waveform with a duration equal to 1 count of timer counter TCNT. When the setting value of duty register TGRB_3 is equal to or greater than that of cycle register TGRA_3, the PWM output toggles between high and low once every PWM cycle.

It is not possible to set the PWM duty to 100% or 0%, that is fixed high-level or low-level PWM output, by changing the setting value of the PWM duty register. To fix the PWM output level high or low, change the pin function select setting in the pin function controller (PFC) from timer pin (PWM output pin) to port output pin, thereby fixing the output signal level.

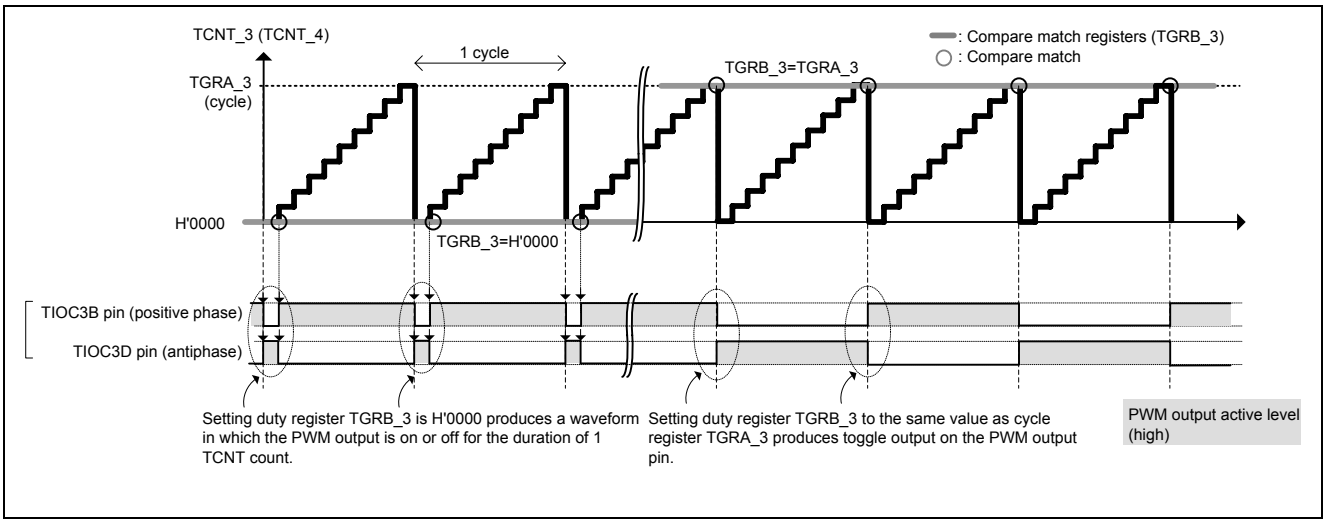


Figure 5 Duty Register Setting Values and PWM Output Waveforms

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 5 lists the functions used in the sample program.

Table 5 Functions Used

Function Name	Label	Description
Main	main ()	Makes initial settings for each module and makes timer start settings for multi-function timer pulse unit 2 (MTU2).
Standby setting	stbcr_init ()	Cancels MTU2 module standby.
MTU2 initial setting	mtu2_init ()	Makes MTU2 (channels 3 and 4) initial settings. Specifies reset-synchronized PWM mode.
PFC initial setting	pfc_init ()	Makes initial settings for the pin function controller (PFC). Sets MTU2-related pins to timer pin function.
TGRA_3 interrupt	int_mtu2_tgia3 ()	Handler for the MTU2 (channel 3) TGRA_3 compare match interrupt. Updates the three-phase PWM duty setting values.

2.3.2 Variable Usage

Table 6 lists the functions used by the sample program.

Table 6 Variable Usage

Label Name	Description	Name of Employing Module
C_cycle	PWM carrier cycle setting value (TGRC_3 register setting value)	• mtu2_init ()
Pul_pwm_duty1	PWM1 output (TIOC3B pin and TIOC3D pin) PWM duty setting value (TGRD_3 register setting value)	• mtu2_init () • int_mtu2_tgia3 ()
Pul_pwm_duty2	PWM2 output (TIOC4A pin and TIOC4C pin) PWM duty setting value (TGRD_3 register setting value)	
Pul_pwm_duty3	PWM3 output (TIOC4B pin and TIOC4D pin) PWM duty setting value (TGRD_4 register setting value)	

2.4 Procedure for Setting the Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 6 shows the flow of processing by the main function.

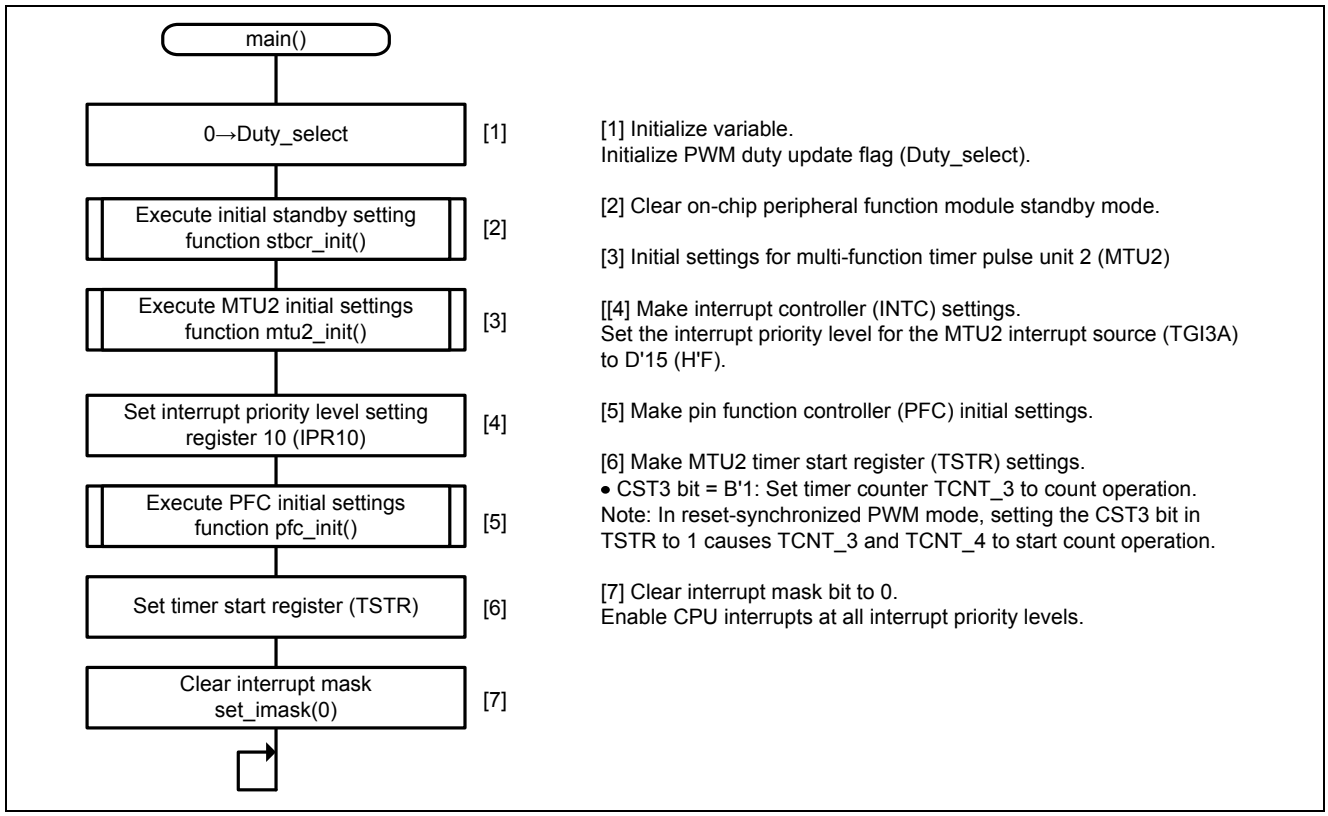


Figure 6 Processing by Function main

2.4.2 Setting to Release the Module from Standby

Figure 7 shows the flow of processing for release of the module from standby.

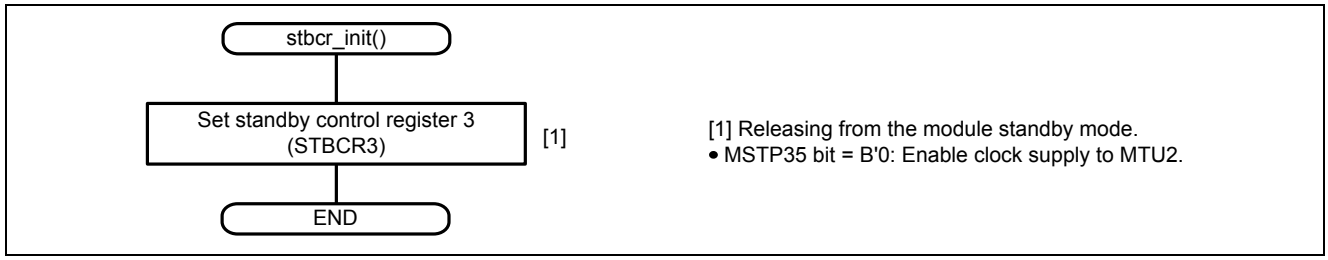


Figure 7 Setting for Release of the Module from Standby

2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 8 shows the processing sequence of the function that makes initial settings for multi-function timer pulse unit 2 (MTU2). Channels 3 and 4 of are set to reset-synchronized PWM mode.

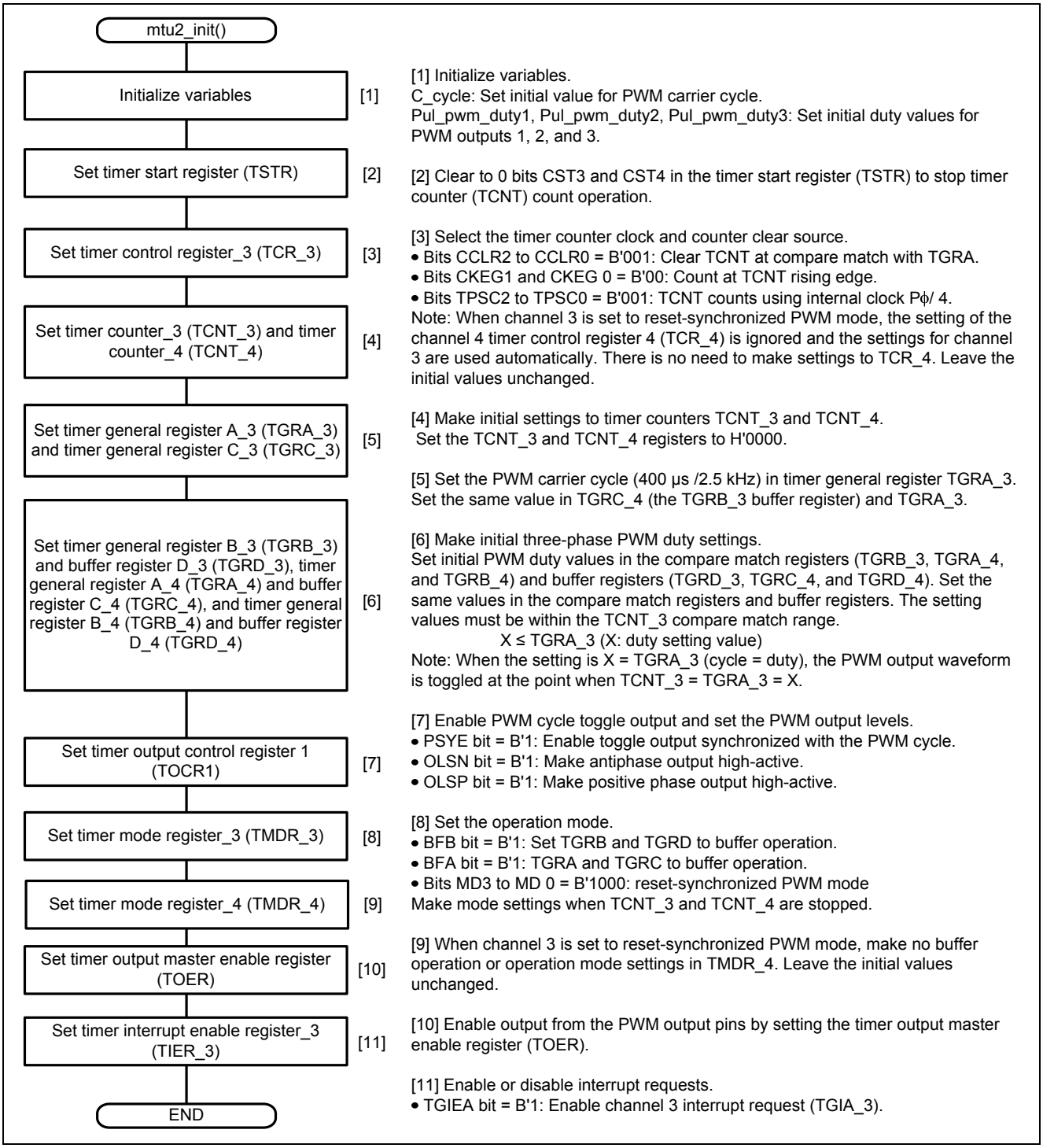
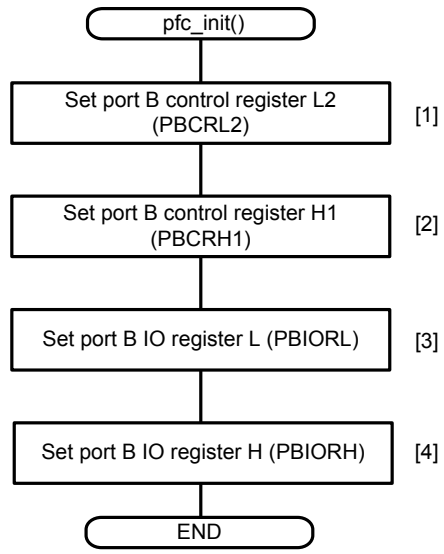


Figure 8 Initialization of MTU2

2.4.4 Initialization of Pin Function Controller (PFC)

Figure 9 shows the processing sequence of the function that makes settings for the pin function controller (PFC).



[1] Set port B multiplexed pin functions.
- PB7MD2 to PB7MD0 = B'100: Set PB7 to TIOC4D pin function (MTU2).
- PB6MD2 to PB6MD0 = B'100: Set PB6 to TIOC4C pin function (MTU2).
- PB5MD2 to PB5MD0 = B'100: Set PB5 to TIOC4B pin function (MTU2).
- PB4MD2 to PB4MD0 = B'100: Set PB4 to TIOC4A pin function (MTU2).

[2] Set port B multiplexed pin functions.
- PB19MD2 to PB19MD0 = B'100: Set PB19 to TIOC3D pin function (MTU2).
- PB18MD2 to PB18MD0 = B'100: Set PB18 to TIOC3B pin function (MTU2).
- PB17MD2 to PB17MD0 = B'100: Set PB17 to TIOC3A pin function (MTU2).

[3] Set port B pin (PB15 to PB0) I/O directions.
- PB7IOR bit = B'1: Set TIOC4D pin (PB7) to output.
- PB6IOR bit = B'1: Set TIOC4C pin (PB6) to output.
- PB5IOR bit = B'1: Set TIOC4B pin (PB5) to output.
- PB4IOR bit = B'1: Set TIOC4A pin (PB4) to output.

[4] Set port B pin (PB30 to PB16) I/O directions.
- PB19IOR bit = B'1: Set TIOC3D pin (PB19) to output.
- PB18IOR bit = B'1: Set TIOC3B pin (PB18) to output.
- PB17IOR bit = B'1: Set TIOC3A pin (PB17) to output.

Figure 9 Initialization of PFC

2.4.5 Handling of the Compare Match Interrupt on Channel 3

Figure 10 shows the processing sequence for the compare match interrupt (TGRA_3) of MTU2 (channel 3).

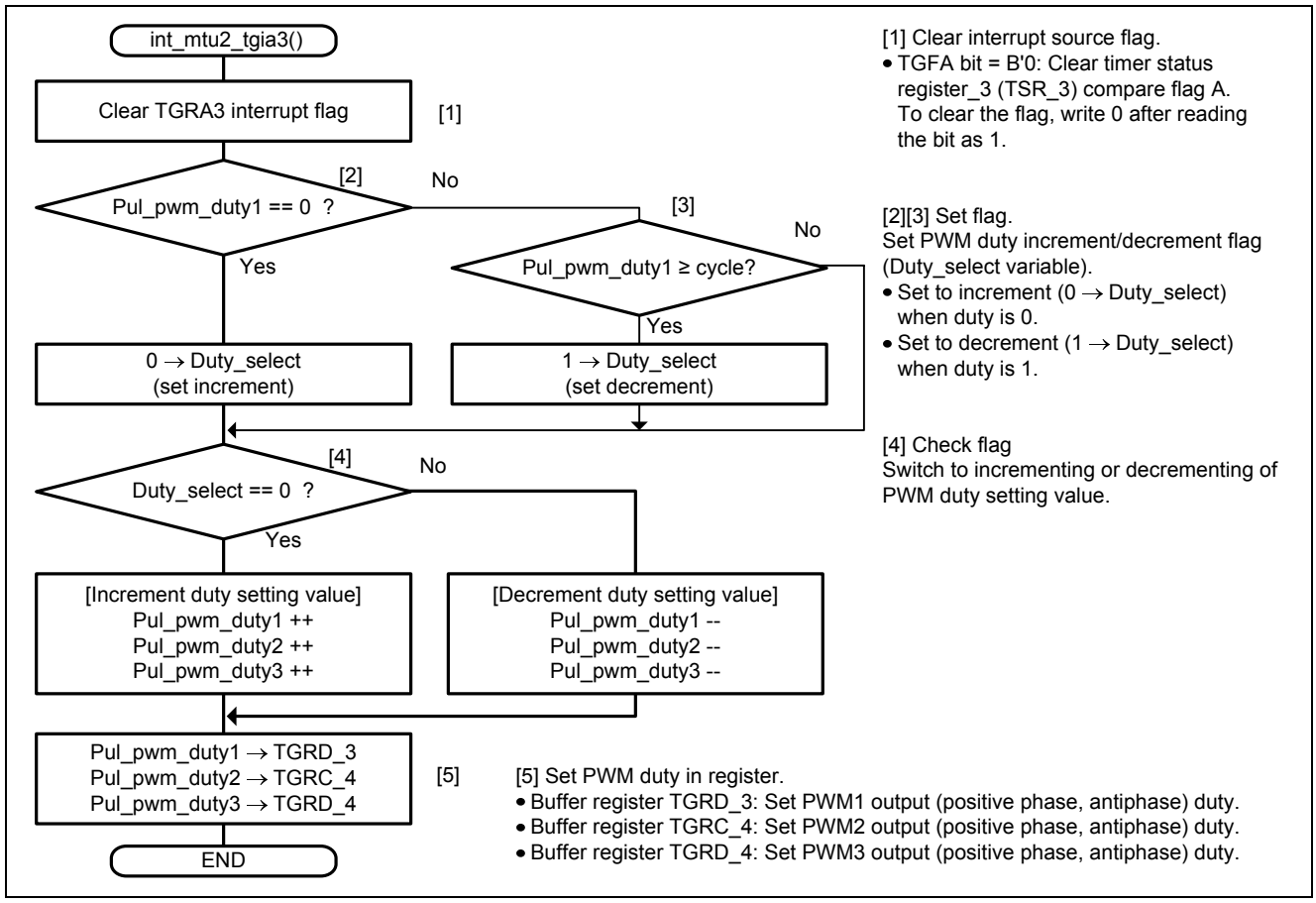


Figure 10 Handling the Compare Match (TGRA_3) Interrupt from Channel 3 of MTU2

2.5 Settings of Registers in the Sample Program

The register setting values used in the sample program are shown below.

2.5.1 Clock Pulse Generator (CPG)

Table 7 shows the register settings for the clock pulse generator (CPG).

Table 7 Clock Pulse Generator (CPG)

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	Specifies the clock output settings and operating frequency multiplication ratios. • CKOEN = B'1: Fix CK pin low level. • STC1 and STC0 = B'11: PLL circuit 1 × 2 • IFC2 to IFC0 = B'000: Internal clock (Iϕ) × 1 • RNGS = B'0: High-frequency mode • PFC2 to PFC0 = B'011: Peripheral clock (Pϕ) × 1/4

2.5.2 Power-Down Modes

Table 8 shows the register settings for low-power mode.

Table 8 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE0408	H'5E	Specifies the operation settings for individual modules. • HIZ= B'0: Maintain pin state in software standby mode. • MSTP36 = B'1: Stop clock supply to MTU2S. • MSTP35 = B'0: Operate MTU2. • MSTP34 = B'1: Stop clock supply to POE2. • MSTP33 = B'1: Stop clock supply to IIC3. • MSTP32 = B'1: Stop clock supply to ADC. • MSTP31 = B'1: Stop clock supply to DAC. • MSTP30 = B'0: Operate flash memory.

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 9 shows the register settings for multi-function timer pulse unit 2 (MTU2).

Table 9 Multi-Function Timer Pulse Unit 2 (MTU2)

Register Name	Address	Setting	Description
Timer control register_3 (TCR_3)	H'FFFE4200	H'21	TCNT control settings • CCLR2 to CCLR0 = B'001: Clear TCNT at TGRA compare match. • CKEG1 and CKEG0 = B'00: Count at rising edge. • TPSC2 to TPSC0 = B'001: TCNT counts using internal clock Pϕ / 4.
Timer control register_4 (TCR_4)	H'FFFE4201	—	TCNT control settings When channel 3 is set to reset-synchronized PWM mode, the settings for channel 4 are ignored and the settings for channel 3 are used automatically. Make no settings to this register. Leave the initial values unchanged.
Timer counter_3 (TCNT_3)	H'FFFE4210	H'0000	16 bit counter Set the initial value to 0.
Timer counter_4 (TCNT_4)	H'FFFE4212	H'0000	16 bit counter Set the initial value to 0.
Timer general register A_3 (TGRA_3)	H'FFFE4218	D'3999	TCNT_3 upper limit setting This sets the PWM carrier cycle. During operation, the buffer register is used to update the cycle setting.
Timer general register C_3 (TGRC_3)	H'FFFE4224		TGRA_3 buffer register Set the initial value to match the setting value of the TGRA_3 register.
Timer general register B_3 (TGRB_3)	H'FFFE421A	D'1999	PWM output 1 compare register This sets the PWM duty (initial output value). During operation, the buffer register is used to update the PWM duty setting.
Timer general register D_3 (TGRD_3)	H'FFFE4226		TGRB_3 buffer register Set the initial value to match the setting value of the TGRB_3 register.
Timer general register A_4 (TGRA_4)	H'FFFE421C	D'1999	PWM output 2 compare register This sets the PWM duty (initial output value). During operation, the buffer register is used to update the PWM duty setting.
Timer general register C_4 (TGRC_4)	H'FFFE4228		TGRA_4 buffer register Set the initial value to match the setting value of the TGRA_4 register.

Register Name	Address	Setting	Description
Timer general register B_4 (TGRB_4)	H'FFFE421E	D'1999	PWM output 3 compare register This sets the PWM duty (initial output value). During operation, the buffer register is used to update the PWM duty setting.
Timer general register D_4 (TGRD_4)	H'FFFE422A		TGRB_4 buffer register Set the initial value to match the setting value of the TGRB_4 register.
Timer output control register 1 (TOCR1)	H'FFFE420E	H'43	Output control in reset-synchronized PWM mode • PSYE = B'1: Enable toggle output synchronized with the PWM cycle. • TOCL = B'0: Enable writing to the TOCS, OLSN, and OLSP bits. • TOCS = B'0: Enable TOCR1 setting. • OLSN = B'1: In reset-synchronized PWM mode, select the antiphase output level: Initial output = low, active level = high. • OLSP = B'1: In reset-synchronized PWM mode, select the positive phase output level: Initial output = low, active level = high.
Timer mode register_3 (TMDR_3)	H'FFFE4202	H'38	Operation mode settings (channel 3) • BFB = B'1: Set TGRB and TGRD to buffer operation. • BFA = B'1: Set TGRA and TGRC to buffer operation. • MD3 to MD0 = B'1000: Reset-synchronized PWM mode
Timer mode register_4 (TMDR_4)	H'FFFE4203	H'00 (Initialize)	Operation mode settings (channel 4) When channel 3 is set to reset-synchronized PWM mode, the settings for channel 4 are ignored and the settings for channel 3 are used automatically. Leave the initial settings for this register unchanged. The settings of Bits BFA and BFB in TMDR_4 may also be left at 0, even when buffer operation is used.
Timer output master enable register (TOER)	H'FFFE420A	H'FF	MTU2 output pin output enable/disable settings • OE4D = B'1: Enable MTU2 output on TIOC4D pin. • OE4C = B'1: Enable MTU2 output on TIOC4C pin. • OE3D = B'1: Enable MTU2 output on TIOC3D pin. • OE4B = B'1: Enable MTU2 output on TIOC4B pin. • OE4A = B'1: Enable MTU2 output on TIOC4A pin. • OE4B = B'1: Enable MTU2 output on TIOC3B pin.

Register Name	Address	Setting	Description
Timer interrupt enable register_3 (TIER_3)	H'FFFE4208	H'01	Interrupt request enable/disable control • TGIEA= B'1: Enable interrupt requests (TGIA) by TGFA bit.
Timer start register (TSTR)	H'FFFE4280	H'40	TCNT start/stop select for channels 0 to 4 • CST3 = B'1: Start TCNT_3 count operation. Stop count operation by TCNT_2, TCNT_1, and TCNT_0. Note: In reset-synchronized PWM mode, setting the CST3 bit in TSTR to 1 causes count operation by TCNT_3 (channel 3) and TCNT_4 (channel 4) to start. There is no need to make the count operation setting (CST4 = B'1) for TCNT_4 (channel 4).

2.5.4 Interrupt Controller (INTC)

Table 10 shows the register settings for the interrupt controller (INTC).

Table 10 Interrupt Controller (INTC)

Register Name	Address	Setting	Description
Interrupt priority level setting register 10 (IPR10)	H'FFFE0C08	H'00F0	Sets interrupt priority levels (level 0 to 15). • Bits 15 to 12 = B'0000: MTU2 (TGI2A and TGI2B) interrupt level = 0 • Bits 11 to 8 = B'0000: MTU2 (TCI2V and TCI2U) interrupt level = 0 • Bits 7 to 4 = B'1111: MTU3 (TGI3A to TGI3D) interrupt level = 15 • Bits 3 to 0 = B'0000: MTU3 (TCI3V) interrupt level = 0 The TGI3A interrupt is used by the reference program.

2.5.5 Pin Function Controller (PFC)

Table 11 shows the register settings for the pin function controller (PFC).

Table 11 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port B control register L2 (PBCRL2)	H'FFFE3894	H'4444	Sets port B multiplexed pin functions. • PB7MD2 to PB7MD0 = B'100: Set PB7 to TIOC4D I/O (MTU2). • PB6MD2 to PB6MD0 = B'100: Set PB6 to TIOC4C I/O (MTU2). • PB5MD2 to PB5MD0 = B'100: Set PB5 to TIOC4B I/O (MTU2). • PB4MD2 to PB4MD0 = B'100: Set PB4 to TIOC4A I/O (MTU2).
Port B control register H1 (PBCRH1)	H'FFFE388E	H'4440	Sets port B multiplexed pin functions. • PB19MD2 to PB19MD0 = B'100: Set PB19 to TIOC3D I/O (MTU2). • PB18MD2 to PB18MD0 = B'100: Set PB18 to TIOC3B I/O (MTU2). • PB17MD2 to PB17MD0 = B'100: Set PB17 to TIOC3A I/O (MTU2). • PB16MD2 to PB16MD0 = B'000: Set PB16 (port) as an input pin.
Port B I/O register H (PBIORH)	H'FFFE3884	H'000E	Sets port B pin I/O directions. • PB19IOR = B'1: Set PB19 (TIOC3D) as an output pin. • PB18IOR = B'1: Set PB18 (TIOC3B) as an output pin. • PB17IOR = B'1: Set PB17 (TIOC3A) as an output pin. • PB16IOR = B'0: Set PB16 (port) as an input pin. Set all the others to B'0: All input pins.
Port B I/O register L (PBIORL)	H'FFFE3886	H'00F0	Sets port B pin I/O directions. • PB7IOR = B'1: Set PB7 (TIOC4D) as an output pin. • PB6IOR = B'1: Set PB6 (TIOC4C) as an output pin. • PB5IOR = B'1: Set PB5 (TIOC4B) as an output pin. • PB4IOR = B'1: Set PB4 (TIOC4A) as an output pin. Set all the others to B'0: All input pins.

3. Documents for Reference

- Hardware Manual
  SH7211 Group Hardware Manual [RJJ09B0338]
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Software Manual
  SH-2A/SH2A-FPU Software Manual [RJJ09B0086]
  (The latest version can be downloaded from the Renesas Technology Web site.)

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.16.09	—	First edition issued

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life

   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.