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April 1st, 2010
Renesas Electronics Corporation

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SH7145 Group Interface Volume

Application Note

Renesas 32-Bit RISC

Microcomputer

SuperH™ RISC engine Family/

SH7144 Series

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.

The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.

Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.

The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.

The undefined or reserved addresses may be used to expand functions, or test registers may have been allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

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Section 1 SH7145 Application Note—Interface Volume Usage Guide

This Application Note consists of two parts, as shown in figure 1.1.

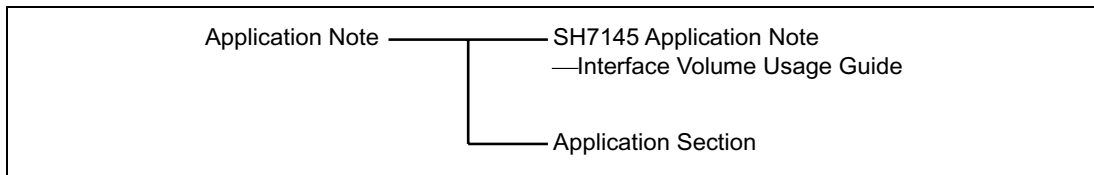


Figure 1.1 Organization of Application Note

(1) SH7145 Application Note—Interface Volume Usage Guide

This section explains how to use the SH7145 Application Note—Interface Volume Usage Guide.

(2) Application Section

The use of the SH7145 with a bus state controller (BSC) is explained based on simple sample tasks.

1.1 Organization of Application Section

The layout shown in figure 1.2 is used to describe the combined use of on-chip peripheral functions.

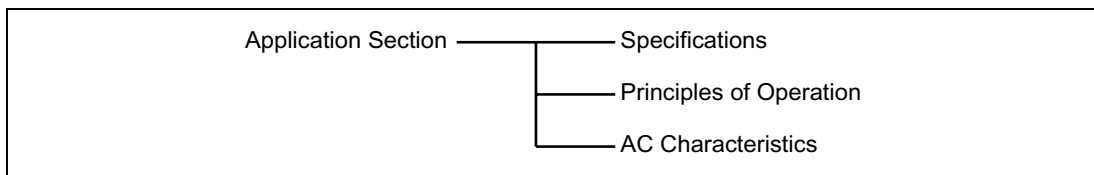


Figure 1.2 Organization of Application Section

(1) Specifications

Describes the system specifications of the sample task.

(2) Principles of Operation

Describes the operation of the sample task, using timing charts.

(3) AC Characteristics

Section 2 Application Section

2.1 4-Mbit (512-kbit × 8) SRAM Interface

SRAM (HM62W8511HC-10) Interface	MCU: SH7145	Functions Used: Bus State Controller (BSC)
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Specifications

(1) SH7145 mode 2 (on-chip ROM-enabled expansion mode) is used to interface with 4 Mbits (512 kbits × 8) of SRAM (HM62W8511HC-10) as shown in figure 2.1.

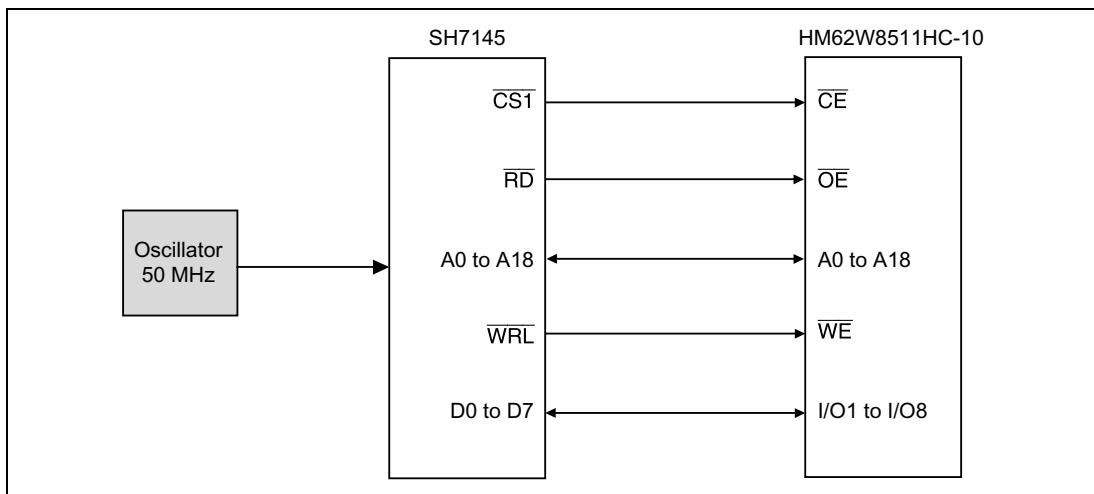


Figure 2.1 SH7145 and HM62W8511HM-10 Connection Block Diagram

(2) Of the memory on the SH7145, area 1 (H'00400000 to H'007FFFFFFF) is allocated, as shown in figure 2.2.

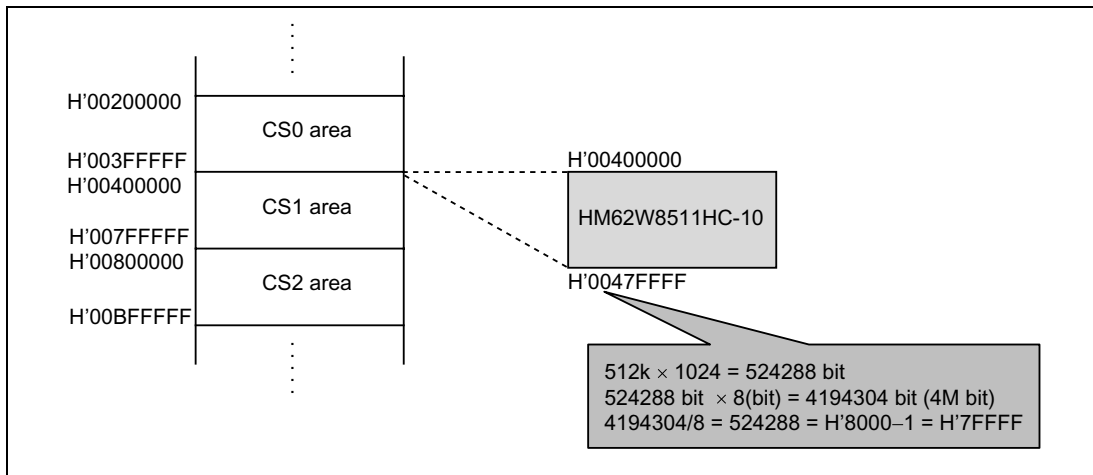


Figure 2.2 Memory Map

(3) The registers of the bus state controller are set to the values listed in table 2.1.

Table 2.1 Register Setting Values

CS1 Space Conditions		Register	Setting Value
Bus size	Byte size	BCR1	H'600d
Idle cycles	None	BCR2	H'0000
Wait states	1 wait state (CS1 space)	WCR1	H'ff1f

Principles of Operation

(1) SH7145 Basic Bus Cycle (1 Software Wait State)

Figure 2.3 illustrates the basic bus cycle of the SH7145 with one software wait state. As shown in figure 2.3, interfacing with the external device (HM62W8511HC-10) takes place in three states. During the data read operation of the SH7145 data is sampled from D0 to D7 at the rising edge of T_2 . For data writes, data is output after the falling edge of T_1 following a delay of t_{WDD} (write data delay time). For timing chart values, refer to the AC characteristics bus timing table.

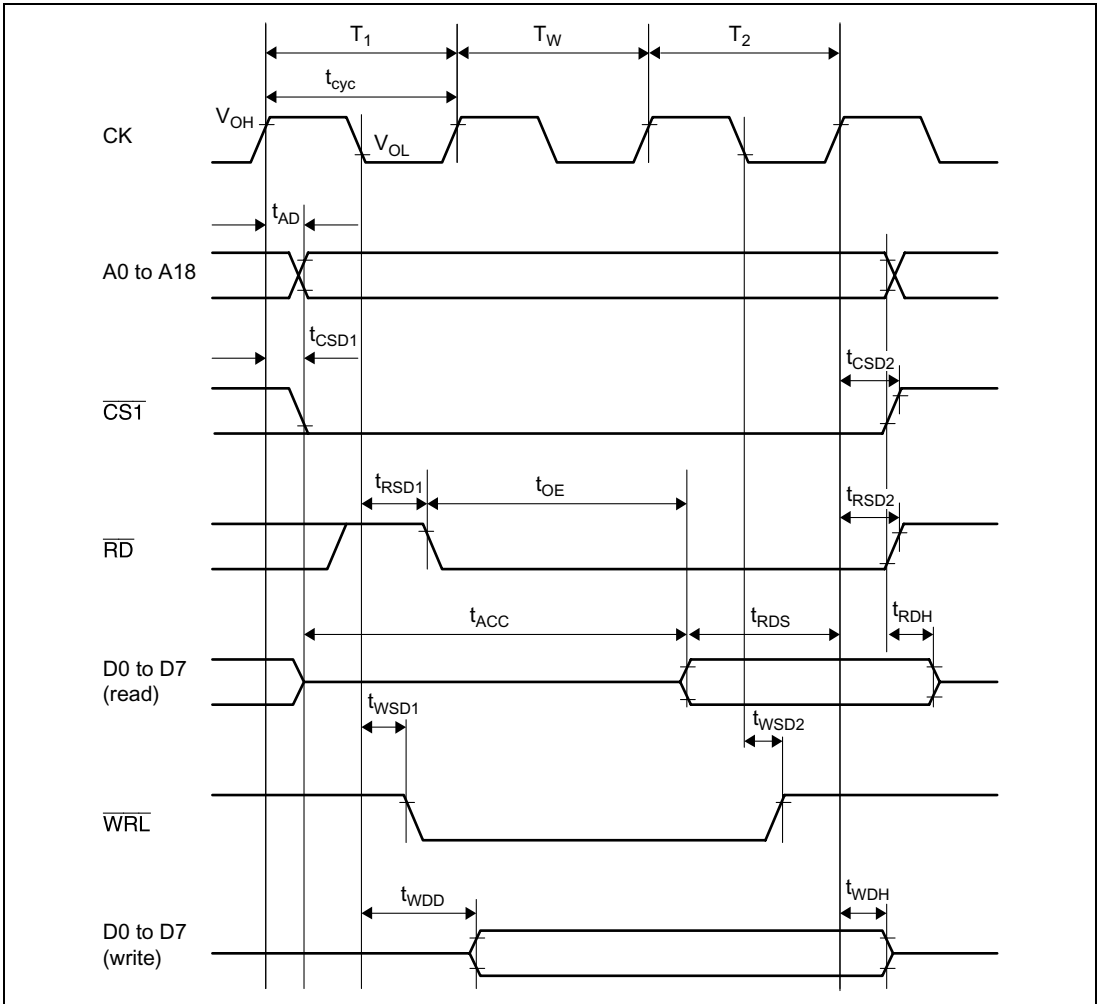


Figure 2.3 SH7145 Basic Bus Cycle (1 Software Wait State)

(2) Reading and Writing Data

Figure 2.4 is a timing chart for data read and write operations. If the SH7145 is connected directly to the HM62W8511HC-10 it is important to make sure that the t_{ACC} (read data access time), t_{OE} (access time from read strobe), and t_{RDH} (read data hold time) of the SH7145 and the t_{DW} (input data set time), t_{DH} (input data hold time), and t_{WP} (write pulse width) of the HM62W8511HC-10 are all satisfied. Operation of the SH7145 has been verified using a system clock of $\phi = 50$ MHz ($t_{cyc} = 20$ ns). Based on figure 2.4, the timing values are as follows.

(a) t_{ACC} and t_{OE} of SH7145

$$\begin{aligned} t_{ACC} &= t_{ACS}(\max) && n: \text{Wait states} = 1 \text{ wait state} \\ &= 10\text{ns} \leq 20\text{ns} \text{ (SH7145 } t_{ACC} = t_{cyc} \times (n+2) - 40) \end{aligned}$$

$$\begin{aligned} t_{OE} &= t_{OE}(\max) \\ &= 5\text{ns} \leq 7\text{ns} \text{ (SH7145 } t_{OE} = t_{cyc} \times (n+1.5) - 43) \end{aligned}$$

(b) t_{RDH} of SH7145

$$\begin{aligned} t_{RDH} &= t_{OH}(\min) \\ &= 3\text{ns} \geq 0\text{ns} \text{ (SH7145 } t_{RDH}) \end{aligned}$$

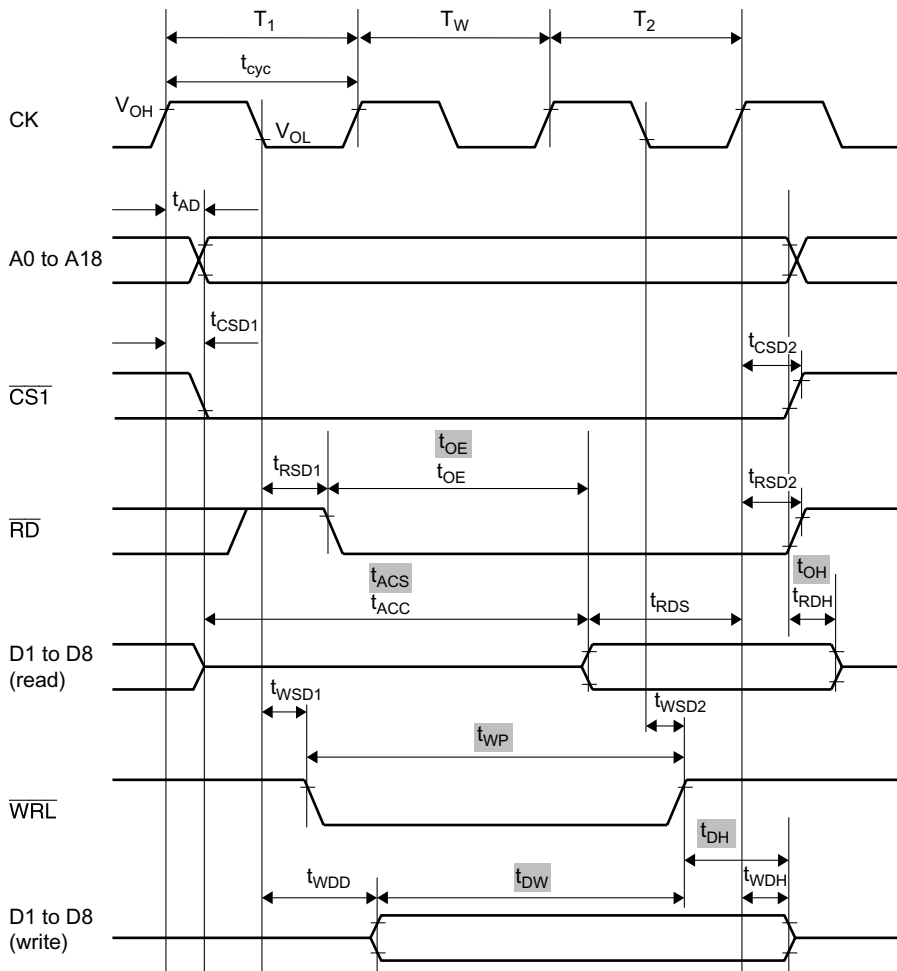
(c) t_{DW} and t_{DH} of HM62W8511HC-10

$$\begin{aligned} t_{DW} &= t_{cyc} \times (n+1) - t_{WDD}(\max) + t_{WSD2}(\max) \\ &= 20 \times (1+1) - 35 + 25 \\ &= 30\text{ns} \geq 5\text{ns} \text{ (HM62W8511HC-10 } t_{DW}) \end{aligned}$$

$$\begin{aligned} t_{WDH} &= t_{DH} \\ &= 0\text{ns} \geq 0\text{ns} \text{ (HM62W8511HC-10 } t_{DH}) \end{aligned}$$

(d) t_{WP} of HM62W8511HC-10

$$\begin{aligned} t_{WP} &= t_{cyc} \times (n+1) - t_{WSD1}(\max) + t_{WSD2}(\max) \\ &= 20 \times (1+1) - 25 + 25 \\ &= 40\text{ns} \geq 7\text{ns} \text{ (HM62W8511HC-10 } t_{WP}) \end{aligned}$$



■ : AC characteristics of HM62W8511HC-10

Figure 2.4 Read/Write Timing Chart

AC Characteristics

(1) AC Characteristics of SH7145

Table 2.2 Bus Timing

Conditions: $V_{cc} = PLLV_{cc} = 3.3\text{ V} \pm 0.3\text{ V}$, $AV_{cc} = 3.3\text{ V} \pm 0.3\text{ V}$, $AV_{cc} = V_{cc} \pm 0.3\text{ V}$,
 $AV_{ref} = 3.0 - AV_{cc}$, $V_{ss} = PLLV_{ss} = AV_{cc} = 0\text{ V}$

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	25	ns
\overline{CS} delay time 1	t_{CSD1}	—	28	ns
\overline{CS} delay time 2	t_{CSD2}	—	28	ns
Read strobe delay time 1	t_{RSD1}	—	25	ns
Read strobe delay time 2	t_{RSD2}	—	25	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
Write strobe delay time 1	t_{WSD1}	—	25	ns
Write strobe delay time 2	t_{WSD2}	—	25	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	0	—	ns
\overline{WAIT} setup time	t_{WTS}	12	—	ns
\overline{WAIT} hold time	t_{WTH}	3	—	ns
Read data access time	t_{ACC}	$t_{cyc} \times (n+2) - 35$	—	ns
Access time from read strobe	t_{OE}	$t_{cyc} \times (n+1.5) - 33$	—	ns
Write data hold time	t_{WRH}	0	—	ns

Note: n indicates number of wait states.

(2) AC Characteristics of HM62W8511HC-10

(a) Read Cycle

Table 2.3 Read Cycle AC Characteristics

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	10	—	ns
Address access time	t_{AA}	—	10	ns
Chip select access time	t_{ACS}	—	10	ns
\overline{CS} set time	t_{CLZ}	3	—	ns
Output enable access time	t_{OE}	—	5	ns
Output enable/output set time	t_{OLZ}	0	—	ns
Chip deselect/output floating time	t_{CHZ}	—	5	ns
Output disable/output floating time	t_{OHZ}	—	5	ns
Output hold time	t_{OH}	3	—	ns

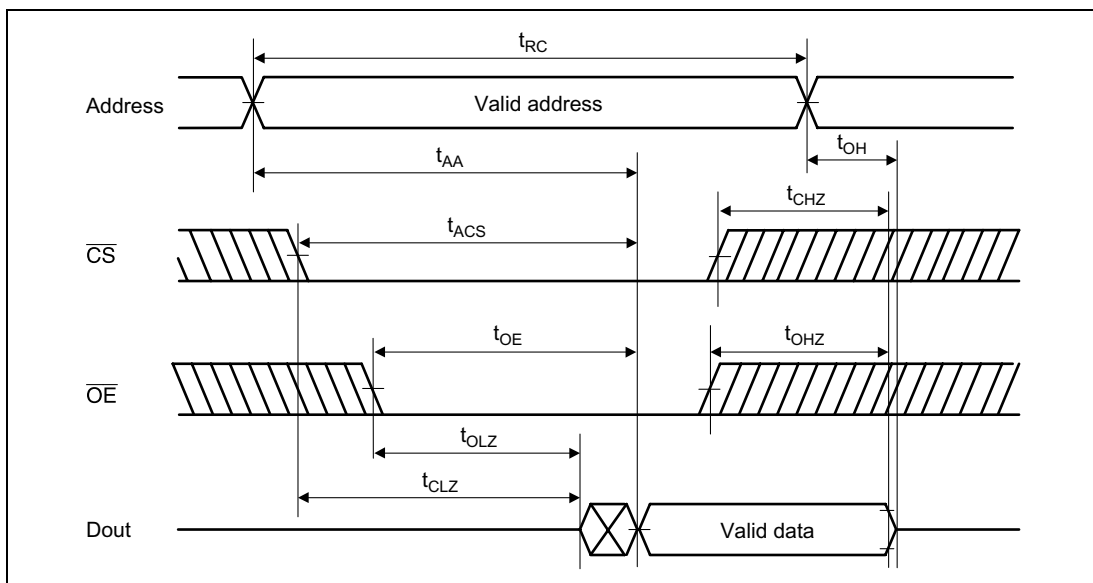


Figure 2.5 Read Cycle Waveforms

(b) Write Cycle

Table 2.4 Write Cycle AC Characteristics

Item	Symbol	Min	Max	Unit
Read cycle time	t_{WC}	10	—	ns
Chip select time	t_{CW}	7	—	ns
Address valid time	t_{AW}	7	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	7	—	ns
Address hold time	t_{WR}	0	—	ns
Output disable/output floating time	t_{OHZ}	—	5	ns
\overline{WE} output floating time	t_{WHZ}	—	5	ns
Input data set time	t_{DW}	5	—	ns
Input data hold time	t_{DH}	0	—	ns
\overline{WE} output set time	t_{OW}	3	—	ns

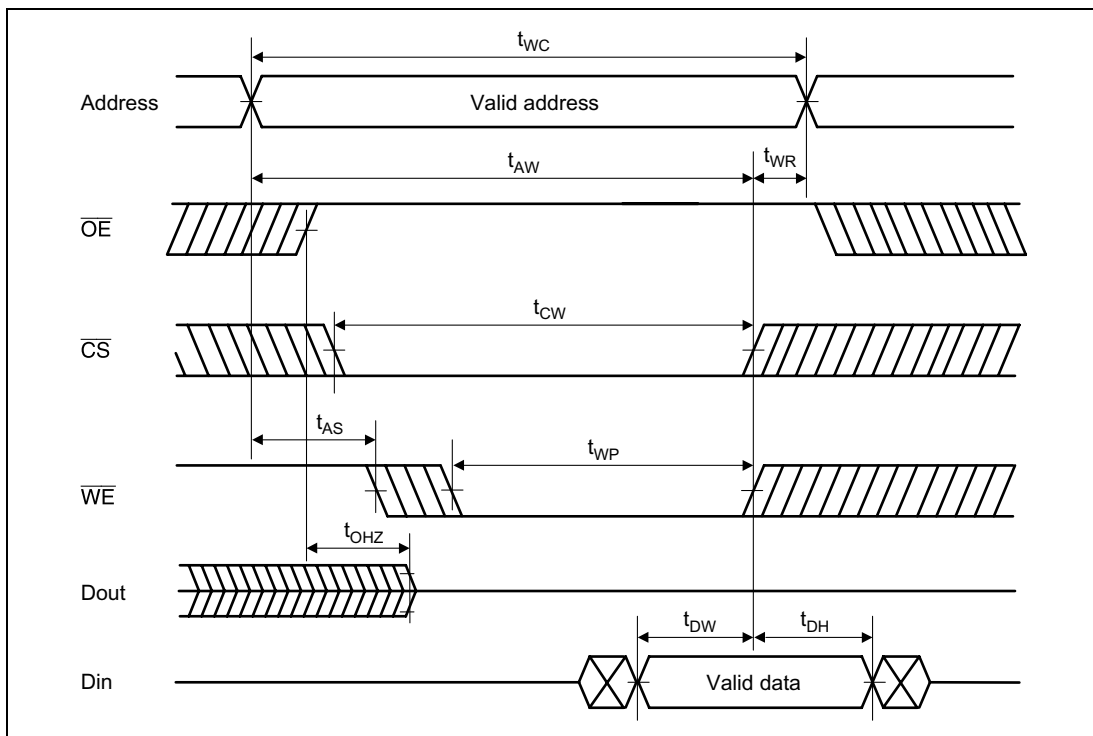


Figure 2.6 Write Cycle Waveforms

2.2 4-Mbit (256-kbit × 16) SRAM Interface

SRAM (HM62W16255HCJP-10) Interface	MCU: SH7145	Functions Used: Bus State Controller (BSC)
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Specifications

(1) SH7145 mode 2 (on-chip ROM-enabled expansion mode) is used to interface with 4 Mbits (256 kbits × 16) of SRAM (HM62W16255HCJP-10) as shown in figure 2.7.

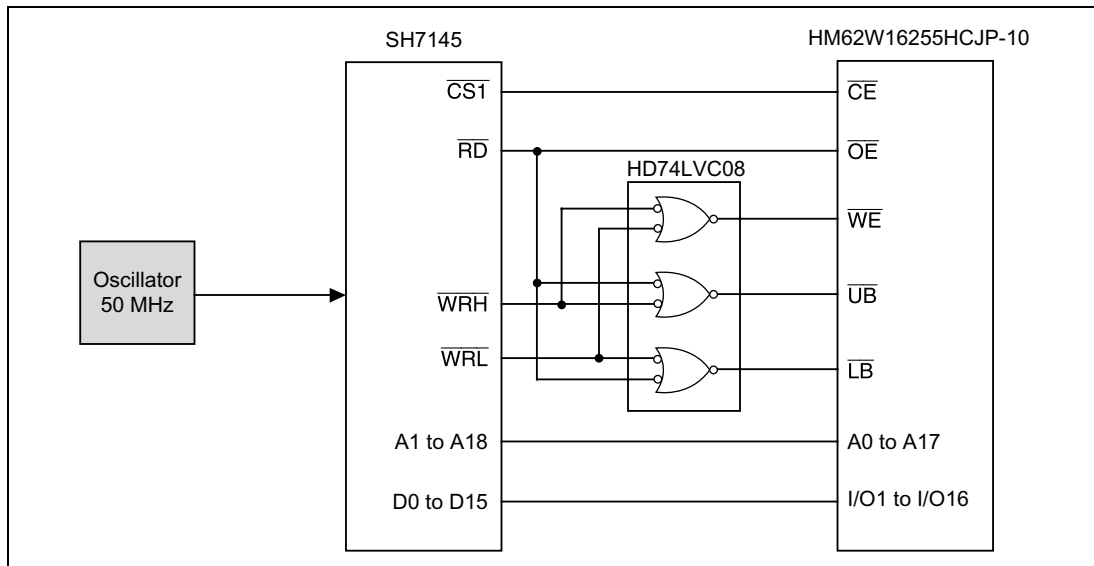


Figure 2.7 SH7145 and HM62W16255HCJP-10 Connection Block Diagram

(2) Of the memory on the SH7145, area 1 (H'00400000 to H'007FFFFFFF) is allocated, as shown in figure 2.8.

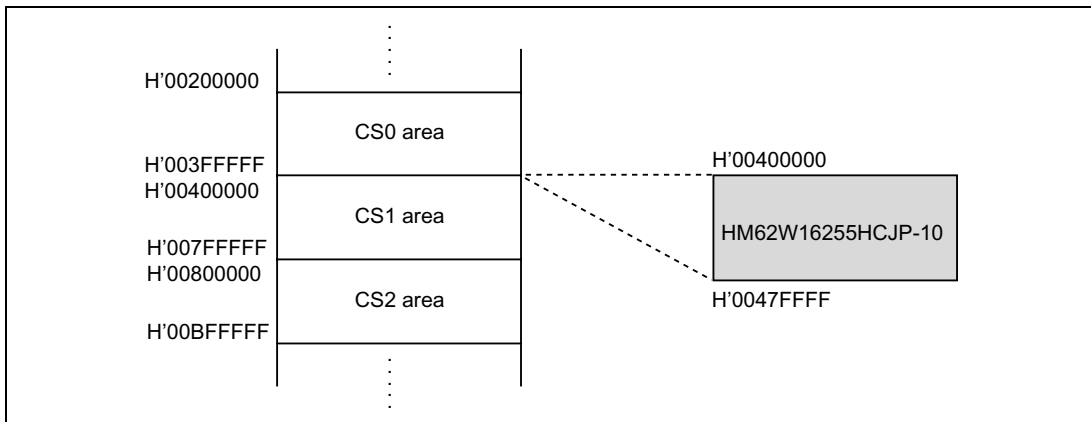


Figure 2.8 Memory Map

(3) The registers of the bus state controller are set to the values listed in table 2.5.

Table 2.5 Register Setting Values

CS1 Space Conditions		Register	Setting Value
Bus size	Word size	BCR1	H'600f
Idle cycles	None	BCR2	H'0000
Wait states	1 wait state (CS1 space)	WCR1	H'ff1f

Principles of Operation

(1) SH7145 Basic Bus Cycle (1 Software Wait State)

Figure 2.9 illustrates the basic bus cycle of the SH7145 with one software wait state. As shown in figure 2.9, interfacing with the external device (HM62W16255HCJP-10) takes place in three states. During the data read operation of the SH7145 data is sampled from D0 to D7 at the rising edge of T_2 . For data writes, data is output after the falling edge of T_1 following a delay of t_{WDD} (write data delay time). For timing chart values, refer to the AC characteristics bus timing table.

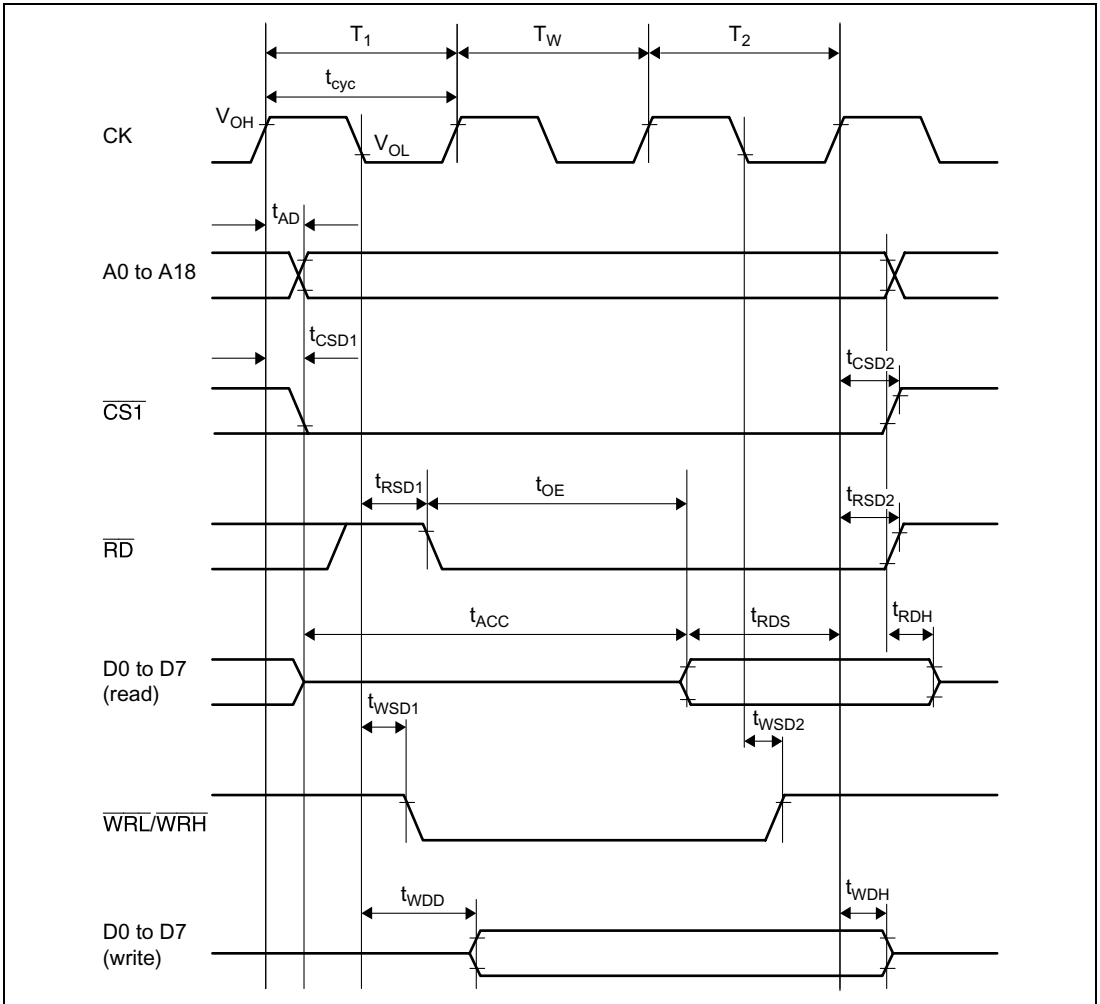


Figure 2.9 SH7145 Basic Bus Cycle (1 Software Wait State)

(1) Reading and Writing Data

Figure 2.10 is a timing chart for data read and write operations. If the SH7145 is connected directly to the HM62W16255HCJP-10 it is important to make sure that the t_{ACC} (read data access time), t_{OE} (access time from read strobe), and t_{RDH} (read data hold time) of the SH7145 and the t_{DW} (input data set time), t_{DH} (read data hold time), and t_{WP} (write pulse width) of the HM62W16255HCJP-10 are all satisfied. Operation of the SH7145 has been verified using a system clock of $\phi = 50$ MHz ($t_{cyc} = 20$ ns). Based on figure 2.10, the timing values are as follows.

(a) t_{ACC} and t_{OE} of SH7145

$$t_{ACC} = t_{ACS}(\max) \quad n: \text{Wait states} = 1 \text{ wait state}$$

$$\begin{aligned} t_{ACC} &= t_{cyc} \times (n+2) - 40 \\ &= 10\text{ns} \leq 20\text{ns} \text{ (SH7145 } t_{ACC}) \end{aligned}$$

$$\begin{aligned} t_{OE} &= t_{cyc} \times (n+1.5) - 43 \\ &= 5\text{ns} \leq 7\text{ns} \text{ (SH7145 } t_{OE}) \end{aligned}$$

(b) t_{RDH} of SH7145

$$\begin{aligned} t_{RDH} &= t_{OH}(\min) \\ &= 3\text{ns} \geq 0\text{ns} \text{ (SH7145 } t_{RDH}) \end{aligned}$$

(c) t_{DW} and t_{DH} of HM62W16255HCJP-10

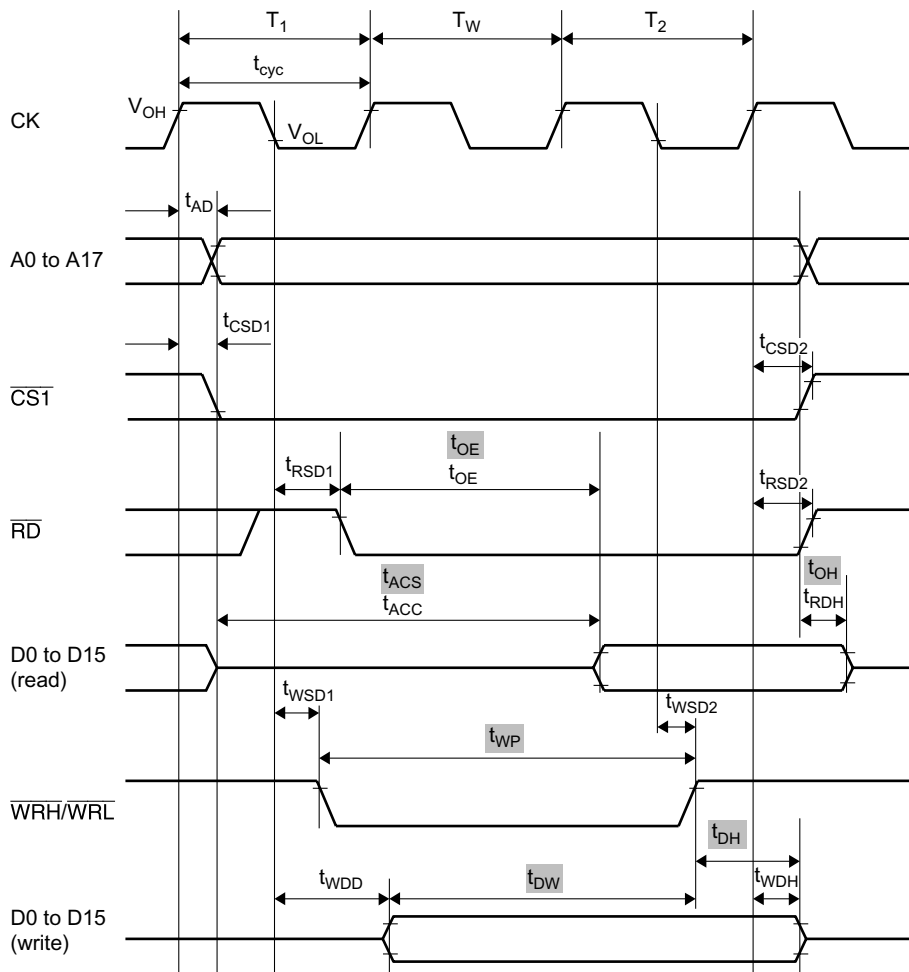
$$\begin{aligned} t_{DW} &= t_{cyc} \times (n+1) - t_{WDD}(\max) + t_{WSD2}(\max) \\ &= 20 \times (1+1) - 35 + 25 \\ &= 30\text{ns} \geq 5\text{ns} \text{ (HM62W16255HCJP-10 } t_{DW}) \end{aligned}$$

$$\begin{aligned} t_{WDH} &= t_{DH} \\ &= 0\text{ns} \geq 0\text{ns} \text{ (HM62W16255HCJP-10 } t_{DH}) \end{aligned}$$

(d) t_{WP} of HM62W16255HCJP-10

$$\begin{aligned} t_{WP} &= t_{cyc} \times (n+1) - t_{WSD1}(\max) + t_{WSD2}(\max) \\ &= 20 \times (1+1) - 25 + 25 \\ &= 40\text{ns} \geq 7\text{ns} \text{ (HM62W16255HCJP-10 } t_{WP}) \end{aligned}$$

HD74LVC08 propagation delay time = 6.0 ns (max.)



■ : AC characteristics of HM62W16255HCJP-10

Figure 2.10 Read/Write Timing Chart

AC Characteristics

(1) AC Characteristics of SH7145

Table 2.6 Bus Timing

Conditions: $V_{cc} = PLLV_{cc} = 3.3\text{ V} \pm 0.3\text{ V}$, $AV_{cc} = 3.3\text{ V} \pm 0.3\text{ V}$, $AV_{cc} = V_{cc} \pm 0.3\text{ V}$,
 $AV_{ref} = 3.0 - AV_{cc}$, $V_{ss} = PLLV_{ss} = AV_{ss} = 0\text{ V}$)

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	25	ns
\overline{CS} delay time 1	t_{CSD1}	—	28	ns
\overline{CS} delay time 2	t_{CSD2}	—	28	ns
Read strobe delay time 1	t_{RSD1}	—	25	ns
Read strobe delay time 2	t_{RSD2}	—	25	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
Write strobe delay time 1	t_{WSD1}	—	25	ns
Write strobe delay time 2	t_{WSD2}	—	25	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	0	—	ns
\overline{WAIT} setup time	t_{WTS}	12	—	ns
\overline{WAIT} hold time	t_{WTH}	3	—	ns
Read data access time	t_{ACC}	$t_{cyc} \times (n+2) - 35$	—	ns
Access time from read strobe	t_{OE}	$t_{cyc} \times (n+1.5) - 33$	—	ns
Write data hold time	t_{WRH}	0	—	ns

Note: n indicates number of wait states.

(2) AC Characteristics of HM62W16255HCJP-10

(a) Read Cycle

Table 2.7 Read Cycle AC Characteristics

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	10	—	ns
Address access time	t_{AA}	—	10	ns
Chip select access time	t_{ACS}	—	10	ns
\overline{CS} set time	t_{CLZ}	3	—	ns
Output enable access time	t_{OE}	—	5	ns
Output enable/output set time	t_{OLZ}	0	—	ns
Chip deselect/output floating time	t_{CHZ}	—	5	ns
Output disable/output floating time	t_{OHZ}	—	5	ns
Output hold time	t_{OH}	3	—	ns
Byte select time	t_{LB}, t_{UB}	—	5	ns

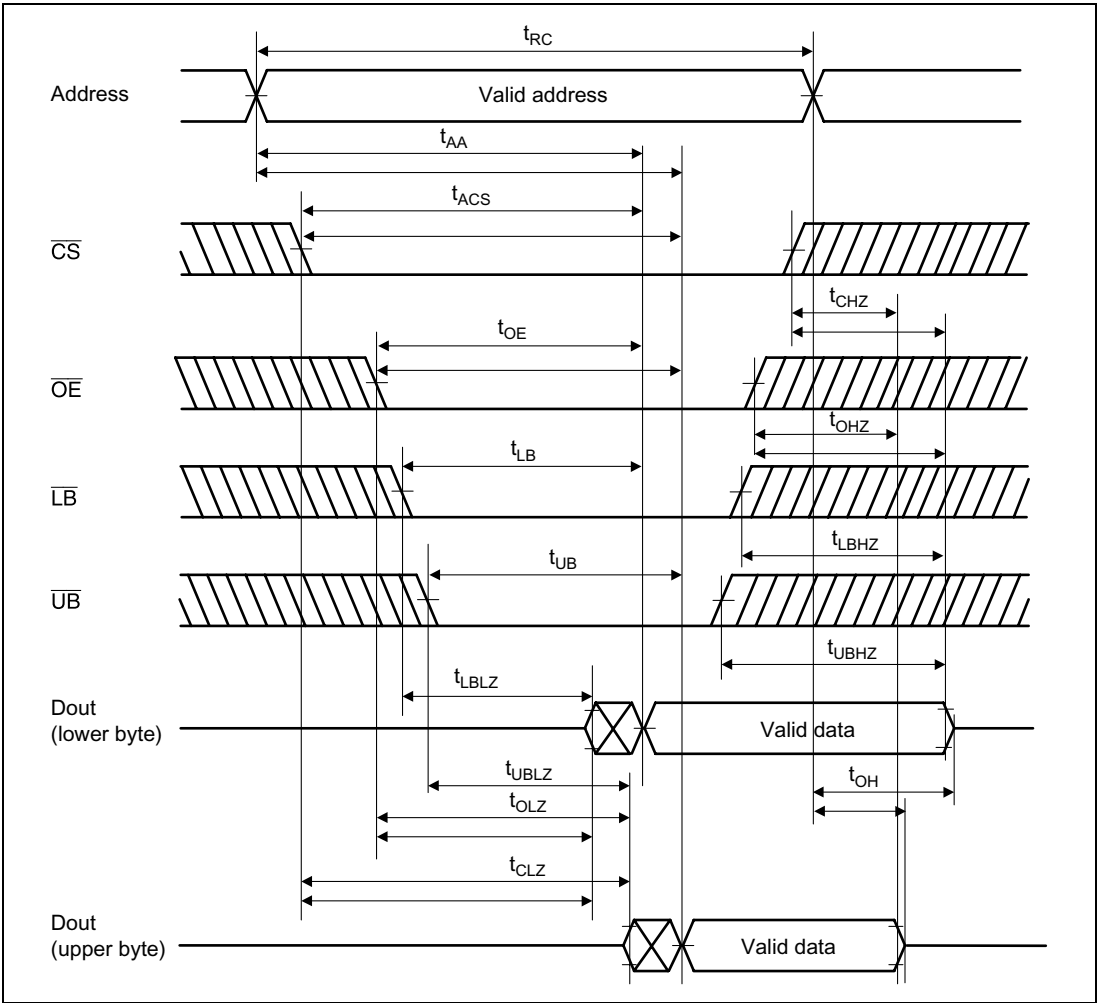


Figure 2.11 Read Cycle Waveforms

(b) Write Cycle

Table 2.8 Write Cycle AC Characteristics

Item	Symbol	Min	Max	Unit
Write cycle time	t_{WC}	10	—	ns
Chip select time	t_{CW}	7	—	ns
Address valid time	t_{AW}	7	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	7	—	ns
Address hold time	t_{WR}	0	—	ns
Output disable/output floating time	t_{OHZ}	—	5	ns
\overline{WE} output floating time	t_{WHZ}	—	5	ns
Input data set time	t_{DW}	5	—	ns
Input data hold time	t_{DH}	0	—	ns
\overline{WE} output set time	t_{OW}	3	—	ns
Byte select time	t_{LBW}, t_{UBW}	7	—	ns

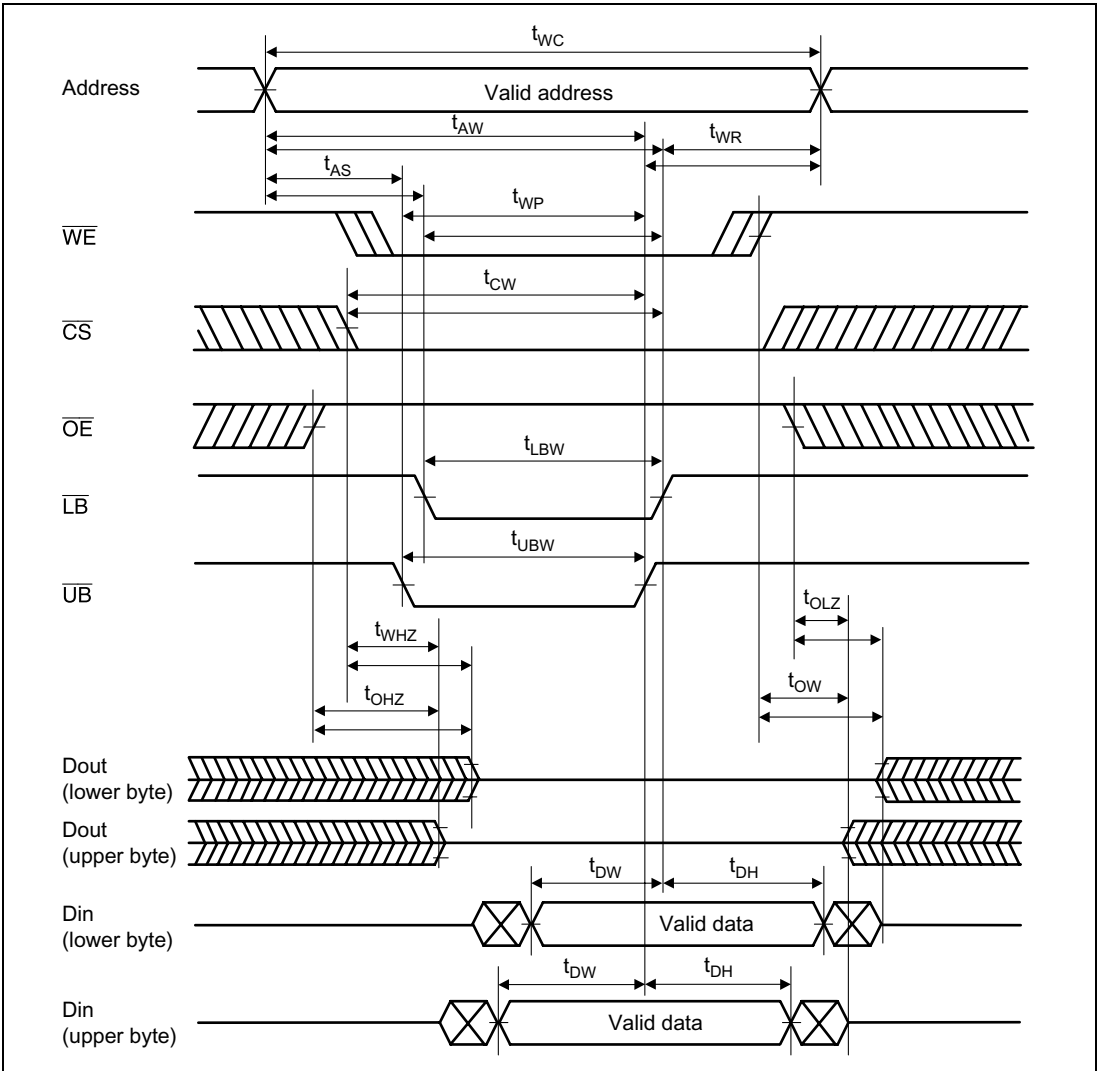


Figure 2.12 Write Cycle Waveforms

Renesas 32-Bit RISC Microcomputer

Application Note

SH7145 Group Interface Volume

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