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SH7144/45 Group

PWM 7-Phase Output

1. Specifications

Seven-phase PWM output allowing the pulse high width and duty cycle to be varied is performed as shown in figure 1.

When operating with on-chip peripheral clock Pϕ = 40.0 MHz, the output PWM period can be set arbitrarily in the range 50 ns to 1.63 ms.

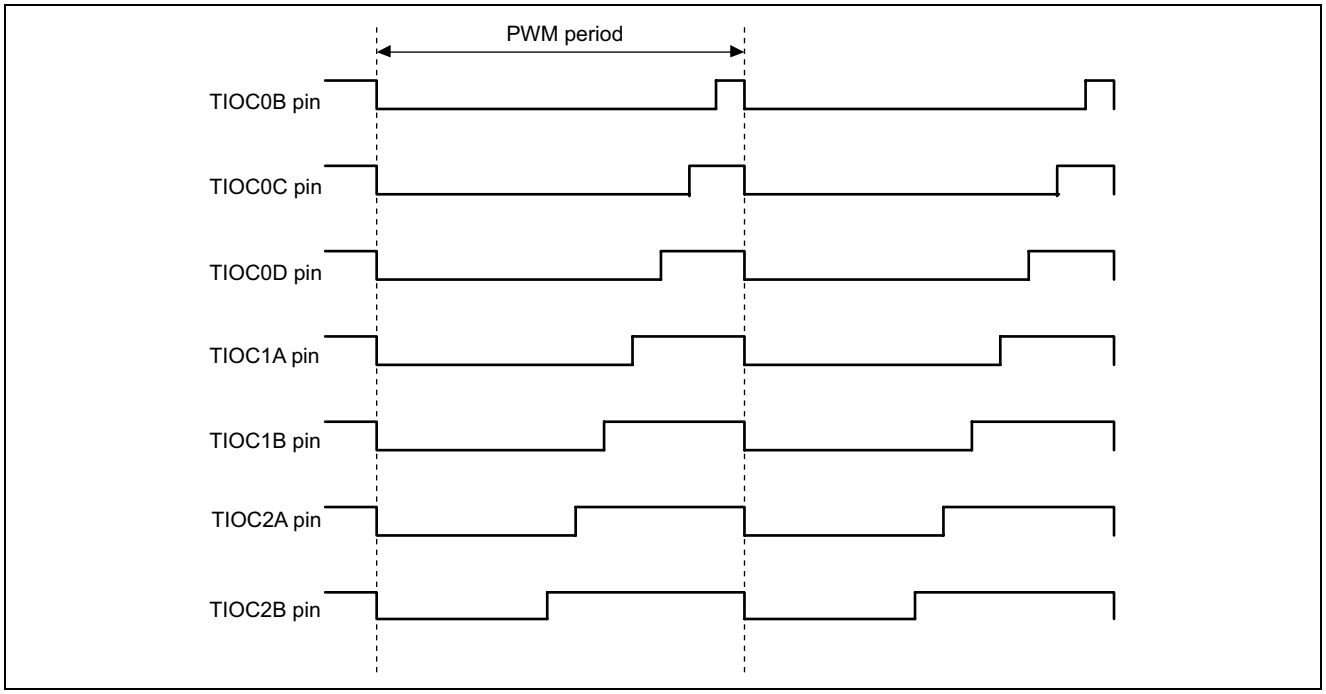


Figure 1 Example of 7-Phase PWM Waveform Output

2. Functions Used

In this sample task, 7-phase PWM output is performed by synchronous operation of MTU ch0 to ch2.

Figure 2 shows a block diagram of the MTU as used in this sample task. This sample task uses the following MTU functions.

- A function that outputs pulses automatically by hardware without software intervention (output compare)
- A function that clears a counter when a compare match occurs (counter clearing)
- A function that reverses output each time a compare match occurs (toggle output)

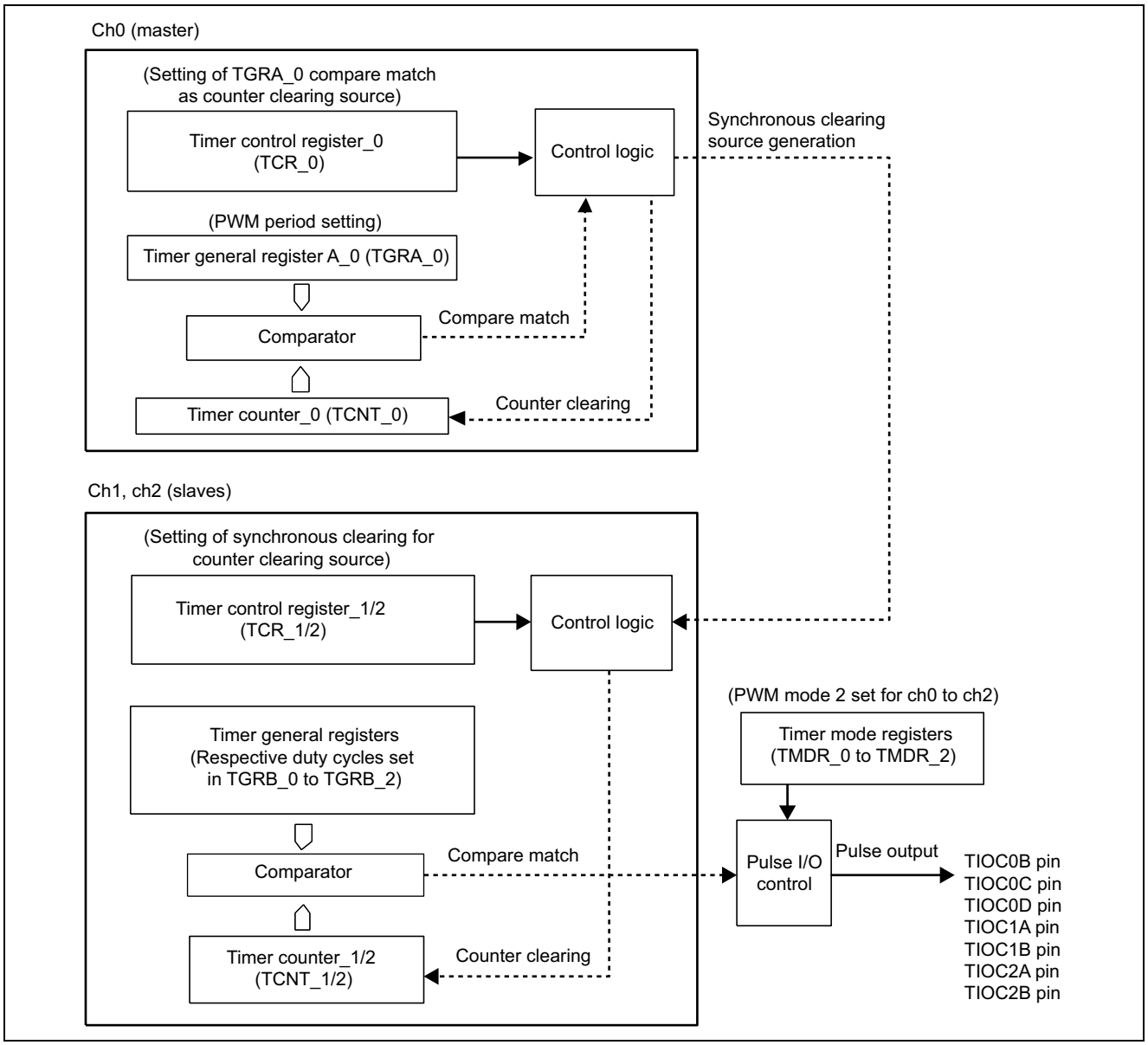


Figure 2 Block Diagram of Synchronous Clearing

Table 1 shows the function assignments used in this task. PWM pulses are output by assigning MTU functions as shown in the table.

Table 1 MTU Function Assignments

Pin or Register Name	Function Assignment
TIOC0B TIOC0C TIOC0D TIOC1A TIOC1B TIOC2A TIOC2B	PWM pulse output pins
TSYR	Ch0/1/2 synchronous operation
TCR_0/1/2	Selection of ch0/1/2 timer counter clearing sources and input clocks
TGRA_0	PWM period setting
TGRB_0 TGRC_0 TGRD_0 TGRA_1 TGRB_1 TGRA_2 TGRB_2	Duty cycle setting
TMDR_0/1/2	Operation of ch0/1/2 in PWM Mode 2

3. Principles of Operation

Figure 3 illustrates the principles of operation of this sample task. Seven-phase PWM output is performed from the ch0/1/2 PWM output pins (TIOC0B/C/D, TIOC1A/B, TIOC2A/B) by SH7145 hardware and software processing as shown in the figure.

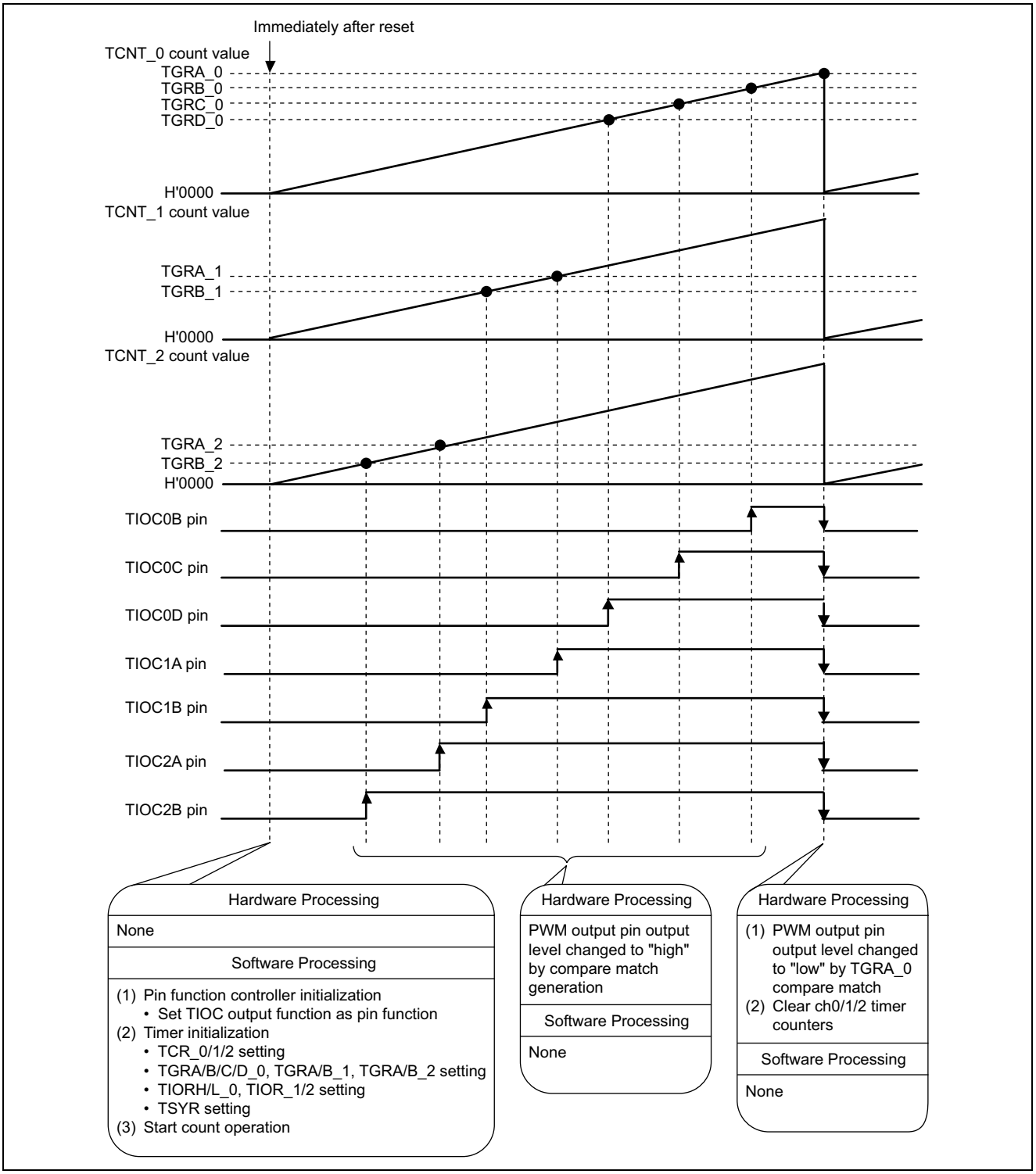


Figure 3 Principles of Operation of PWM Output (7-Phase) Using Sawtooth Waveform Generation

4. Software

(1) Modules

Module Name	Label	Function Assignment
Main routine	pwm_2	PFC and PWM output setting

(2) Arguments

Label or Register Name	Function Assignment	Data Length	Module	Input/Output
pul_cyc0a	Used to set timer value for pulse period Pulse period is calculated using following equation: Pulse period (ns) = timer value × ϕ period (25 ns at 40.0 MHz operation)	1 word	Main routine	Input
pul_duty0b pul_duty0c pul_duty0d pul_duty1a pul_duty1b pul_duty2a pul_duty2b	Used to set TIOC pin output waveform transition timing			

(3) Internal Registers Used

Register Name	Function Assignment	Address	Set Value
P_STBY.MSTCR2	Module standby mode clearing	H'FFFF861E	H'd0fd
P_PORTE.PECRL2	Used to set TIOC0B/C/D, TIOC1A/B, TIOC2A/B output as pin functions	H'FFFF83BA	H'5554
P_MTU34.TSYR	Synchronous operation set for timer counters 0/1/2	H'FFFF8241	H'07
P_MTU0.TCR_0 P_MTU1.TCR_1 P_MTU2.TCR_2	Clearing by TGRA_0 compare match set as timer counter clearing source Pϕ/16 selected as input clock	H'FFFF8260 H'FFFF8280 H'FFFF82A0	H'22 H'62 H'62
P_MTU0.TGRA_0	PWM period setting	H'FFFF8268	pul_cyc0
P_MTU0.TGRB_0	Used to set timer counter value causing high output from TIOC0B	H'FFFF826A	pul_duty0b
P_MTU0.TGRC_0	Used to set timer counter value causing high output from TIOC0C	H'FFFF826C	pul_duty0c
P_MTU0.TGRD_0	Used to set timer counter value causing high output from TIOC0D	H'FFFF826E	pul_duty0d
P_MTU1.TGRA_1	Used to set timer counter value causing high output from TIOC1A	H'FFFF8288	pul_duty1a
P_MTU1.TGRB_1	Used to set timer counter value causing high output from TIOC1B	H'FFFF828A	pul_duty1b
P_MTU2.TGRA_2	Used to set timer counter value causing high output from TIOC2A	H'FFFF82A8	pul_duty2a
P_MTU2.TGRB_2	Used to set timer counter value causing high output from TIOC2B	H'FFFF82AA	pul_duty2b

Register Name	Function Assignment	Address	Set Value
P_MTU0.TIORH_0	Sets TGRA_0 initial output 0, 0 output on output compare, TGRB_0 initial output 0, 1 output on output compare	H'FFFF8262	H'21
P_MTU0.TIORL_0	Sets TGRC_0 initial output 0, 1 output on output compare, TGRD_0 initial output 0, 1 output on output compare	H'FFFF8263	H'22
P_MTU1.TIOR_1	Sets TGRA_1 initial output 0, 1 output on output compare, TGRB_1 initial output 0, 1 output on output compare	H'FFFF8282	H'22
P_MTU1.TIOR_2	Sets TGRA_2 initial output 0, 1 output on output compare, TGRB_2 initial output 0, 1 output on output compare	H'FFFF82A2	H'22
P_MTU0.TMDR_0 P_MTU1.TMDR_1 P_MTU2.TMDR_2	Used to set PWM Mode 2 as operating mode of each channel	H'FFFF8261 H'FFFF8281 H'FFFF82A1	H'c3 H'c3 H'c3

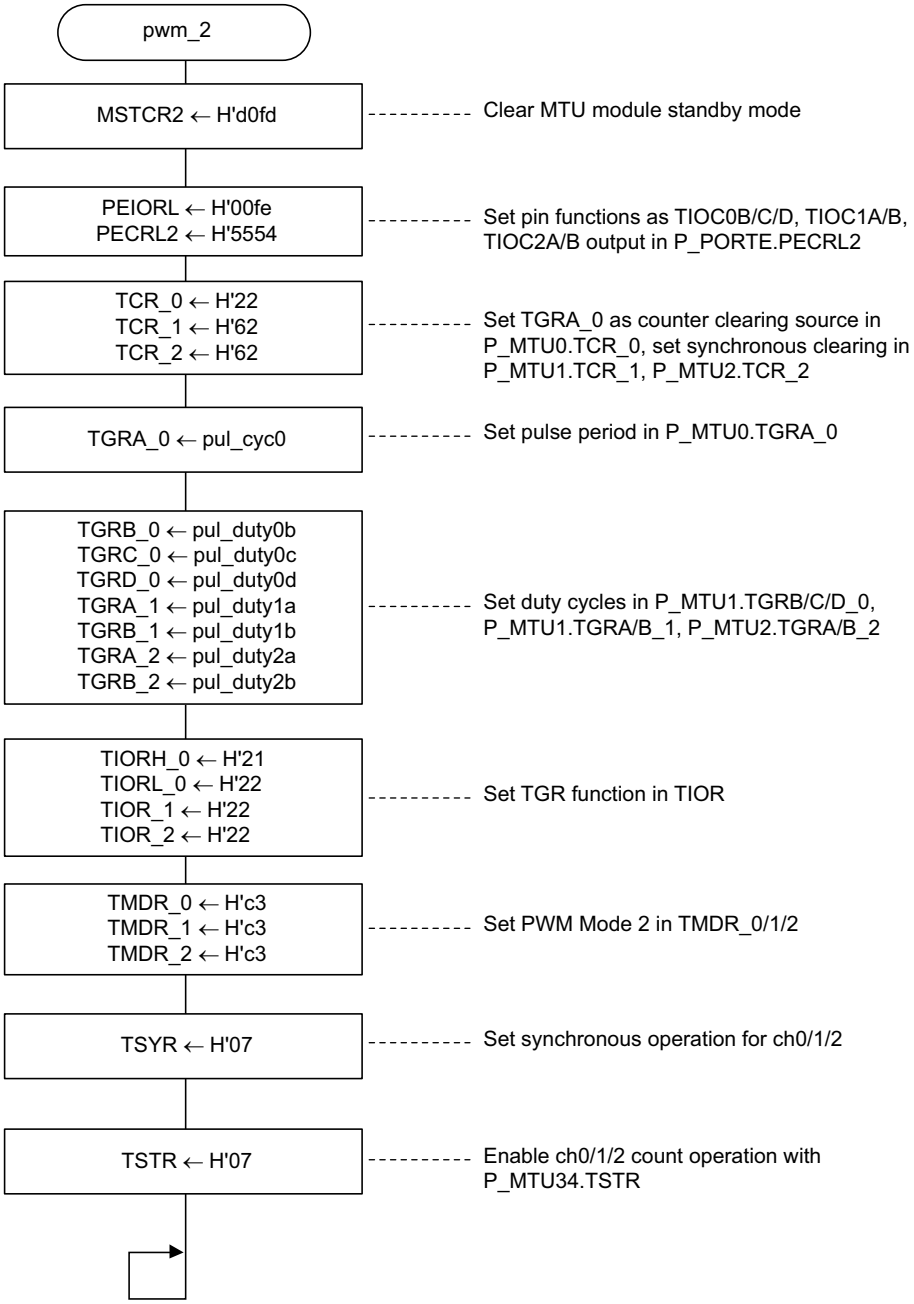
(4) RAM Used

This sample task does not use any RAM apart from the arguments.

Note: SH7145 header file names are used for register label names.

5. Flowcharts

(1) Main routine



6. Program Listing

```
/************************************************************************/
/*                              INCLUDE   FILE                          */
/************************************************************************/
#include<machine.h>
#include"iodefine_7145F.h"
/************************************************************************/
/*                                PROTOTYPE                             */
/************************************************************************/
void pwm_2(void);
/************************************************************************/
/*                              RAM ALLOCATION                          */
/************************************************************************/
#define pul_cyc0      (*(unsigned short *)0xffffe000)
#define pul_duty0b    (*(unsigned short *)0xffffe002)
#define pul_duty0c    (*(unsigned short *)0xffffe004)
#define pul_duty0d    (*(unsigned short *)0xffffe006)
#define pul_duty1a    (*(unsigned short *)0xffffe008)
#define pul_duty1b    (*(unsigned short *)0xffffe00a)
#define pul_duty2a    (*(unsigned short *)0xffffe00c)
#define pul_duty2b    (*(unsigned short *)0xffffe00e)
/************************************************************************/
/*                               MAIN PROGRAM                           */
/************************************************************************/
void pwm_2(void)
 {
   P_STBY.MSTCR2.WORD = 0xd0fd;    /* Clear module standby mode */
   P_PORTE.PEIORL.WORD = 0x00fe;   /* TIOC0B/C/D,TIOC1A/B,TIOC2A/B output */
   P_PORTE.PECRL2.WORD = 0x5554;

   P_MTU0.TCR_0.BYTE = 0x22;       /* Counter clear by TGRA_0 */
   P_MTU1.TCR_1.BYTE = 0x62;       /* Counter clear by TGRA_0 */
   P_MTU2.TCR_2.BYTE = 0x62;       /* Counter clear by TGRA_0 */

   P_MTU0.TGRA_0 = pul_cyc0;       /* Set PWM period */
   P_MTU0.TGRB_0 = pul_duty0b;     /* Set PWM duty */
   P_MTU0.TGRC_0 = pul_duty0c;
   P_MTU0.TGRD_0 = pul_duty0d;
   P_MTU1.TGRA_1 = pul_duty1a;
   P_MTU1.TGRB_1 = pul_duty1b;
   P_MTU2.TGRA_2 = pul_duty2a;
   P_MTU2.TGRB_2 = pul_duty2b;

   P_MTU0.TIORH_0.BYTE = 0x21;     /* TIOC0B=start"0",compare match"1"output */
   P_MTU0.TIORL_0.BYTE = 0x22;     /* TIOC0B/0C=start"0",compare match"1"output*/
   P_MTU1.TIOR_1.BYTE = 0x22;      /* TIOC1A/1B=start"0",compare match"1"output */
   P_MTU2.TIOR_2.BYTE = 0x22;      /* TIOC2A/2B=start"0",compare match"1"output */

   P_MTU0.TMDR_0.BYTE = 0xc3;      /* Set PWM mode2 */
   P_MTU1.TMDR_1.BYTE = 0xc3;      /* Set PWM mode2 */
   P_MTU2.TMDR_2.BYTE = 0xc3;      /* Set PWM mode2 */

   P_MTU34.TSYR.BYTE = 0x07;       /* Synchronize ch0,ch1,ch2 */
   P_MTU34.TSTR.BYTE = 0x07;       /* Start timer counter */
   while(1);
  }
```

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