To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

SH7080 Group

SCIF serial data reception function in the clock synchronous mode

Introduction

This application note describes the clock synchronous serial data reception function that use the receive-data-full interrupt sources of the SCIF (Serial Communications Interface with FIFO). This application note is for your reference in the design of user software.

Target Device

SH7085

Contents

1. Specification

This sample task uses the clock synchronous serial transfer function with FIFO to receive 256 bytes of data. Figure 1 shows the operation in this sample task.

- The communications format has a fixed data length of 8 bits.
- The reception trigger number is set to 8, and 256 bytes of data are received by using the receive data-full interrupt source.

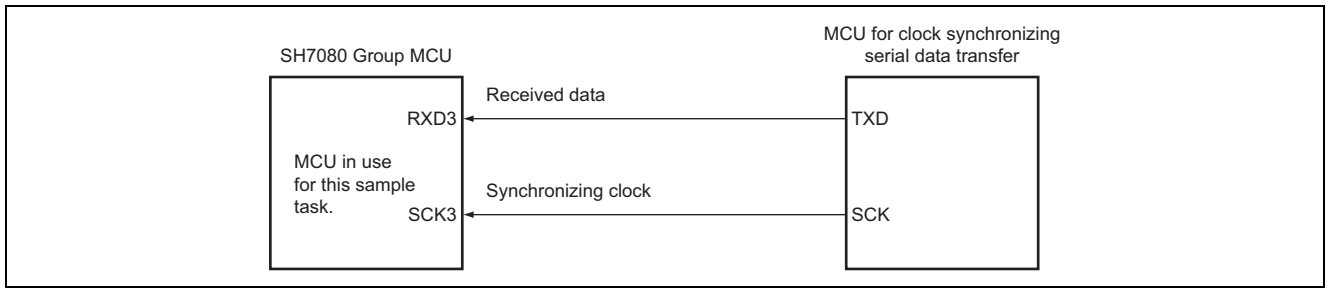


Figure 1 SCIF Serial Data Reception in the Clock Synchronous Mode

2. Applicable Conditions

- Microcontroller: SH7085 (R5F7085)
- Operating frequencies: Internal clock 80 MHz
  : Bus clock 40 MHz
  : Peripheral clock 40 MHz
  : MTU2 clock 40 MHz
  : MTU2S clock 80 MHz
- C compiler: Renesas Technology V.8.00.04

3. Description of Functions Used

This sample application uses the transmit-FIFO data-empty interrupt source of the SCIF (Serial Communications Interface with FIFO) to transmit serial data in the clock synchronous mode. In the SCIF clock synchronous mode, data is transmitted in synchronization with the clock pulse. When the internal clock is selected, the synchronizing clock signal is output through the SCK pin. When the external clock signal is selected, the synchronizing clock signal is input through the SCK pin. A block diagram of the SCIF is given as figure 2.

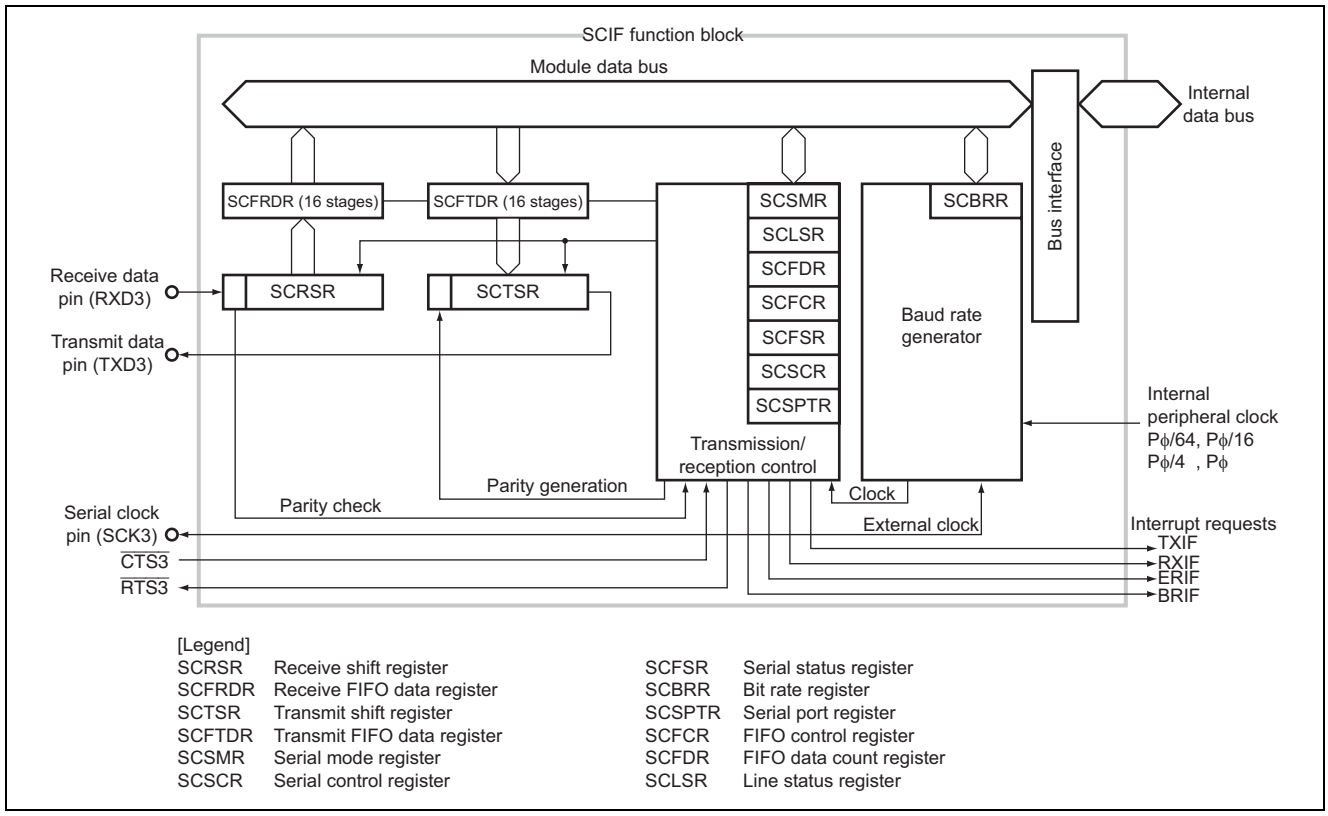


Figure 2 Block Diagram of the SCIF (Serial Communications Interface with FIFO)

- Provision of one 16-stage FIFO register each for transmission and reception enables efficient, high-speed serial communications.
- Serial data transfer proceeds in synchronization with the clock pulses. The SCIF provides a way to communicate with other LSI circuits that have clock synchronous communications functionality.
- The Receive Shift Register (SCRSR) is used to receive serial data. The SCIF places the serial data input from the RDX pin in SCRSR in the order of reception, starting with the LSB (bit 0), and converts the data to parallel data. When 1 byte of data has been received, the data is automatically transferred to the Receive FIFO Data Register (SCFRDR). The CPU cannot directly transfer data to or from SCRSR.
- The Receive FIFO Data Register (SCFRDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold received serial data. After 1 byte of data has been received, the received serial data is transferred from the Receive Shift Register (SCRSR) to SCFRDR for storage, completing reception. Successive reception operations can proceed in this way until 16 bytes of data have been stored in the register. The CPU can read data from SCFRDR, but it cannot write data to SCFRDR. If a read from the Receive FIFO Data Register is attempted when there is no received data in the register, the value read is undefined. After the register has been filled with received data, any subsequently received serial data is lost.
- The Transmit Shift Register (SCTSR) is used to transmit serial data. The SCIF transfers data for transmission from the Transmit FIFO Data Register (SCFTDR) to SCTSR, and then performs serial data transmission by sending the data to the TXD pin in order starting with the LSB (bit 0). When 1 byte of data has been transmitted, the next byte of data for transmission is automatically transferred from SCFTDR to SCTSR to start transmission. The CPU cannot directly transfer data to or from SCTSR.
- The Transmit FIFO Data Register (SCFTDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold the data that is to be transmitted serially. When the SCIF detects that the Transmit Shift Register (SCTSR) is empty, the SCIF starts serial transmission by transferring the data for transmission that has been written in SCFTDR to SCTSR. Serial transmission will proceed until SCFTDR is empty. The CPU can continue to write data to SCFTDR with any timing until SCFTDR becomes full of data for transmission (16 bytes), after which no more data can be written. If an attempt is made to write more data, the data is ignored.
- The Serial Mode Register (SCSMR) is a 16-bit register used to set the SCIF serial communications format and select the clock source for the baud rate generator. The CPU can read data from and write data to SCSMR at any time.
- The Serial Control Register (SCSCR) is a 16-bit register used to enable or disable SCIF transmission, reception, and interrupt requests, and to select the clock source for transmission and reception. The CPU can read data from and write data to SCSCR at any time.
- The Serial Status Register (SCFSR) is a 16-bit register. The upper 8 bits indicate the number of reception errors in the data in the Receive FIFO Data Register, and the lower 8 bits consist of status flags indicating the SCIF operating state. The CPU can read data from and write data to SCFSR at any time. However, 1 cannot be written to the ER, TEND, TDFE, BRK, RDF, and DR status flags. Before these flags can be cleared to 0, they must first be read as 1. The FER and PER flags are read-only flags, and data cannot be written to them.
- The Bit Rate Register (SCBRR) is an 8-bit register that, together with the baud rate generator clock source selection by the CKS1 and CKS0 bits of the Serial Mode Register (SCSMR), sets the bit rate for serial transmission and reception. The CPU can read data from and write data to SCBRR at any time. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO Control Register (SCFCR) is a 16-bit register that resets the number of data and sets the trigger data numbers for the Transmit FIFO Data Register and the Receive FIFO Data Register. The register also contains a loop-back test enable bit. The CPU can read data from and write data to SCFCR at any time.

- The FIFO Data Count Register (SCFDR) is a 16-bit register that indicates the number of data bytes stored in the Transmission FIFO Data Register (SCFTDR) and in the Receive FIFO Data Register (SCFRDR). The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicate the number of receive data bytes in SCFRDR. The CPU can read data from SCFDR at any time.
- The Line Status Register (SCLSR) is a 16-bit register that the CPU can read from and write to at any time. However, 1 cannot be written to the ORER status flag. Before the ORER status flag can be cleared, it must first be read as 1.

4. Principles of Operation

The settings for communications functions in this sample task are described in table 1. The principles of operation for this sample task are illustrated in figure 3.

Table 1 Settings for communications functions in this sample task

Communication format	Function settings
Communication mode	Clock synchronous mode
Interrupts	Receive data full interrupt (RXIF) Receive error interrupt (ERIF)
Communication rate	100 Kbps
Data length	8 bits
Bit order	LSB first
Synchronizing clock	External clock; SCK pin as synchronizing clock output
FIFO data trigger numbers	Reception: 8
Loop-back test function	Disabled

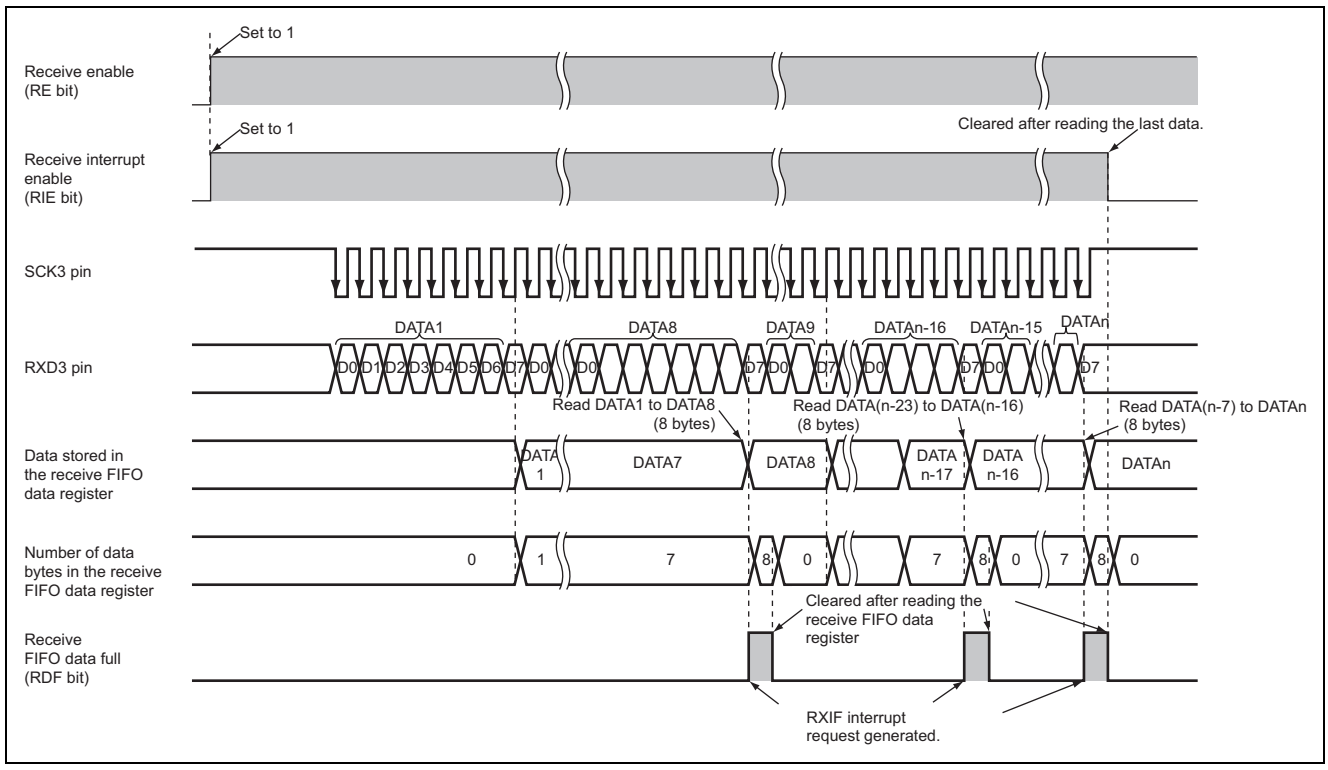


Figure 3 Principles of Operation

5. Description of Software

5.1 Description of Modules Used

The modules of this sample task are described in table 2.

Table 2 Modules

Module Name	Label Name	Description
Main routine	main()	Makes initial settings for the SCIF and enables transmission.
SCIF initial settings	io_init_scif( )	Processing to make initial settings for reception by the SCIF in the clock synchronous mode
SCIF receive data-full interrupt routine	int_scif_rxif ( )	Handles SCIF receive data-full interrupts.
SCIF reception-error interrupt routine	int_scif_erif ( )	Handles SCIF reception-error interrupts.

5.2 Variables Used

The variables used in this sample task are described in table 3.

Table 3 Variables

Variables, Label Name	Description	Used In
unsigned int DataNum	Amount of data to be received	int_scif_rxif ( )
unsigned int RcvCnt	Reception counter	main( ), int_scif_rxif ( )
unsigned char RcvData[256]	Received-data storage buffer	main( ), int_scif_rxif ( )
unsigned int RXIFCnt	Receive data-full interrupt counter	main( ), int_scif_rxif ( )
unsigned int ERCnt	Reception error interrupt counter	main( ), int_scif_erif ( )

5.3 Setting the Registers

This section describes the setting of registers used in this sample task. Note that the settings shown below are used in the sample task and are not initial values.

5.3.1 Register for Setting the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  The Frequency Control Register specifies the division ratio of the operating frequency.
  Setting: H'0241

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	IFC[2:0]	000	Division ratio of the internal clock (Iϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
11 to 9	BFC[2:0]	001	Division ratio of the bus clock (Bϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
8 to 6	PFC[2:0]	001	Division ratio of the peripheral clock (Pϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz
5 to 3	MIFC[2:0]	000	Division ratio of the MTU2S clock (MIϕ) frequency 000: × 1, 80 MHz when the input clock is 10 MHz
2 to 0	MPFC[2:0]	001	Division ratio of the MTU2 clock (MPϕ) frequency 001: × 1/2, 40 MHz when the input clock is 10 MHz

5.3.2 Register for Setting the Low Power Consumption Mode

- Standby Control Register 3 (STBCR3)
  This register controls the operation of each module in the low power consumption mode.
  Setting: H'BF

Bit	Bit Name	Setting	Function
7	MSTP15	1	1: Stops clock supply to I^2C2 module.
6	MSTP14	0	0: SCIF in operation.
5	MSTP13	1	1: Stops clock supply to SCI_2 module.
4	MSTP12	1	1: Stops clock supply to SCI_1 module.
3	MSTP11	1	1: Stops clock supply to SCI_0 module.
2	MSTP10	1	1: Stops clock supply to the SSU module.
1 to 0	—	11	Reserved

5.3.3 Settings for Serial Communications with FIFO

- Serial Control Register (SCSCR)

  This register enables and disables transmission, reception, and interrupt requests, and selects the clock source for transmission and reception.

  Setting: H'0052

Bit	Bit Name	Setting	Function
15 to 8	—	0000 0000	Reserved
7	TIE	0	0: Disables transmit-FIFO data-empty interrupt (TXIF) requests.
6	RIE	1	0: Disables receive-data-full interrupt (RXIF) requests, reception error interrupt (ERIF) requests, and break interrupt (BRIF) requests. 1: Enables receive-data-full interrupt (RXIF) requests, reception error interrupt (ERIF) requests, and break interrupt (BRIF) requests.
5	TE	0	0: Disables transmission.
4	RE	1	0: Disables reception. 1: Enables reception.
3	REIE	0	0: Disables reception error interrupt (ERIF) requests and break interrupt (BRIF) requests.
2	—	0	Reserved
1 to 0	CKE[1:0]	10	10: The external clock; the SCK pin functions as the output for the synchronizing clock signal

- FIFO Control Register (SCFCR)

  This register resets the data count and sets the trigger data numbers for the Transmission FIFO Data Register and the Receive FIFO Data Register.

  Setting: H'0080

Bit	Bit Name	Setting	Function
15 to 11	—	00000	Reserved
10 to 8	RSTRG[2:0]	000	000: $\overline{\text{RTS}}$ output active trigger. Invalid because modem signals are not allowed.
7 to 6	RTRG[1:0]	10	10: Receive FIFO data trigger number = 8
5 to 4	TTRG[1:0]	00	00: Transmit FIFO data trigger number = 8
3	MCE	0	0: Disables modem signals.
2	TFRST	0	0: Disables resetting of the Transmit FIFO Data Register. 1: Enables resetting of the Transmit FIFO Data Register.
1	RFRST	0	0: Disables resetting of the Receive FIFO Data Register. 1: Enables resetting of the Receive FIFO Data Register.
0	LOOP	0	0: Disables loop-back testing.

- Serial Status Register (SCFSR)
  The upper 8 bits of this register indicate the number of errors in reception, and the lower 8 bits indicate the operating state of the SCIF.
  Setting: H'0000

Bit	Bit Name	Setting	Function
15 to 12	PER[3:0]	0000	Number of parity errors
11 to 8	FER[3:0]	0000	Number of framing errors
7	ER	0	0: Reception is in progress, or reception has ended.
6	TEND	0	0: Transmission is in progress. 1: Transmission has ended.
5	TDFE	0	0: The number of data items for transmission written to SCFTDR is greater than the specified trigger number for transmission. 1: The number of data items for transmission written to SCFTDR is less than the specified trigger number for transmission.
4	BRK	0	0: No break signal
3	FER	0	0: No framing error
2	PER	0	0: No parity error
1	RDF	0	0: Fewer data items have been received in SCFRDR than the specified trigger number for reception.
0	DR	0	0: Reception is in progress, or there is no received data left in SCFRDR after normal reception.

- Serial Mode Register (SCSMR)
  This register sets the transfer format and selects the clock source for the baud rate generator.
  Setting: H'0080

Bit	Bit Name	Setting	Function
15 to 8	—	0000 0000	Reserved
7	C/$\overline{A}$	1	0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	0: 8-bit data
5	PE	0	0: Disables parity bit addition and checking.
4	O/$\overline{E}$	0	0: Ignores the O/$\overline{E}$ bit specification because PE = 0.
3	STOP	0	0: 1 stop bit
2	—	0	Reserved
1 to 0	CKS[1:0]	00	00: Pϕ clock

- Bit Rate Register (SCBRR)
  This register sets the bit rate for serial transmission and reception.
  Setting: H'0063

Bit	Bit Name	Setting	Function
7 to 0	—	0110 0011	Bit rate for serial transmission/reception

5.3.4 Settings for Pin Function Controller (PFC)

- Port E I/O register L (REIORL)
  This register selects the input directions for the pins of port E.
  Setting: H'0000

Bit	Bit Name	Setting	Function
15	PE15IOR	0	0: PE15 input
14	PE14IOR	0	0: PE14 input
13	PE13IOR	0	0: PE13 input
12	PE12IOR	0	0: PE12 input
11	PE11IOR	0	0: PE11 input, RXD3
10	PE10IOR	0	0: PE10 input
9	PE9IOR	0	0: PE9 input
8	PE8IOR	0	0: PE8 input
7	PE7IOR	0	0: PE7 input
6	PE6IOR	0	0: PE6 input, SCK3
5	PE5IOR	0	0: PE5 input
4	PE4IOR	0	0: PE4 input
3	PE3IOR	0	0: PE3 input
2	PE2IOR	0	0: PE2 input
1	PE1IOR	0	0: PE1 input
0	PE0IOR	0	0: PE0 input

- Port E Control Register L3 (PECRL3)
  This register selects the functions of port E pins with multiplexed functions.
  Setting: H'3000

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	PE11MD[2:0]	011	011: RXD3 input (SCIF)
11	—	0	Reserved
10 to 8	PE10MD[2:0]	000	000: PE10 input/output (port)
7	—	0	Reserved
6 to 4	PE9MD[2:0]	000	000: PE9 input/output (port)
3	—	0	Reserved
2 to 0	PE8MD[2:0]	000	000: PE8 input/output (port)

- Port E Control Register L2 (PECRL2)
  This register selects the functions of port E pins with multiplexed functions.
  Setting: H'0200

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	PE7MD[2:0]	000	000: PE7 input/output (port)
11	—	0	Reserved
10 to 8	PE6MD[2:0]	010	010: SCK3 input/output (SCIF)
7	—	0	Reserved
6 to 4	PE5MD[2:0]	000	000: PE5 input/output (port)
3	—	0	Reserved
2 to 0	PE4MD[2:0]	000	000: PE4 input/output (port)

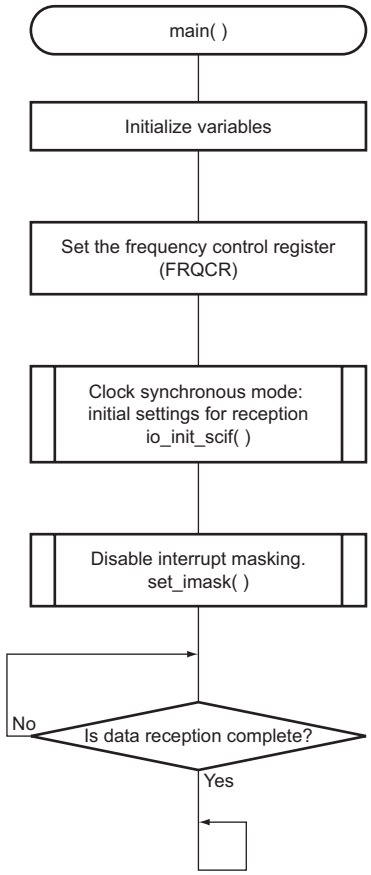
5.3.5 Settings for interrupt controller (INTC)

- Interrupt priority register L (IPRL)
  This register determines the priority levels of the corresponding interrupt requests.
  Setting: H'000F

Bit	Bit Name	Setting	Function
15 to 12	IPR[15:12]	0000	Priority level 0
11 to 8	IPR[11:8]	0000	Priority level 0
7 to 4	IPR[7:4]	0000	Priority level 0
3 to 0	IPR[3:0]	1111	Priority level 15, SCIF interrupts

6. Flowchart

6.1 Main routine



• Initialize variables
Clear the reception counter to 0.
Clear the receive data full interrupt counter to 0.
Clear the receive error interrupt counter to 0.

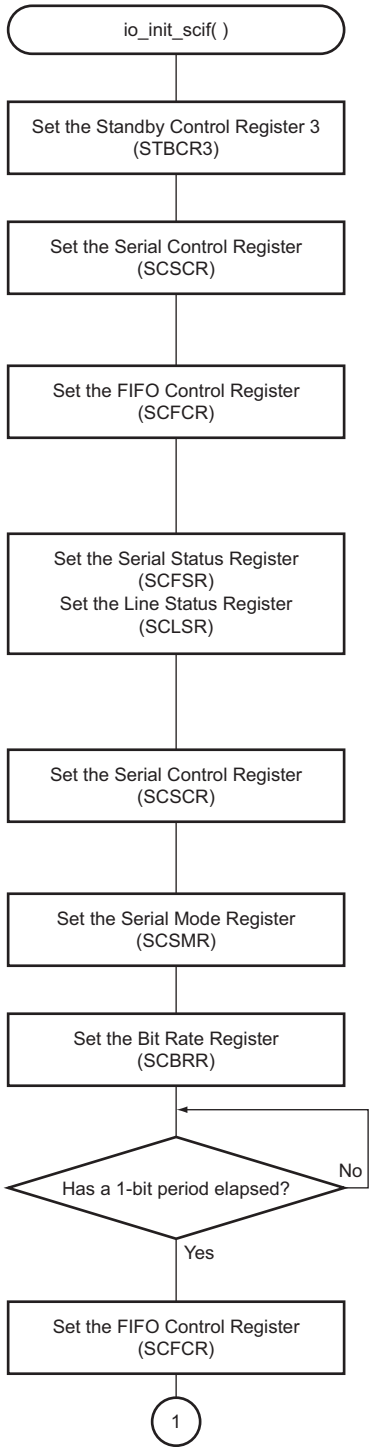
• Set the clock pulse generator (CPG).
Set the operating frequency.
When the external input clock is 10 MHz:
internal (Iϕ) = 80 MHz, bus (Bϕ) = 40 MHz, peripheral (Pϕ) = 40 MHz,
MTU2S (MIϕ) = 80 MHz, MTU2 (MPϕ) = 40 MHz

• Initial settings for reception in the clock synchronous mode.
Make the clock selection and set the bit rate to 100 Kbps.

• Release interrupt masking
Set the interrupt mask level to 0
(de-mask all interrupt levels).

• Reception processing is executed
by the interrupt processing routine.

6.2 SCIF reception initial setting routine in the clock synchronous mode



- Enabling clock supply to SCIF (STBCR3)
  When SCIF is in use:
  Clear the MSTP14 (Module Stop Bit 14) bit to 0.
  [Function] Enables clock supply to SCIF.

- Disabling transmission/reception (SCSCR)
  Clear the TE (transmit enable) bit to 0.
  [Function] Disables transmission.
  Clear the RE (receive enable) bit to 0.
  [Function] Disables reception.

- Invalidating data in the FIFOs (SCFCR)
  Set the TFRST (transmit FIFO data register reset) bit to 1.
  [Function] Invalidates any remaining data for transmission.
  Set the RFRST (receive FIFO data register reset) bit to 1.
  [Function] Invalidates any received data.

- Clearing error status (SCFSR, SCLSR)
  Read all bits, and then write 0.
  Clear the ER (receive error) bit to 0.
  [Function] Clears the receive error flag.
  Clear the BRK (break detection) bit to 0.
  [Function] Clears the break detection flag.
  Clear the DR (receive data ready) bit to 0.
  [Function] Clears the receive data ready flag.
  Clear the ORER (overrun error) bit to 0.
  [Function] Clears the overrun error flag.

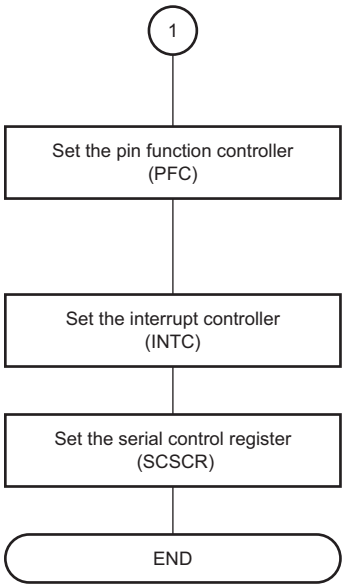
- Clock source selection and enabling/disabling clock output (SCSCR)
  Set the CKE (1 : 0) (clock enable) to B'10
  (selects the external clock, set the SCK pin to synchronizing clock input).
  [Function] Selects a clock source.

- Setting serial communications format (SCSMR)
  Set the C/$\overline{A}$ (communications mode) bit to 1.
  [Function] Selects clock synchronous mode.
  Set the CKS (1 : 0) (clock select) bit to B'00 (Pϕ clock).
  [Function] Selects a specific internal clock source.

- Setting transfer rate (SCBRR)

- Wait for at least a 1-bit period.

- Setting FIFO data trigger number and taking the FIFO out of the reset state (SCFCR)
  RTRG (1 : 0) (receive FIFO data trigger) bits to B'10 (receive trigger number: 8)
  [Function] Selects the number that triggers reception.
  Clear the RFRST (receive FIFO data register reset) bit to 0.
  [Function] Validates the received data.
  Clear the TRRST (transmit FIFO data register reset) bit to 0.
  [Function] Validates the data for transmission.

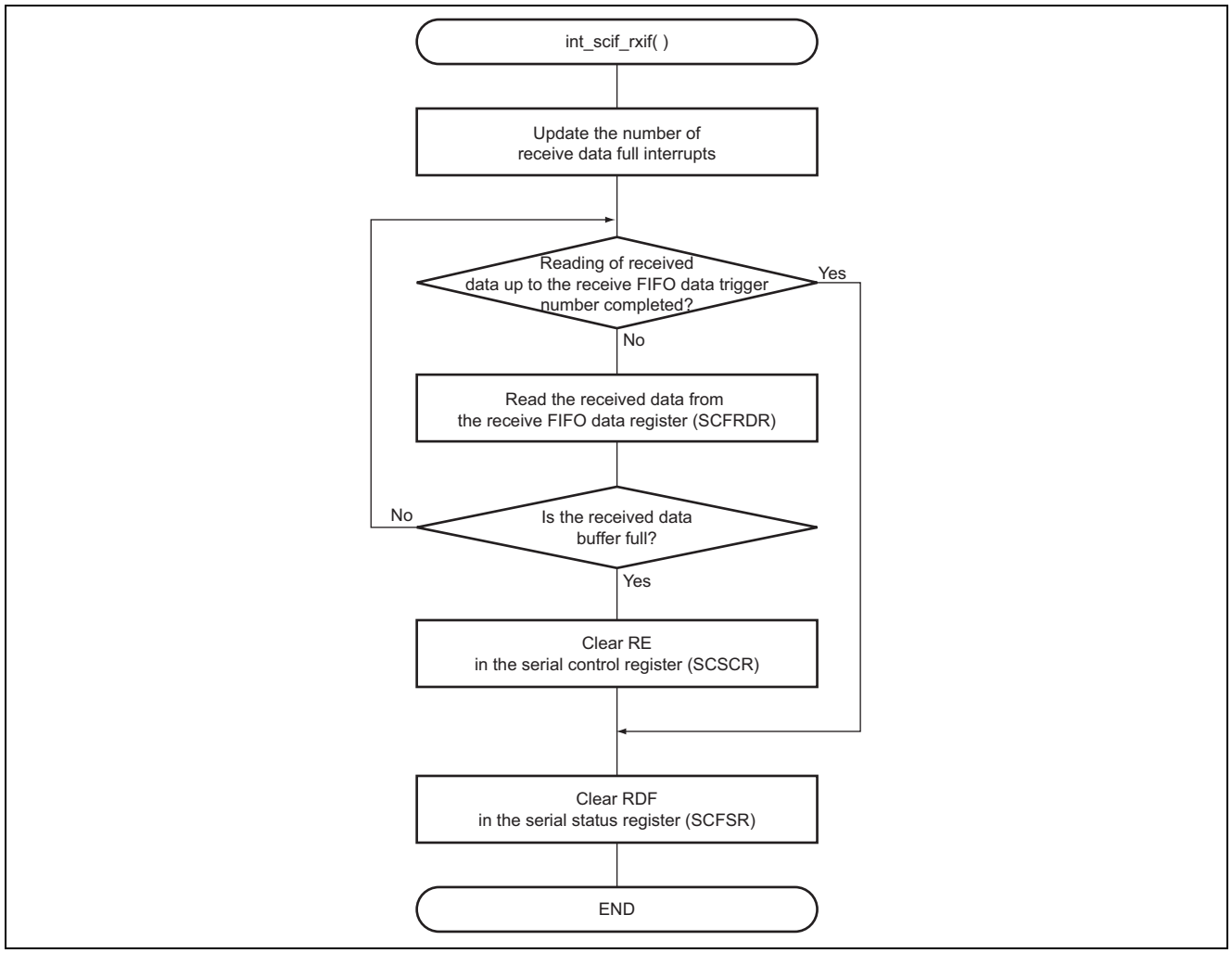


• Setting the multiplexed pins up for the serial transfer functnion
(PEIORL, PECRL2)
PE11IOR of PEIORL (Port E I/O register L) to (RXD3) input pin
[Function] Sets PE11 pin as an input pin.
Set the PE6IOR bit of PEIORL (Port E I/O register L) to 1.
[Function] Sets PE6 pin as an output pin.
Set the PE11 bit mode of PECRL3 (Port E control register L3) to B011.
[Function] Selects RXD3 input (SCIF).
Set the PE6 bit mode of PECRL2 (Port E control register L2) to B010.
[Function] Selects SCK3 input/output (SCIF).

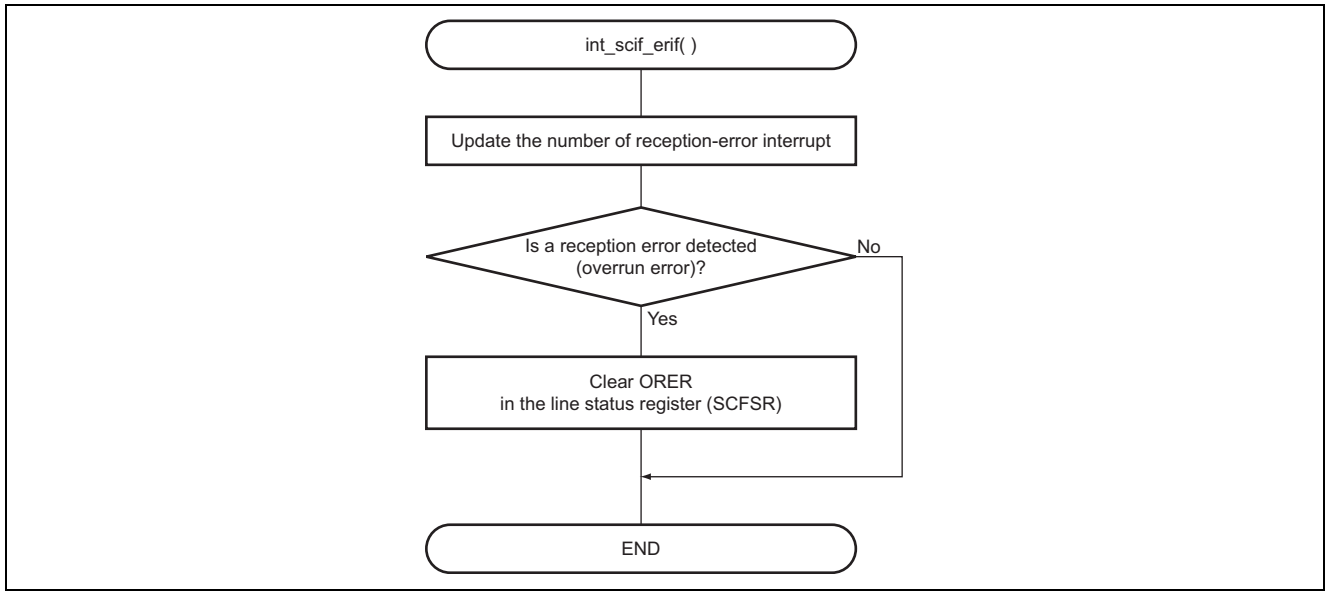
• Setting Interrupt priority register L (IPRL)
[Function] Sets the SCIF interrupt priority level to 15 (H'F).

• Enabling reception and interrupts (SCSCR)
Set the RIE (receive interrupt enable) bit to 1.
[Function] Enables the receive data full interrupt (RXIF) request,
the receive error interrupt (ERIF) request and
the break interrupt (BRIF) request.
Set the RE (receive enable) bit to 1.
[Function] Enables reception.

6.3 SCIF receive-data-full interrupt routine



6.4 SCIF reception error interrupt routine



Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.11.06	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.