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SH7263/SH7203 Group

Sample Application for the CAN Module (Remote Frame Reception)

Introduction

This application note describes the controller area network module (RCAN-TL1) and provides an example of its application to remote frame reception.

Target Devices

SH7263 and SH7203 Groups

Contents

1. Introduction

1.1 Specifications

- Transfer rate: 500 kbps
- Mailbox for transmission: Mailbox 1
- Mailbox for reception: Mailbox 1
- Remote frame for reception is as follows.
  IDE: 0 (standard format) and data length code (DLC): 2
- Data frame for transmission is as follows.
  IDE: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

1.2 Module Used

- Controller area network (RCAN-TL1): 1

1.3 Applicable Conditions

• MCU	SH7263/SH7203 (R5S72630/R5S72030)
• Clock operating mode	3 (the input from the USB_X1 pin is in use as the clock source)
• Operating frequency	Internal clock: 192 MHz Bus clock: 48 MHz Peripheral clock: 24 MHz
• C compiler:	SuperH RISC engine family C/C++ compiler package Ver.9.01Release01 from Renesas Technology
• Compiler options:	Default settings of the High-performance Embedded Workshop -cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1

1.4 Related Application Note

None

2. Description of the Sample Application

This sample program employs the RCAN-TL1 module to receive a remote frame (IDE: 0 and DLC: 2) and transmit a data frame (DLC: 2 and data: H'C1C2) in standard format (IDE: 0).

2.1 Overview of Operations by the Module Used

The SH7203 CPU has two internal RCAN-TL1 modules that support CAN2.0B and comply with ISO-11898.

The RCAN-TL1 module has 32 programmable mailboxes, each supporting a reception filter mask, and a 16-bit timer function, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-TL1 module. For details on the module, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

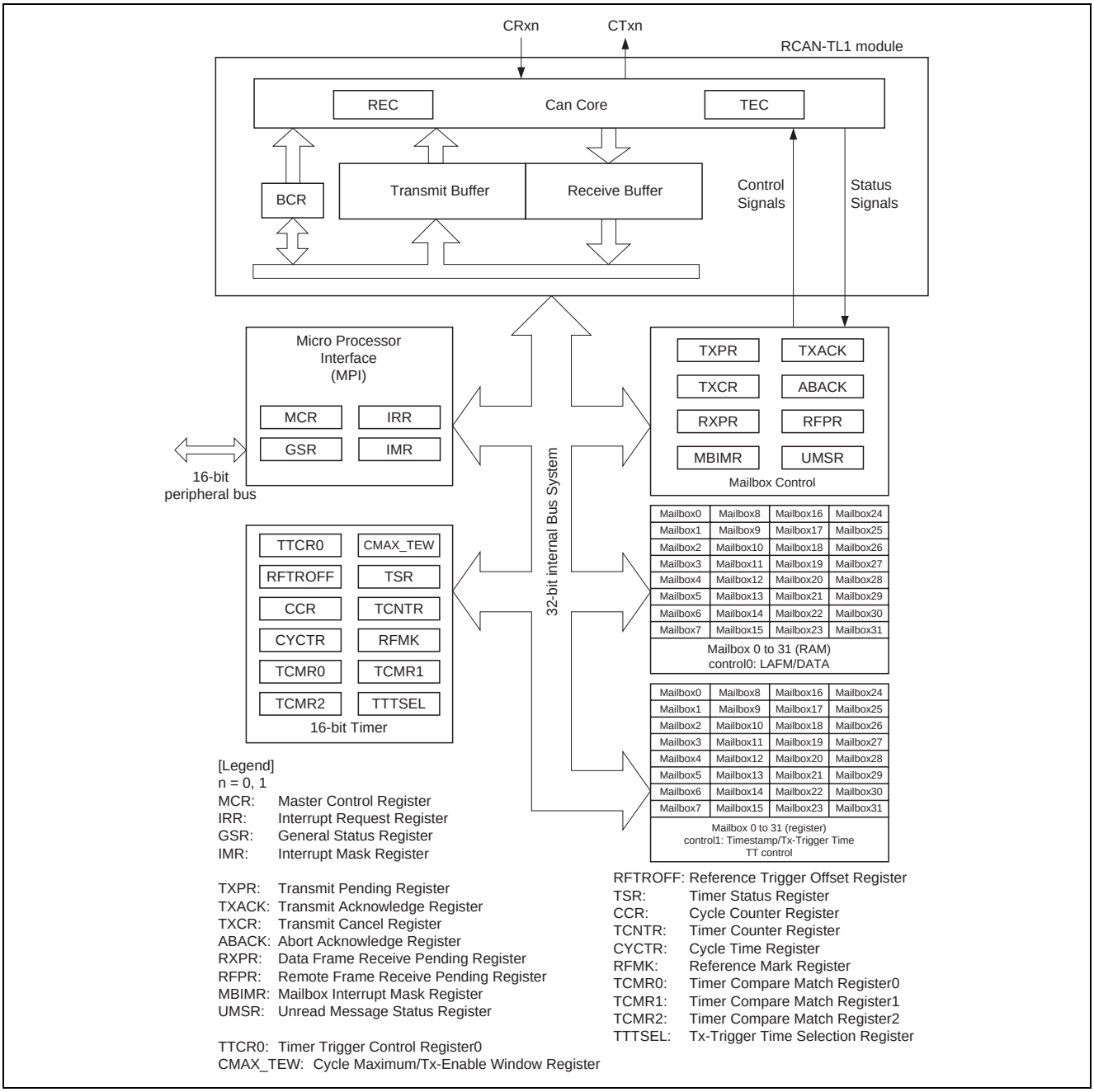


Figure 1 Structure of the RCAN-TL1 Module

2.2 Procedure for Setting the Module Used

This section describes initial settings for the reception of remote frames by the RCAN-TL1 module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-TL1 module participates in CAN-bus activity. In initial settings in this sample program, one mailbox is set for transmission and reception respectively. Figures 2 and 3 show examples of the flow of initialization for the RCAN-TL1 module. For details on settings made to individual registers, refer to the *SH7203 Group Hardware Manual*.

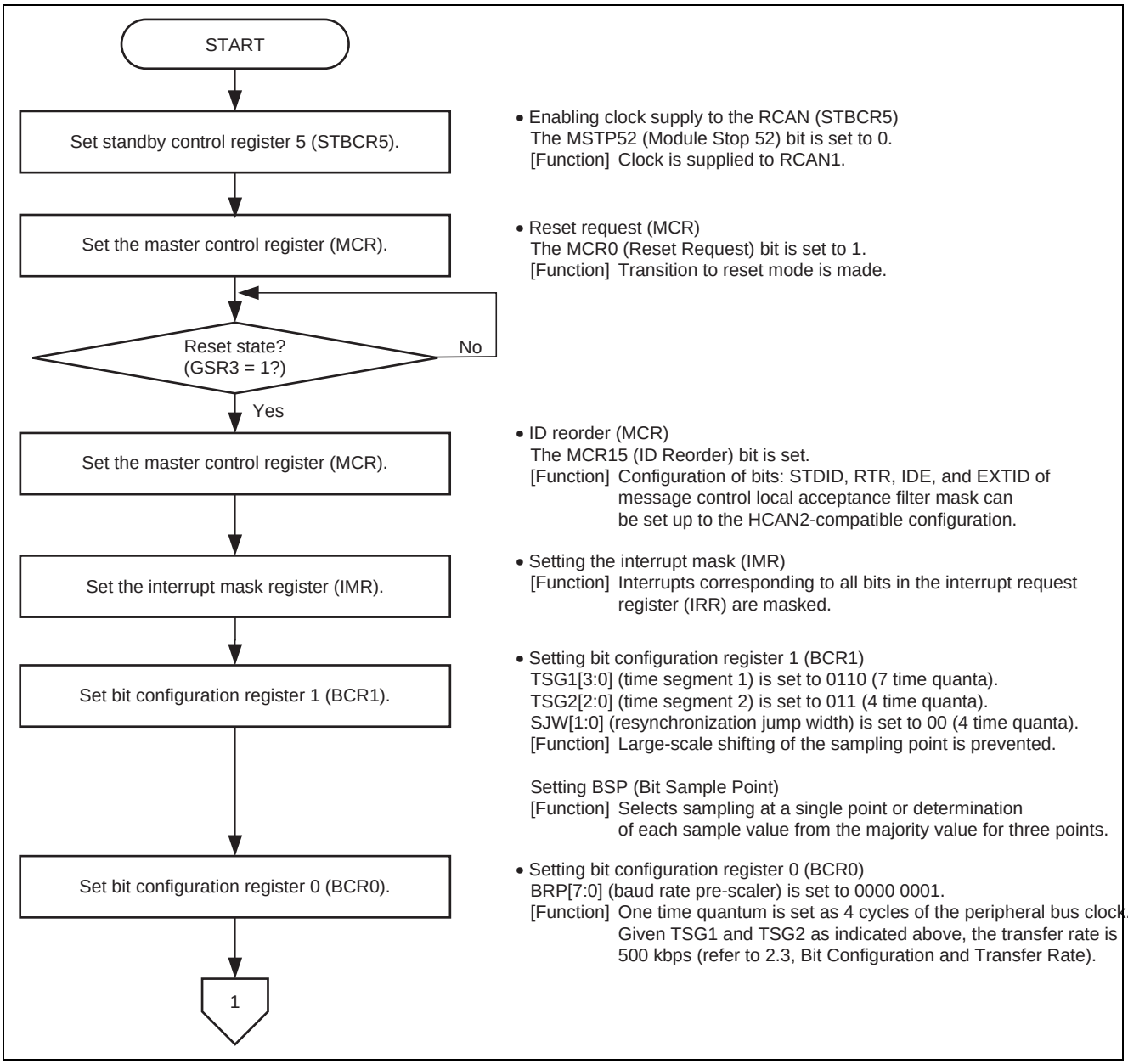
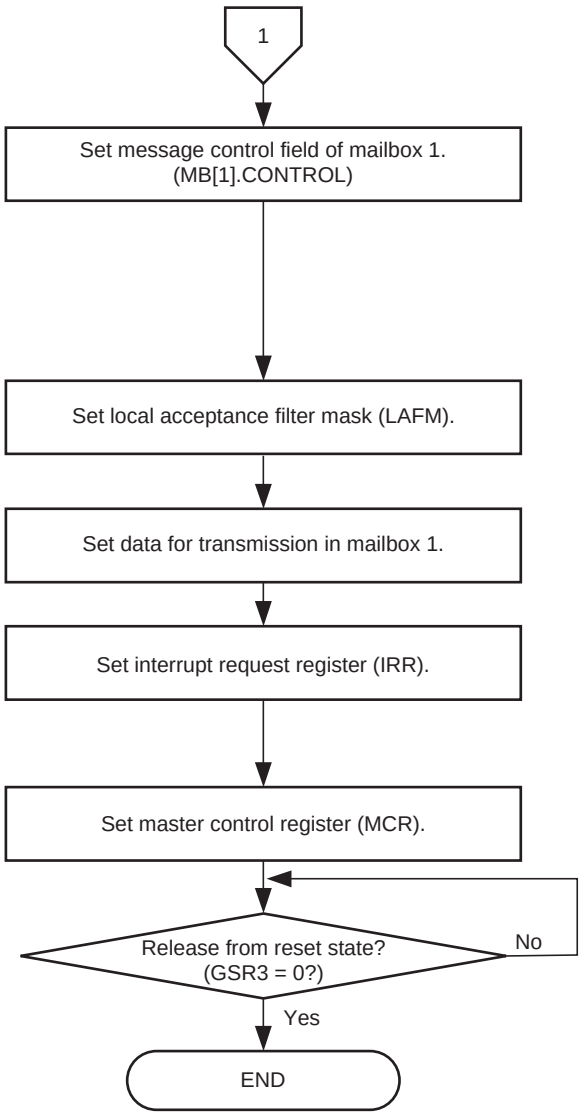


Figure 2 Example of Initialization Flow for the RCAN-TL1 Module (1)



- Setting message control (MB[0].CONTROL)
  ATX (automatic transmission of data frame) is set to 1.
  [Function] Automatic transmission of data frame is enabled.
  MBC[2:0] (mailbox configuration) is set to 010.
  [Function] Transmission of remote/data frame and reception of remote frame are enabled.
  IDE (identifier extension bit) is set to 0.
  [Function] Standard format
  RTR (remote transmission request bit) is set to 0.
  [Function] Data frame
  STDID[10:0] (standard identifier) is set to 0.
  [Function] ID = 0
- Setting local acceptance filter mask (LAFM)
  LAFM is set to H'0000 0000.
- Setting data for transmission in mailbox 1
- Clearing interrupt request register (IRR)
  IRR0 to IRR15 are cleared.
  [Function] All interrupt flags are cleared, including the flag for the soft reset.
- Setting master control register (MCR)
  MCR0 (reset request) is cleared.
  [Function] Reset mode request is cleared.
  MCR1 (halt request) is cleared.
  [Function] Halt mode request is cleared.

Figure 3 Example of Initialization Flow for the RCAN-TL1 Module (2)

2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

(1) Synchronization segment (SS)
(2) Propagation time segment (PRSEG)
(3) Phase buffer segment 1 (PHSEG1)
(4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (Tq). Figure 4 shows an example of the configuration of a bit in the case where SS = Tq, PRSEG = 3Tq, PHSEG1 = 4Tq, and PHSEG2 = 4Tq.

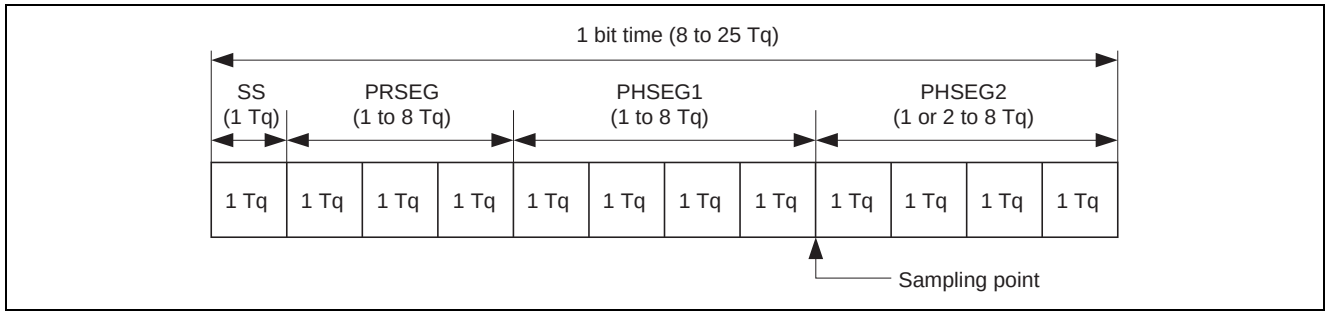


Figure 4 Configuration of One-Bit Time

In the RCAN-TL1, the Tq of PRSEG + PHSEG1 is set to TSG1[3:0] in bit configuration register 1 (BCR1) and the Tq of PHSEG2 is set to TSG2[2:0] (Tq = set value + 1). Additionally, the number of cycles of the peripheral-bus clock corresponding to 1Tq is set in BRP[7:0] of bit configuration register 0 (BCR0).

In the following description, BRP[7:0], TSG1[3:0] and TSG2[2:0] indicate the register settings, and BRP, TSEG1, TSEG2, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

By definition, Tq for the RCAN-TL1 module is 1Tq = 2 × (BRP[7:0] + 1)/peripheral bus clock, and the transfer rate is calculated as follows.

Transfer rate = peripheral bus clock/(2 × (BRP[7:0] + 1) × the number of Tq in 1-bit time) =
peripheral bus clock/(2 × (BRP[7:0] + 1) × ((TSG1[3:0] + 1) + (TSG2[2:0] + 1) + 1)

The following restrictions apply to settings of the bit-configuration registers.

TSEG1 (Min) > TSEG2 ≥ SJW (Max) (SJW = 1 to 4)

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

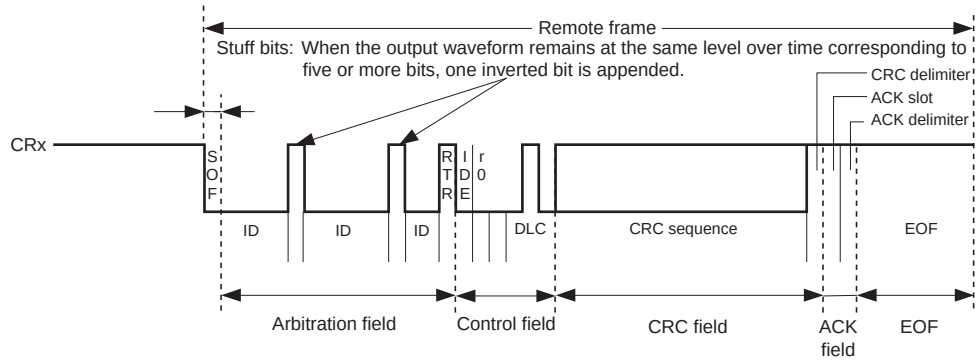
8 ≤ TSEG1 + TSEG2 + 1 ≤ 25 time quanta
TSEG2 ≥ 2

Since the settings in this sample program are as follows: peripheral bus clock = 24 MHz, BRP[7:0] = 1, TSG1[3:0] = 6, TSG2[2:0] = 3, the transfer rate is calculated with the following formula.

Transfer rate (bps) = 24 M (2 × (1+1) × ((6 + 1) + (3 + 1) + 1) = 500 k

2.4 Operation of the Sample Program

In this sample program, a remote frame (DLC: 2) in standard format (IDE: 0) is received in mailbox 1 and a data frame (DLC: 2 and data: H'C1C2) in standard format (IDE: 0) is transmitted from mailbox 1 at a transfer rate of 500 kbps. Figure 5 shows the waveform for remote frame reception.



SOF (Start of frame)	: Indicates start of data frame and remote frame.
ID (Identifier)	: Indicates priority of data.
RTR (Request for remote transmission)	: Indicates distinction between data frame and remote frame.
IDE (Identifier extension)	: Indicates distinction between standard format and extended format.
r0	: Reserved bit
DLC (Data length code)	: Indicates the number of bytes in the data field. Setting range: 0 to 8 bytes
CRC sequence	: This value is used to check frames.
CRC delimiter	: This bit is used to delimit the CRC field and ACK field.
ACK slot	: The receiving unit is dominant, and overwrites this when no errors are detected in a transmitted message.
ACK delimiter	: This bit is used to delimit the ACK field and EOF.
EOF (End of frame):	: Indicates the end of the frame.

Figure 5 Waveform for Remote Frame Reception by the RCAN-TL1

2.5 Procedure of Processing by the Sample Program

Tables 1 and 2 give an example of the settings for the controller area network (RCAN-TL1). Figure 6 shows an example of the flow of processing by this sample program.

Table 1 Register Settings for Controller Area Network (RCAN-TL1) (1)

Register Name	Address	Setting Value	Description
Standby control register (STBCR5)	H'FFFE 0410	H'FB	• MSTP52 = 0: RCAN1 runs
Master control register_1 (MCR_1)	H'FFFF 0800	H'0001	• MCR0 = 1: Reset mode transition request
		H'8001	• MCR15 = 1: RCAN-TL1 is not the same as HCAN2
		H'8000	• MCR0 = 0: Release from reset mode
Interrupt mask register_1 (IMR_1)	H'FFFF 080A	H'FFFF	• Disables all interrupts of RCAN1
Bit configuration register 1_1 (BCR1_1)	H'FFFF 0804	H'6300	• TSG1[3:0] = 0110: PRSEG + PHSEG1 = 6 Tq • TSG2[2:0] = 011: PHSEG2 = 4 Tq • SJW = 0: SJW = 2 Tq • BSP = 0: Bit sampling at one point
Bit configuration register 0_1 (BCR0_1)	H'FFFF 0806	H'0001	• BRP[7:0] = 1: 1 Tq = 4 × Pϕ

Table 2 Register Settings for Controller Area Network (RCAN-TL1) (2)

Register Name	Address	Setting Value	Description
Message control field (MB[1].CONTROL1_1)	H'FFFF 0942	H'1100	• ATX = 1: Automatic transmission of data frame MBC[2:0] = 001: Enables transmission of data frames and remote frames, and reception of remote frames
Message control field (MB[1].CONTROL0_1)	H'FFFF 0932	H'0000 0000	• IDE = 0: Standard format • RTR = 0: Data frame • STDID[10:0] = 0: Standard ID = 0
Local acceptance filter mask_1 (MB[0].LAFM_1)	H'FFFF 0904	H'0000 0000	• Clear: MASK is not set
Remote frame receive pending register 0_1 (RFPR0_1)	H'FFFF 084A	H'0000 0002	• Clears the remote frame reception-completed flag
Transmit acknowledge register 0_1 (TXACK0)	H'FFFF 0832	H'0002	• Clears the transmit acknowledge flag

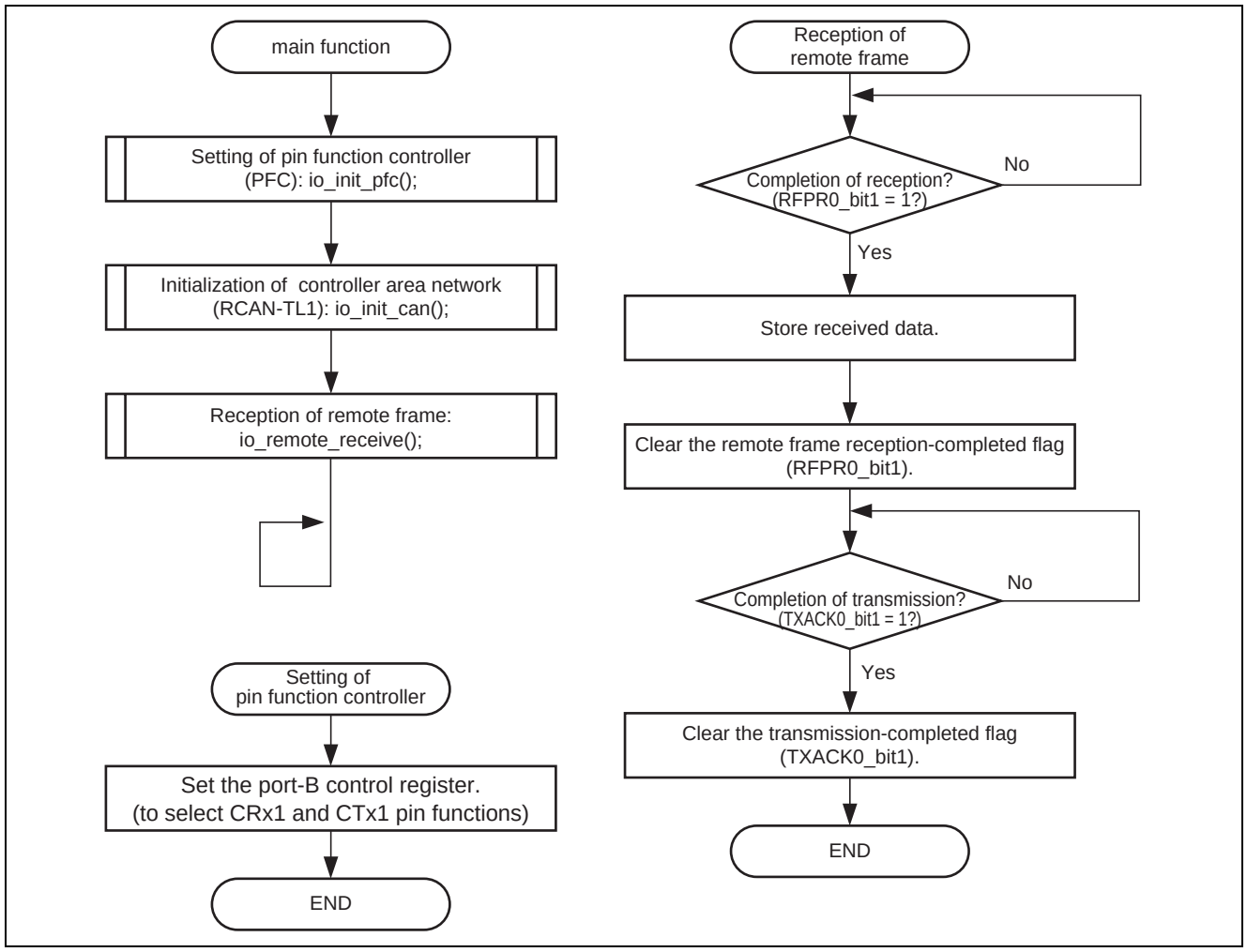


Figure 6 Example of Flow of Processing by the Sample Program

3. Sample Program

```
/*""FILE COMMENT""*****************************************************************
*
*       System Name : SH7203 Sample Program
*       File Name   : main.c
*       Contents    : Application of CAN Module (Remote Frame Reception)
*       Version     : 1.00.00
*       Model       : M3A-HS30
*       CPU         : SH7203
*       Compiler    : SHC9.0.3.0
*       note        : The module receives a remote frame (DLC: 2) in standard format (IDE
*                     = 0) from mailbox 1 of CAN1 at a 500-kbps transfer rate over the
*                     CAN bus, and sores data in RAM.
*                     After completion of remote-frame reception, the module automatically
*                     transmits a data frame from mailbox 1.
*
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*
*       history   : 2007.06.26 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include "iodefine.h"       /* SH7203 iodefine  */

/* ---- prototype declaration ---- */
void main(void);
void io_init_pfc(void);
void io_init_can(void);
void io_remote_receive(void);

/* ---- symbol definition ---- */
#define CAN_GSR3 0x0008
#define CAN_MB1  0x0002

/* ---- RAM allocation variable declaration ---- */
unsigned char   nIDE = 0;           /* ide */
unsigned char   nRTR = 0;           /* rtr */
unsigned char   nDLC = 0;           /* dlc */
unsigned int    nSID = 0;           /* sid */
unsigned int    nEID = 0;           /* eid */
unsigned char   gSnd_data[8] = {0xc1, 0xc2, 0xc3, 0xc4, 0xc5, 0xc6, 0xc7, 0xc8};
```

Figure 7 Sample Program Listing: "main.c" (1)

```
 46    /*""FUNC COMMENT""*****************************************************
 47     * Outline     : Sample Program main
 48     *-------------------------------------------------------------------
 49     * Include     : none
 50     *-------------------------------------------------------------------
 51     * Declaration : void main(void);
 52     *-------------------------------------------------------------------
 53     * Function    : Sample Program main
 54     *-------------------------------------------------------------------
 55     * Argument    : none
 56     *-------------------------------------------------------------------
 57     * Return Value: none
 58     *-------------------------------------------------------------------
 59     * Notice      : none
 60     *""FUNC COMMENT END""*************************************************/
 61    void main(void)
 62    {
 63
 64        /* ==== Setting of PFC ==== */
 65        io_init_pfc();
 66
 67        /* ==== Initializing CAN module ==== */
 68        io_init_can();
 69
 70        /* ==== CAN remote frame reception ==== */
 71        io_remote_receive();
 72
 73        while(1){
 74            /* loop */
 75        }
 76
 77    }
 78
 79    /*""FUNC COMMENT""*****************************************************
 80     * Outline     : Setting of PFC
 81     *-------------------------------------------------------------------
 82     * Include     : #include "iodefine.h"
 83     *-------------------------------------------------------------------
 84     * Declaration : void io_init_pfc(void);
 85     *-------------------------------------------------------------------
 86     * Function    : Setting of Pin Function Controller (PFC)
 87     *-------------------------------------------------------------------
 88     * Argument    : none
 89     *-------------------------------------------------------------------
 90     * Return Value: none
 91     *-------------------------------------------------------------------
 92     * Notice      : none
 93     *""FUNC COMMENT END""*************************************************/
 94    void io_init_pfc(void)
 95    {
 96        /* ==== Setting of PFC ==== */
 97        /* ---- Port B control register L3 ---- */
 98        PORT.PBCRL3.BIT.PB10MD = 0x1;   /* Set CRx1 */
 99        PORT.PBCRL3.BIT.PB11MD = 0x1;   /* Set CTx1 */
100
101    }
```

Figure 8 Sample Program Listing: "main.c" (2)

```
/*""FUNC COMMENT""*****************************************************
 * Outline     : Setting of RCAN
 *-------------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-------------------------------------------------------------------
 * Declaration : void io_init_can(void);
 *-------------------------------------------------------------------
 * Function    : Setting of Controller Area Network(RCAN)
 *-------------------------------------------------------------------
 * Argument    : none
 *-------------------------------------------------------------------
 * Return Value: none
 *-------------------------------------------------------------------
 * Notice      : none
 *""FUNC COMMENT END""*************************************************/
void io_init_can(void)
{
    int i;

    /* ==== Setting of power down mode(RCAN1) ==== */
    CPG.STBCR5.BIT.MSTP52 = 0;

    /* ==== Initializing CAN module ==== */
    RCAN1.MCR.WORD |= 0x0001;       /* CAN Interface reset mode */
    while((RCAN1.GSR.WORD & CAN_GSR3) != CAN_GSR3){
        /* Reset state waiting */
    }

    /* ---- RCAN mode selection ---- */
    RCAN1.MCR.WORD |= 0x8000;       /* RCAN-TL1 is not same as HCAN2 */

    /* ---- Disable all can interrupt ---- */
    RCAN1.IMR.WORD  = 0xFFFF;

    /* ---- Config baudrate ---- */
    RCAN1.BCR1.WORD = 0x6300;       /* tsg1=6(7bit),tsg2=3(4bit),sjw=0(1bit),bsp=0 */
    RCAN1.BCR0.WORD = 0x0001;       /* 500K bps */
//  RCAN1.BCR0.WORD = 0x0003;       /* 250K bps */
//  RCAN1.BCR0.WORD = 0x0007;       /* 125K bps */

    /* ---- Config mailbox1 as transmission/reception slot ---- */
    RCAN1.MB[1].CONTROL1.WORD = 0x1100;     /* Auto dataframe transmission,
                                               Can send data or remote frame,
                                               receive remote frame, dlc=0 */
    RCAN1.MB[1].CONTROL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
    RCAN1.MB[1].LAFM.LONG = 0x00000000;
    for(i = 0; i < 8; i++){                  /* send data */
        RCAN1.MB[1].MSG_DATA[i] =  gSnd_data[i];
    }

    /* ---- Clear interrupt flags ---- */
    RCAN1.IRR.WORD = 0xffff;

    /* ---- Clear reset and halt ---- */
    RCAN1.MCR.WORD &= 0xfffc;
    while( (RCAN1.GSR.WORD & CAN_GSR3) != 0x0000 ){
        /* reset state is end */
    }

}
```

Figure 9 Sample Program Listing: "main.c" (3)

```
162    /*""FUNC COMMENT""************************************************
163     * Outline     : Reception of Remote Frame
164     *-----------------------------------------------------------------
165     * Include     : #include "iodefine.h"
166     *-----------------------------------------------------------------
167     * Declaration : void io_remote_receive(void);
168     *-----------------------------------------------------------------
169     * Function    : RCAN1 is used to receive remote frame.
170     *-----------------------------------------------------------------
171     * Argument    : none
172     *-----------------------------------------------------------------
173     * Return Value: none
174     *-----------------------------------------------------------------
175     * Notice      : none
176     *""FUNC COMMENT END""*******************************************/
177    void io_remote_receive(void)
178    {
179        /* ---- Reception completion waiting ---- */
180        while((RCAN1.RFPR0.WORD & CAN_MB1) != CAN_MB1){
181        }
182
183        /* ---- Receive data storage ---- */
184        nIDE = RCAN1.MB[1].CONTROL0.BIT.IDE;
185        nRTR = RCAN1.MB[1].CONTROL0.BIT.RTR;
186        nDLC = RCAN1.MB[1].CONTROL1.BIT.DLC;
187        nSID = RCAN1.MB[1].CONTROL0.BIT.STDID;
188        nEID = RCAN1.MB[1].CONTROL0.BIT.EXDID;
189
190        /* ---- Reception completion flag clear ---- */
191        RCAN1.RXPR0.WORD = CAN_MB1;
192
193        /* ---- Transmission completion waiting ---- */
194        while((RCAN1.TXACK0.WORD & CAN_MB1) != CAN_MB1){
195        }
196
197        /* ---- Transmission completion flag clear ---- */
198        RCAN1.TXACK0.WORD = CAN_MB1;
199
200    }
201
202    /* End of File */
```

Figure 10 Sample Program Listing: "main.c" (4)

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
  SH7263 Group Hardware Manual
  SH7203 Group Hardware Manual
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Rev.	**Date**	**Page**	**Summary**
1.00	Sep.19.08	—	First edition issued
1.01	Dec.17.08	—	Source file is updated

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