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SH7263/SH7203 Group

Sample Application for the CAN Module (Data Frame Transmission)

Introduction

This application note describes the controller area network module (RCAN-TL1) and provides an example of its application to data frame transmission.

Target Devices

SH7263 and SH7203 Groups

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1. Introduction

1.1 Specifications

- Transfer rate: 500 kbps
- Mailbox for transmission: Mailbox 1
- A data frame as described below is transmitted once.
IDE: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

1.2 Module Used

- Controller area network (RCAN-TL1): 1

1.3 Applicable Conditions

- MCU SH7263/SH7203 (R5S72630/R5S72030)
- Clock operating mode 3 (the input from the USB_X1 pin is in use as the clock source)
- Operating frequency Internal clock: 192 MHz
Bus clock: 48 MHz
Peripheral clock: 24 MHz
- C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01Release01
from Renesas Technology
- Compiler options: Default settings of the High-performance Embedded Workshop
-cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0
-del_vacant_loop=0 -struct_alloc=1

1.4 Related Application Note

None

2. Description of the Sample Application

This sample program employs the RCAN-TL1 module to transmit a single frame with two bytes of data.

2.1 Overview of Operations by the Module Used

The SH7203 CPU has two internal RCAN-TL1 modules that support CAN2.0B and comply with ISO-11898.

The RCAN-TL1 module has 32 programmable mailboxes, each supporting a reception filter mask, and a 16-bit timer function, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-TL1 module. For details on the module, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

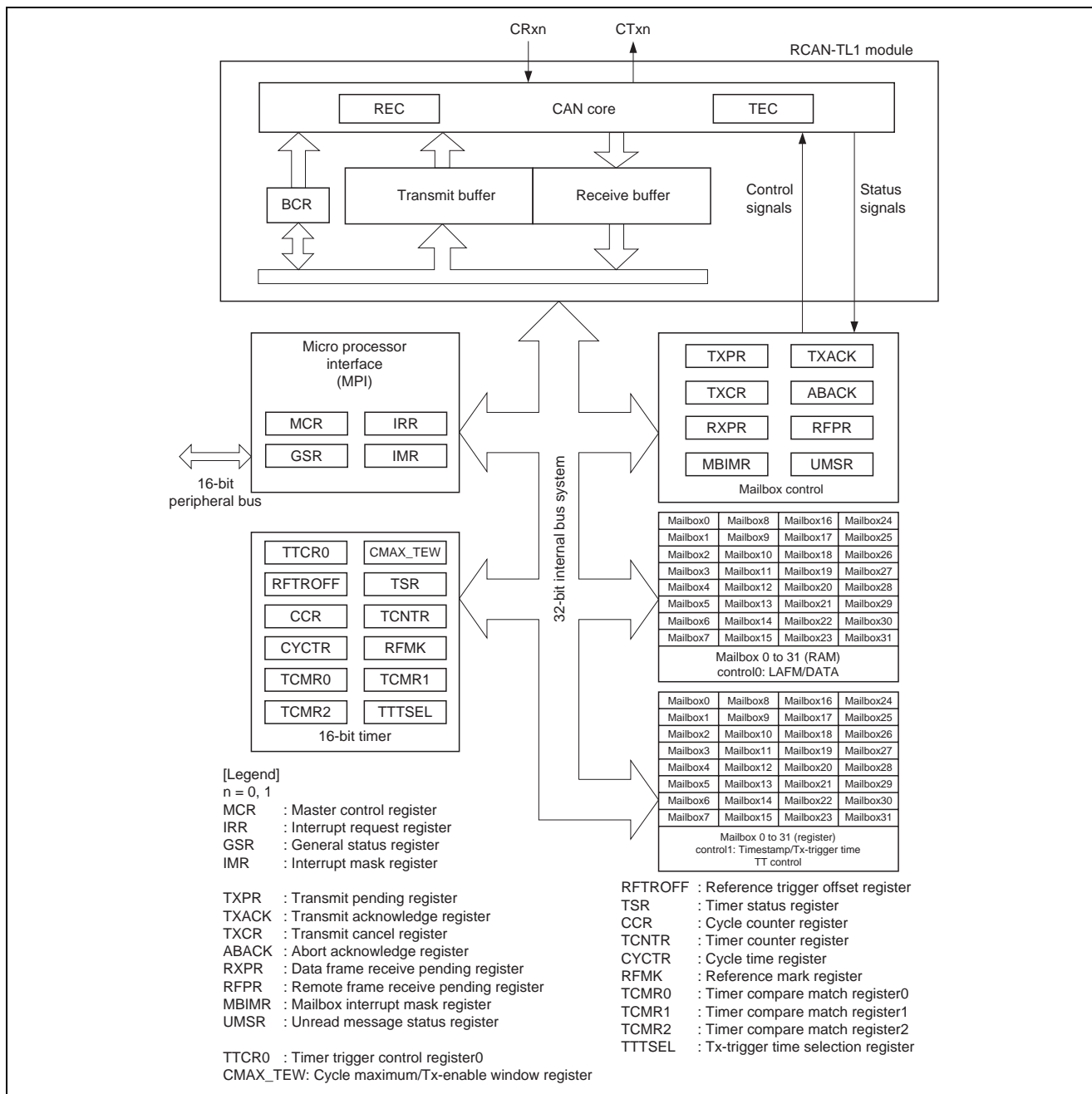


Figure 1 Structure of the RCAN-TL1 Module

2.2 Procedure for Setting the Module Used

This section describes initial settings for the transmission of data frames by the RCAN-TL1 module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-TL1 module participates in CAN-bus activity. In initial settings in this sample program, one mailbox is set for transmission and reception respectively. Figures 2 and 3 show examples of the flow of initialization for the RCAN-TL1 module. For details on settings made to individual registers, refer to the *SH7203 Group Hardware Manual*.

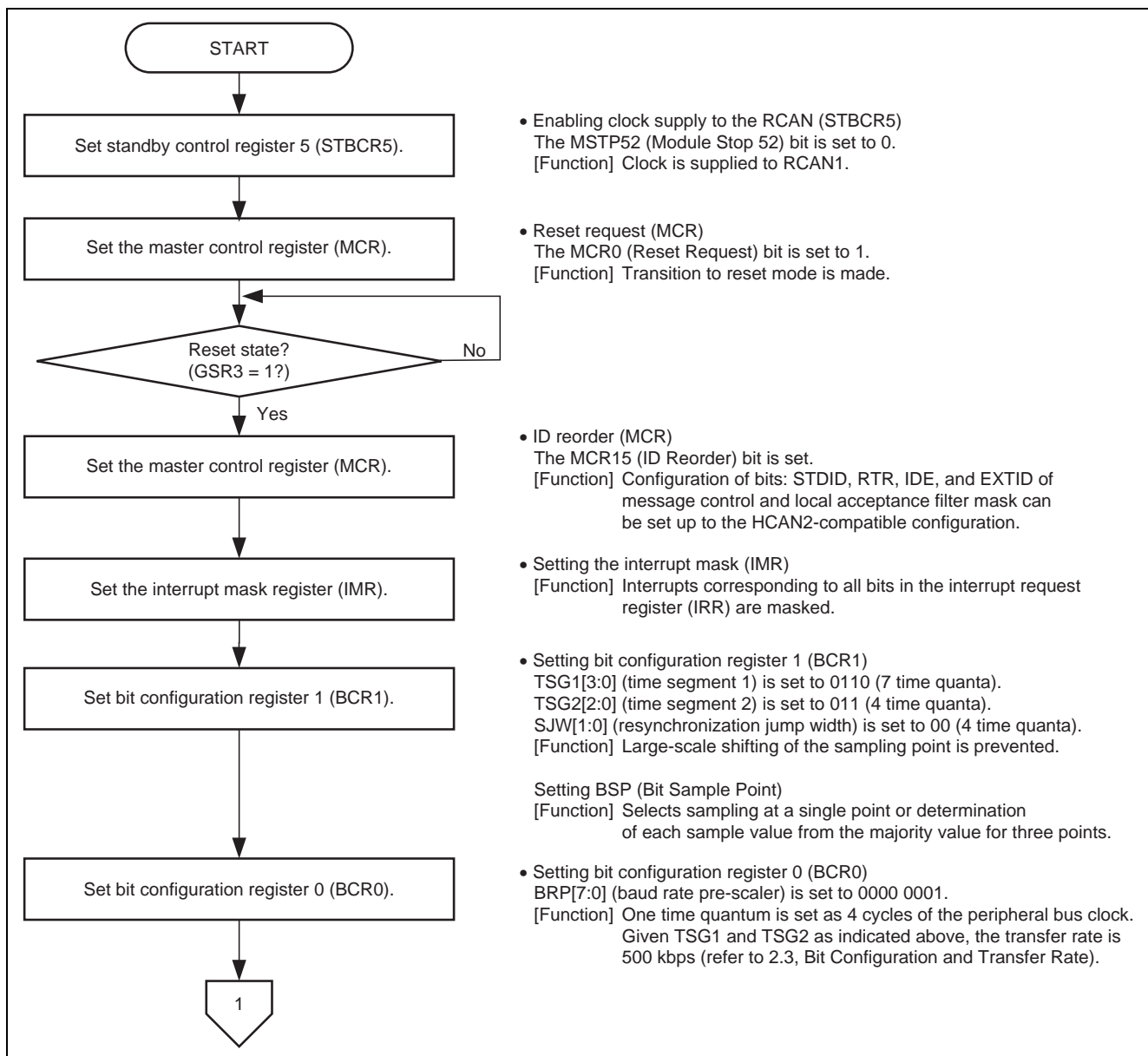


Figure 2 Example of Initialization Flow for the RCAN-TL1 Module (1)

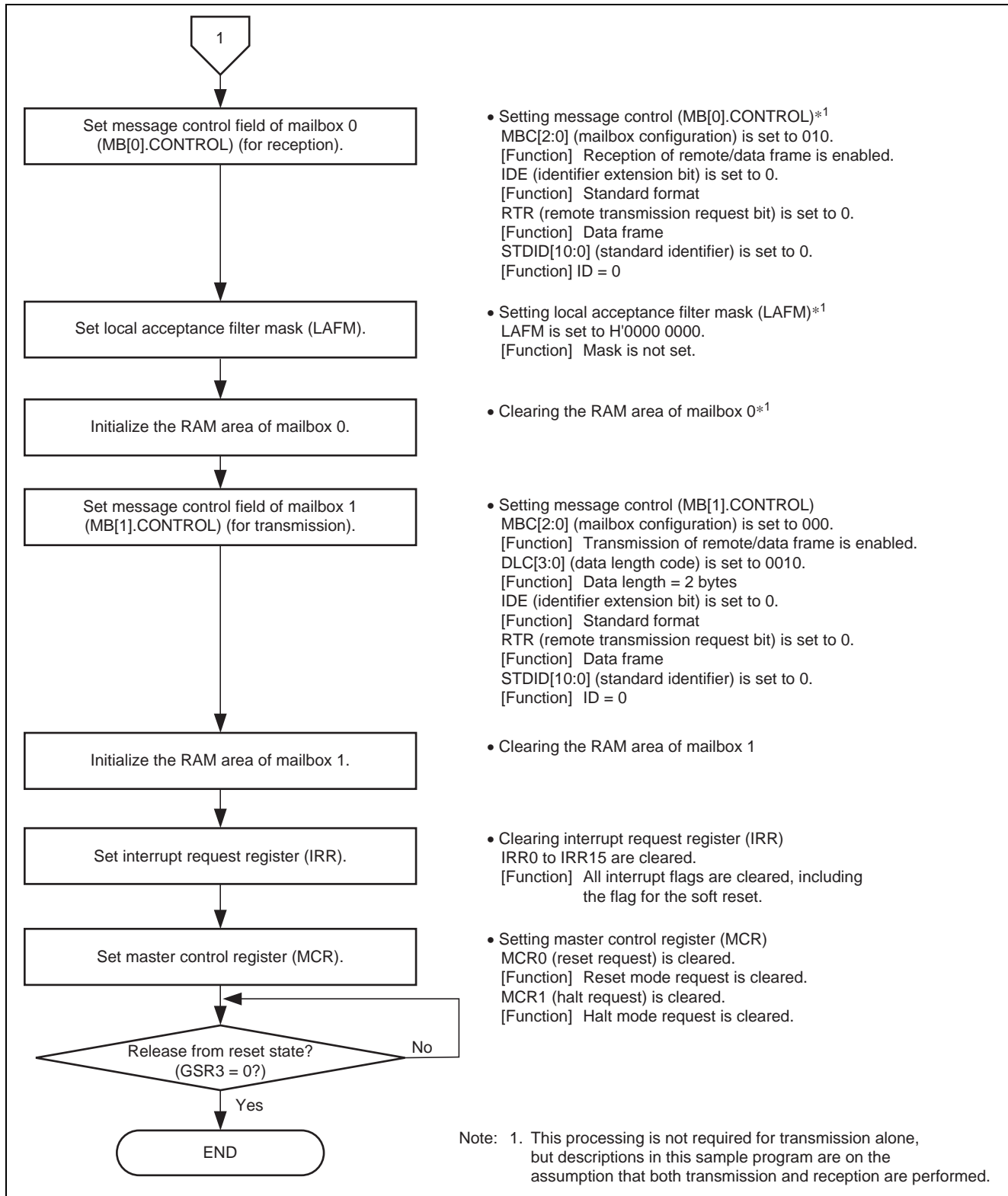


Figure 3 Example of Initialization Flow for the RCAN-TL1 Module (2)

2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

- (1) Synchronization segment (SS)
- (2) Propagation time segment (PRSEG)
- (3) Phase buffer segment 1 (PHSEG1)
- (4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (T_q). Figure 4 shows an example of the configuration of a bit in the case where $SS = T_q$, $PRSEG = 3T_q$, $PHSEG1 = 4T_q$, and $PHSEG2 = 4T_q$.

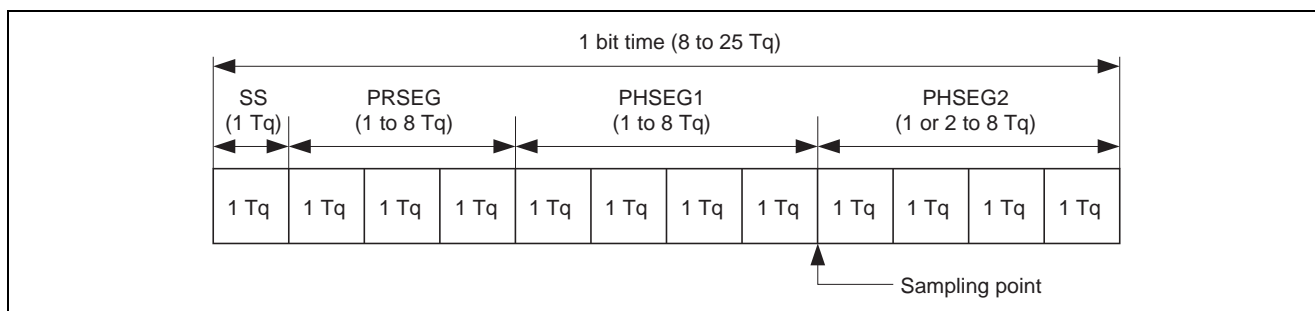


Figure 4 Configuration of One-Bit Time

In the RCAN-TL1, the T_q of $PRSEG + PHSEG1$ is set to $TSG1[3:0]$ in bit configuration register 1 (BCR1) and the T_q of $PHSEG2$ is set to $TSG2[2:0]$ ($T_q = \text{set value} + 1$). Additionally, the number of cycles of the peripheral-bus clock corresponding to $1T_q$ is set in $BRP[7:0]$ of bit configuration register 0 (BCR0).

In the following description, $BRP[7:0]$, $TSG1[3:0]$ and $TSG2[2:0]$ indicate the register settings, and BRP , $TSEG1$, $TSEG2$, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

By definition, T_q for the RCAN-TL1 module is $1T_q = 2 \times (BRP[7:0] + 1) / \text{peripheral bus clock}$, and the transfer rate is calculated as follows.

$$\text{Transfer rate} = \text{peripheral bus clock} / (2 \times (BRP[7:0] + 1) \times \text{the number of } T_q \text{ in 1-bit time}) = \text{peripheral bus clock} / (2 \times (BRP[7:0] + 1) \times ((TSG1[3:0] + 1) + (TSG2[2:0] + 1) + 1))$$

The following restrictions apply to settings of the bit-configuration registers.

$$TSEG1 (\text{Min}) > TSEG2 \geq SJW (\text{Max}) \quad (SJW = 1 \text{ to } 4)$$

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

$$8 \leq TSEG1 + TSEG2 + 1 \leq 25 \text{ time quanta}$$

$$TSEG2 \geq 2$$

Since the settings in this sample program are as follows: peripheral bus clock = 24 MHz, $BRP[7:0] = 1$, $TSG1[3:0] = 6$, $TSG2[2:0] = 3$, the transfer rate is calculated with the following formula.

$$\text{Transfer rate (bps)} = 24 \text{ M} (2 \times (1+1) \times ((6 + 1) + (3 + 1) + 1)) = 500 \text{ k}$$

2.4 Operation of the Sample Program

In this sample program, a data frame in standard format (IDE = 0) with DLC = 2 and H'C1C2 as the data is transmitted once from mailbox 1 at a transfer rate of 500 kbps. Figure 5 shows the waveform for data frame transmission.

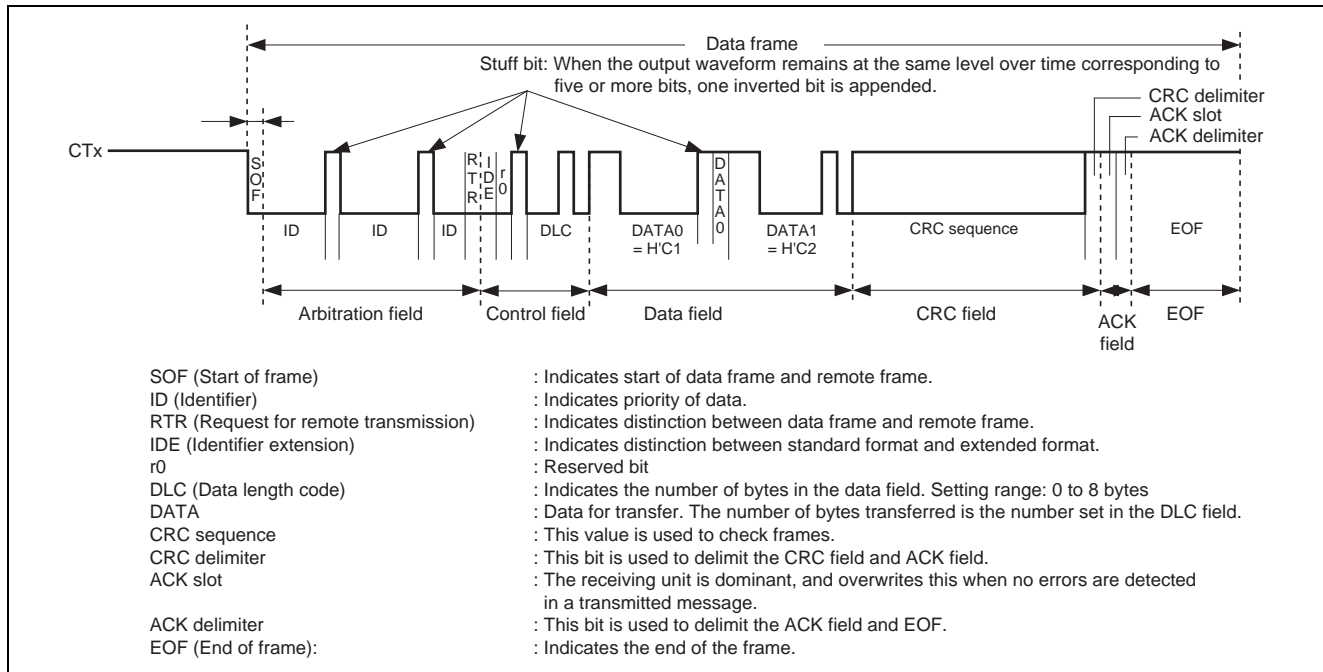


Figure 5 Waveform for Data Frame Transmission by the RCAN-TL1

2.5 Procedure of Processing by the Sample Program

Tables 1 and 2 give an example of the settings for the controller area network (RCAN-TL1). Figure 6 shows an example of the flow of processing by this sample program.

Table 1 Register Settings for Controller Area Network (RCAN-TL1) (1)

Register Name	Address	Setting Value	Description
Standby control register (STBCR5)	H'FFFE 0410	H'FB	<ul style="list-style-type: none"> MSTP52 = 0: RCAN1 runs
Master control register_1 (MCR_1)	H'FFFF 0800	H'0001	<ul style="list-style-type: none"> MCR0 = 1: Reset mode transition request
		H'8001	<ul style="list-style-type: none"> MCR15 = 1: RCAN-TL1 is not the same as HCAN2
		H'8000	<ul style="list-style-type: none"> MCR0 = 0: Release from reset mode
Interrupt mask register_1 (IMR_1)	H'FFFF 080A	H'FFFF	<ul style="list-style-type: none"> Disables all interrupts of RCAN1
Bit configuration register 1_1 (BCR1_1)	H'FFFF 0804	H'6300	<ul style="list-style-type: none"> TSG1[3:0] = 0110: PRSEG + PHSEG1 = 6 Tq TSG2[2:0] = 011: PHSEG2 = 4 Tq SJW = 0: SJW = 2 Tq BSP = 0: Bit sampling at one point
Bit configuration register 0_1 (BCR0_1)	H'FFFF 0806	H'0001	<ul style="list-style-type: none"> BRP[7:0] = 1: 1 Tq = 4 × Pφ
Message control field (MB[0].CONTROL1_1)	H'FFFF 0910	H'0200	<ul style="list-style-type: none"> MBC[2:0] = 010: Enables reception of data frames and remote frames

Table 2 Register Settings for Controller Area Network (RCAN-TL1) (2)

Register Name	Address	Setting Value	Description
Message control field (MB[1].CONTROL1_1)	H'FFFF 0942	H'0002	<ul style="list-style-type: none"> MBC[2:0] = 000: Enables transmission of data frames and remote frames DLC[3:0] = 0010: 2-byte data length
Message control field (MB[1].CONTROL0_1)	H'FFFF 0932	H'0000 0000	<ul style="list-style-type: none"> IDE = 0: Standard format RTR = 0: Data frame STDID[10:0] = 0: Standard ID = 0
Local acceptance filter mask_1 (MB[0].LAFM_1)	H'FFFF 0904	H'0000 0000	<ul style="list-style-type: none"> Clear: MASK is not set
Local acceptance filter mask_1 (MB[1].LAFM_1)	H'FFFF 0936	H'0000 0000	
Message data field_1 (MB[0].MSG_DATA01 to 67)	H'FFFF 0908 to H'FFFF 090F	H'0000	<ul style="list-style-type: none"> H'C1C2 is set as data for transmission.
Message data field_1 (MB[1].MSG_DATA01 to 67)	H'FFFF 093A to H'FFFF 0941	H'0000	
Transmit pending register_1 (TXPR_1)	H'FFFF 0820	H'0000 0002	<ul style="list-style-type: none"> TXPR[31:0] = H'0000 0002: Generates a transmission request for mailbox 1
Transmit acknowledge register 0_1 (TXACK0)	H'FFFF 0832	H'0002	<ul style="list-style-type: none"> Clears the transmit acknowledge flag

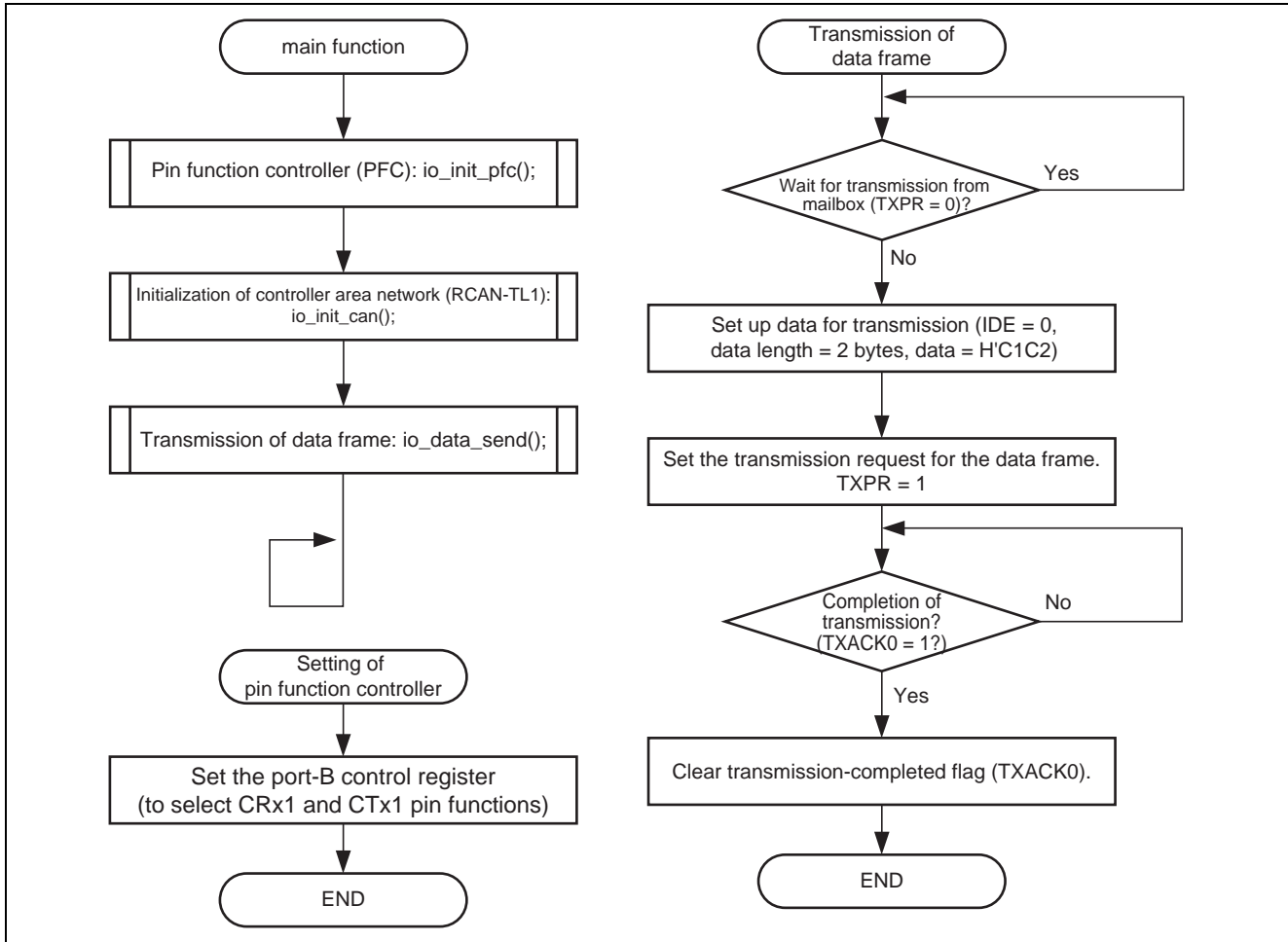


Figure 6 Example of Flow of Processing by the Sample Program

3. Sample Program

```

1  /*"FILE COMMENT"*****
2  *
3  *      System Name : SH7203 Sample Program
4  *      File Name   : main.c
5  *      Contents    : Application of CAN Module (Data Frame Transmission)
6  *      Version     : 1.00.00
7  *      Model       : M3A-HS30
8  *      CPU         : SH7203
9  *      Compiler    : SHC9.0.3.0
10 *      note        : The module transmits a single data frame in standard format (IDE = 0)
11 *                   with DLC = 2 and DATA = 0xC1C2, from mailbox 1 of CAN1 at a 500-kbps
12 *                   transfer rate over the CAN bus.
13 *
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21 *
22 *      history     : 2007.06.26 ver.1.00.00
23 *"FILE COMMENT END"*****/
24 #include <machine.h>
25 #include "iodefine.h"      /* SH7203 iodefine */
26
27 /* ---- prototype declaration ---- */
28 void main(void);
29 void io_init_pfc(void);
30 void io_init_can(void);
31 void io_data_send(void);
32
33 /* ---- symbol definition ---- */
34 #define CAN_GSR3 0x0008
35 #define CAN_MB1  0x0002

```

Figure 7 Sample Program Listing: "main.c" (1)

```

36  /*"FUNC COMMENT"*****
37  * Outline      : Sample Program main
38  *-----
39  * Include      : none
40  *-----
41  * Declaration  : void main(void);
42  *-----
43  * Function     : Sample Program main
44  *-----
45  * Argument     : none
46  *-----
47  * Return Value: none
48  *-----
49  * Notice      : none
50  /*"FUNC COMMENT END"*****/
51  void main(void)
52  {
53
54      /* ==== Setting of PFC ==== */
55      io_init_pfc();
56
57      /* ==== Initializing CAN module ==== */
58      io_init_can();
59
60      /* ==== CAN data frame transmission ==== */
61      io_data_send();
62
63      while(1){
64          /* loop */
65      }
66
67  }
68
69  /*"FUNC COMMENT"*****
70  * Outline      : Setting of PFC
71  *-----
72  * Include      : #include "iodefine.h"
73  *-----
74  * Declaration  : void io_init_pfc(void);
75  *-----
76  * Function     : Setting of Pin Function Controller(PFC)
77  *-----
78  * Argument     : none
79  *-----
80  * Return Value: none
81  *-----
82  * Notice      : none
83  /*"FUNC COMMENT END"*****/
84  void io_init_pfc(void)
85  {
86      /* ==== Setting of PFC ==== */
87      /* ---- Port B control register L3 ---- */
88      PORT.PBCRL3.BIT.PB10MD = 0x1; /* Set CRx1 */
89      PORT.PBCRL3.BIT.PB11MD = 0x1; /* Set CTx1 */
90
91  }
92

```

Figure 8 Sample Program Listing: "main.c" (2)

```

93  /*"FUNC COMMENT"*****
94  * Outline      : Setting of RCAN
95  *-----
96  * Include      : #include "iodefine.h"
97  *-----
98  * Declaration  : void io_init_can(void);
99  *-----
100 * Function     : Setting of Controller Area Network(RCAN)
101 *-----
102 * Argument     : none
103 *-----
104 * Return Value: none
105 *-----
106 * Notice       : none
107 *"FUNC COMMENT END"*****/
108 void io_init_can(void)
109 {
110     int i;
111
112     /* ==== Setting of power down mode(RCAN1) ==== */
113     CPG.STBCR5.BIT.MSTP52 = 0;
114
115     /* ==== Initializing CAN module ==== */
116     RCAN1.MCR.WORD |= 0x0001; /* CAN Interface reset mode */
117     while((RCAN1.GSR.WORD & CAN_GSR3) != CAN_GSR3){
118         /* Reset state waiting */
119     }
120
121     /* ---- RCAN mode selection ---- */
122     RCAN1.MCR.WORD |= 0x8000; /* RCAN-TL1 is not same as HCAN2 */
123
124     /* ---- Disable all can interrupt ---- */
125     RCAN1.IMR.WORD = 0xFFFF;
126
127     /* ---- Config baudrate ---- */
128     RCAN1.BCR1.WORD = 0x6300; /* tsg1=6(7bit),tsg2=3(4bit),sjw=0(1bit),bsp=0 */
129     RCAN1.BCR0.WORD = 0x0001; /* 500K bps */
130     // RCAN1.BCR0.WORD = 0x0003; /* 250K bps */
131     // RCAN1.BCR0.WORD = 0x0007; /* 125K bps */
132
133     /* ---- Config mailbox0 as reception slot ---- */
134     RCAN1.MB[0].CONTROL1.WORD = 0x0200; /* can receive data and remote frame */
135     RCAN1.MB[0].CONTROL0.LONG = 0x00000000; /* Initialize the Message Control Field */
136     RCAN1.MB[0].LAFM.LONG = 0x00000000;
137     for(i = 0; i < 8; i++){ /* data clear */
138         RCAN1.MB[0].MSG_DATA[i] = 0x00;
139     }
140     /* ---- Config mailbox1 as transmission slot ---- */
141     RCAN1.MB[1].CONTROL1.WORD = 0x0002; /* Can send data or remote frame, dlc=2 */
142     RCAN1.MB[1].CONTROL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
143     RCAN1.MB[1].LAFM.LONG = 0x00000000;
144     for(i = 0; i < 8; i++){ /* data clear */
145         RCAN1.MB[1].MSG_DATA[i] = 0x00;
146     }
147
148     /* ---- Clear interrupt flags ---- */
149     RCAN1.IRR.WORD = 0xffff;
150
151     /* ---- Clear reset and halt ---- */
152     RCAN1.MCR.WORD &= 0xffffc;
153     while( (RCAN1.GSR.WORD & CAN_GSR3) != 0x0000 ){
154         /* reset state is end */
155     }
156 }

```

Figure 9 Sample Program Listing: "main.c" (3)

```

157  /*"FUNC COMMENT"*****
158  * Outline      : Data Frame Transmission
159  *-----
160  * Include      : #include "iodefine.h"
161  *-----
162  * Declaration  : void io_data_send(void);
163  *-----
164  * Function     : RCAN1 is used to transmit a data frame.
165  *-----
166  * Argument     : none
167  *-----
168  * Return Value: none
169  *-----
170  * Notice      : none
171  *"FUNC COMMENT END"*****/
172  void io_data_send(void)
173  {
174      /* ---- Transmission waiting ---- */
175      while((RCAN1.TXPR0.LONG & CAN_MB1) == CAN_MB1){
176      }
177
178      /* ---- transmission data set ---- */
179      RCAN1.MB[1].CONTROL1.WORD = 0x0002; /* Can send data or remote frame, dlc=2 */
180      RCAN1.MB[1].CONTROL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
181      RCAN1.MB[1].MSG_DATA[0] = 0xc1;
182      RCAN1.MB[1].MSG_DATA[1] = 0xc2;
183
184      /* ---- transmit the data ---- */
185      RCAN1.TXPR0.LONG = CAN_MB1;
186
187      /* ---- Transmission completion waiting ---- */
188      while((RCAN1.TXACK0.WORD & CAN_MB1) != CAN_MB1){
189      }
190
191      /* ---- Transmission completion flag clear ---- */
192      RCAN1.TXACK0.WORD = CAN_MB1;
193
194  }
195
196  /* End of File */

```

Figure 10 Sample Program Listing: "main.c" (4)

4. Documents for Reference

- Software Manual
SH-2A, SH2A-FPU Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
SH7263 Group Hardware Manual
SH7203 Group Hardware Manual
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