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April 1st, 2010
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SH7137 Group

Sample Application for the CAN Module (Data Frame Reception)

Introduction

This application note describes the controller area network module (RCAN-ET) and provides an example of its application to data frame reception.

Target Devices

SH7137

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1. Preface

1.1 Specifications

- Transfer rate: 500 kbps
- Mailbox for transmission: Mailbox 0
- Received data frame is as follows.
ID: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

1.2 Module Used

- Controller area network (RCAN-ET)

1.3 Applicable Conditions

- MCU SH7137
- Operating frequency Internal clock: 80 MHz
Bus clock: 40 MHz
Peripheral clock: 40 MHz
- C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01 Release01
from Renesas Technology
- Compiler options: Default settings of the High-performance Embedded Workshop
(-cpu = sh2 -debug -gbr = auto -global_volatile = 0 -opt_range = all -infinite_loop = 0
-del_vacant_loop = 0 -struct_alloc = 1)

1.4 Related Application Note

None

2. Description of the Sample Application

This sample program employs the RCAN-ET module to receive a data frame in standard format (ID: 0).

2.1 Overview of Operations by the Module Used

The SH7137 CPU has an internal RCAN-ET module that support CAN2.0B and comply with ISO-11898.

The RCAN-ET module has 15 programmable transmit/receive mailboxes and one receive-only mailbox, each supporting a programmable reception filter mask, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-ET module. For details on the module, refer to the section on the controller area network in the *SH7137 Group Hardware Manual*.

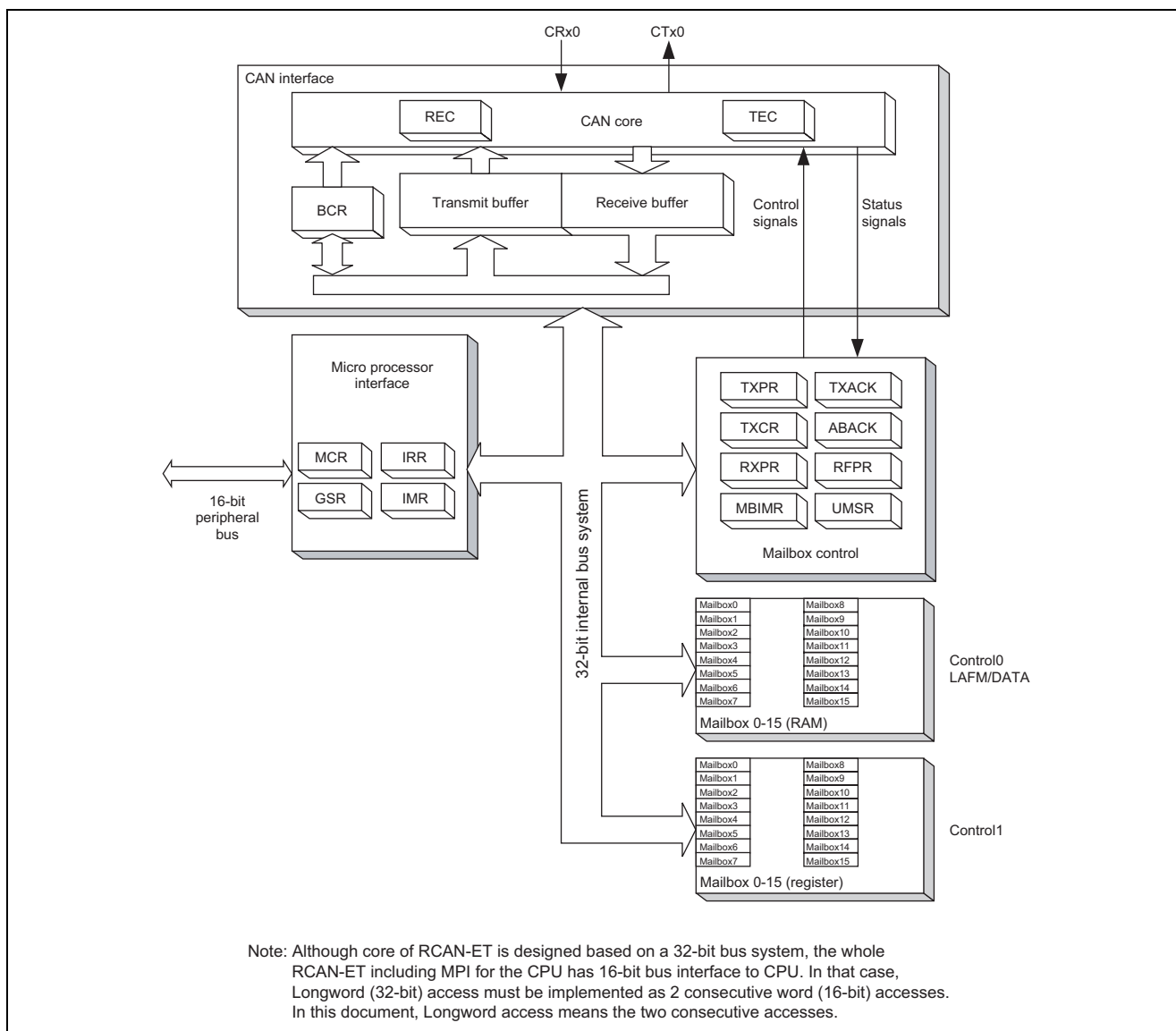


Figure 1 Structure of the RCAN-ET Module

2.2 Procedure for Setting the Module Used

This section describes initial settings for the reception of data frames by the RCAN-ET module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-ET module participates in CAN-bus activity. In initial settings in this sample program, one mailbox is set for transmission and reception respectively. Figures 2 and 3 show examples of the flow of initialization for the RCAN-ET module. For details on the settings made to individual registers, refer to the *SH7137 Group Hardware Manual*.

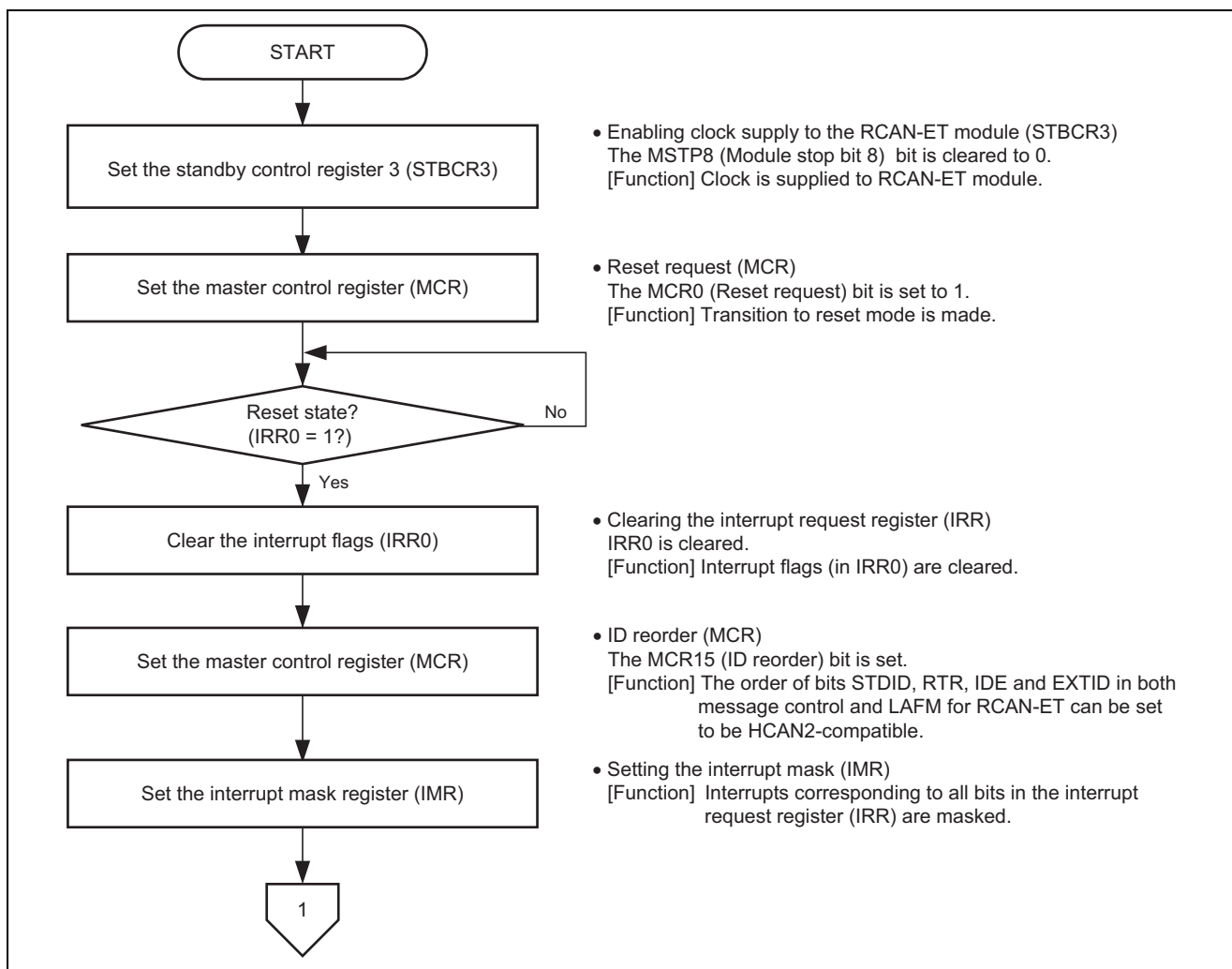


Figure 2 Example of Initialization Flow for the RCAN-ET Module (1)

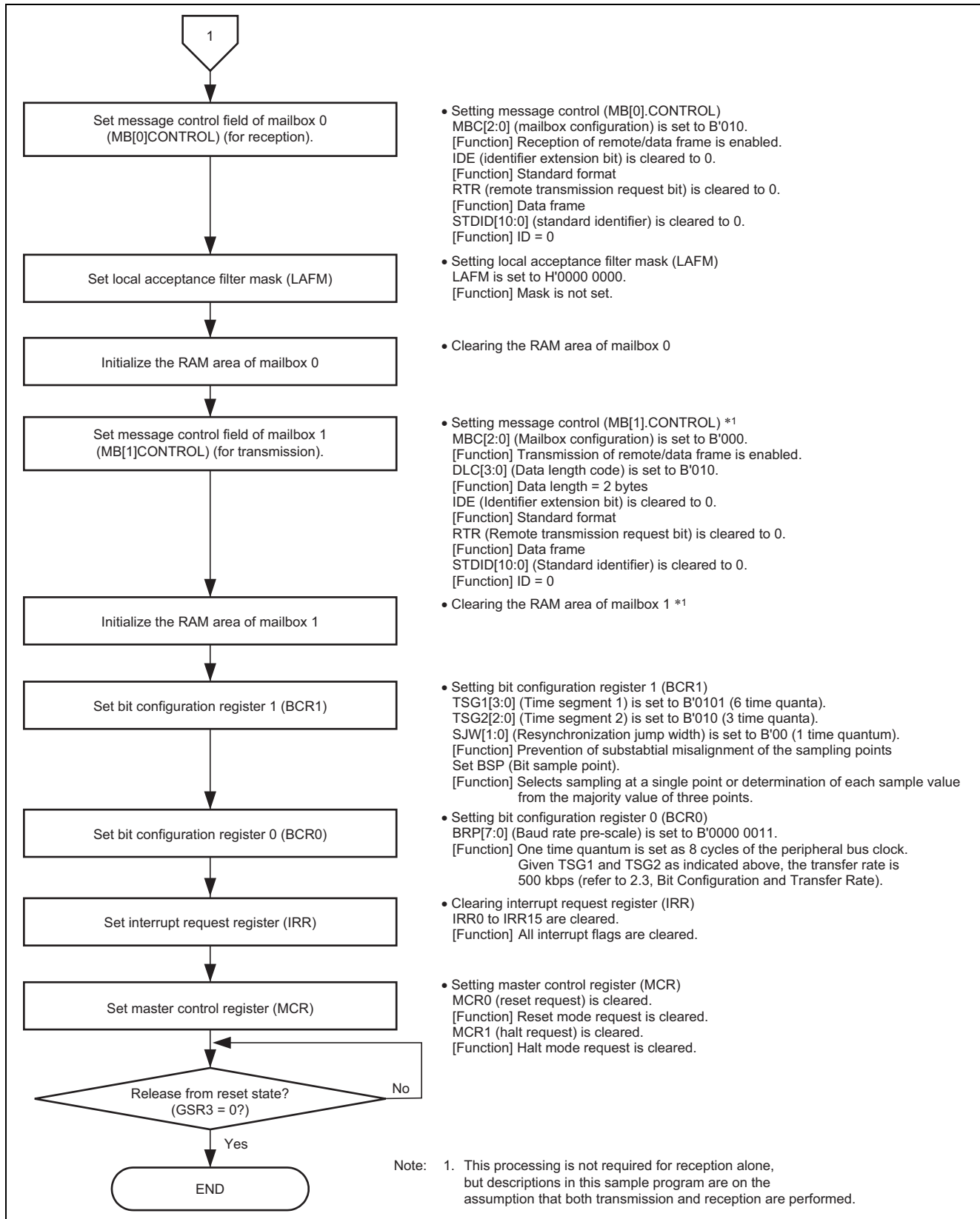


Figure 3 Example of Initialization Flow for the RCAN-ET Module (2)

2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

- (1) Synchronization segment (SS)
- (2) Propagation time segment (PRSEG)
- (3) Phase buffer segment 1 (PHSEG1)
- (4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (T_q). Figure 4 shows an example of the configuration of a bit in the case where $SS = 1T_q$, $PRSEG = 3T_q$, $PHSEG1 = 3T_q$, and $PHSEG2 = 3T_q$.

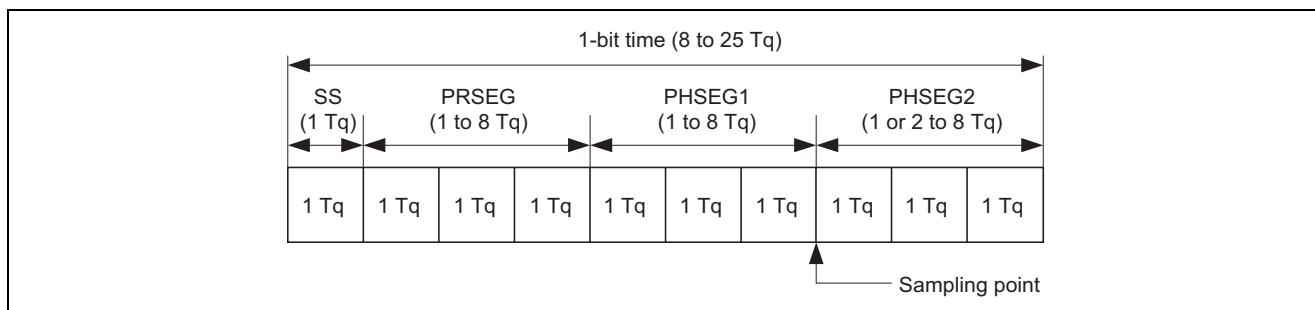


Figure 4 Configuration of One-Bit Time

In the RCAN-ET, the T_q of $PRSEG + PHSEG1$ is set to $TSG1[3:0]$ in bit configuration register 1 (BCR1) and the T_q of $PHSEG2$ is set to $TSG2[2:0]$ ($T_q = \text{set value} + 1$). Additionally, the number of cycles of the peripheral-bus clock corresponding to $1T_q$ is set in $BRP[7:0]$ of bit configuration register 0 (BCR0).

In the following description, $BRP[7:0]$, $TSG1[3:0]$ and $TSG2[2:0]$ indicate the register settings, and BRP , $TSEG1$, $TSEG2$, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the *SH7137 Group Hardware Manual*.

By definition, T_q for the RCAN-ET module is $1T_q = 2 \times (BRP[7:0] + 1) / \text{peripheral bus clock}$, and the transfer rate is calculated as follows.

$$\text{Transfer rate} = \text{peripheral bus clock} / (2 \times (BRP[7:0] + 1) \times \text{the number of } T_q \text{ in 1-bit time}) = \text{peripheral bus clock} / (2 \times (BRP[7:0] + 1) \times ((TSG1[3:0] + 1) + (TSG2[2:0] + 1) + 1))$$

The following restrictions apply to settings of the bit-configuration registers.

$$TSEG1 (\text{Min}) > TSEG2 \geq SJW (\text{Max}) \quad (SJW = 1 \text{ to } 4)$$

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

$$8 \leq TSEG1 + TSEG2 + 1 \leq 25 \text{ time quanta}$$

$$TSEG2 \geq 2$$

Since the settings in this sample program are as follows: peripheral bus clock = 40 MHz, $BRP = 3$, $TSG1 = 5$, $TSG2 = 2$, the transfer rate is calculated with the following formula.

$$\text{Transfer rate (bps)} = 40 \text{ M} (2 \times (3 + 1) \times ((5 + 1) + (2 + 1) + 1)) = 500 \text{ k}$$

2.4 Operation of the Sample Program

In this sample program, a data frame in standard format (ID: 0) is received in mailbox 0 at a transfer rate of 500 kbps. Figure 5 shows waveforms for data frame reception.

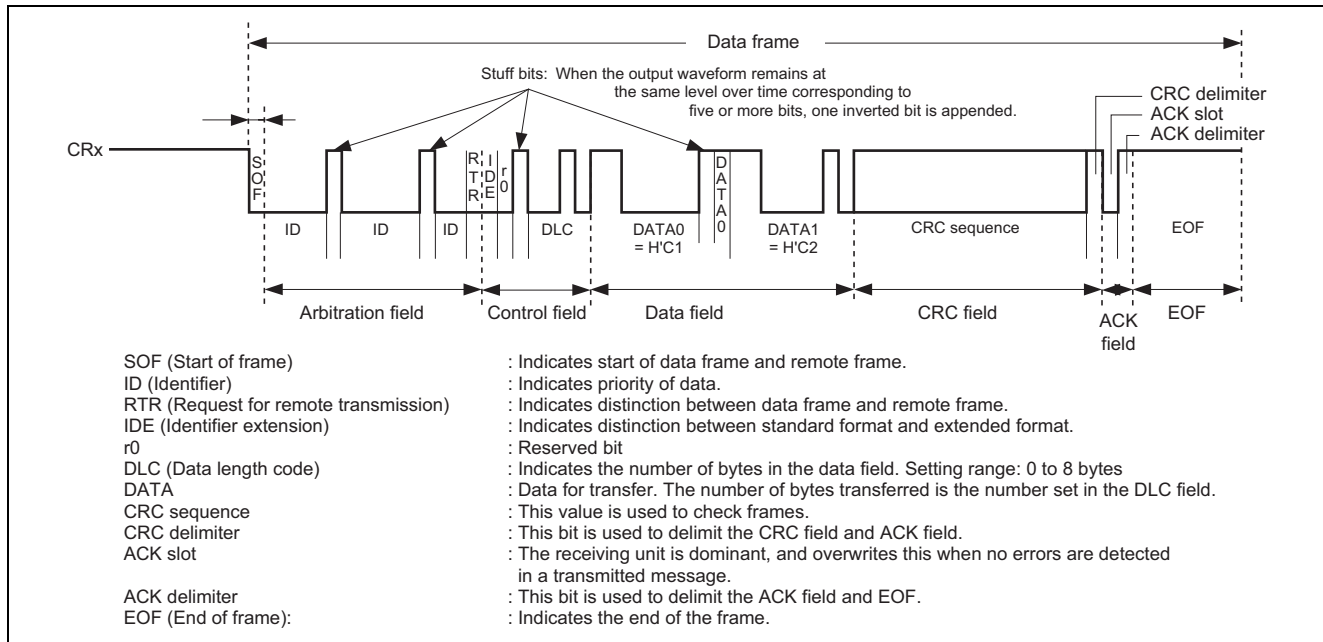


Figure 5 Waveform for Data Frame Reception by the RCAN-ET

2.5 Procedure of Processing by the Sample Program

Table 1 gives an example of the settings for the controller area network (RCAN-ET). Figure 6 shows an example of the flow of processing by this sample program.

Table 1 Register Settings for Controller Area Network (RCAN-ET)

Register Name	Address	Setting Value	Description
Standby control register 3 (STBCR3)	H'FFFF E806	H'F6	<ul style="list-style-type: none"> MSTP8 = 0: RCAN-ET runs
Master control register (MCR)	H'FFFF D800	H'0001	<ul style="list-style-type: none"> MCR0 = 1: Reset mode transition request
		H'1001	<ul style="list-style-type: none"> MCR15 = 1: RCAN-ET is not the same as HCAN2
		H'1000	<ul style="list-style-type: none"> MCR0 = 0: Release from reset mode
Interrupt mask register (IMR)	H'FFFF D80A	H'FFFF	<ul style="list-style-type: none"> Disables all interrupts of RCAN
Bit configuration register 1 (BCR1)	H'FFFF D804	H'5200	<ul style="list-style-type: none"> TSG1[3:0] = 0101: PRSEG + PHSEG1 = 6 T_q TSG2[2:0] = 010: PHSEG2 = 3 T_q SJW[1:0] = 00: SJW = 1 T_q BSP = 0: Bit sampling at one point
Bit configuration register 0 (BCR0)	H'FFFF D806	H'0003	<ul style="list-style-type: none"> BRP[7:0] = 3: 1 T_q = 8 × P_φ
Message control field (MB[0].CONTROL1H)	H'FFFF D910	H'0200	<ul style="list-style-type: none"> MBC[2:0] = 010: Enables reception of data frames and remote frames
Message control field (MB[1].CONTROL1H)	H'FFFF D930	H'0002	<ul style="list-style-type: none"> MBC[2:0] = 000: Enables transmission of data frames and remote frames DLC[3:0] = 0010: 2-byte data length
Message control field (MB[1].CONTROL0H)	H'FFFF D920	H'0000 0000	<ul style="list-style-type: none"> IDE = 0: Standard format RTR = 0: Data frame STDID[10:0] = 0: Standard ID = 0
Local acceptance filter mask (MB[0].LAFMH)	H'FFFF D904	H'0000 0000	<ul style="list-style-type: none"> Clear: MASK is not set
Message data field (MB[0].MSG_DATA_0)	H'FFFF D908	H'0000	<ul style="list-style-type: none"> Data field clear (RAM area is cleared)
Data frame receive pending register 0 (RXPR0)	H'FFFF D842	H'0001	<ul style="list-style-type: none"> RXPR[31:0] = H'0001: Clears the reception-completed flag

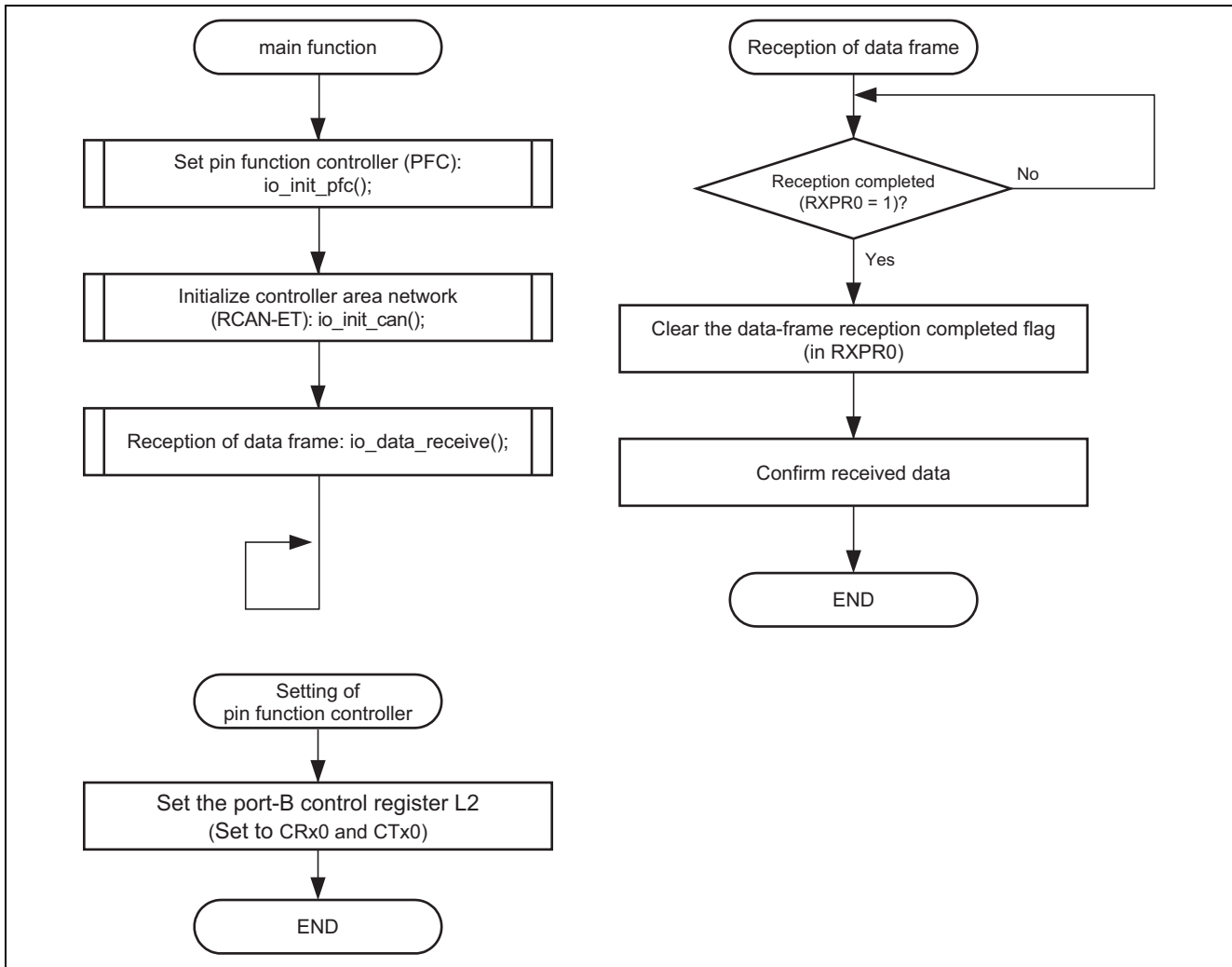


Figure 6 Example of Flow of Processing by the Sample Program

3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```

1  /*"FILE COMMENT"*****
2  *
3  *      System Name : SH7137 Sample Program
4  *      File Name   : main.c
5  *      Contents    : CAN Module Application (Data Frame Receive)
6  *      Version     : 1.00.00
7  *      Model       : M3A-HS37
8  *      CPU         : SH7137
9  *      Compiler    : SHC9.1.1.0
10 *      note        : CAN bus speed 500 kbps
11 *                  The mailbox 0 in CAN1 receives the data frame (ID=0,
12 *                  standard format) once to write the received data in RAM.
13 *
14 *                  <Caution>
15 *                  This sample program is for reference
16 *                  and its operation is not guaranteed.
17 *                  Customers should use this sample program for technical reference
18 *                  in software development.
19 *
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27 *
28 *                  history      : 2008.03.24 ver.1.00.00
29 *
30 * "FILE COMMENT END"*****
31 #include "iodefine.h"      /* SH7137 iodefine */
32
33 /* ---- prototype declaration ---- */
34 void main(void);
35 void io_init_pfc(void);
36 void io_init_can(void);
37 void io_data_receive(void);
38
39 /* ---- symbol definition ---- */
40 #define CAN_GSR3 0x0008
41 #define CAN_IRR0 0x0001
42 #define CAN_MB0  0x0001
43
44 /* ---- RAM allocation variable declaration ---- */
45 unsigned char  nIDE = 0;      /* ide */
46 unsigned char  nRTR = 0;     /* rtr */
47 unsigned char  nDLC = 0;     /* dlc */
48 unsigned int   nSID = 0;     /* sid */
49 unsigned int   nEID = 0;     /* eid */
50 unsigned char  gRcv_data[8]; /* data of message */

```

2. Sample Program Listing: main.c (2)

```

51  /*"FUNC COMMENT"*****
52  * Outline      : Sample program main
53  *-----
54  * Include      : non
55  *-----
56  * Declaration : void main(void);
57  *-----
58  * Function     : Sample program main
59  *-----
60  * Argument     : void
61  *-----
62  * Return Value: void
63  *-----
64  * Notice       : non
65  /*"FUNC COMMENT END"*****/
66 void main(void)
67 {
68
69     /* ==== Setting of PFC ==== */
70     io_init_pfc();
71
72     /* ==== Initializing CAN module ==== */
73     io_init_can();
74
75     /* ==== CAN data frame reception ==== */
76     io_data_receive();
77
78     while(1){
79         /* loop */
80     }
81
82 }
83
84 /*"FUNC COMMENT"*****
85 * Outline      : PFC setting
86 *-----
87 * Include      : #include "iodefine.h"
88 *-----
89 * Declaration : void io_init_pfc(void);
90 *-----
91 * Function     : Pin function CTRLler (PFC) setting
92 *-----
93 * Argument     : void
94 *-----
95 * Return Value: void
96 *-----
97 * Notice       : non
98 /*"FUNC COMMENT END"*****/
99 void io_init_pfc(void)
100 {
101     /* ==== Setting of PFC ==== */
102     /* ---- Port B CTRL register L2 ---- */
103     PFC.PBCRL2.BIT.PB7MD = 0x6; /* Set CRx0 */
104     PFC.PBCRL2.BIT.PB6MD = 0x6; /* Set CTx0 */
105     PFC.PBIORL.BIT.B7    = 0; /* PB7(CRX0) input */
106     PFC.PBIORL.BIT.B6    = 1; /* PB6(CTX0) output */
107 }
108

```

3. Sample Program Listing: main.c (3)

```

109  /*"FUNC COMMENT"*****
110  * Outline      : RCAN setting
111  *-----
112  * Include      : #include "iodefine.h"
113  *-----
114  * Declaration : void io_init_can(void);
115  *-----
116  * Function    : Controller area network (RCAN) set
117  *-----
118  * Argument    : void
119  *-----
120  * Return Value: void
121  *-----
122  * Notice      : non
123  *"FUNC COMMENT END"*****/
124  void io_init_can(void)
125  {
126      int i;
127
128      /* ==== Setting of power down mode(RCAN) ==== */
129      STB.CR3.BYTE = 0xf6;          /* Module Standby Clear */
130                                  /* RCAN */
131
132      /* ==== Initializing CAN module ==== */
133      RCANET.MCR.WORD |= 0x0001;    /* CAN Interface reset mode */
134      while((RCANET.IRR.WORD & CAN_IRR0) != CAN_IRR0){
135          /* Reset state waiting */
136      }
137
138      /* ==== IRR = 1, GSR = 1 (Auto SET) ==== */
139
140      /* ---- Clear IRR0 ---- */
141      RCANET.IRR.WORD = 0x0001;
142
143      /* ---- RCAN mode selection(MCR15) ---- */
144      RCANET.MCR.WORD |= 0x8000;    /* RCAN-ET is not same as HCAN2 */
145
146      /* ---- Disable all can interrupt ---- */
147      RCANET.IMR.WORD = 0xffff; /*
148
149      ---- Config mailbox0 as reception slot ---- */
150      RCANET.MB[0].CTRL1.WORD = 0x0200; /* can receive data and remote frame */
151      RCANET.MB[0].CTRL0.LONG = 0x00000000; /* Initialize the Message Control Field */
152      RCANET.MB[0].LAFM.LONG = 0x00000000;
153      for(i = 0; i < 8; i++){ /* data clear */
154          RCANET.MB[0].MSG_DATA[i] = 0x00;
155      }
156
157      /* ---- Config mailbox1 as transmission slot ---- */
158      RCANET.MB[1].CTRL1.WORD = 0x0002; /* Can send data or remote frame, dlc=2 */
159      RCANET.MB[1].CTRL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
160      RCANET.MB[1].LAFM.LONG = 0x00000000;
161      for(i = 0; i < 8; i++){ /* data clear */
162          RCANET.MB[1].MSG_DATA[i] = 0x00;
163      }
164
165      /* ---- Config baudrate ---- */
166      RCANET.BCR1.WORD = 0x5200; /* tsg1=5(6 bit),tsg2=2(3 bit),sjw=0(1 bit),bsp=0 */
167      RCANET.BCR0.WORD = 0x0003; /* 500 Kbps */
168      // RCANET.BCR0.WORD = 0x0007; /* 250 Kbps */
169      // RCANET.BCR0.WORD = 0x000f; /* 125 Kbps */
170
171      /* ---- Clear interrupt flags ---- */
172      RCANET.IRR.WORD = 0xffff;

```

4. Sample Program Listing: main.c (4)

```

171     /* ---- Clear reset and halt ---- */
172     RCANET.MCR.WORD &= 0xf8fc;    /* MCR0,MCR1 clear */
173     while( (RCANET.GSR.WORD & CAN_GSR3) != 0x0000 ){
174         /* reset state is end */
175     }
176 }
177
178 /*"FUNC COMMENT"*****
179 * Outline      : Data frame receive
180 *-----
181 * Include      : #include "iodefine.h"
182 *-----
183 * Declaration  : void io_data_receive(void);
184 *-----
185 * Function     : Receives the data frame by using RCANET
186 *-----
187 * Argument     : void
188 *-----
189 * Return Value: void
190 *-----
191 * Notice       : non
192 *"FUNC COMMENT END"*****/
193 void io_data_receive(void)
194 {
195     int i;
196
197     /* ---- Reception completion waiting ---- */
198     while((RCANET.RXPRO.WORD & CAN_MB0) != CAN_MB0){
199     }
200
201     /* ---- Receive data storage ---- */
202     nIDE = RCANET.MB[0].CTRL0.BIT.IDE;
203     nRTR = RCANET.MB[0].CTRL0.BIT.RTR;
204     nDLC = RCANET.MB[0].CTRL1.BIT.DLC;
205     nSID = RCANET.MB[0].CTRL0.BIT.STDID;
206     nEID = RCANET.MB[0].CTRL0.BIT.EXDID;
207     if(nDLC > 8){
208         nDLC = 8;
209     }
210     for(i = 0; i < nDLC; i++){
211         gRcv_data[i] = RCANET.MB[0].MSG_DATA[i];
212     }
213
214     /* ---- Reception completion flag clear ---- */
215     RCANET.RXPRO.WORD = CAN_MB0;
216
217 }
218
219 /* End of File */

```

4. Documents for Reference

- Software Manual
SH-1/SH2/SH-DSP Software Manual (REJ09B0171)
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
SH7137 Group Hardware Manual (REJ09B0402)
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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Nov.19.08	—	First edition issued

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