Renesas Synergy™ Platform

S7G2 Group MCU to S5D9 Group MCU Migration Guide

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Introduction

This Application Note compares hardware peripherals, port select features, and functional differences between the Synergy S7G2 MCU Group and S5D9 MCU Group.

Target Device

Synergy S5D9 MCU Group

Contents

How to Use This Application Note

1. About this Document

This document is designed to provide the user with an overview of the functional, hardware, and electrical characteristic differences when migrating from the Synergy S7G2 MCU Group to the S5D9 MCU Group.

2. Audience

This document is intended for users who are designing application systems using the Synergy S5D9 MCU Group devices. Users are expected to have a technical understanding of the peripherals provided in the S7G2 MCU Group. This application note should be used in conjunction with the *S5D9 MCU Group User's Manual: Microcontrollers*.

The application note presents two major sections. The first section specifies functional and specification differences between the S7G2 MCU Group and the S5D9 MCU Group's, respectively. The second section details the differences in port functionality between the two MCU's.

3. References

Renesas provides the following documents for the Synergy S5 Series MCUs. Before using any of these documents, visit our web site to obtain the latest versions.

Document Type	Description	Description Title	Description No.
Datasheet S5D9 MCU Group	Overview and electrical characteristics of MCU.	S5D9 MCU Group Datasheet	R01DS0303EU0100
S5D9 MCU Group User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S5D9 MCU Group User's Manual: Microcontrollers	R01UM0004EU0100
Datasheet S7G2 MCU Group	Overview and electrical characteristics of MCU.	S7G2 MCU Group Datasheet	R01DS0262EU0100
S7G2 User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S7G2 MCU Group User's Manual: Microcontrollers	R01UM0001EU0120
Renesas Synergy Software Package (SSP) user's manual	API reference and introduction to SSP architecture and programming.	Renesas Synergy Software Package (SSP) User's Manual	R01US0171EU

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x.
1234	Decimal number. a decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.
Bit 4	Specifies the bit position in field or register.

1. Specification and Hardware Differences: Synergy S7G2 and S5D9 MCU Groups

Table 1.1 compares hardware compatibility and differences between the S7G2 MCU Group and S5D9 MCU Group. The table is ordered with increasing specificity from left to right. The left most column corresponds to a system as noted in the user manual for the S5D9 MCU Group or S7G2 MCU Group. Values in the S7G2 column represent whether a system, subsystem, or field in register exists/has a certain value. Values in the S5D9 column show the change in hardware, new feature addition, or notes a deprecated feature. The Reference column specifies the section in the S5D9 MCU Group User's Manual that can be referred to for more information.

Note: The following terms describe the functionality of the peripherals mentioned in the table below.

Terms	**Description**
Exists or Available	The peripheral or function is implemented for the particular MCU Group
Does Not Exist or Not Available	The peripheral specified has been removed (when compared to the other MCU Group) or does not exist in the MCU Group
Not Applicable	The criteria for comparison is invalid for the MCU Group

Table 1.1 Specification Difference (1 of 15)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
System	CPU Clock		240 MHz	120 MHz	2.1.3
	Trace (4-bit TPIU)		120 MHz	60 MHz	2.1.3
	CoreSight Register	PID0 (Initial Value)	00000001h	00000010h	2.6.3.2
Address Space	On-Chip flash	Program Flash	Up to 4 MB	Up to 2 MB	4.1
		Option-Setting Memory - 1	32 KB	4 KB	4.1
		Option-Setting Memory - 2	40 B	24 B	4.1
Option-Setting Memory	FSPR Bit. Responsible for Protection of Access Window and Startup Area Select Function		Present in AWSC Register	FSPR moved to AWS Register, AWSC Does Not Exist	7.2.3
Clock Generation Circuit	System Clock		Up to 240 MHz, Division ratios: 1, 2, 4, 8, 16, 32, 64	Up to 120 MHz, Division ratios: 1, 2, 4, 8, 16, 32, 64	Table 9.2
	USB-PHY Clock (USBMCLK)		20 or 24 MHz	12, 20 or 24 MHz	Table 9.2
	Trace Clock (TRCLK)		Up to 120 MHz	Up to 60 MHz	Table 9.2
	TCLK Pin Output (TCLK)		Up to 60 MHz	Up to 30 MHz	Table 9.2
	Main Clock Oscillator Mode Oscillation Control Register (MOMCR)		Bit 7 is Reserved	Bit 7 is AUTODRVEN, controls the drive capability auto switching	9.2.19

Table 1.1 Specification Difference (2 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
Low Power Mode	IIC0 (Interrupt Source)	Bus Interface	Operation Prohibited in Snooze mode	Selectable in Snooze Mode	Table 11.2
		IIC0_WUI	Cancels Software Standby Mode	Cancels Software Standby Mode and **Snooze Mode**	Table 11.3
	Module Stop Control	Register B (MSTPCRB)	Bit 14 is MSTPB14, ETHERC1 and EDMAC1 Module Stop	Bit 14 is Reserved	11.2.3
	Deep Software Standby	Interrupt Enable Register 1 (DPSIER1)	Bit 7 is DIRQ15E, enables canceling of Deep Software Standby mode via IRQ15-DS pin	Bit 7 is Reserved	11.2.13
		Interrupt Flag Register 1 (DPSIFR1)	Bit 7 is DIRQ15F, indicates Deep Software Standby cancel request via IRQ15-DS pin	Bit 7 is Reserved	11.2.17
		Interrupt Edge Register 1 (DPSIEGR1)	Bit 7 is DIRQ15EG, generates cancel request on falling/rising edge	Bit 7 is Reserved	11.2.21
Interrupts	Peripheral Function Interrupts	Number of Sources	316	315	Table 14.1
	Interrupt Request Source	ETHER_EINT1	Exists	Does Not Exist	
	DMAC Event Link Setting Register n (DELSRn (n = 0 to 7))		Bit 16 Does Not Exist	Bit 16 (IR Flag) notes the status of an individual DMA transfer request	14.2.7
			Bit 17 to 31 Do Not Exist	Bit 17 to 31 are reserved	14.2.7

Table 1.1 Specification Difference (3 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
Buses	CS Area Controller	Address/Data Multiplexed Bus	Not Available	Available	Table 15.3
	External Bus I/O Pins	ALE (Output)	Does Not Exist	Exists	Table 15.4
	CSn Control Register (CSnCR) (n = 0 to 7)		Bit 14 is reserved	Bit 14 is MPXEN, Address/Data Multiplexed I/O Interface Select	15.3.1
	CS Recovery Cycle Insertion Enable Register (CSRECEN)		Bit 8 to 15 are reserved	Bit 8 to 15 are RCVENMn, Multiplexed Bus Recovery Cycle Insertion Enable	15.3.3
	CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 7)		Bit 12 to 13 are reserved	Bit 12 to 13 are AWAIT[1:0], Address Cycle Wait Select	15.3.6
	Master Bus Control Register (BUSMCNT<master>)		Bit 8 is EWRES, Early Write Response	Bit 8 is reserved	15.3.19
Memory Protection Unit	Security		Does Not Exist	2 regions (PC)	Table 16.1
			Does Not Exist	4 regions (code flash, SRAM, secure function, secure function)	Table 16.1
I/O Ports Specification and Functions	GPIO	I/O Pins	172	133	Features Section
		CMOS I/O	163	124	Features Section
		5-V tolerant I/O	22	21	Features Section
		High Current (20 mA) Pins	24	18	Features Section

Table 1.1 Specification Difference (4 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
I/O Ports Specification and Functions	Pin Package	224 Pins	Available	Not Available	Table 20.1
	176 Pins Package	Port 2	P200 to P207, P212, P213	P200 to P214	Table 20.1
		Port 5	P500 to P507, P511 to P513	P500 to P508, P511 to P513	Table 20.1
		Port 7	P700 to P707	P700 to P708	Table 20.1
		Total I/O pins	126	133	Table 20.1
	144 Pins Package	Port 2	P200 to P207, P212, P213	P200 to P214	Table 20.1
		Port 5	P500 to P506, P511, P512	P500 to P506, P508, P511, P512	Table 20.1
		Total I/O pins	104	110	Table 20.1
	100 Pins Package	Port 2	P200, P201, P205 to P207, P212, P213	P200, P201, P205 to P214	Table 20.1
		Port 5	P500 to P504	P500 to P504, P508	Table 20.1
		Total I/O pins	70	76	Table 20.1
	Drive Capacity Switching	P201	Low	None	Table 20.2
		P212	Low	Low, Middle, High	Table 20.2
		P213	High	Low, Middle, High	Table 20.2
		P208 to P211, P214	None	Low, Middle, High	Table 20.2
		P400, P401	Middle	Low, Middle, High	Table 20.2
		P402, P403, P404	Low, Middle	Low, Middle, High	Table 20.2
		P511, P512	Middle	Low, Middle, High	Table 20.2
		P514, P515	Low, Middle, High	None	Table 20.2
		P807 to P813	Low, Middle, High	None	Table 20.2

Table 1.1 Specification Difference (5 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
I/O Ports Specification and Functions	Drive Capacity Switching	P902 to P904, P909 to P915	Low, Middle, High	None	Table 20.2
		PA02 to PA07, PA11 to PA15	Low, Middle, High	None	Table 20.2
		PB02 to PB07	Low, Middle, High	None	Table 20.2
	Port mn Pin Function Select Register (PmnPFS) (m = 0 to 9, A, B; n = 00 to 15)	Initial Value - P000 to P007	0000_0000h	0000_8000h	20.2.5
	Ethernet Control Register (PFENET)		Bit 5 is PHYMODE1. The PHYMODE1 bit specifies the PHY mode of ETHERC channel 1	Bit 5 is Reserved, no ETHERC channel 1 in S5D9	20.2.7
AGT	AGT Pin Select Register (AGTIOSEL)	Responsible for setting the AGTIO pin when using the AGTIO in Deep Software Standby mode and Software Standby mode	Refer to Manual	Refer to Manual	25.2.10
ETHERC	Peripheral Name	Ethernet Channel 1 (ETHERC1)	Exists	Does Not Exist	
	Specifications	Number of Channels	2	1	Table 29.1
EPTPC	Peripheral Name	EPTPC1	Exists	Does Not Exist	
	Synchronization Frame Processing units	SYNFP1	Exists	Does Not Exist	

Table 1.1 Specification Difference (6 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
EPTPC	Synchronization Frame Processing units	SYNFP0	Boundary Clock is Available	Boundary Clock is Not Available	Table 30.1
			Transparent Clock is Available	Transparent Clock is Not Available	Table 30.1
			E2E and P2P master/slave operation is Available	E2E and P2P master/slave operation is Not Available	Table 30.1
	Packet Relation Controller unit	PRC-TC	Exists	Does Not Exist	
		Status Register (PRSR)	Exists	Does Not Exist	
		Status Notification Enable Register (PRIPR)	Exists	Does Not Exist	
	ETHER_MINT	Interrupt Source Status Register (MIESR)	Bit 2 is SY1. SYNFP1 Status Flag	Bit 2 is Reserved, no SYNFP1 in S5D9	30.2.1
			Bit 3 is PRC. PRC-TC Status Flag	Bit 3 is Reserved, no PRC-TC in S5D9	30.2.1
			Bit 2 is SY1. SYNFP1 Status Interrupt Request Enable	Bit 2 is Reserved, no SYNFP1 in S5D9	30.2.2
			Bit 3 is PR. PRC-TC Status Interrupt Request Enable	Bit 3 is Reserved, no PRC-TC in S5D9	30.2.2
	EPTPC0 (PTP Module 0 for the Ethernet Controller)	SYNFP Reception Filter Register 1 (SYRFL1R)	Bit 1 is ANCE1, relays messages between ports 0 and 1 via PRC-TC	Bit 1 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 5 is SYNC1, relays messages between ports 0 and 1 via PRC-TC	Bit 5 is Reserved, no PRC-TC in S5D9	30.2.44

Table 1.1 Specification Difference (7 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
EPTPC	EPTPC0 (PTP Module 0 for the Ethernet Controller)	SYNFP Reception Filter Register 1 (SYRFL1R)	Bit 9 is FUP1, relays messages between ports 0 and 1 via PRC-TC	Bit 9 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 13 is DRQ1, relays messages between ports 0 and 1 via PRC-TC	Bit 13 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 17 is DRP1, relays messages between ports 0 and 1 via PRC-TC	Bit 17 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 21 is PDRQ1, relays messages between ports 0 and 1 via PRC-TC	Bit 21 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 25 is PDRP1, relays messages between ports 0 and 1 via PRC-TC	Bit 25 is Reserved, no PRC-TC in S5D9	30.2.44
			Bit 29 is PDFUP1, relays messages between ports 0 and 1 via PRC-TC	Bit 29 is Reserved, no PRC-TC in S5D9	30.2.44
		SYNFP Reception Filter Register 2 (SYRFL2R). Specifies filtering for the reception of PTP messages	Bit 1 is MAN1, relays messages between ports 0 and 1 via PRC-TC	Bit 1 is Reserved, no PRC-TC in S5D9	30.2.45
			Bit 5 is SIG1, relays messages between ports 0 and 1 via PRC-TC	Bit 5 is Reserved, no PRC-TC in S5D9	30.2.45
			Bit 29 is ILL1. Handles the PRC-TC relays messages between ports 0 and 1.	Bit 29 is Reserved, no PRC-TC in S5D9	30.2.45

Table 1.1 Specification Difference (8 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
EPTPC	EPTPC0 (PTP Module 0 for the Ethernet Controller)	SYNFP Operation Setting Register (SYCONFR)	Bit 20 is TCMOD, relays messages between ports 0 and 1 via PRC-TC	Bit 20 is Reserved	30.2.74
	EPTPC Configuration (EPTPC_CFG)	Bypass 1588 Module Register (BYPASS)	Bit 16 is BYPASS1, Bypass 1588 module for Ether channel 1	Bit 16 is Reserved, no Ether channel 1 in S5D9	30.2.79
	Local MAC Address Register	Channel 0 (PRMACRU0, PRMACRL0)	Exists	Does Not Exist	
		Channel 1 (PRMACRU1, PRMACRL1)	Exists	Does Not Exist	
	Packet Transmission Control Register (TRNDISR)		Exists	Does Not Exist	
	Relay Mode Register (TRNMR)		Exists	Does Not Exist	
	Cut-Through Transfer Start Threshold Register (TRNCTTDR)		Exists	Does Not Exist	
EDMAC	Peripheral Name	Ethernet DMA Controller 1 (EDMAC1)	Exists	Does Not Exist	
	PTPEDMAC	Status Register (EESR)	Bit 7 is RPORT. Indicates which Ethernet port was used for receiving a PTP message	Bit 7 is Reserved	31.2.7
		Status Interrupt Enable Register (EESIPR)	Bit 7 is RPORTIP. Receive Port Interrupt Request Enable	Bit 7 is Reserved	31.2.9
	Specifications	Channel Priority	EDMAC0 > EDMAC1 > PTPEDMAC	EDMAC0 > PTPEDMAC	31.3.5

Table 1.1 Specification Difference (9 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
USBHS	PHY Setting Register (PHYSET)	Input System Clock Frequency - CLKSEL [1:0] (Bit 5, Bit 4) = 00	Settings Prohibited	12 MHz	33.2.17
I2C Bus Interface	I2C-Bus Wakeup Unit Register 2 (ICWUR2)		Bit 0 is Reserved	Bit 0 is WUSEN, sets the Wake-up Function Synchronous Enable	36.2.12
			Bit 1 is Reserved	Bit 1 is WUASYF, sets the Wake-up Function Asynchronous Operation Status Flag	36.2.12
			Bit 2 is Reserved	Bit 2 is WUSYF, sets the Wake-up Function Synchronous Operation Status Flag	36.2.12
			Value after Reset for Bit 1 is 1. IIC asynchronous circuit enable condition	Value after Reset for Bit 1 is 0, sets the IIC synchronous circuit enable condition	36.2.12
SPI	Specification	Data Format	Byte Swap Operating Function is Not Available	Byte Swap Operating Function is Available	Table 38.1
	Slave SPI Operation	Max Transfer Rate	PCLKA/6	PCLKA/4	Table 38.5
	Slave (clock synchronous operation)	Max Transfer Rate	PCLKA/6	PCLKA/4	Table 38.5
	Data Control Register (SPDCR)		Bit 6 is Reserved	Bit 6 is SPBYT, sets the data width of access to the SPI Data Register	38.2.9
	Data Control Register 2 (SPDCR2)		Does Not Exist	Exists	38.2.15

Table 1.1 Specification Difference (10 of 16)

SPECIFICATION		S7G2	S5D9	S5D9 HUM REFERENCE
SSIE	Status Register (SSISR)	Bit 6, Bit 5 is TCHNO[1:0], transmits Channel Number	Bit 6, Bit 5 is Reserved	41.4.2
	FIFO Control Register (SSIFCR)	Bit 5, Bit 4 is RTRG[1:0], receives FIFO Threshold Setting Trigger	Bit 5, Bit 4 is Reserved	41.4.3
		Bit 7, Bit 6 is TTRG, transmits FIFO Threshold Setting Trigger	Bit 7, Bit 6 is Reserved	41.4.3
		Bit 11 is Reserved	Bit 11 is BSW, controls byte swap of register access for SSIFTDR and SSIFRDR	41.4.3
	FIFO Status Register (SSIFSR)	RDC width is 4 bits [11:8]	RDC width is 6 bits [13:8]	41.4.4
		TDC width is 4 bits [27:24]	TDC width is 6 bits [29:24]	41.4.4
	Audio Format Register (SSITDMR/SSIOFR)	Bit 1, Bit 0 is Reserved	Bit 1, Bit 0 is OMOD[1:0], sets the Audio format	41.4.7
		Bit 8 is CONT, controls WS Continue Mode	Bit 8 is LRCONT, controls LRCK/FS continuation	41.4.7
		Bit 9 is Reserved	Bit 9 is BCKASTP, controls output of BCK to the SSIBCK pin.	41.4.7
	Status Control Register (SSISCR)	Does Not Exist	Exists	41.4.8

Table 1.1 Specification Difference (11 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
Boundary Scan	VLO (Switching Regulator Pin)		Cannot be Boundary Scanned	VLO Does Not Exist	45.4
	P200 (Non Maskable Interrupt Pin)		Cannot be Boundary Scanned	Can be Boundary Scanned	45.4
	Register	JTIDR (ID Code Register)	Value after reset is 0824_9447h	Value after reset is 0832_9447h	Table 45.3
ADC12	No. of Analog Channels	Unit 1	12	11	47.1
	Analog Input Channel	Unit 0	AN000 to AN006 AN016 to AN021	AN000 to AN007 AN016 to AN020	Table 47.2
	Analog Input Channel	Unit 1	AN100 to AN106 AN116 to AN120	AN100 to AN103 AN105 to AN107 AN116 to AN119	Table 47.2
	ADCSR	(Unit 0) DBLANS [00111]	Does Not Exist	AN007	Table 47.4
		(Unit 0) DBLANS [10101]	AN021	Does Not Exist	Table 47.4
		(Unit 1) DBLANS [00100]	AN104	Does Not Exist	Table 47.4
		(Unit 1) DBLANS [00111]	Does Not Exist	AN107	Table 47.4
		(Unit 1) DBLANS [10100]	AN120	Does Not Exist	Table 47.4
	ADSSTR07.SST[7:0] bits	Unit 0	Does Not Exist	AN007	Table 47.8
		Unit 1	Does Not Exist	AN107	Table 47.8
	ADSSTRL.SST[7:0] bits	Unit 0	AN016-AN021	AN016-AN020	Table 47.8
		Unit 1	AN116-AN120	AN116-AN119	Table 47.8
	A/D Channel Select	Register A0 (ADANSA0)	Bit 7 is Reserved	Bit 7 is ANSA07, additional A/D Conversion Channel	47.2.4
		Register A1 (ADANSA1)	Bit 5 is ANSA21, A/D Conversion Channel	Bit 5 is Reserved	47.2.5

Table 1.1 Specification Difference (12 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
ADC12	A/D Channel Select	Register B0 (ADANSB0)	Bit 7 is Reserved	Bit 7 is ADSB07, additional A/D Conversion Channel	47.2.6
		Register B1 (ADANSB1)	Bit 5 is ANSB21, A/D Conversion Channel	Bit 5 is Reserved	47.2.7
	A/D-Converted Value Addition/Average	Channel Select Register 0 (ADADS0)	Bit 7 is Reserved	Bit 7 is ADS07, additional A/D-Converted Value Addition/Average Channel	47.2.8
		Channel Select Register 1 (ADADS1)	Bit 5 is ADS21, A/D-Converted Value Addition/Average Channel	Bit 5 is Reserved	47.2.9
	A/D Compare Function Window A	Channel Select Register 0 (ADCMPANSR0)	Bit 7 is Reserved	Bit 7 is CMPCHA07, additional Compare Window A Channel	47.2.20
		Channel Select Register 1 (ADCMPANSR1)	Bit 5 is CMPCHA21, Compare Window A Channel	Bit 5 is Reserved	47.2.21
		Comparison Condition Setting Register 0 (ADCMPLR0)	Bit 7 is Reserved	Bit 7 is CMPLCHA07, additional Compare Window (Comparison Condition)	47.2.23
		Comparison Condition Setting Register 1 (ADCMPLR1)	Bit 5 is CMPLCHA21, Compare Window A Comparison Condition	Bit 5 is Reserved	47.2.24

Table 1.1 Specification Difference (13 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
ADC12	A/D Compare Function Window A	Channel Status Register 0 (ADCMPSR0)	Bit 7 is Reserved	Bit 7 is CMPSTCHA07, additional Compare Window (Flag)	47.2.27
		Channel Status Register1 (ADCMPSR1)	Bit 5 is CMPSTCHA21, Compare Window A Flag	Bit 5 is Reserved	47.2.28
	A/D Compare Function Window B	Channel Select Register (ADCMPBNSR)	Refer to Manual	Refer to Manual	47.2.30
	A/D Programmable Gain Amplifier	Control Register (ADPGACR)	Value after reset for Bits: 0, 3, 4, 7, 8, 11, 12, 15 is 1	Value after reset for Bits: 0, 3, 4, 7, 8, 11, 12, 15 is 0	47.2.33
		Differential Input Control Register (ADPGADCR0)	Value after reset for Bits: 3, 7, 11, 15 is 0	Value after reset for Bits: 3, 7, 11, 15 is 1	47.2.35
DAC12	D/A Amplifier Stabilization Wait Control Register (DAASWCR)		Does Not Exist	Exists	48.2.6
	Initialization Procedure with the Output Amplifier		Refer to Manual	Refer to Manual	48.6.5
CTSU	CTSU Control Register 0 (CTSUCR0)		Bit 7 is Reserved	Bit 7 is CTSUTXVSEL, CTSU Transmission Power Supply Select	51.2.1
SRAM	Error Protocol		DED	ECC	53.1
	ACCESS Wait State Requirement (with/without DED or ECC)	Frequency < 60 MHz	No	No	Table 53.1
		120 MHz > Frequency > 60 MHz	No	Yes	Table 53.1
		240 MHz > Frequency > 120 MHz	Yes	Not Applicable	Table 53.1

Table 1.1 Specification Difference (14 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
SRAM	ACCESS Wait State Requirement (for SRAMHS)	240 MHz > Frequency > 200 MHz	Yes	Not Applicable	Table 53.1
		Frequency < 200 MHz	No	Not Applicable	Table 53.1
	SRAM Wait State Control Register (SRAMWTSC)		Bit 0 is SRAM0DWRWTEN, adds wait state in write access cycle to SRAM0	Bit 0 is Reserved	53.2.3
			Bit 4 is SRAMHSWTEN, adds wait state in read access cycle to SRAMHS	Bit 4 is Reserved	53.2.3
	ECC	Operating Mode Control Register (ECCMODE)	Refer to Manual	Refer to Manual	53.2.4
		Test Control Register (ECCETST)	Does Not Exist	Exists	53.2.9
	Access Cycle - SRAMHS (Parity area)	Word Access	2 or 3 Read Cycles	2 Read Cycles	53.3.7
	Access Cycle - SRAM0 (DED/EEC area), SRAM0 (Parity area), SRAM1 (Parity area)	Word Access	4 or 5 Read Cycles	2 or 3 Read Cycles	53.3.7
	Access Cycle - SRAM0 (DED/EEC area), SRAM0 (Parity area), SRAM1 (Parity area)	Word Access	4 or 5 Write Cycles	2 Write Cycles	53.3.7
	Access Cycle - SRAM0 (DED/EEC area)	Byte Access	6 Write Cycles	4 Write Cycles	53.3.7

Table 1.1 Specification Difference (15 of 16)

SPECIFICATION			S7G2	S5D9	S5D9 HUM REFERENCE
Standby SRAM	Access Cycle - Word Access (Read Cycles)	ICLK = PCLKA (for S7G2) ICLK = PCLKB (for S5D9)	5 ICLK	3 ICLK	Table 54.2
	Access Cycle - Word Access (Write Cycles)	ICLK = PCLKA (for S7G2) ICLK = PCLKB (for S5D9)	4 ICLK	2 ICLK	Table 54.2
	Access Cycle - Word Access (Read Cycles)	ICLK > PCLKA (for S7G2) ICLK > PCLKB (for S5D9)	2 ICLK + 2 to 3 PCLKA	1 ICLK + 2 to 3 PCLKB	Table 54.2
	Access Cycle - Word Access (Write Cycles)	ICLK > PCLKA (for S7G2) ICLK > PCLKB (for S5D9)	2 ICLK + 1 to 2 PCLKA	1 ICLK + 1 to 2 PCLKB	Table 54.2
FLASH Memory	Code Flash Memory	Capacity	Up to 4 MB	Up to 2 MB	Table 55.1
		Read Cycle	80 MHz	40 MHz	Table 55.1
		Units of Programming	256 B	128 B	Table 55.1
	Data Flash Memory	Capacity	64 KB	64 KB	Table 55.1
		Units of Programming	4 B	4/8/16 B	Table 55.1
		Units of Erasure	64 B	64/128/256 B	Table 55.1
	Read Cycle	Cache hit: 1 cycle Cache miss: 3 cycles	160 MHz < ICLK frequency ≤ 240 MHz	80 MHz < ICLK frequency ≤ 120 MHz	Table 55.1
		Cache hit: 1 cycle Cache miss: 2 cycles	80 MHz < ICLK frequency ≤ 160 MHz	40 MHz < ICLK frequency ≤ 80 MHz	Table 55.1
		Cache hit: 1 cycle Cache miss: 1 cycle	ICLK frequency ≤ 80 MHz	ICLK frequency ≤ 40 MHz	Table 55.1

Table 1.1 Specification Difference (16 of 16)

SPECIFICATION		S7G2	S5D9	S5D9 HUM REFERENCE
FLASH Memory	Background Operation	Data Flash Memory is not accessible during flash code programming	Data Flash Memory is accessible during flash code programming	Table 55.1
	Conditions for Background Operation Availability	Refer to Manual	Refer to Manual	Table 55.11
	Configuration Area Bit Map	Base R-address is 4012_0000h FSPR Bit Address is 0040h	Base R-address is 0100_A100h FSPR Bit Address is 0064h	55.6.1
Clock Change step	Register setting when clock setting needs to be changed	The procedure is simpler than S5D9	Specific procedure is necessary when changing mode or clocks	11.4 Module-Stop Function 9.2.1 System Clock Division Control Register (SCKDIVCR) 9.2.3 System Clock Source Control Register (SCKSCR) 11.7.1 Transition to Software Standby Mode 11.7.2 Canceling Software Standby Mode 11.9.1 Transition to Deep Software Standby Mode

2. Port Select Function Difference

Tables 2.1, 3.1, and 4.1 compare the PSEL, ASEL, and ISEL functions for the S7G2 MCU Group and S5D9 MCU Group respectively. For each port number, the first row specifies the bitwise select values. The second row specifies the functionality enabled by the select values on the S7G2 MCU Group. The third column specifies the functionality enabled by the select values on the S5D9. Differences in functionality are notated with bold text and highlighted background. The comments section provides additional details or specifies the migration type from S7G2 MCU Group to S5D9 MCU Group. For more information on the comments column please refer to the Typography Notation table after the contents page in the How to use this Application Note section.

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

The following typographic notation is used for the pin differences sections of the document to denote the changes happening at the individual ports:

Example	Description
▲PIXD0_B	The '▲' denotes that signal PIXD0_B is being added to the previously unused/reserved or replacing a deprecated function.
▼ET1_TX_CLK	The '▼' denotes that signal ET1_TX_CLK is being deprecated at the bit position and being replaced by a new signal or remain unused/reserved.

The following gradients visualize whether signals are added, replaced, or removed from the S7G2 and S5D9 MCU Group.

Example	Description
	Highlights a bit position where a new function is being added to the previously unused/reserved bit position.
	Highlights a bit position where a new function is replacing an existing function in the bit position.
	Highlights a bit position being reserved by deprecating the function that existed previously at that bit position.

Appendix 1. 100 Pin Package

Table 2.1 100 Pin Package Difference (1 of 9)

PORT	MCU	SELECT								COMMENTS
P003		ASEL								Alternate Name AN007
	S7G2	PGAVSS000								
	S5D9	PGAVSS000/AN007								
P007		ASEL								Alternate Name AN107
	S7G2	PGAVSS100								
	S5D9	PGAVSS100/AN107								
P100		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5B_D
	S7G2	AGTIO0_A	GTETRGA_A	-	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
	S5D9	AGTIO0_A	GTETRGA_A	**GTIOC5B_D**	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
	S5D9	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
P101		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5A_D
	S7G2	AGTEE0	GTETRGB_A	-	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
	S5D9	AGTEE0_A	GTETRGB_A	**GTIOC5A_D**	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D1	DQ1	LCD_CLK_A	IRQ1_A					
	S5D9	D1	DQ1	LCD_CLK_A	IRQ1_A					

Table 2.1 100 Pin Package Difference (2 of 9)

PORT	MCU	SELECT								COMMENTS
P102		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01010b	PSEL 01011b	▲CRX0_D
	S7G2	AGTO0	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
	S5D9	AGTO0_A	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
		PSEL 01011b	PSEL 10000b	PSEL 11001b						
	S7G2	DQ2	-	LCD_TCON0_A						
	S5D9	DQ2	**CRX0_D**	LCD_TCON0_A						
P103		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 10000b	▲CTX0_D
	S7G2	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	-	
	S5D9	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	**CTX0_D**	
		PSEL 11001b								
	S7G2	LCD_TCON1_A								
	S5D9	LCD_TCON1_A								
P104		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1B_C
	S7G2	GTETRGB_B	-	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
	S5D9	GTETRGB_B	**GTIOC1B_C**	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
		ISEL								
	S7G2	IRQ1_B								
	S5D9	IRQ1_B								
P105		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1A_C
	S7G2	GTETRGA_C	-	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
	S5D9	GTETRGA_C	**GTIOC1A_C**	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
		ISEL								
	S7G2	IRQ0_B								
	S5D9	IRQ0_B								

Table 2.1 100 Pin Package Difference (3 of 9)

PORT	MCU	SELECT								COMMENTS
P106		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲AGTOB0_C
	S7G2	-	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
	S5D9	**AGTOB0_C**	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
P107		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b		▲AGTOA0_C
	S7G2	-	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
	S5D9	**AGTOA0_C**	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
P108		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00110b				▲GTOULO_C
	S7G2	TMS/SWDIO	-	GTIOC0B_A	CTS9_B	SSLB0_B				
	S5D9	TMS/SWDIO	**GTOULO_C**	GTIOC0B_A	CTS9_B	SSLB0_B				
P112		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	PSEL 10010b	▲SCK1_D ▲SSLB0_B
	S7G2	HRMON1	GTIOC3B_A	TXD2_B	-	-	A4	A4	SSISCK0_B	
	S5D9	HRMON1	GTIOC3B_A	TXD2_B	**SCK1_D**	**SSLB0_B**	A4	A4	SSISCK0_B	
		PSEL 11001b								
	S7G2	LCD_DATA11_A								
	S5D9	LCD_DATA11_A								
P113		PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b			▲GTIOC2A_C
	S7G2	-	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
	S5D9	**GTIOC2A_C**	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
P114		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC2B_C
	S7G2	-	A2	A2	SSIRXD0_B	LCD_DATA9_A				
	S5D9	**GTIOC2B_C**	A2	A2	SSIRXD0_B	LCD_DATA9_A				
P115		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC4A_C
	S7G2	-	A1	A1	SSITXD0_B	LCD_DATA8_A				
	S5D9	**GTIOC4A_C**	A1	A1	SSITXD0_B	LCD_DATA8_A				

Table 2.1 100 Pin Package Difference (4 of 9)

PORT	MCU	SELECT								COMMENTS
P207		PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 10001b	PSEL 11001b				▲QSSL_C ▲LCD_DATA23_B
	S7G2	SSLB2_A	A17	TS2	-	-				
	S5D9	SSLB2_A	A17	TS2	**QSSL_C**	**LCD_DATA23_B**				
VCC(IO)		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P208	S5D9	**GTOVLO_C**	**QIO3_C**	**SD0DAT0_B**	**ET0_LINKSTA_C**	**ET0_LINKSTA_C**	**LCD_DATA18_B**	**TDATA3**		
VLO		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P209	S5D9	**GTOVUP_C**	**QIO2_C**	**SD0WP_B**	**ET0_EXOUT_C**	**ET0_EXOUT_C**	**LCD_DATA19_B**	**TDATA2**		
VLO		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P210	S5D9	**GTIW_C**	**QIO1_C**	**SD0CD_B**	**ET0_WOL_C**	**ET0_WOL_C**	**LCD_DATA20_B**	**TDATA1**		
VSS(IO/DCDC)		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P211	S5D9	**GTIV_C**	**QIO0_C**	**SD0CMD_B**	**ET0_MDIO_B**	**ET0_MDIO_B**	**LCD_DATA21_B**	**TDATA0**		
P212/EXTAL		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	ISEL				▲GTIOC0A
	S7G2	AGTEE1	GTETRGD_A	-	RXD1_A	IRQ3_B				
	S5D9	AGTEE1_A	GTETRGD_A	**GTIOC0B_D**	RXD1_A	IRQ3_B				
P213/XTAL		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01010b	ISEL				▲GTIOC0A
	S7G2	GTETRGC_A	-	TXD1_A	ADTRG1_A	IRQ2_B				
	S5D9	GTETRGC_A	**GTIOC0A_D**	TXD1_A	ADTRG1_A	IRQ2_B				
VCL1		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P214	S5D9	**GTIU_C**	**QSPCLK_C**	**SD0CLK_B**	**ET0_MDC_B**	**ET0_MDC_B**	**LCD_DATA22_B**	**TCLK**		

Table 2.1 100 Pin Package Difference (5 of 9)

PORT	MCU	SELECT								COMMENTS
P300		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00110b					▲GTOUUP_C
	S7G2	TCK/SWCLK	-	GTIOC0A_A	SSLB1_B					
	S5D9	TCK/SWCLK	**GTOUUP_C**	GTIOC0A_A	SSLB1_B					
P301		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	▲AGTIO0_F ▲CTS9_D
	S7G2	-	GTOULO_A	GTIOC4B_A	RXD2_A	-	SSLB2_B	A6	A6	
	S5D9	**AGTIO0_F**	GTOULO_A	GTIOC4B_A	RXD2_A	**CTS9_D**	SSLB2_B	A6	A6	
		PSEL 11001b	ISEL							
	S7G2	LCD_DATA13_A	IRQ6_A							
	S5D9	LCD_DATA13_A	IRQ6_A							
P304		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL		▲GTOWLO_C
	S7G2	-	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
	S5D9	**GTOWLO_C**	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
P305		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b	ISEL		▲GTOWUP_C ▲QSPCLK_B
	S7G2	-	TXD6_A	A10	A10	-	LCD_DATA17_A	IRQ8_B		
	S5D9	**GTOWUP_C**	TXD6_A	A10	A10	**QSPCLK_B**	LCD_DATA17_A	IRQ8_B		
P306		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOULO_D ▲QSSL_B
	S7G2	-	SCK6_A	A11	A11	-	LCD_DATA18_A			
	S5D9	**GTOULO_D**	SCK6_A	A11	A11	**QSSL_B**	LCD_DATA18_A			
P307		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOUUP_D ▲QIO0_B
	S7G2	-	CTS6_A	A12	A12	-	LCD_DATA19_A			
	S5D9	**GTOUUP_D**	CTS6_A	A12	A12	**QIO0_B**	LCD_DATA19_A			

Table 2.1 100 Pin Package Difference (6 of 9)

PORT	MCU	SELECT								COMMENTS
P400		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01010b	PSEL 10010b	PSEL 10110b	▲AGTIO1_D ▲ET0_WOL_B ▼ET0_WOL_B ▼ET1_TX_CLK
	S7G2	-	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK	**ET1_TX_CLK**	
	S5D9	**AGTIO1_D**	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK_A	**ET0_WOL_B**	
		PSEL 10111b	ISEL							
	S7G2	-	IRQ0_A							
	S5D9	**ET0_WOL_B**	IRQ0_A							
P402		PSEL 00001b	PSEL 00101b	PSEL 01010b	PSEL 10000b	PSEL 10010b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲CACREF_C ▲AUDIO_CLK_B ▲VSYNC_B
	S7G2	AGTIO0_B/AGTIO1_B	RXD7_A	-	CRX0_B	-	ET0_MDIO	ET0_MDIO	-	
	S5D9	AGTIO0_B/AGTIO1_B	RXD7_A	**CACREF_C**	CRX0_B	**AUDIO_CLK_B**	ET0_MDIO_A	ET0_MDIO_A	**VSYNC_B**	
		ISEL								
	S7G2	IRQ4-DS								
	S5D9	IRQ4-DS								
P403		PSEL 00001b	PSEL 00011b	PSEL 00101b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲SD1DAT7_B ▼ET0_LINKSTA_B ▼ET1_MDC
	S7G2	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	-	**ET1_MDC**	**ET1_MDC**	PIXD7	
	S5D9	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	**SD1DAT7_B**	**ET0_LINKSTA_B**	**ET0_LINKSTA_B**	PIXD7_A	
P404		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT6_B ▼ET0_TX_EN_B ▼ET1_MDIO
	S7G2	GTIOC3B_B	SSIWS0_A	-	**ET1_MDIO**	**ET1_MDIO**	PIXD6			
	S5D9	GTIOC3B_B	SSIWS0_A	**SD1DAT6_B**	**ET0_EXOUT_B**	**ET0_EXOUT_B**	PIXD6_A			
P405		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT5_B ▼ET0_TX_EN_B ▼RMII0_TXD_EN_B ▼ET1_TX_EN ▼RMII1_TXD_EN
	S7G2	GTIOC1A_B	SSITXD0_A	-	**ET1_TX_EN**	**RMII1_TXD_EN**	PIXD5			
	S5D9	GTIOC1A_B	SSITXD0_A	**SD1DAT5_B**	**ET0_TX_EN_B**	**RMII0_TXD_EN_B**	PIXD5_A			
P406		PSEL 00011b	PSEL 00110b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB3_C ▲SD1DAT4_B ▼ET0_RX_ER_B ▼RMII0_TXD1_B ▼ET1_RX_ER ▼RMII1_TXD1
	S7G2	GTIOC1B_B	-	SSIRXD0_A	-	**ET1_RX_ER**	**RMII1_TXD1**	PIXD4		
	S5D9	GTIOC1B_B	**SSLB3_C**	SSIRXD0_A	**SD1DAT4_B**	**ET0_RX_ER_B**	**RMII0_TXD1_B**	PIXD4_A		

Table 2.1 100 Pin Package Difference (7 of 9)

PORT	MCU	SELECT								COMMENTS
P407		PSEL 00001b	PSEL 00100b	PSEL 00110b	PSEL 00111b	PSEL 01010b	PSEL 01100b	PSEL 10011b	PSEL 10110b	▲AGTIO0_E
	S7G2	-	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT	
	S5D9	**AGTIO0_E**	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT_A	
		PSEL 10111b								
	S7G2	ET0_EXOUT								
	S5D9	ET0_EXOUT_A								
P408		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00111b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	▲SCL0_B ▲PIXCLK_B
	S7G2	GTOWLO_B	GTIOC10B_A	RXD3_A	-	TS4	USB_ID_A	USBHS_ID	ET0_CRS	
	S5D9	GTOWLO_B	GTIOC10B_A	RXD3_A	**SCL0_B**	TS4	USB_ID_A	USBHS_ID	ET0_CRS_A	
		PSEL 10111b	PSEL 11000b	ISEL						
	S7G2	RMII0_CRS_DV	-	IRQ7_B						
	S5D9	RMII0_CRS_DV_A	**PIXCLK_B**	IRQ7_B						
P409		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	PSEL 10111b	▲HSYNC_B
	S7G2	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK	RMII0_RX_ER	
	S5D9	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK_A	RMII0_RX_ER_A	
		PSEL 11000b	ISEL							
	S7G2	-	IRQ6_B							
	S5D9	**HSYNC_B**	IRQ6_B							
P410		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD0_B
	S7G2	AGTOB1	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1	
	S5D9	AGTOB1_A	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD0	RMII0_RXD1	-	IRQ5_B					
	S5D9	ET0_ERXD0_A	RMII0_RXD1_A	**PIXD0_B**	IRQ5_B					

Table 2.1 100 Pin Package Difference (8 of 9)

PORT	MCU	SELECT								COMMENTS
P411		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD1_B
	S7G2	AGTOA1	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0	
	S5D9	AGTOA1_A	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD1	RMII0_RXD0	-	IRQ4_B					
	S5D9	ET0_ERXD1_A	RMII0_RXD0_A	**PIXD1_B**	IRQ4_B					
P412		PSEL 00001b	PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	▲AGTEE1_C ▲PIXD2_B
	S7G2	-	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD	ET0_ETXD0	REF50CK0	
	S5D9	**AGTEE1_C**	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD_A	ET0_ETXD0_A	REF50CK0_A	
		PSEL 11000b								
	S7G2	-								
	S5D9	**PIXD2_B**								
P413		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲PIXD3_B
	S7G2	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK	ET0_ETXD1	RMII0_TXD0	-	
	S5D9	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK_A	ET0_ETXD1_A	RMII0_TXD0_A	**PIXD3_B**	
P414		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL	▲GTIOC0B_C ▲PIXD4_B ▲IRQ9_C
	S7G2	-	SSLA1_B	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	-	-	
	S5D9	**GTIOC0B_C**	SSLA1_B	TS10	SD0WP_A	ET0_RX_ER_A	RMII0_TXD1_A	**PIXD4_B**	**IRQ9_C**	
P415		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲GTIOC0A_C ▲USB_VBUSEN_C ▲SD0CD_A ▲PIXD5_B ▲IRQ8_C
	S7G2	-	SSLA2_B	TS11	-	-	ET0_TX_EN	RMII0_TXD_EN	-	
	S5D9	**GTIOC0A_C**	SSLA2_B	TS11	**USB_VBUSEN_C**	**SD0CD_A**	ET0_TX_EN_A	RMII0_TXD_EN_A	**PIXD5_B**	
		ISEL								
	S7G2	-								
	S5D9	**IRQ8_C**								

Table 2.1 100 Pin Package Difference (9 of 9)

PORT	MCU	SELECT								COMMENTS
		PSEL 00100b	PSEL 00101b	ASEL						ALL ▲
VCL2	S7G2	-	-	-						
P508	S5D9	**SCK6_C**	**SCK5_B**	**AN020**						
		PSEL 00011b	PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 11001b			▲GTIOC6B_C ▲SCK9_C ▲CLKOUT_D ▲CACREF_E
P600	S7G2	-	-	-	-	RD	LCD_DATA2_A			
	S5D9	**GTIOC6B_C**	**SCK9_C**	**CLKOUT_D**	**CACREF_E**	RD	LCD_DATA2_A			
		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC6A_C ▲RXD9_C
P601	S7G2	-	-	WR/WR0	DQM0	LCD_DATA3_A				
	S5D9	**GTIOC6A_C**	**RXD9_C**	WR/WR0	DQM0	LCD_DATA3_A				
		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC7B_C ▲TXD9_C
P602	S7G2	-	-	BCLK	SDCLK	LCD_DATA4_A				
	S5D9	**GTIOC7B_C**	**TXD9_C**	BCLK	SDCLK	LCD_DATA4_A				
		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 11001b					▲GTIOC4B_C
P608	S7G2	-	A0/BC0	A0/DQM1	LCD_DATA7_A					
	S5D9	**GTIOC4B_C**	A0/BC0	A0/DQM1	LCD_DATA7_A					
		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5A_C ▲CTX1_C
P609	S7G2	-	CS1#	CKE	-	LCD_DATA6_A				
	S5D9	**GTIOC5A_C**	CS1#	CKE	**CTX1_C**	LCD_DATA6_A				
		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5B_C ▲CRX1_C
P610	S7G2	-	CS0#	WE	-	LCD_DATA5_A				
	S5D9	**GTIOC5B_C**	CS0#	WE	**CRX1_C**	LCD_DATA5_A				
		PSEL 00101b	PSEL 00110b	PSEL 01010b	PSEL 01100b	PSEL 10010b	PSEL 10110b	PSEL 11000b	ISEL	▲AUDIO_CLK_C ▲PCKO_B
P708	S7G2	RXD1_B	SSLA3_B	CACREF_B	TS12	-	ET0_ETXD3	-	IRQ11_B	
	S5D9	RXD1_B	SSLA3_B	CACREF_B	TS12	**AUDIO_CLK_C**	ET0_ETXD3	**PCKO_B**	IRQ11_B	

Appendix 2. 144 Pin Package

Table 3.1 144 Pin Package Difference (1 of 12)

PORT	MCU	SELECT								COMMENTS
P003		ASEL								Alternate Name AN007
	S7G2	PGAVSS000								
	S5D9	**PGAVSS000/AN007**								
P007		ASEL								Alternate Name AN107
	S7G2	PGAVSS100								
	S5D9	**PGAVSS100/AN107**								
P100		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5B_D
	S7G2	AGTIO0_A	GTETRGA_A	**-**	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
	S5D9	AGTIO0_A	GTETRGA_A	**GTIOC5B_D**	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
	S5D9	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
P101		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5A_D
	S7G2	AGTEE0	GTETRGB_A	**-**	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
	S5D9	AGTEE0_A	GTETRGB_A	**GTIOC5A_D**	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D1	DQ1	LCD_CLK_A	IRQ1_A					
	S5D9	D1	DQ1	LCD_CLK_A	IRQ1_A					

Table 3.1 144 Pin Package Difference (2 of 12)

PORT	MCU	SELECT								COMMENTS
P102		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01010b	PSEL 01011b	▲CRX0_D
	S7G2	AGTO0	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
	S5D9	AGTO0_A	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
		PSEL 01011b	PSEL 10000b	PSEL 11001b						
	S7G2	DQ2	**-**	LCD_TCON0_A						
	S5D9	DQ2	**CRX0_D**	LCD_TCON0_A						
P103		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 10000b	▲CTX0_D
	S7G2	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	**-**	
	S5D9	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	**CTX0_D**	
		PSEL 11001b								
	S7G2	LCD_TCON1_A								
	S5D9	LCD_TCON1_A								
P104		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1B_C
	S7G2	GTETRGB_B	**-**	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
	S5D9	GTETRGB_B	**GTIOC1B_C**	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
		ISEL								
	S7G2	IRQ1_B								
	S5D9	IRQ1_B								
P105		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1A_C
	S7G2	GTETRGA_C	**-**	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
	S5D9	GTETRGA_C	**GTIOC1A_C**	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
		ISEL								
	S7G2	IRQ0_B								
	S5D9	IRQ0_B								

Table 3.1 144 Pin Package Difference (3 of 12)

PORT	MCU	SELECT								COMMENTS
P106		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲AGTOB0_C
	S7G2	-	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
	S5D9	**AGTOB0_C**	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
P107		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b		▲AGTOA0_C
	S7G2	-	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
	S5D9	**AGTOA0_C**	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
P108		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00110b				▲GTOULO_C
	S7G2	TMS/SWDIO	-	GTIOC0B_A	CTS9_B	SSLB0_B				
	S5D9	TMS/SWDIO	**GTOULO_C**	GTIOC0B_A	CTS9_B	SSLB0_B				
P112		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	PSEL 10010b	▲SCK1_D ▲SSLB0_B
	S7G2	HRMON1	GTIOC3B_A	TXD2_B	-	-	A4	A4	SSISCK0_B	
	S5D9	HRMON1	GTIOC3B_A	TXD2_B	**SCK1_D**	**SSLB0_B**	A4	A4	SSISCK0_B	
		PSEL 11001b								
	S7G2	LCD_DATA11_A								
	S5D9	LCD_DATA11_A								
P113		PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b			▲GTIOC2A_C
	S7G2	-	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
	S5D9	**GTIOC2A_C**	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
P114		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC2B_C
	S7G2	-	A2	A2	SSIRXD0_B	LCD_DATA9_A				
	S5D9	**GTIOC2B_C**	A2	A2	SSIRXD0_B	LCD_DATA9_A				
P115		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC4A_C
	S7G2	-	A1	A1	SSITXD0_B	LCD_DATA8_A				
	S5D9	**GTIOC4A_C**	A1	A1	SSITXD0_B	LCD_DATA8_A				

Table 3.1 144 Pin Package Difference (4 of 12)

PORT	MCU	SELECT								COMMENTS
P207		PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 10001b	PSEL 11001b				▲QSSL_C ▲LCD_DATA23_B
	S7G2	SSLB2_A	A17	TS2	-	-				
	S5D9	SSLB2_A	A17	TS2	**QSSL_C**	**LCD_DATA23_B**				
VCC(IO)		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P208	S5D9	**GTOVLO_C**	**QIO3_C**	**SD0DAT0_B**	**ET0_LINKSTA_C**	**ET0_LINKSTA_C**	**LCD_DATA18_B**	**TDATA3**		
VLO		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P209	S5D9	**GTOVUP_C**	**QIO2_C**	**SD0WP_B**	**ET0_EXOUT_C**	**ET0_EXOUT_C**	**LCD_DATA19_B**	**TDATA2**		
VLO		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P210	S5D9	**GTIW_C**	**QIO1_C**	**SD0CD_B**	**ET0_WOL_C**	**ET0_WOL_C**	**LCD_DATA20_B**	**TDATA1**		
VSS(IO/DCDC)		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P211	S5D9	**GTIV_C**	**QIO0_C**	**SD0CMD_B**	**ET0_MDIO_B**	**ET0_MDIO_B**	**LCD_DATA21_B**	**TDATA0**		
P212/EXTAL		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	ISEL				▲GTIOC0A
	S7G2	AGTEE1	GTETRGD_A	-	RXD1_A	IRQ3_B				
	S5D9	AGTEE1_A	GTETRGD_A	**GTIOC0B_D**	RXD1_A	IRQ3_B				
P213/XTAL		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01010b	ISEL				▲GTIOC0A
	S7G2	GTETRGC_A	-	TXD1_A	ADTRG1_A	IRQ2_B				
	S5D9	GTETRGC_A	**GTIOC0A_D**	TXD1_A	ADTRG1_A	IRQ2_B				
VCL1		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
	S7G2	-	-	-	-	-	-	-		
P214	S5D9	**GTIU_C**	**QSPCLK_C**	**SD0CLK_B**	**ET0_MDC_B**	**ET0_MDC_B**	**LCD_DATA22_B**	**TCLK**		

Table 3.1 144 Pin Package Difference (5 of 12)

PORT	MCU	SELECT								COMMENTS
P300		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00110b					▲GTOUUP_C
	S7G2	TCK/SWCLK	-	GTIOC0A_A	SSLB1_B					
	S5D9	TCK/SWCLK	**GTOUUP_C**	GTIOC0A_A	SSLB1_B					
P301		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	▲AGTIO0_F ▲CTS9_D
	S7G2	-	GTOULO_A	GTIOC4B_A	RXD2_A	-	SSLB2_B	A6	A6	
	S5D9	**AGTIO0_F**	GTOULO_A	GTIOC4B_A	RXD2_A	**CTS9_D**	SSLB2_B	A6	A6	
		PSEL 11001b	ISEL							
	S7G2	LCD_DATA13_A	IRQ6_A							
	S5D9	LCD_DATA13_A	IRQ6_A							
P304		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL		▲GTOWLO_C
	S7G2	-	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
	S5D9	**GTOWLO_C**	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
P305		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b	ISEL		▲GTOWUP_C ▲QSPCLK_B
	S7G2	-	TXD6_A	A10	A10	-	LCD_DATA17_A	IRQ8_B		
	S5D9	**GTOWUP_C**	TXD6_A	A10	A10	**QSPCLK_B**	LCD_DATA17_A	IRQ8_B		
P306		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOULO_D ▲QSSL_B
	S7G2	-	SCK6_A	A11	A11	-	LCD_DATA18_A			
	S5D9	**GTOULO_D**	SCK6_A	A11	A11	**QSSL_B**	LCD_DATA18_A			
P307		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOUUP_D ▲QIO0_B
	S7G2	-	CTS6_A	A12	A12	-	LCD_DATA19_A			
	S5D9	**GTOUUP_D**	CTS6_A	A12	A12	**QIO0_B**	LCD_DATA19_A			
P308		PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b					▲QIO1_B
	S7G2	A13	A13	-	LCD_DATA20_A					
	S5D9	A13	A13	**QIO1_B**	LCD_DATA20_A					

Table 3.1 144 Pin Package Difference (6 of 12)

PORT	MCU	SELECT								COMMENTS
P309		PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b				▲RXD3_C ▲QIO2_B
	S7G2	-	A14	A14	-	LCD_DATA21_A				
	S5D9	**RXD3_C**	A14	A14	**QIO2_B**	LCD_DATA21_A				
P310		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲AGTEE1_B ▲TXD3_C ▲QIO3_B
	S7G2	-	-	A15	A15	-	LCD_DATA22_A			
	S5D9	**AGTEE1_B**	**TXD3_C**	A15	A15	**QIO3_B**	LCD_DATA22_A			
P311		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲AGTOB1_B ▲SCK3_C
	S7G2	-	-	CS2#	RAS	LCD_DATA23_A				
	S5D9	**AGTOB1_B**	**SCK3_C**	CS2#	RAS	LCD_DATA23_A				
P312		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b					▲AGTOA1_B ▲CTS3_C
	S7G2	-	-	CS3#	CAS					
	S5D9	**AGTOA1_B**	**CTS3_C**	CS3#	CAS					
P400		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01010b	PSEL 10010b	PSEL 10110b	▲AGTIO1_D ▲ET0_WOL_B ▼ET0_WOL_B ▼ET1_TX_CLK
	S7G2	-	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK	**ET1_TX_CLK**	
	S5D9	**AGTIO1_D**	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK_A	**ET0_WOL_B**	
		PSEL 10111b	ISEL							
	S7G2	-	IRQ0_A							
	S5D9	**ET0_WOL_B**	IRQ0_A							
P402		PSEL 00001b	PSEL 00101b	PSEL 01010b	PSEL 10000b	PSEL 10010b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲CACREF_C ▲AUDIO_CLK_B ▲VSYNC_B
	S7G2	AGTIO0_B/AGTIO1_B	RXD7_A	-	CRX0_B	-	ET0_MDIO	ET0_MDIO	-	
	S5D9	AGTIO0_B/AGTIO1_B	RXD7_A	**CACREF_C**	CRX0_B	**AUDIO_CLK_B**	ET0_MDIO_A	ET0_MDIO_A	**VSYNC_B**	
		ISEL								
	S7G2	IRQ4-DS								
	S5D9	IRQ4-DS								

Table 3.1 144 Pin Package Difference (7 of 12)

PORT	MCU	SELECT								COMMENTS
P403		PSEL 00001b	PSEL 00011b	PSEL 00101b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲SD1DAT7_B ▼ET0_LINKSTA_B ▼ET0_LINKSTA_B ▼ET1_MDC ▼ET1_MDC
	S7G2	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	-	ET1_MDC	ET1_MDC	PIXD7	
	S5D9	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	SD1DAT7_B	ET0_LINKSTA_B	ET0_LINKSTA_B	PIXD7_A	
P404		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT6_B ▼ET0_TX_EN_B ▼ET0_EXOUT_B ▼ET1_MDIO ▼ET1_MDIO
	S7G2	GTIOC3B_B	SSIWS0_A	-	ET1_MDIO	ET1_MDIO	PIXD6			
	S5D9	GTIOC3B_B	SSIWS0_A	SD1DAT6_B	ET0_EXOUT_B	ET0_EXOUT_B	PIXD6_A			
P405		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT5_B ▼ET0_TX_EN_B ▼RMII0_TXD_EN_B ▼ET1_TX_EN ▼RMII1_TXD_EN
	S7G2	GTIOC1A_B	SSITXD0_A	-	ET1_TX_EN	RMII1_TXD_EN	PIXD5			
	S5D9	GTIOC1A_B	SSITXD0_A	SD1DAT5_B	ET0_TX_EN_B	RMII0_TXD_EN_B	PIXD5_A			
P406		PSEL 00011b	PSEL 00110b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB3_C ▲SD1DAT4_B ▼ET0_RX_ER_B ▼RMII0_TXD1_B ▼ET1_RX_ER ▼RMII1_TXD1
	S7G2	GTIOC1B_B	-	SSIRXD0_A	-	ET1_RX_ER	RMII1_TXD1	PIXD4		
	S5D9	GTIOC1B_B	SSLB3_C	SSIRXD0_A	SD1DAT4_B	ET0_RX_ER_B	RMII0_TXD1_B	PIXD4_A		
P407		PSEL 00001b	PSEL 00100b	PSEL 00110b	PSEL 00111b	PSEL 01010b	PSEL 01100b	PSEL 10011b	PSEL 10110b	▲AGTIO0_E
	S7G2	-	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT	
	S5D9	AGTIO0_E	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT_A	
		PSEL 10111b								
	S7G2	ET0_EXOUT								
	S5D9	ET0_EXOUT_A								
P408		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00111b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	▲SCL0_B ▲PIXCLK_B
	S7G2	GTOWLO_B	GTIOC10B_A	RXD3_A	-	TS4	USB_ID_A	USBHS_ID	ET0_CRS	
	S5D9	GTOWLO_B	GTIOC10B_A	RXD3_A	SCL0_B	TS4	USB_ID_A	USBHS_ID	ET0_CRS_A	
		PSEL 10111b	PSEL 11000b	ISEL						
	S7G2	RMII0_CRS_DV	-	IRQ7_B						
	S5D9	RMII0_CRS_DV_A	PIXCLK_B	IRQ7_B						

Table 3.1 144 Pin Package Difference (8 of 12)

PORT	MCU	SELECT								COMMENTS
P409		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	PSEL 10111b	▲HSYNC_B
	S7G2	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK	RMII0_RX_ER	
	S5D9	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK_A	RMII0_RX_ER_A	
		PSEL 11000b	ISEL							
	S7G2	**-**	IRQ6_B							
	S5D9	**HSYNC_B**	IRQ6_B							
P410		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD0_B
	S7G2	AGTOB1	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1	
	S5D9	AGTOB1_A	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD0	RMII0_RXD1	**-**	IRQ5_B					
	S5D9	ET0_ERXD0_A	RMII0_RXD1_A	**PIXD0_B**	IRQ5_B					
P411		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD1_B
	S7G2	AGTOA1	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0	
	S5D9	AGTOA1_A	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD1	RMII0_RXD0	**-**	IRQ4_B					
	S5D9	ET0_ERXD1_A	RMII0_RXD0_A	**PIXD1_B**	IRQ4_B					
P412		PSEL 00001b	PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	▲AGTEE1_C ▲PIXD2_B
	S7G2	**-**	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD	ET0_ETXD0	REF50CK0	
	S5D9	**AGTEE1_C**	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD_A	ET0_ETXD0_A	REF50CK0_A	
		PSEL 11000b								
	S7G2	**-**								
	S5D9	**PIXD2_B**								

Table 3.1 144 Pin Package Difference (9 of 12)

PORT	MCU	SELECT								COMMENTS
P413		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲PIXD3_B
	S7G2	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK	ET0_ETXD1	RMII0_TXD0	-	
	S5D9	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK_A	ET0_ETXD1_A	RMII0_TXD0_A	**PIXD3_B**	
P414		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL	▲GTIOC0B_C ▲PIXD4_B ▲IRQ9_C
	S7G2	-	SSLA1_B	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	-	-	
	S5D9	**GTIOC0B_C**	SSLA1_B	TS10	SD0WP_A	ET0_RX_ER_A	RMII0_TXD1_A	**PIXD4_B**	**IRQ9_C**	
P415		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲GTIOC0A_C ▲USB_VBUSEN_C ▲SD0CD_A ▲PIXD5_B ▲IRQ8_C
	S7G2	-	SSLA2_B	TS11	-	-	ET0_TX_EN	RMII0_TXD_EN	-	
	S5D9	**GTIOC0A_C**	SSLA2_B	TS11	**USB_VBUSEN_C**	**SD0CD_A**	ET0_TX_EN_A	RMII0_TXD_EN_A	**PIXD5_B**	
		ISEL								
	S7G2	-								
	S5D9	**IRQ8_C**								
VCL2		PSEL 00100b	PSEL 00101b	ASEL						ALL ▲
	S7G2	-	-	-						
P508	S5D9	**SCK6_C**	**SCK5_B**	**AN020**						
P511		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 10110b	PSEL 11000b	ISEL		▼ET1_TX_ER
	S7G2	GTIOC0B_B	RXD4_B	SDA2	CRX1_B	**ET1_TX_ER**	PCKO	IRQ15_A		
	S5D9	GTIOC0B_B	RXD4_B	SDA2	CRX1_B	-	PCKO_A	IRQ15_A		
P512		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 10110b	PSEL 11000b	ISEL		▼ET1_ETXD2
	S7G2	GTIOC0A_B	TXD4_B	SCL2	CTX1_B	**ET1_ETXD2**	VSYNC	IRQ14_A		
	S5D9	GTIOC0A_B	TXD4_B	SCL2	CTX1_B	-	VSYNC_A	IRQ14_A		
P600		PSEL 00011b	PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 11001b			▲GTIOC6B_C ▲SCK9_C ▲CLKOUT_D ▲CACREF_E
	S7G2	-	-	-	-	RD	LCD_DATA2_A			
	S5D9	**GTIOC6B_C**	**SCK9_C**	**CLKOUT_D**	**CACREF_E**	RD	LCD_DATA2_A			

Table 3.1 144 Pin Package Difference (10 of 12)

PORT	MCU	SELECT								COMMENTS
P601		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC6A_C ▲RXD9_C
	S7G2	-	-	WR/WR0	DQM0	LCD_DATA3_A				
	S5D9	**GTIOC6A_C**	**RXD9_C**	WR/WR0	DQM0	LCD_DATA3_A				
P602		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC7B_C ▲TXD9_C
	S7G2	-	-	BCLK	SDCLK	LCD_DATA4_A				
	S5D9	**GTIOC7B_C**	**TXD9_C**	BCLK	SDCLK	LCD_DATA4_A				
P603		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b					▲GTIOC7A_C ▲CTS9_C
	S7G2	-	-	D13	DQ13					
	S5D9	**GTIOC7A_C**	**CTS9_C**	D13	DQ13					
P604		PSEL 00011b	PSEL 01011b	PSEL 01011b						▲GTIOC8B_C
	S7G2	-	D12	DQ12						
	S5D9	**GTIOC8B_C**	D12	DQ12						
P605		PSEL 00011b	PSEL 01011b	PSEL 01011b						▲GTIOC8A_C
	S7G2	-	D11	DQ11						
	S5D9	**GTIOC8A_C**	D11	DQ11						
P608		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 11001b					▲GTIOC4B_C
	S7G2	-	A0/BC0	A0/DQM1	LCD_DATA7_A					
	S5D9	**GTIOC4B_C**	A0/BC0	A0/DQM1	LCD_DATA7_A					
P609		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5A_C ▲CTX1_C
	S7G2	-	CS1#	CKE	-	LCD_DATA6_A				
	S5D9	**GTIOC5A_C**	CS1#	CKE	**CTX1_C**	LCD_DATA6_A				
P610		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5B_C ▲CRX1_C
	S7G2	-	CS0#	WE	-	LCD_DATA5_A				
	S5D9	**GTIOC5B_C**	CS0#	WE	**CRX1_C**	LCD_DATA5_A				

Table 3.1 144 Pin Package Difference (11 of 12)

PORT	MCU	SELECT								COMMENTS
P611		PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b					▲CTS7_C ▲CLKOUT_C ▲CACREF_D
	S7G2	-	-	-	SDCS					
	S5D9	**CTS7_C**	**CLKOUT_C**	**CACREF_D**	SDCS					
P612		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲SCK7_C
	S7G2	-	D8	DQ8						
	S5D9	**SCK7_C**	D8	DQ8						
P613		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲TXD7_C
	S7G2	-	D9	DQ9						
	S5D9	**TXD7_C**	D9	DQ9						
P614		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲RXD7_C
	S7G2	-	D10	DQ10						
	S5D9	**RXD7_C**	D10	DQ10						
P700		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MISOB_C ▲SD1DAT3_B ▼ET0_ETXD1_B ▼RMII0_TXD0_B ▼ET1_ETXD1 ▼RMII1_TXD0
	S7G2	GTIOC5A_B	-	-	**ET1_ETXD1**	**RMII1_TXD0**	PIXD3			
	S5D9	GTIOC5A_B	**MISOB_C**	**SD1DAT3_B**	**ET0_ETXD1_B**	**RMII0_TXD0_B**	PIXD3_A			
P701		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MISOB_C ▲SD1DAT2_B ▼ET0_ETXD0_B ▼REF50CK0_B ▼ET1_ETXD0 ▼REF50CK1
	S7G2	GTIOC5B_B	-	-	**ET1_ETXD0**	**REF50CK1**	PIXD2			
	S5D9	GTIOC5B_B	**MOSIB_C**	**SD1DAT2_B**	**ET0_ETXD0_B**	**REF50CK0_B**	PIXD2_A			
P702		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲RSPCKB_C ▲SD1DAT1_B ▼ET0_ERXD1_B ▼RMII0_RXD0_B ▼ET1_ERXD1 ▼RMII1_RXD0
	S7G2	GTIOC6A_B	-	-	**ET1_ERXD1**	**RMII1_RXD0**	PIXD1			
	S5D9	GTIOC6A_B	**RSPCKB_C**	**SD1DAT1_B**	**ET0_ERXD1_B**	**RMII0_RXD0_B**	PIXD1_A			
P703		PSEL 00011b	PSEL 00110b	PSEL 01001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB0_C ▲VCOUT_B ▲SD1DAT0_B ▼ET0_ERXD0_B ▼RMII0_RXD1_B ▼ET1_ERXD0 ▼RMII1_RXD1
	S7G2	GTIOC6B_B	-	-	-	**ET1_ERXD0**	**RMII1_RXD1**	PIXD0		
	S5D9	GTIOC6B_B	**SSLB0_C**	**VCOUT_B**	**SD1DAT0_B**	**ET0_ERXD0_B**	**RMII0_RXD1_B**	PIXD0_A		

Table 3.1 144 Pin Package Difference (12 of 12)

PORT	MCU	SELECT								COMMENTS
P704		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲AGTO0_B ▲SSLB1_C ▲CTX0_E ▲SD1CLK_B ▼ET0_RX_CLK_B ▼RMII0_RX_ER_B ▼ET1_RX_CLK ▼RMII1_RX_ER
	S7G2	-	-	-	-	**ET1_RX_CLK**	**RMII1_RX_ER**	HSYNC		
	S5D9	**AGTO0_B**	**SSLB1_C**	**CTX0_E**	**SD1CLK_B**	**ET0_RX_CLK_B**	**RMII0_RX_ER_B**	HSYNC_A		
P705		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲AGTIO0_D ▼ET1_CR ▲SSLB2_C ▲CRXO_E ▲SD1CMD_B ▼ET0_CRS_B ▼RMII0_CRS_DV_B ▼RMII1_CRS_DV
	S7G2	-	-	-	-	**ET1_CRS**	**RMII1_CRS_DV**	PIXCLK		
	S5D9	**AGTIO0_D**	**SSLB2_C**	**CRX0_E**	**SD1CMD_B**	**ET0_CRS_B**	**RMII0_CRS_DV_B**	PIXCLK_A		
P708		PSEL 00101b	PSEL 00110b	PSEL 01010b	PSEL 01100b	PSEL 10010b	PSEL 10110b	PSEL 11000b	ISEL	▲AUDIO_CLK_C ▲PCKO_B
	S7G2	RXD1_B	SSLA3_B	CACREF_B	TS12	-	ET0_ETXD3	-	IRQ11_B	
	S5D9	RXD1_B	SSLA3_B	CACREF_B	TS12	**AUDIO_CLK_C**	ET0_ETXD3	**PCKO_B**	IRQ11_B	
P711		PSEL 00001b	PSEL 00101b	PSEL 01100b	PSEL 10110b					▲AGTEE0_B
	S7G2	-	CTS1_B	TS15	ET0_TX_CLK					
	S5D9	**AGTEE0_B**	CTS1_B	TS15	ET0_TX_CLK					
P712		PSEL 00001b	PSEL 00011b	PSEL 01100b						▲AGTOB0_B
	S7G2	-	GTIOC2B_B	TS16						
	S5D9	**AGTOB0_B**	GTIOC2B_B	TS16						
P713		PSEL 00001b	PSEL 00011b	PSEL 01100b	PSEL 10110b	PSEL 10111b				▲AGTOA0_B ▼ET1_EXOUT ▼ET1_EXOUT
	S7G2	-	GTIOC2A_B	TS17	**ET1_EXOUT**	**ET1_EXOUT**				
	S5D9	**AGTOA0_B**	GTIOC2A_B	TS17	-	-				

Appendix 3. 176 Pin Package

Table 4.1 176 Pin Package Difference (1 of 14)

PORT	MCU	SELECT								COMMENTS
P003		ASEL								Alternate Name AN007
	S7G2	PGAVSS000								
	S5D9	**PGAVSS000/AN007**								
P007		ASEL								Alternate Name AN107
	S7G2	PGAVSS100								
	S5D9	**PGAVSS100/AN107**								
P100		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5B_D
	S7G2	AGTIO0_A	GTETRGA_A	-	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
	S5D9	AGTIO0_A	GTETRGA_A	**GTIOC5B_D**	RXD0_A	SCK1_A	MISOA_A	SCL1_B	KRM00	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
	S5D9	D0	DQ0	LCD_EXTCLK_A	IRQ2_A					
P101		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲GTIOC5A_D
	S7G2	AGTEE0	GTETRGB_A	-	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
	S5D9	AGTEE0_A	GTETRGB_A	**GTIOC5A_D**	TXD0_A	CTS1_A	MOSIA_A	SDA1_B	KRM01	
		PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL					
	S7G2	D1	DQ1	LCD_CLK_A	IRQ1_A					
	S5D9	D1	DQ1	LCD_CLK_A	IRQ1_A					

Table 4.1 176 Pin Package Difference (2 of 14)

PORT	MCU	SELECT								COMMENTS
P102		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01010b	PSEL 01011b	▲CRX0_D
	S7G2	AGTO0	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
	S5D9	AGTO0_A	GTOWLO_A	GTIOC2B_A	SCK0_A	RSPCKA_A	KRM02	ADTRG0_A	D2	
		PSEL 01011b	PSEL 10000b	PSEL 11001b						
	S7G2	DQ2	-	LCD_TCON0_A						
	S5D9	DQ2	**CRX0_D**	LCD_TCON0_A						
P103		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 10000b	▲CTX0_D
	S7G2	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	-	
	S5D9	GTOWUP_A	GTIOC2A_A	CTS0_A	SSLA0_A	KRM03	D3	DQ3	**CTX0_D**	
		PSEL 11001b								
	S7G2	LCD_TCON1_A								
	S5D9	LCD_TCON1_A								
P104		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1B_C
	S7G2	GTETRGB_B	-	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
	S5D9	GTETRGB_B	**GTIOC1B_C**	RXD8_A	SSLA1_A	KRM04	D4	DQ4	LCD_TCON2_A	
		ISEL								
	S7G2	IRQ1_B								
	S5D9	IRQ1_B								
P105		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲GTIOC1A_C
	S7G2	GTETRGA_C	-	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
	S5D9	GTETRGA_C	**GTIOC1A_C**	TXD8_A	SSLA2_A	KRM05	D5	DQ5	LCD_TCON3_A	
		ISEL								
	S7G2	IRQ0_B								
	S5D9	IRQ0_B								

Table 4.1 176 Pin Package Difference (3 of 14)

PORT	MCU	SELECT								COMMENTS
P106		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b	▲AGTOB0_C
	S7G2	-	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
	S5D9	**AGTOB0_C**	GTIOC8B_A	SCK8_A	SSLA3_A	KRM06	D6	DQ6	LCD_DATA0_A	
P107		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 01000b	PSEL 01011b	PSEL 01011b	PSEL 11001b		▲AGTOA0_C
	S7G2	-	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
	S5D9	**AGTOA0_C**	GTIOC8A_A	CTS8_A	KRM07	D7	DQ7	LCD_DATA1_A		
P108		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00110b				▲GTOULO_C
	S7G2	TMS/SWDIO	-	GTIOC0B_A	CTS9_B	SSLB0_B				
	S5D9	TMS/SWDIO	**GTOULO_C**	GTIOC0B_A	CTS9_B	SSLB0_B				
P112		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	PSEL 10010b	▲SCK1_D ▲SSLB0_B
	S7G2	HRMON1	GTIOC3B_A	TXD2_B	-	-	A4	A4	SSISCK0_B	
	S5D9	HRMON1	GTIOC3B_A	TXD2_B	**SCK1_D**	**SSLB0_B**	A4	A4	SSISCK0_B	
		PSEL 11001b								
	S7G2	LCD_DATA11_A								
	S5D9	LCD_DATA11_A								
P113		PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b			▲GTIOC2A_C
	S7G2	-	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
	S5D9	**GTIOC2A_C**	RXD2_B	A3	A3	SSIWS0_B	LCD_DATA10_A			
P114		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC2B_C
	S7G2	-	A2	A2	SSIRXD0_B	LCD_DATA9_A				
	S5D9	**GTIOC2B_C**	A2	A2	SSIRXD0_B	LCD_DATA9_A				
P115		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10010b	PSEL 11001b				▲GTIOC4A_C
	S7G2	-	A1	A1	SSITXD0_B	LCD_DATA8_A				
	S5D9	**GTIOC4A_C**	A1	A1	SSITXD0_B	LCD_DATA8_A				

Table 4.1 176 Pin Package Difference (4 of 14)

PORT	MCU	SELECT								COMMENTS
		PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 10001b	PSEL 11001b				▲QSSL_C ▲LCD_DATA23_B
P207	S7G2	SSLB2_A	A17	TS2	-	-				
	S5D9	SSLB2_A	A17	TS2	**QSSL_C**	**LCD_DATA23_B**				
		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
VCC(IO)	S7G2	-	-	-	-	-	-	-		
P208	S5D9	**GTOVLO_C**	**QIO3_C**	**SD0DAT0_B**	**ET0_LINKSTA_C**	**ET0_LINKSTA_C**	**LCD_DATA18_B**	**TDATA3**		
		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
VLO	S7G2	-	-	-	-	-	-	-		
P209	S5D9	**GTOVUP_C**	**QIO2_C**	**SD0WP_B**	**ET0_EXOUT_C**	**ET0_EXOUT_C**	**LCD_DATA19_B**	**TDATA2**		
		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
VLO	S7G2	-	-	-	-	-	-	-		
P210	S5D9	**GTIW_C**	**QIO1_C**	**SD0CD_B**	**ET0_WOL_C**	**ET0_WOL_C**	**LCD_DATA20_B**	**TDATA1**		
		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
VSS(IO/DCDC)	S7G2	-	-	-	-	-	-	-		
P211	S5D9	**GTIV_C**	**QIO0_C**	**SD0CMD_B**	**ET0_MDIO_B**	**ET0_MDIO_B**	**LCD_DATA21_B**	**TDATA0**		
		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	ISEL				▲GTIOC0A
P212/EXTAL	S7G2	AGTEE1	GTETRGD_A	-	RXD1_A	IRQ3_B				
	S5D9	AGTEE1_A	GTETRGD_A	**GTIOC0B_D**	RXD1_A	IRQ3_B				
		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01010b	ISEL				▲GTIOC0A
P213/XTAL	S7G2	GTETRGC_A	-	TXD1_A	ADTRG1_A	IRQ2_B				
	S5D9	GTETRGC_A	**GTIOC0A_D**	TXD1_A	ADTRG1_A	IRQ2_B				
		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11001b	PSEL 11010b		All ▲
VCL1	S7G2	-	-	-	-	-	-	-		
P214	S5D9	**GTIU_C**	**QSPCLK_C**	**SD0CLK_B**	**ET0_MDC_B**	**ET0_MDC_B**	**LCD_DATA22_B**	**TCLK**		

Table 4.1 176 Pin Package Difference (5 of 14)

PORT	MCU	SELECT								COMMENTS
P300		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00110b					▲GTOUUP_C
	S7G2	TCK/SWCLK	-	GTIOC0A_A	SSLB1_B					
	S5D9	TCK/SWCLK	GTOUUP_C	GTIOC0A_A	SSLB1_B					
P301		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01011b	▲AGTIO0_F ▲CTS9_D
	S7G2	-	GTOULO_A	GTIOC4B_A	RXD2_A	-	SSLB2_B	A6	A6	
	S5D9	AGTIO0_F	GTOULO_A	GTIOC4B_A	RXD2_A	CTS9_D	SSLB2_B	A6	A6	
		PSEL 11001b	ISEL							
	S7G2	LCD_DATA13_A	IRQ6_A							
	S5D9	LCD_DATA13_A	IRQ6_A							
P304		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 11001b	ISEL		▲GTOWLO_C
	S7G2	-	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
	S5D9	GTOWLO_C	GTIOC7A_A	RXD6_A	A9	A9	LCD_DATA16_A	IRQ9_B		
P305		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b	ISEL		▲GTOWUP_C ▲QSPCLK_B
	S7G2	-	TXD6_A	A10	A10	-	LCD_DATA17_A	IRQ8_B		
	S5D9	GTOWUP_C	TXD6_A	A10	A10	QSPCLK_B	LCD_DATA17_A	IRQ8_B		
P306		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOULO_D ▲QSSL_B
	S7G2	-	SCK6_A	A11	A11	-	LCD_DATA18_A			
	S5D9	GTOULO_D	SCK6_A	A11	A11	QSSL_B	LCD_DATA18_A			
P307		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲GTOUUP_D ▲QIO0_B
	S7G2	-	CTS6_A	A12	A12	-	LCD_DATA19_A			
	S5D9	GTOUUP_D	CTS6_A	A12	A12	QIO0_B	LCD_DATA19_A			
P308		PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b					▲QIO1_B
	S7G2	A13	A13	-	LCD_DATA20_A					
	S5D9	A13	A13	QIO1_B	LCD_DATA20_A					

Table 4.1 176 Pin Package Difference (6 of 14)

PORT	MCU	SELECT								COMMENTS
P309		PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b				▲RXD3_C ▲QIO2_B
	S7G2	-	A14	A14	-	LCD_DATA21_A				
	S5D9	**RXD3_C**	A14	A14	**QIO2_B**	LCD_DATA21_A				
P310		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 10001b	PSEL 11001b			▲AGTEE1_B ▲TXD3_C ▲QIO3_B
	S7G2	-	-	A15	A15	-	LCD_DATA22_A			
	S5D9	**AGTEE1_B**	**TXD3_C**	A15	A15	**QIO3_B**	LCD_DATA22_A			
P311		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲AGTOB1_B ▲SCK3_C
	S7G2	-	-	CS2#	RAS	LCD_DATA23_A				
	S5D9	**AGTOB1_B**	**SCK3_C**	CS2#	RAS	LCD_DATA23_A				
P312		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 01011b					▲AGTOA1_B ▲CTS3_C
	S7G2	-	-	CS3#	CAS					
	S5D9	**AGTOA1_B**	**CTS3_C**	CS3#	CAS					
P314		PSEL 01010b	PSEL 01011b	PSEL 11001b						▲ADTRG0_C
	S7G2	-	A21	LCD_TCON1_B						
	S5D9	**ADTRG0_C**	A21	LCD_TCON1_B						
P315		PSEL 00100b	PSEL 01011b	PSEL 11001b						▲RXD4_C
	S7G2	-	A22	LCD_TCON0_B						
	S5D9	**RXD4_C**	A22	LCD_TCON0_B						
P400		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01010b	PSEL 10010b	PSEL 10110b	▲AGTIO1_D ▲ET0_WOL_B ▼ET0_WOL_B ▼ET1_TX_CLK
	S7G2	-	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK	**ET1_TX_CLK**	
	S5D9	**AGTIO1_D**	GTIOC6A_A	SCK4_B	SCK7_A	SCL0_A	ADTRG1_B	AUDIO_CLK_A	**ET0_WOL_B**	
		PSEL 10111b	ISEL							
	S7G2	-	IRQ0_A							
	S5D9	**ET0_WOL_B**	IRQ0_A							

Table 4.1 176 Pin Package Difference (7 of 14)

PORT	MCU	SELECT								COMMENTS
P402		PSEL 00001b	PSEL 00101b	PSEL 01010b	PSEL 10000b	PSEL 10010b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲CACREF_C ▲AUDIO_CLK_B ▲VSYNC_B
	S7G2	AGTIO0_B/AGTIO1_B	RXD7_A	-	CRX0_B	-	ET0_MDIO	ET0_MDIO	-	
	S5D9	AGTIO0_B/AGTIO1_B	RXD7_A	**CACREF_C**	CRX0_B	**AUDIO_CLK_B**	ET0_MDIO_A	ET0_MDIO_A	**VSYNC_B**	
		ISEL								
	S7G2	IRQ4-DS								
	S5D9	IRQ4-DS								
P403		PSEL 00001b	PSEL 00011b	PSEL 00101b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲SD1DAT7_B ▼ET0_LINKSTA_B ▼ET0_LINKSTA_B ▼ET1_MDC ▼ET1_MDC
	S7G2	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	-	**ET1_MDC**	**ET1_MDC**	PIXD7	
	S5D9	AGTIO0_C/AGTIO1_C	GTIOC3A_B	CTS7_A	SSISCK0_A	**SD1DAT7_B**	**ET0_LINKSTA_B**	**ET0_LINKSTA_B**	PIXD7_A	
P404		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT6_B ▼ET0_TX_EN_B ▼ET0_EXOUT_B ▼ET1_MDIO ▼ET1_MDIO
	S7G2	GTIOC3B_B	SSIWS0_A	-	**ET1_MDIO**	**ET1_MDIO**	PIXD6			
	S5D9	GTIOC3B_B	SSIWS0_A	**SD1DAT6_B**	**ET0_EXOUT_B**	**ET0_EXOUT_B**	PIXD6_A			
P405		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT5_B ▼ET0_TX_EN_B ▼RMII0_TXD_EN_B ▼ET1_TX_EN ▼RMII1_TXD_EN
	S7G2	GTIOC1A_B	SSITXD0_A	-	**ET1_TX_EN**	**RMII1_TXD_EN**	PIXD5			
	S5D9	GTIOC1A_B	SSITXD0_A	**SD1DAT5_B**	**ET0_TX_EN_B**	**RMII0_TXD_EN_B**	PIXD5_A			
P406		PSEL 00011b	PSEL 00110b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB3_C ▲SD1DAT4_B ▼ET0_RX_ER_B ▼RMII0_TXD1_B ▼ET1_RX_ER ▼RMII1_TXD1
	S7G2	GTIOC1B_B	-	SSIRXD0_A	-	**ET1_RX_ER**	**RMII1_TXD1**	PIXD4		
	S5D9	GTIOC1B_B	**SSLB3_C**	SSIRXD0_A	**SD1DAT4_B**	**ET0_RX_ER_B**	**RMII0_TXD1_B**	PIXD4_A		
P407		PSEL 00001b	PSEL 00100b	PSEL 00110b	PSEL 00111b	PSEL 01010b	PSEL 01100b	PSEL 10011b	PSEL 10110b	▲AGTIO0_E
	S7G2	-	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT	
	S5D9	**AGTIO0_E**	CTS4_A	SSLB3_A	SDA0_B	ADTRG0_B	TS3	USB_VBUS	ET0_EXOUT_A	
		PSEL 10111b								
	S7G2	ET0_EXOUT								
	S5D9	ET0_EXOUT_A								

Table 4.1 176 Pin Package Difference (8 of 14)

PORT	MCU	SELECT								COMMENTS
P408		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00111b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	▲SCL0_B ▲PIXCLK_B
	S7G2	GTOWLO_B	GTIOC10B_A	RXD3_A	**-**	TS4	USB_ID_A	USBHS_ID	ET0_CRS	
	S5D9	GTOWLO_B	GTIOC10B_A	RXD3_A	**SCL0_B**	TS4	USB_ID_A	USBHS_ID	ET0_CRS_A	
		PSEL 10111b	PSEL 11000b	ISEL						
	S7G2	RMII0_CRS_DV	**-**	IRQ7_B						
	S5D9	RMII0_CRS_DV_A	**PIXCLK_B**	IRQ7_B						
P409		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01100b	PSEL 10011b	PSEL 10100b	PSEL 10110b	PSEL 10111b	▲HSYNC_B
	S7G2	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK	RMII0_RX_ER	
	S5D9	GTOWUP_B	GTIOC10A_A	TXD3_A	TS5	USB_EXICEN_A	USBHS_EXICEN	ET0_RX_CLK_A	RMII0_RX_ER_A	
		PSEL 11000b	ISEL							
	S7G2	**-**	IRQ6_B							
	S5D9	**HSYNC_B**	IRQ6_B							
P410		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD0_B
	S7G2	AGTOB1	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1	
	S5D9	AGTOB1_A	GTOVLO_B	GTIOC9B_A	RXD0_B	SCK3_A	MISOA_B	TS6	SD0DAT1_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD0	RMII0_RXD1	**-**	IRQ5_B					
	S5D9	ET0_ERXD0_A	RMII0_RXD1_A	**PIXD0_B**	IRQ5_B					
P411		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 10101b	▲PIXD1_B
	S7G2	AGTOA1	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0	
	S5D9	AGTOA1_A	GTOVUP_B	GTIOC9A_A	TXD0_B	CTS3_A	MOSIA_B	TS7	SD0DAT0_A	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S7G2	ET0_ERXD1	RMII0_RXD0	**-**	IRQ4_B					
	S5D9	ET0_ERXD1_A	RMII0_RXD0_A	**PIXD1_B**	IRQ4_B					

Table 4.1 176 Pin Package Difference (9 of 14)

PORT	MCU	SELECT								COMMENTS
P412		PSEL 00001b	PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	▲AGTEE1_C ▲PIXD2_B
	S7G2	-	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD	ET0_ETXD0	REF50CK0	
	S5D9	**AGTEE1_C**	GTOULO_B	SCK0_B	RSPCKA_B	TS8	SD0CMD_A	ET0_ETXD0_A	REF50CK0_A	
		PSEL 11000b								
	S7G2	-								
	S5D9	**PIXD2_B**								
P413		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲PIXD3_B
	S7G2	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK	ET0_ETXD1	RMII0_TXD0	-	
	S5D9	GTOUUP_B	CTS0_B	SSLA0_B	TS9	SD0CLK_A	ET0_ETXD1_A	RMII0_TXD0_A	**PIXD3_B**	
P414		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL	▲GTIOC0B_C ▲PIXD4_B ▲IRQ9_C
	S7G2	-	SSLA1_B	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	-	-	
	S5D9	**GTIOC0B_C**	SSLA1_B	TS10	SD0WP_A	ET0_RX_ER_A	RMII0_TXD1_A	**PIXD4_B**	**IRQ9_C**	
P415		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲GTIOC0A_C ▲USB_VBUSEN_C ▲SD0CD_A ▲PIXD5_B ▲IRQ8_C
	S7G2	-	SSLA2_B	TS11	-	-	ET0_TX_EN	RMII0_TXD_EN	-	
	S5D9	**GTIOC0A_C**	SSLA2_B	TS11	**USB_VBUSEN_C**	**SD0CD_A**	ET0_TX_EN_A	RMII0_TXD_EN_A	**PIXD5_B**	
		ISEL								
	S7G2	-								
	S5D9	**IRQ8_C**								
VCL2		PSEL 00100b	PSEL 00101b	ASEL						ALL ▲
	S7G2	-	-	-						
P508	S5D9	**SCK6_C**	**SCK5_B**	**AN020**						
P511		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 10110b	PSEL 11000b	ISEL		▼ET1_TX_ER
	S7G2	GTIOC0B_B	RXD4_B	SDA2	CRX1_B	**ET1_TX_ER**	PCKO	IRQ15_A		
	S5D9	GTIOC0B_B	RXD4_B	SDA2	CRX1_B	-	PCKO_A	IRQ15_A		

Table 4.1 176 Pin Package Difference (10 of 14)

PORT	MCU	SELECT								COMMENTS
P512		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 10110b	PSEL 11000b	ISEL		▼ET1_ETXD2
	S7G2	GTIOC0A_B	TXD4_B	SCL2	CTX1_B	**ET1_ETXD2**	VSYNC	IRQ14_A		
	S5D9	GTIOC0A_B	TXD4_B	SCL2	CTX1_B	**-**	VSYNC_A	IRQ14_A		
P513		PSEL 00101b	PSEL 10110b	PSEL 11001b						▲RXD5_B ▼ET1_ETXD3
	S7G2	**-**	**ET1_ETXD3**	LCD_DATA16_B						
	S5D9	**RXD5_B**	**-**	LCD_DATA16_B						
P600		PSEL 00011b	PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 11001b			▲GTIOC6B_C ▲SCK9_C ▲CLKOUT_D ▲CACREF_E
	S7G2	**-**	**-**	**-**	**-**	RD	LCD_DATA2_A			
	S5D9	**GTIOC6B_C**	**SCK9_C**	**CLKOUT_D**	**CACREF_E**	RD	LCD_DATA2_A			
P601		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC6A_C ▲RXD9_C
	S7G2	**-**	**-**	WR/WR0	DQM0	LCD_DATA3_A				
	S5D9	**GTIOC6A_C**	**RXD9_C**	WR/WR0	DQM0	LCD_DATA3_A				
P602		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b	PSEL 11001b				▲GTIOC7B_C ▲TXD9_C
	S7G2	**-**	**-**	BCLK	SDCLK	LCD_DATA4_A				
	S5D9	**GTIOC7B_C**	**TXD9_C**	BCLK	SDCLK	LCD_DATA4_A				
P603		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01011b					▲GTIOC7A_C ▲CTS9_C
	S7G2	**-**	**-**	D13	DQ13					
	S5D9	**GTIOC7A_C**	**CTS9_C**	D13	DQ13					
P604		PSEL 00011b	PSEL 01011b	PSEL 01011b						▲GTIOC8B_C
	S7G2	**-**	D12	DQ12						
	S5D9	**GTIOC8B_C**	D12	DQ12						
P605		PSEL 00011b	PSEL 01011b	PSEL 01011b						▲GTIOC8A_C
	S7G2	**-**	D11	DQ11						
	S5D9	**GTIOC8A_C**	D11	DQ11						

Table 4.1 176 Pin Package Difference (11 of 14)

PORT	MCU	SELECT								COMMENTS
P606		PSEL 00100b	PSEL 11001b							▲CTS8_C
	S7G2	-	LCD_DATA3_B							
	S5D9	**CTS8_C**	LCD_DATA3_B							
P607		PSEL 00100b	PSEL 11001b							▲RXD8_C
	S7G2	-	LCD_DATA4_B							
	S5D9	**RXD8_C**	LCD_DATA4_B							
P608		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 11001b					▲GTIOC4B_C
	S7G2	-	A0/BC0	A0/DQM1	LCD_DATA7_A					
	S5D9	**GTIOC4B_C**	A0/BC0	A0/DQM1	LCD_DATA7_A					
P609		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5A_C ▲CTX1_C
	S7G2	-	CS1#	CKE	-	LCD_DATA6_A				
	S5D9	**GTIOC5A_C**	CS1#	CKE	**CTX1_C**	LCD_DATA6_A				
P610		PSEL 00011b	PSEL 01011b	PSEL 01011b	PSEL 10000b	PSEL 11001b				▲GTIOC5B_C ▲CRX1_C
	S7G2	-	CS0#	WE	-	LCD_DATA5_A				
	S5D9	**GTIOC5B_C**	CS0#	WE	**CRX1_C**	LCD_DATA5_A				
P611		PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b					▲CTS7_C ▲CLKOUT_C ▲CACREF_D
	S7G2	-	-	-	SDCS					
	S5D9	**CTS7_C**	**CLKOUT_C**	**CACREF_D**	SDCS					
P612		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲SCK7_C
	S7G2	-	D8	DQ8						
	S5D9	**SCK7_C**	D8	DQ8						
P613		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲TXD7_C
	S7G2	-	D9	DQ9						
	S5D9	**TXD7_C**	D9	DQ9						

Table 4.1 176 Pin Package Difference (12 of 14)

PORT	MCU	SELECT								COMMENTS
P614		PSEL 00101b	PSEL 01011b	PSEL 01011b						▲RXD7_C
	S7G2	-	D10	DQ10						
	S5D9	**RXD7_C**	D10	DQ10						
P700		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MISOB_C ▲SD1DAT3_B ▼ET0_ETXD1_B ▼RMII0_TXD0_B ▼ET1_ETXD1 ▼RMII1_TXD0
	S7G2	GTIOC5A_B	-	-	**ET1_ETXD1**	**RMII1_TXD0**	PIXD3			
	S5D9	GTIOC5A_B	**MISOB_C**	**SD1DAT3_B**	**ET0_ETXD1_B**	**RMII0_TXD0_B**	PIXD3_A			
P701		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MISOB_C ▲SD1DAT2_B ▼ET0_ETXD0_B ▼REF50CK0_B ▼ET1_ETXD0 ▼REF50CK1
	S7G2	GTIOC5B_B	-	-	**ET1_ETXD0**	**REF50CK1**	PIXD2			
	S5D9	GTIOC5B_B	**MOSIB_C**	**SD1DAT2_B**	**ET0_ETXD0_B**	**REF50CK0_B**	PIXD2_A			
P702		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲RSPCKB_C ▲SD1DAT1_B ▼ET0_ERXD1_B ▼RMII0_RXD0_B ▼ET1_ERXD1 ▼RMII1_RXD0
	S7G2	GTIOC6A_B	-	-	**ET1_ERXD1**	**RMII1_RXD0**	PIXD1			
	S5D9	GTIOC6A_B	**RSPCKB_C**	**SD1DAT1_B**	**ET0_ERXD1_B**	**RMII0_RXD0_B**	PIXD1_A			
P703		PSEL 00011b	PSEL 00110b	PSEL 01001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB0_C ▲SD1DAT0_B ▲VCOUT_B ▼ET0_ERXD0_B ▼RMII0_RXD1_B ▼ET1_ERXD0 ▼RMII1_RXD1
	S7G2	GTIOC6B_B	-	-	-	**ET1_ERXD0**	**RMII1_RXD1**	PIXD0		
	S5D9	GTIOC6B_B	**SSLB0_C**	**VCOUT_B**	**SD1DAT0_B**	**ET0_ERXD0_B**	**RMII0_RXD1_B**	PIXD0_A		
P704		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲AGTO0_B ▲SSLB1_C ▲CTX0_E ▲SD1CLK_B ▼ET0_RX_CLK_B ▼RMII0_RX_ER_B ▼ET1_RX_CLK ▼RMII1_RX_ER
	S7G2	-	-	-	-	**ET1_RX_CLK**	**RMII1_RX_ER**	HSYNC		
	S5D9	**AGTO0_B**	**SSLB1_C**	**CTX0_E**	**SD1CLK_B**	**ET0_RX_CLK_B**	**RMII0_RX_ER_B**	HSYNC_A		
P705		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲AGTIO0_D ▼ET1_CR ▲SSLB2_C ▲CRXO_E ▲SD1CMD_B ▼ET0_CRS_B ▼RMII0_CRS_DV_B ▼RMII1_CRS_DV
	S7G2	-	-	-	-	**ET1_CRS**	**RMII1_CRS_DV**	PIXCLK		
	S5D9	**AGTIO0_D**	**SSLB2_C**	**CRX0_E**	**SD1CMD_B**	**ET0_CRS_B**	**RMII0_CRS_DV_B**	PIXCLK_A		
P706		PSEL 00101b	PSEL 10100b	PSEL 10101b	ISEL					▲SD1CD_B
	S7G2	RXD3_B	USBHS_OVRCURB	-	IRQ7_A					
	S5D9	RXD3_B	USBHS_OVRCURB	**SD1CD_B**	IRQ7_A					

Table 4.1 176 Pin Package Difference (13 of 14)

PORT	MCU	SELECT								COMMENTS
P707		PSEL 00101b	PSEL 10100b	PSEL 10101b	ISEL					▲SD1WP_B
	S7G2	TXD3_B	USBHS_OVRCURA	-	IRQ8_A					
	S5D9	TXD3_B	USBHS_OVRCURA	**SD1WP_B**	IRQ8_A					
VSS		PSEL 00101b	PSEL 00110b	PSEL 01010b	PSEL 01100b	PSEL 10010b	PSEL 10110b	PSEL 11000b	ISEL	All ▲
	S7G2	-	-	-	-	-	-	-	-	
P708	S5D9	**RXD1_B**	**SSLA3_B**	**CACREF_B**	**TS12**	**AUDIO_CLK_C**	**ET0_ETXD3**	**PCKO_B**	**IRQ11_B**	
P805		PSEL 00101b	PSEL 11001b							▲TXD5_B
	S7G2	-	LCD_DATA17_B							
	S5D9	**TXD5_B**	LCD_DATA17_B							
P900		PSEL 00100b	PSEL 01011b	PSEL 11001b						▲TXD4_C
	S7G2	-	A23	LCD_CLK_B						
	S5D9	**TXD4_C**	A23	LCD_CLK_B						
P901		PSEL 00001b	PSEL 00100b	PSEL 11001b						▲AGTIO1_E ▲SCK4_C
	S7G2	-	-	LCD_DATA15_B						
	S5D9	**AGTIO1_E**	**SCK4_C**	LCD_DATA15_B						
P905		PSEL 00011b	PSEL 01011b	PSEL 11001b						▲GTIOC13B_B
	S7G2	-	CS4#	LCD_DATA11_B						
	S5D9	**GTIOC13B_B**	CS4#	LCD_DATA11_B						
P906		PSEL 00011b	PSEL 01011b	PSEL 11001b						▲GTIOC13A_B
	S7G2	-	CS5#	LCD_DATA12_B						
	S5D9	**GTIOC13A_B**	CS5#	LCD_DATA12_B						
P907		PSEL 00011b	PSEL 01011b	PSEL 11001b						▲GTIOC12B_B
	S7G2	-	CS6#	LCD_DATA13_B						
	S5D9	**GTIOC12B_B**	CS6#	LCD_DATA13_B						

Table 4.1 176 Pin Package Difference (14 of 14)

PORT	MCU	SELECT								COMMENTS
P908		PSEL 00011b	PSEL 01011b	PSEL 11001b						▲GTIOC12A_B
	S7G2	-	CS7#	LCD_DATA14_B						
	S5D9	GTIOC12A_B	CS7#	LCD_DATA14_B						
PA00		PSEL 00100b	PSEL 11001b							▲TXD8_C
	S7G2	-	LCD_DATA5_B							
	S5D9	TXD8_C	LCD_DATA5_B							
PA01		PSEL 00100b	PSEL 11001b							▲SCK8_C
	S7G2	-	LCD_DATA6_B							
	S5D9	SCK8_C	LCD_DATA6_B							

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar 17, 2017	-	Initial version

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