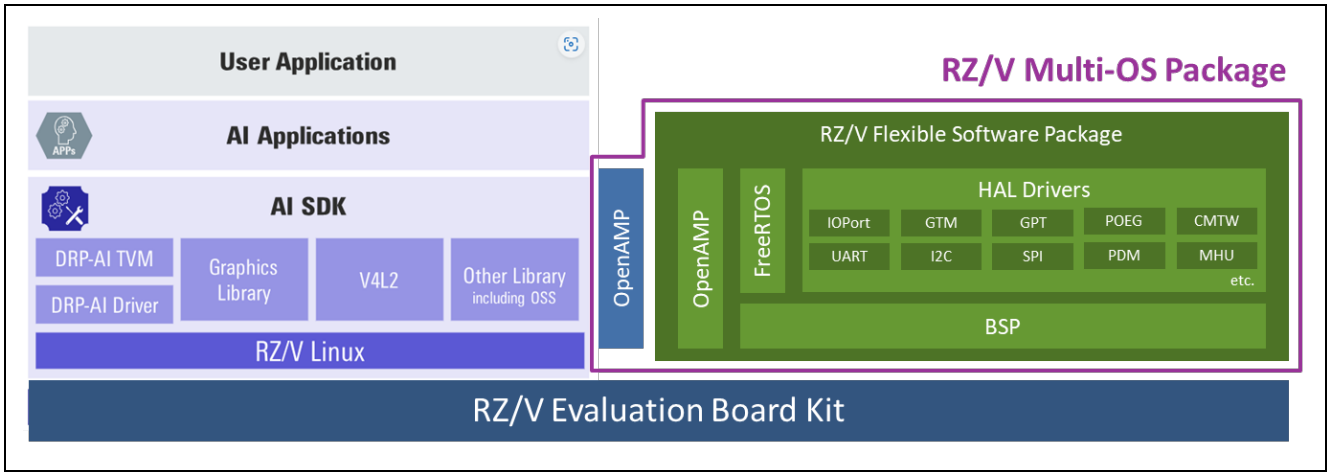
RZ/V2N

Quick Start Guide for RZ/V Multi-OS Package

Introduction

This document outlines the procedure for integrating the RZ/V Multi-OS Package into RZ/V2N AI SDK. By integrating the Multi-OS Package, users can efficiently establish a Multi-OS environment wherein Linux operates on the Cortex®-A55 and FreeRTOS/BareMetal runs on the Cortex-M33 with support for Inter-Processor Communication between these CPU cores.

This package requires the RZ/V Flexible Software Package (FSP) for an RTOS/BareMetal environment. The figure below illustrates the software stack of the RZ/V Multi-OS Package with the RZ/V2N:



Here are brief descriptions of each component related to RZ/V Multi-OS Package:

- RZ/V FSP
  This software package consists of production ready peripheral drivers, FreeRTOS and portable middleware stacks and best in-case HAL drivers with low memory footprint.
- OpenAMP
  The framework includes the software components required for Asymmetric Multiprocessing (AMP) systems, such as Inter-Processor Communication.

Target Device

RZ/V2N

Contents

1. Specifications

Table 1-1 lists the on-chip peripheral modules to be used in this package.

Table 1-1 Peripheral modules to be used in this package

Peripheral module	Usage
Message Handling Unit (MHU)	Configure Inter-Processor Interrupt.
Serial Communications Interface with FIFO (SCIFA)	Perform standard serial communications sending and receiving console messages.
Interrupt controller (INTC)	Handle the following types of interrupts as shown below for example: • Processors should receive interrupts during buffered serial communications. • MHU module fires Inter-Processor Interrupt.
General Purpose Input Output (GPIO)	Configure I/O lines used by serial communications.
General Timer (GTM)	Configure the tick for FreeRTOS.

2. Verified Operation Conditions

Table 2-1 shows the verified operation conditions.

Item	Contents
Integrated Development Environment	e^2 studio 2025-01
Toolchain	GNU Arm Toolchain 13.3.Rel1 AArch32 bare-metal target (arm-none-eabi)
Dependent Software	• RZ/V Flexible Software Package (FSP) v3.1.0 • RZ/V2N AI Software Development Kit (SDK) v5.00

3. Sample Program Setup

3.1 Flexible Software Package Setup

Multi-OS Package expects RZ/V Flexible Software Package (FSP) to be installed in advance. For details on the installation, please refer to Getting Started with RZ/V Flexible Software Package.

3.2 Integration of OpenAMP related stuff

This section describes how to integrate OpenAMP related stuff into **RZ/V2N AI Software Development Kit** (hereinafter referred to as **RZ/V2N AI SDK**).

1. Carry out **Step 1**, **Step 2** and **1-11 of Step 3** stated in **How to build RZ/V2N AI SDK Source Code** showcased at AI Applications and AI SDK of RZ/V series.
2. Download Multi-OS Package (r01an7254ej0311-rzv-multi-os-pkg.zip) to a working directory and run the commands stated below:

```
$ cd ${YOCTO_WORK}
$ unzip <Multi-OS Dir>/r01an7254ej0311-rzv-multi-os-pkg.zip
$ tar zxvf r01an7254ej0311-rzv-multi-os-pkg/meta-rz-features_multi-os_v3.1.1.tar.gz
```

   Here, <Multi-OS Dir> stands for the path to the directory where Multi-OS Package is placed.

3. Add the layer for Multi-OS Package.

```
$ cd build
$ bitbake-layers add-layer ../meta-rz-features/meta-rz-multi-os/meta-rzv2n
```

(Optional for remoteproc support)

4. Apply the modification below to **meta-rz-features/meta-rz-multi-os/meta-rzv2n/recipes-kernel/linux/linux-renesas_5.10.bbappend** for enabling remoteproc support:

```
$ FILESEXTRAPATHS_prepend := "${THISDIR}/${PN}:"
$ ENABLE_REMOTEPROC = "1"
```

(Optional for CM33 invocation from u-boot)

5. Uncomment the following 2nd line stated in **meta-rz-features/meta-rz-multi-os/meta-rzv2h/conf/layer.conf**. For details on CM33 invocation from u-boot, please see 4.3.2.

```
#MACHINE_FEATURES_append = " RZV2H_CM33_BOOT"
MACHINE_FEATURES_append = " SRAM_REGION_ACCESS"
#MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
#MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

6. Carry out **13 of Step 3** of **How to build RZ/V2N AI SDK Source Code** for building Linux kernel related stuff.

3.3 Note for Integration

The peripherals which are NOT enabled enter Module Standby Mode after Linux kernel is booted up. That means the peripherals used on CM33 side might stop working at that time. To avoid such a situation, Multi-OS Package incorporates the patch below:

- 0002-Set-OSTM-for-MCPU-and-RCPU.patch

This patch prevents GTM used in RPMsg demo program from entering Module Standby Mode. If you have any other peripherals which you would like to stop entering Module Standby implicitly, please update the patch as shown below:

```
diff --git a/drivers/clk/renesas/r9a09g056-cpg.c b/drivers/clk/renesas/r9a09g056-cpg.c
index 03a7be492353..cdb2c6bf659e 100644
--- a/drivers/clk/renesas/r9a09g056-cpg.c
+++ b/drivers/clk/renesas/r9a09g056-cpg.c
@@ -886,6 +886,13 @@ static const unsigned int r9a09g056_crit_mod_clks[] __initconst = {
  MOD_CLK_BASE + R9A09G056_ACPU_DMAC_1_ACLK,
  MOD_CLK_BASE + R9A09G056_RCPU_DMAC_0_ACLK,
  MOD_CLK_BASE + R9A09G056_RCPU_DMAC_1_ACLK,
+ MOD_CLK_BASE + R9A09G056_MCPU_OSTM0_PCLK,
+ MOD_CLK_BASE + R9A09G056_MCPU_OSTM1_PCLK,
+ MOD_CLK_BASE + R9A09G056_RCPU_OSTM0_PCLK,
+ MOD_CLK_BASE + R9A09G056_RCPU_OSTM1_PCLK,
+ MOD_CLK_BASE + R9A09G056_RCPU_OSTM2_PCLK,
+ MOD_CLK_BASE + R9A09G056_RCPU_OSTM3_PCLK,
+ MOD_CLK_BASE + R9A09G056_xxxx_PCLK,
 };

 static struct clk_mon r9a09g056_clk_mon[] = {
```

With respect to the allowable value for **xxxx**, please refer to the link below:

- https://github.com/renesas-rz/rz_linux-cip/blob/e619ed8241f998b0e7f6e70feab606272e27655a/drivers/clk/renesas/r9a09g056-cpg.c#L325-L770

3.4 Deployment of RZ/V2N AI SDK

With respect to the deployment of Linux kernel, device tree and root filesystem for RZ/V2N, please refer to https://renesas-rz.github.io/rzv_ai_sdk/5.00/.

4. Sample Program Invocation on RZ/V2N

4.1 Hardware setup

Connect J-Link to RZ/V2N EVK. For details, please refer to Getting Started with RZ/V Flexible Software Package.

4.2 CM33 Sample Program Setup

Here are the procedures for setting up the sample program running on CM33.

1. Extract **r01an7254ej0311-rzv-multi-os-pkg.zip** on your development PC.
2. Extract **rzv2n_cm33_rpmsg_linux-rtos_demo.zip** included in **r01an7254ej0311-rzv-multi-os-pkg.zip**.
3. Open e² studio 2025-01 and click **File** > **Import**.
4. Double-click General and select **Existing Projects into Workspace** as shown in Figure 4-1:

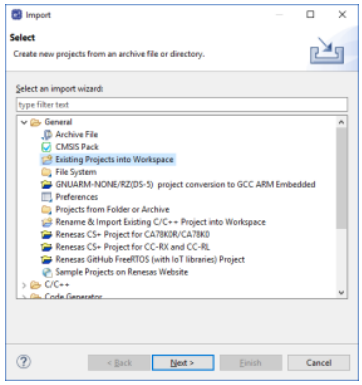


Figure 4-1. Import sample project (1)

5. Input the path to the directory where sample project you would like to import to **Select root directory**, press **Enter** key and click **Finish** button.

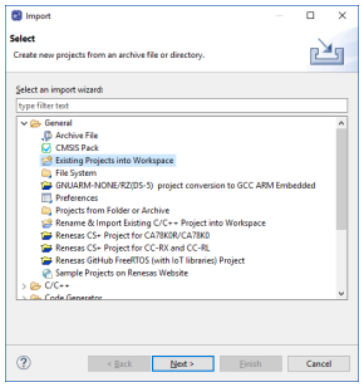


Figure 4-2. Import sample project (2)

(Optional)

6. By default, RPMsg channel 0 configured to be used on CM33. If you would like to change the channel, you need to open the property of **MainTask#0** on FSP Smart Configurator, specify the channel number

you would like to use for **Thread Control** and push **Generate Project Content** button. If **Generate Project Content** pop-up is shown, click **Proceed** to reflect the changes to source code.

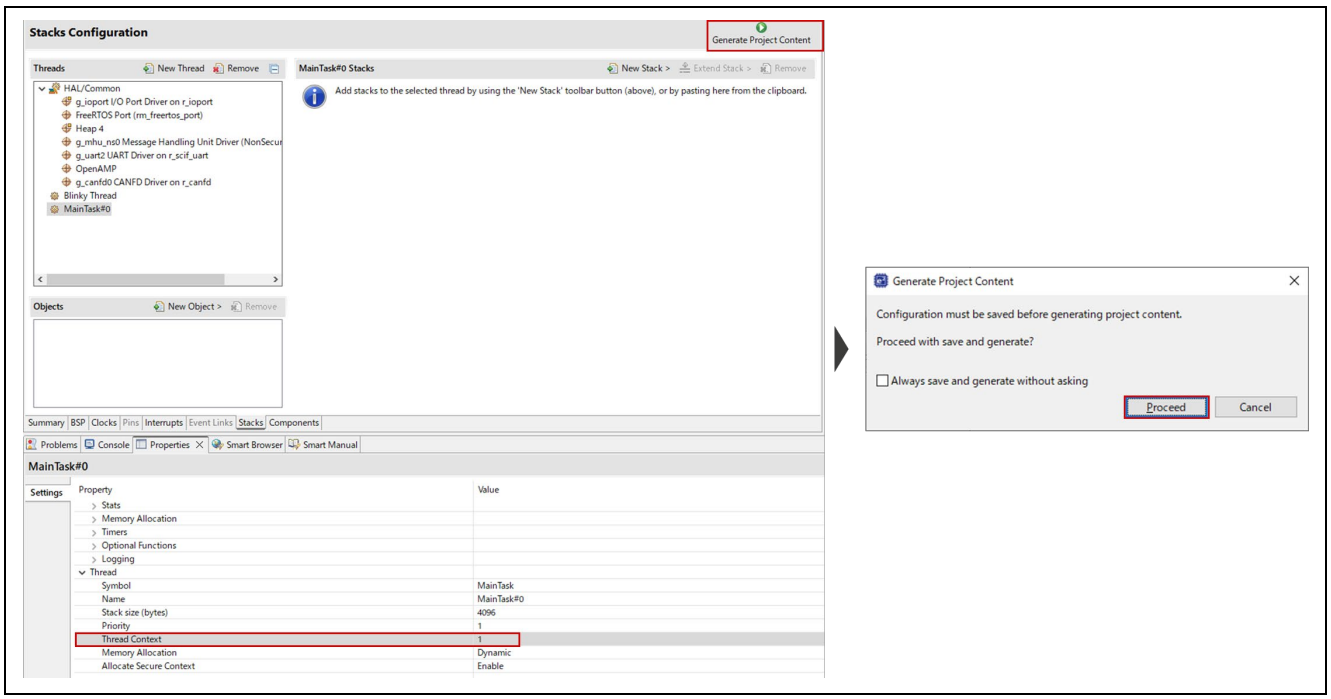


Figure 4-3. RPMsg Channel Setting

7. Build the project from **Choose Project** > **Build Project**.
8. If building project is successfully completed, build artifacts as listed below should be generated in **Debug** or **Release** directory of the project you imported in accordance with the active Build Configuration.
   - rzv2n_cm33_rpmsg_linux-rtos_demo.elf
   - rzv2n_cm33_rpmsg_linux-rtos_demo.bin

4.3 CM33 Sample Project Invocation for communicating with Linux

4.3.1 CM33 Sample Project Invocation using Segger J-Link

Carry out the procedure shown below for invoking CM33 sample project using J-Link:

1. Click Debug button as shown below:

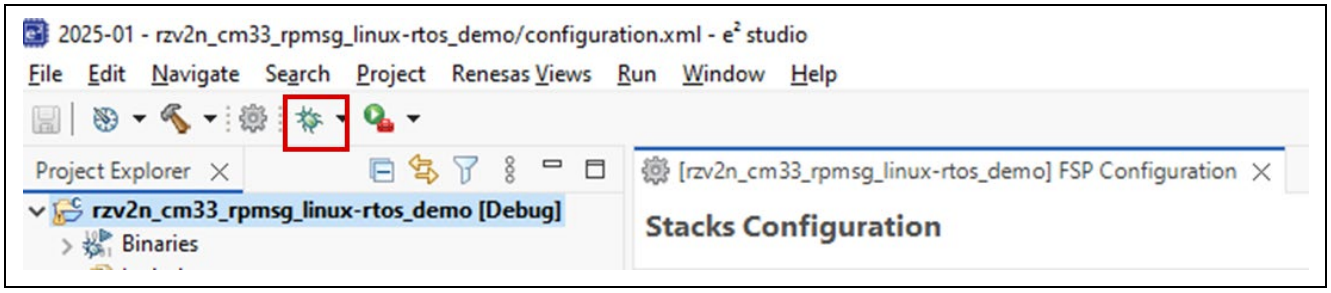


Figure 4-4. Selection of Debug Configuration

2. If the following **Select Configuration** window is shown, choose rzv2n_cm33_rpmsg_linux-rtos_demo_Debug_Flat or rzv2n_cm33_rpmsg_linux-rtos_demo_Release_Flat in accordance with the build configuration you are using and click **OK**.

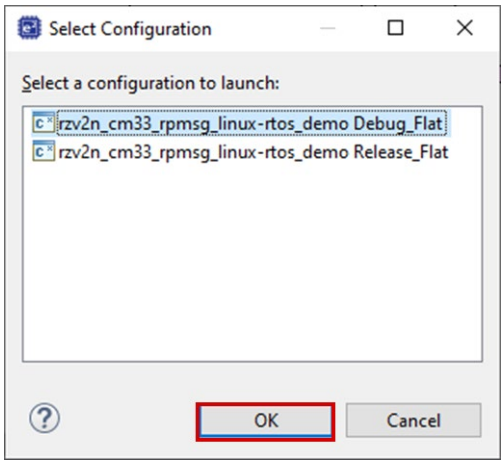


Figure 4-5. Debug Perspective Launch (1)

If the following **Confirm Perspective Switch** window appears, press **Switch** to go ahead.

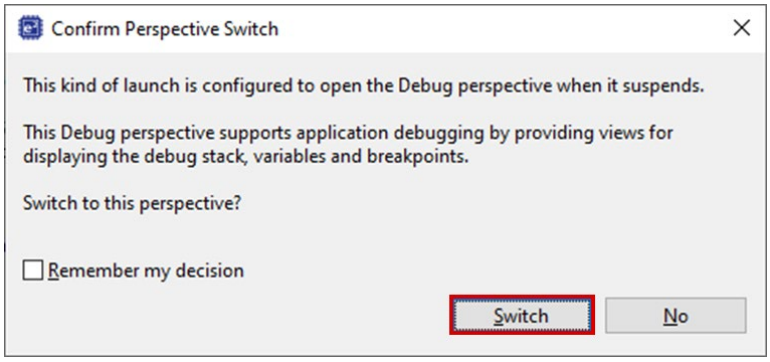


Figure 4-6. Debug Perspective Launch (2)

3. When **Debug Perspective** is opened, Program Counter (PC) should be located at the top of **Entry_Function_S**. Then, press the button shown in Figure 4.7.

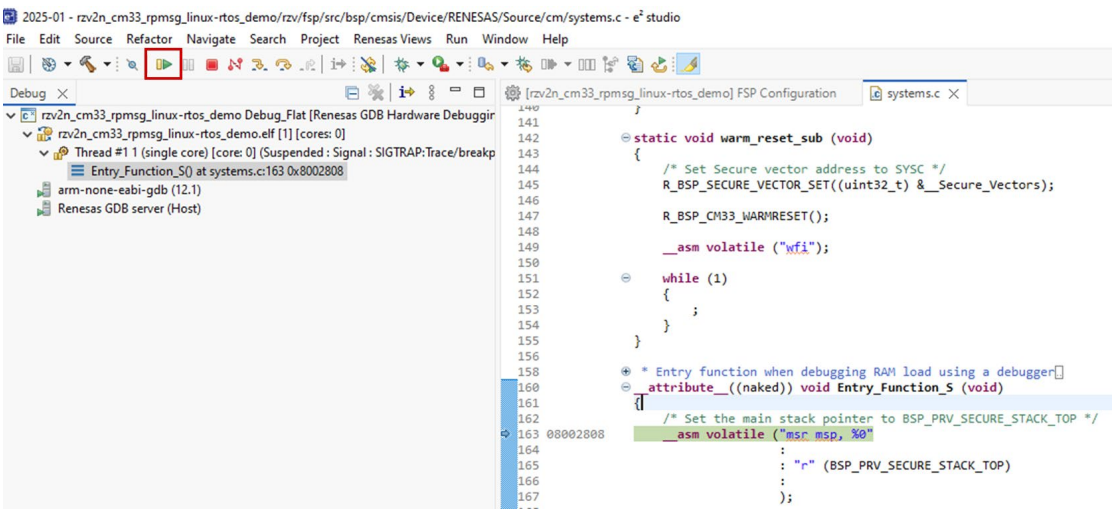


Figure 4-7. How to start to debug Sample Project (1)

4. PC should be stopped at the top of **main** function. Then, click the same button in the previous step to continue.

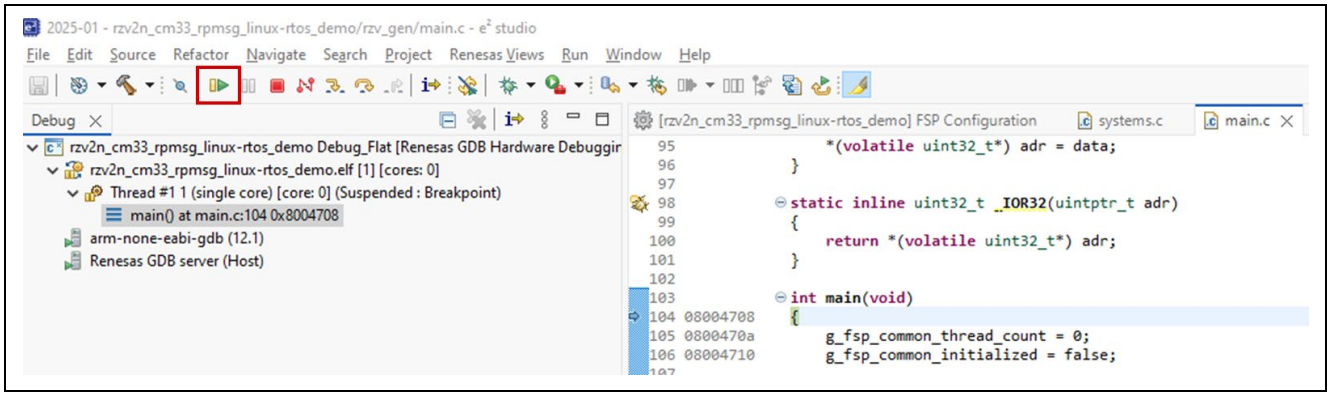


Figure 4-8. How to start to debug Sample Project (2)

5. CM33 Sample Project starts to work and wait for the launch of CA55 RPMsg Sample Program.

4.3.2 CM33 Sample Program Invocation from u-boot

Here is the procedure for invoking CM33 Sample Program from u-boot:

1. Place rzv2n_cm33_rpmsg_linux-rtos_demo.bin together with Linux kernel and Device Tree Blob.
2. Insert SD card into SD0 of RZ/V2N EVK.
3. Turn on RZ/V2N EVK. Then, you should see the following message on the console associated with CN12 of RZ/V2N EVK.

```
U-Boot 2021.10 (Nov 21 2023 - 11:34:15 +0000)
CPU: Renesas Electronics CPU rev 1.2
Model: Renesas EVK based on r9a09g056
DRAM: 7.9 GiB
MMC: mmc@15c00000: 0, mmc@15c10000: 1
Loading Environment from SPIFlash... SF: Detected mt25qu512a with page size
256 Bytes, erase size 64 KiB, total 64 MiB
OK
In: serial@11c01400
Out: serial@11c01400
Err: serial@11c01400
Net:
Error: ethernet@15c30000 address not set.
No ethernet found.
Hit any key to stop autoboot: 0
=>
```

4. Hit any key within 3 sec. to stop autoboot.
5. Carry out the following setup on u-boot to kick CM33.

```
=> setenv cm33start 'dcache off; mw.l 0x10420D2C 0x02000000; mw.l 0x1043080c
0x08003000; mw.l 0x10430810 0x18003000; mw.l 0x10420604 0x00040004; mw.l
0x10420C1C 0x00003100; mw.l 0x10420C0C 0x00000001; mw.l 0x10420904 0x00380008;
mw.l 0x10420904 0x00380038; ext4load mmc 0:2 0x08001e00 boot/
rzv2n_cm33_rpmsg_linux-rtos_demo.bin; mw.l 0x10420C0C 0x00000000; dcache on'
=> saveenv
=> run cm33start
```

4.3.3 CM33 Sample Program Invocation with remoteproc

Here is the procedure for invoking CM33 Sample Program with remoteproc:

1. Booting up Linux by following RZ/V2N EVK Getting Started.
2. Invoke the command stated below to specify the sample program to be loaded:

```
root@rzv2n-evk:~# echo rzv2n_cm33_rpmsg_linux-rtos_demo.elf >
/sys/class/remoteproc/remoteproc0/firmware
```

3. Kick CM33 by invoking the command below:

```
root@rzv2n-evk:~# echo start > /sys/class/remoteproc/remoteproc0/state
```

If CM33 Sample Program starts to work successfully, the following message should be shown on Linux console:

```
root@rzv2n-evk:~# echo start > /sys/class/remoteproc/remoteproc0/state
[ 737.289773] remoteprocremoteproc0: powering up cm33
[ 737.348226] remoteprocremoteproc0: Booting fwimage rzv2n_cm33_rpmsg_linux-rtos_demo, size 1347660
[ 737.356732] remoteprocremoteproc0: unsupported resource 4
[ 737.366255] remoteproc0#vdev0buffer: assigned reserved memory node vdev0buffer@0x43200000
[ 737.374784] remoteproc0#vdev0buffer: registered virtio0 (type 7)
[ 737.380989] remoteprocremoteproc0: remote processor cm33 is now up
```

4.4 CA55 Sample Program Invocation

This section describes how to invoke RPMsg sample program running on CA55 side.

1. Boot up Linux by executing the following command on u-boot for example:

```
=> run bootcmd
```

2. Login as **root**.

```
rzv2n-evk login: root
```

3. Invoke RPMsg sample program as shown below:

```
root@rzv2n-evk:~# rpmsg_sample_client
```

4. If the sample program started to work successfully, you can see the following message on Linux console:

```
metal: info: metal_uio_dev_open: No IRQ for device 10480000.mbox-uio.
Successfully probed IPI device
metal: info: metal_uio_dev_open: No IRQ for device 42f00000.rsctbl.
Successfully open uio device: 42f00000.rsctbl.
Successfully added memory device 42f00000.rsctbl.
metal: info: metal_uio_dev_open: No IRQ for device 43000000.vring-ctl0.
Successfully open uio device: 43000000.vring-ctl0.
Successfully added memory device 43000000.vring-ctl0.
metal: info: metal_uio_dev_open: No IRQ for device 43200000.vring-shm0.
Successfully open uio device: 43200000.vring-shm0.
Successfully added memory device 43200000.vring-shm0.
metal: info: metal_uio_dev_open: No IRQ for device 43100000.vring-ctl1.
Successfully open uio device: 43100000.vring-ctl1.
Successfully added memory device 43100000.vring-ctl1.
metal: info: metal_uio_dev_open: No IRQ for device 43500000.vring-shm1.
Successfully open uio device: 43500000.vring-shm1.
Successfully added memory device 43500000.vring-shm1.
metal: info: metal_uio_dev_open: No IRQ for device 42f01000.mhu-shm.
Successfully open uio device: 42f01000.mhu-shm.
Successfully added memory device 42f01000.mhu-shm.
Initialize remoteproc successfully.
Initialize remoteproc successfully.
****************************************
* rpmsg communication sample program *
****************************************
1. communicate with RZ/V2N CM33 ch0
2. communicate with RZ/V2N CM33 ch1
e. exit
please input
>
```

5. Type **1** if RPMsg channel 0 is used on CM33 RPMsg sample program under default setting. Otherwise, type **2** for starting the communication.
6. By typing e, the sample program should be terminated with the message shown below:

```
please input
> e
[xxx] 42f00000.rsctbl closed
[xxx] 43000000.vring-ctl0 closed
[xxx] 43200000.vring-shm0 closed
[xxx] 43100000.vring-ctl1 closed
[xxx] 43500000.vring-shm1 closed
[xxx] 42f01000.bhu-shm closed
```

4.5 Overview of Sample Program's behavior

This section describes the overview of sample program's behavior.

1. When the CA55 sample program is successfully executed, the communication channel between CA55 and CM33 is established.
2. The CA55 sample program starts to send the message to CM33 with incrementing the message size from the minimum value 17 to the maximum value 488. During the communication, the message as shown below is displayed on your console:

```
[xxx] Sending payload number 148 of size 165
```

3. When CM33 sample program receives the message sent from CA55, the echo reply is sent back to CA55 sample program.
4. When CA55 receives the echo reply, the message below should be displayed on your console:

```
[xxx] received payload number 148 of size 165
```

5. After the 488-byte sized payload is sent from CA55 to CM33 and CM33 sends back the echo reply, the message indicating the termination of the communication channel is sent from CA55 to CM33. Then, the CA55 sample program outputs the following log messages to your console:

```
[xxx] ***********************************
[xxx] Test Results: Error count = 0
[xxx] ***********************************
[xxx] Quitting application .. Echo test end
[xxx] Stopping application...
```

5. CA55 1.8GHz configuration support at CA55 cold boot mode

This chapter describes how to configure 1.8GHz as operational frequence of CA55 at CA55 cold boot.

5.1 Setup of CA55 related stuff

1. Uncomment the following lines in meta-rz-features/meta-rz-multi-os/meta-rzv2n/conf/layer.conf

```
#MACHINE_FEATURES_append = " RZV2N_CM33_BOOT"
#MACHINE_FEATURES_append = " SRAM_REGION_ACCESS"
MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

   Be sure NOT to uncomment the 1st line for CM33 cold boot support.

2. Rebuild TrustedFirmware-A as shown below:

```
MACHINE=rzv2n-evk bitbake trusted-firmware-a -c cleansstate
MACHINE=rzv2n-evk bitbake firmware-pack -c cleansstate
MACHINE=rzv2n-evk bitbake core-image-weston
```

3. Deploy build artifacts to SD card by following Renesas RZ/V AI | The best solution for starting your AI applications.

5.2 Setup of CM33 related stuff

1. Import or create RZ/V FSP project for CM33.
2. Open **configurator.xml** in the project and choose **BSP** tab.
3. Configure **Clock up for CA55** properties as Enable. Also, enabled **Launch CA55(core0)** if you would like to configure operational at CM33 cold boot mode.
4. Click **Generate Project Content** to reflect the changes to your project.

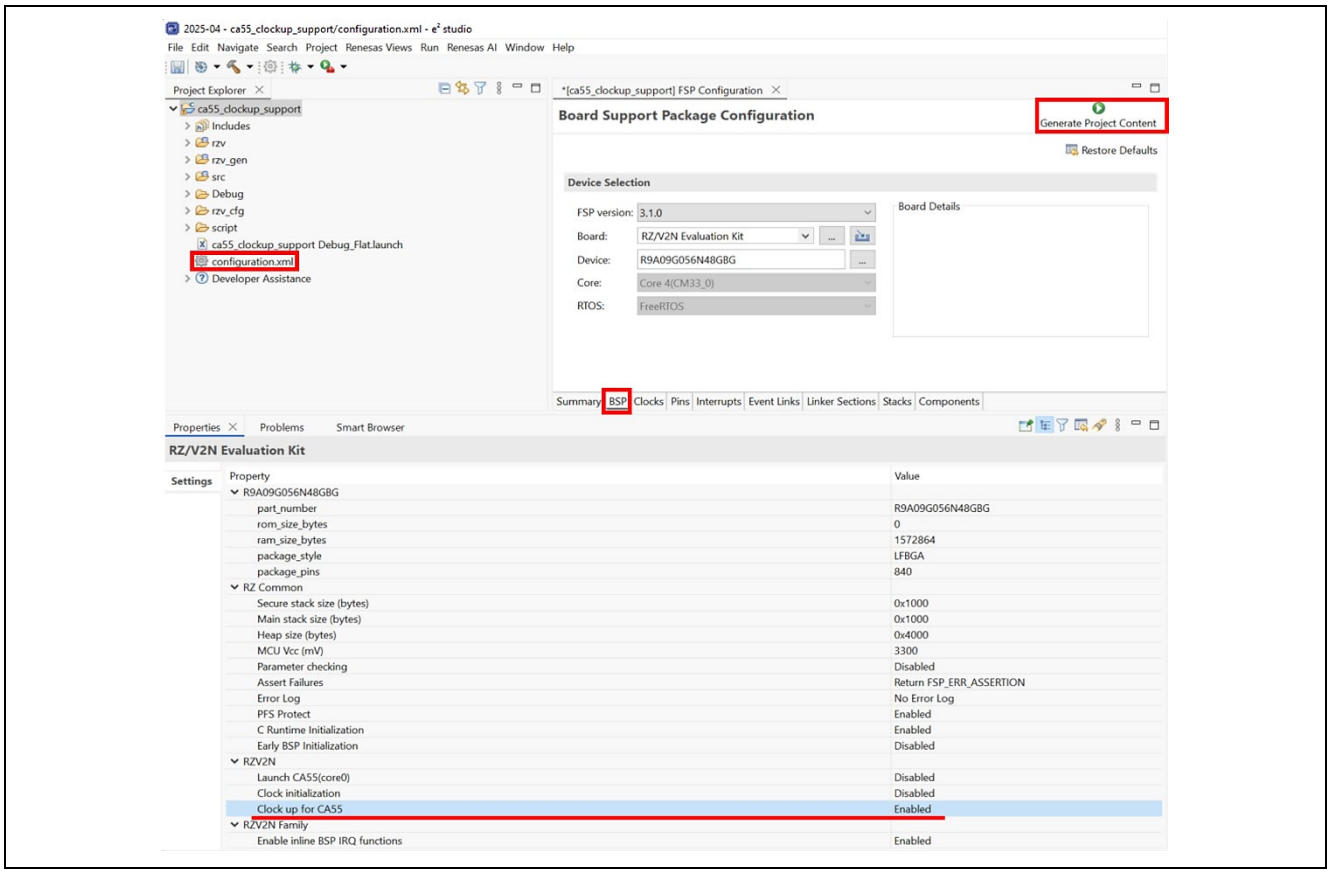


Figure 5-1. CM33 project setting for CA55 1.8GHz support (CA55 coldboot)

6. Build the project from **Project** > **Build Project**.

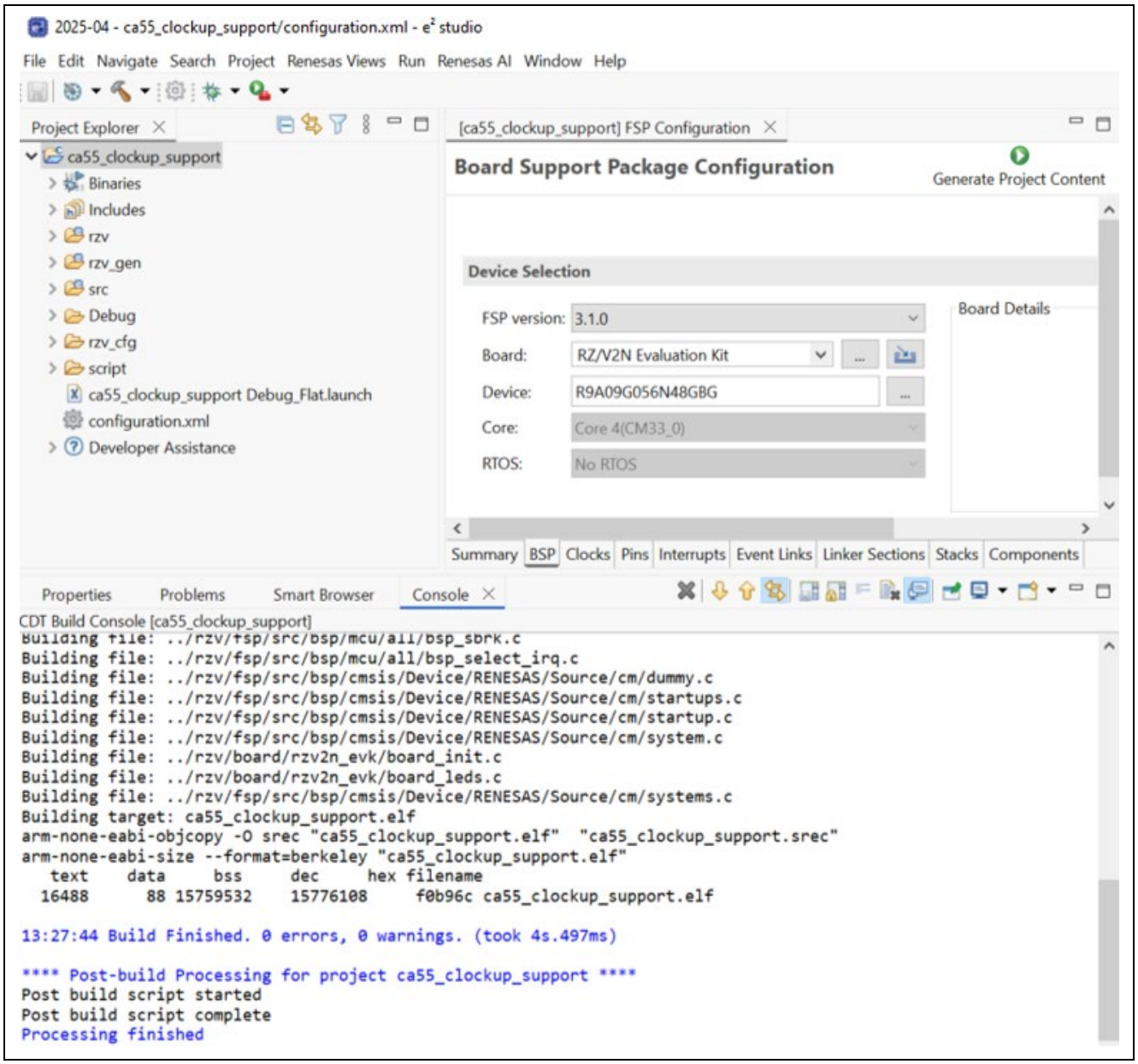


Figure 5-2. Build CM33 project for CA55 1.8GHz support

5.3 Deployment of Build Artifacts to RZ/V2N EVK

This section describes the procedure to program the build artifacts to RZ/V2N EVK.

1. Connect CN12 of RZ/V2N EVK with Host PC and established serial port connection.
2. Configure DSW1-4 and DSW1-5 of RZ/V2N EVK as OFF and ON respectively to specify boot mode as SCIF download mode.
3. Turn on RZ/V2N EVK. Then, the following message is shown on your terminal:

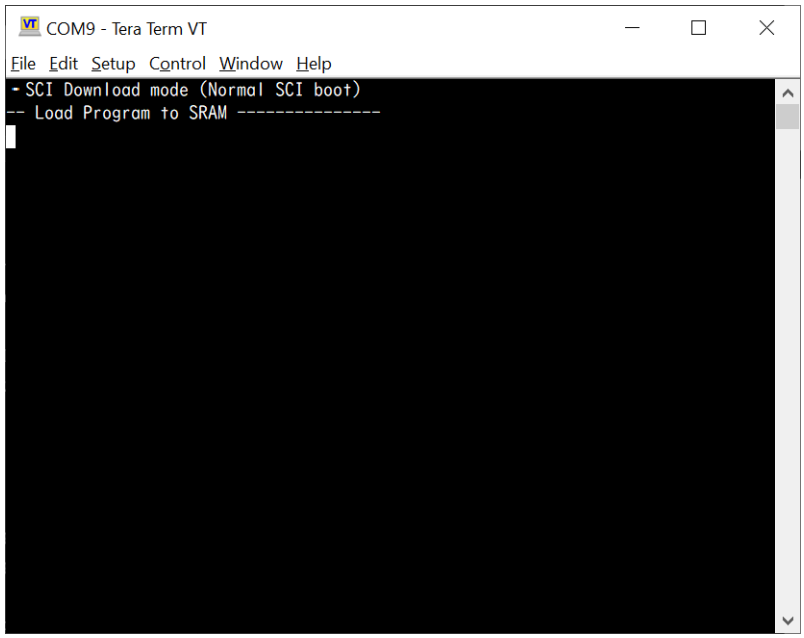


Figure 5-3. SCIF Download mode

4. Send **Flash_Writer_SCIF_RZV2N_DEV_INTERNAL_MEMORY.mot** to RZ/V2N EVK via terminal software. If it's successfully transferred, the following message is shown on your terminal:

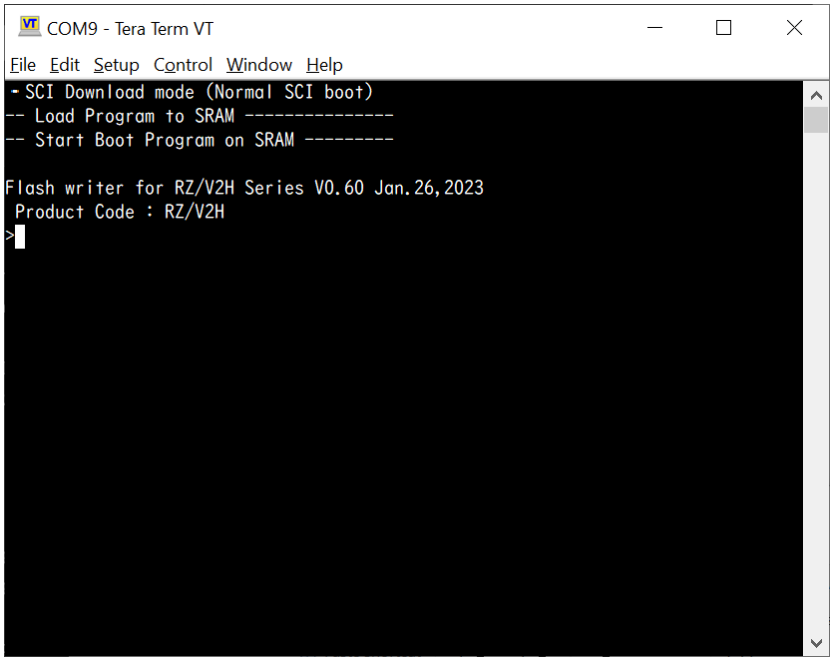


Figure 5-4. Flash Writer invocation

5. Program **bl2_bp_spi-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'8101E00

===== Please Input Qspi Save Address ===
  Please Input : H'00000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00000000
SpiFlashMemory End Address  : H'00037E57
============================================================
```

6. Program **fip-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'60000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00060000
SpiFlashMemory End Address  : H'0011C2BE
============================================================
```

7. Program CM33 FW (S-record formatted one) with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'202000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00202000
SpiFlashMemory End Address  : H'002071F2
============================================================
```

6. CM33 cold boot support

This chapter describes how CA55 and CM33 related stuff should be built for CM33 cold boot.

6.1 Setup of CA55 related stuff

1. Uncomment the following lines in meta-rz-features/meta-rz-multi-os/meta-rzv2n/conf/layer.conf

```
MACHINE_FEATURES_append = " RZV2N_CM33_BOOT"
#MACHINE_FEATURES_append = " SRAM_REGION_ACCESS"
#MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
#MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

   Be sure to uncomment the above mentioned 3rd and 4th line when CM33 cold boot support is enabled.

2. Rebuild TrustedFirmware-A as shown below:

```
MACHINE=rzv2n-evk bitbake trusted-firmware-a -c cleansstate
MACHINE=rzv2n-evk bitbake firmware-pack -c cleansstate
MACHINE=rzv2n-evk bitbake core-image-weston
```

3. Deploy build artifacts to SD card by following Renesas RZ/V AI | The best solution for starting your AI applications.

6.2 Deployment of CA55 Build Artifacts to RZ/V2N EVK

This section describes how to deploy CA55 Build Artifacts to RZ/V2N EVK. First, please carry out the same procedure as 1 to 4 stated in **5.3 Deployment of Build Artifacts to RZ/V2N EVK**. Then, follow the steps stated below:

1. Program **bl2_bp_spi-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'8101E00

===== Please Input Qspi Save Address ===
  Please Input : H'100000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00100000
SpiFlashMemory End Address  : H'00136D17
============================================================
```

2. Program **fip-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'280000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00280000
SpiFlashMemory End Address  : H'0033C2BE
============================================================
```

6.3 Setup of CM33 related stuff

1. Import or create RZ/V FSP project for CM33.
2. Open **configurator.xml** in the project and choose **BSP** tab.
3. (Optional) Configure **Launch CA55(core0) and Clock up for CA55** as Enabled.
4. Click **Generate Project Content** to reflect the changes to your project.

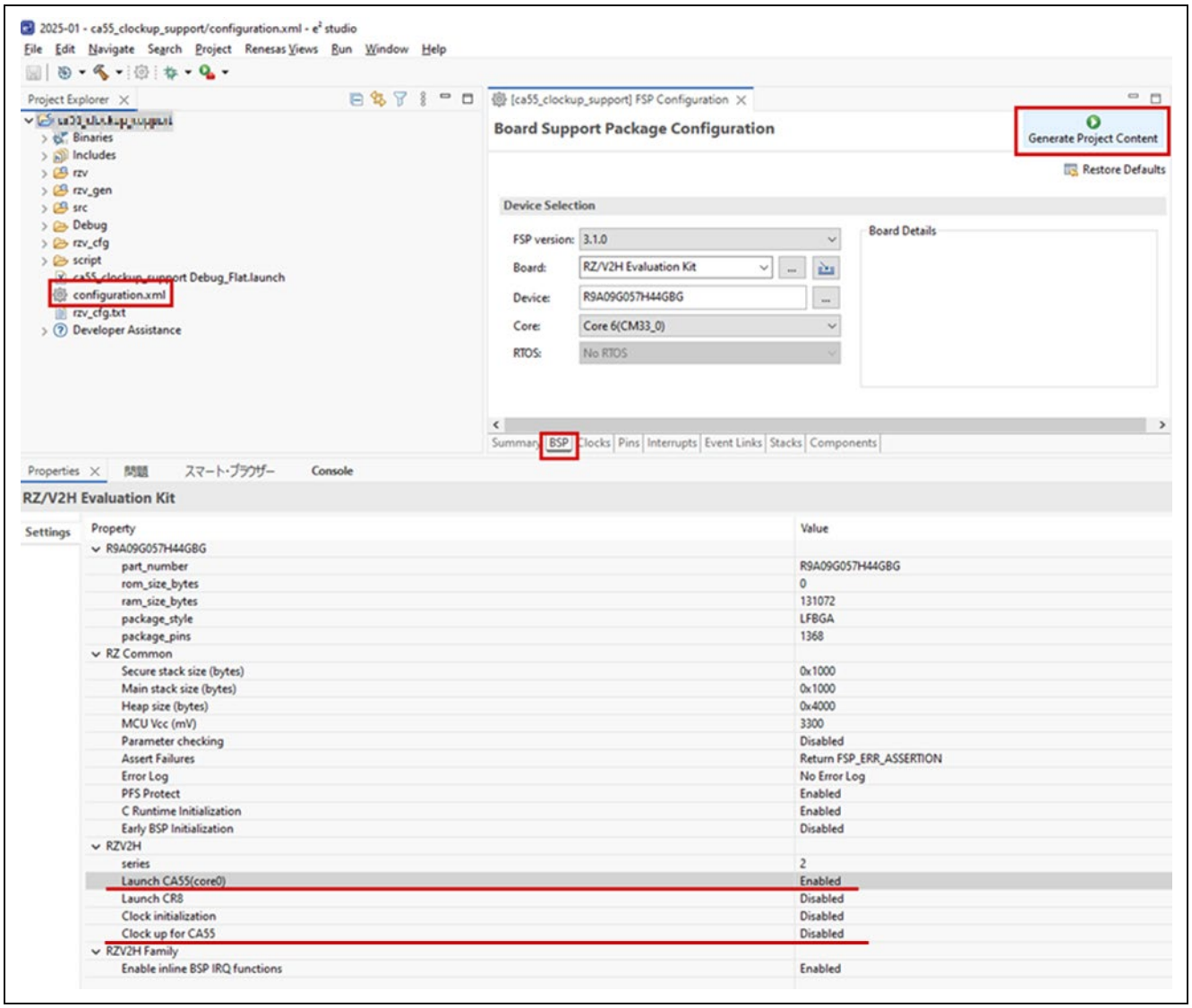


Figure 5-5. CM33 project setting for CM33 cold boot

5. Build the project from **Project** > **Build Project**.
6. Click **Run** > **Debug Configurations...** , expand **Renesas GDB Hardware Debugging** and choose **<project name> Debug_Flat**.

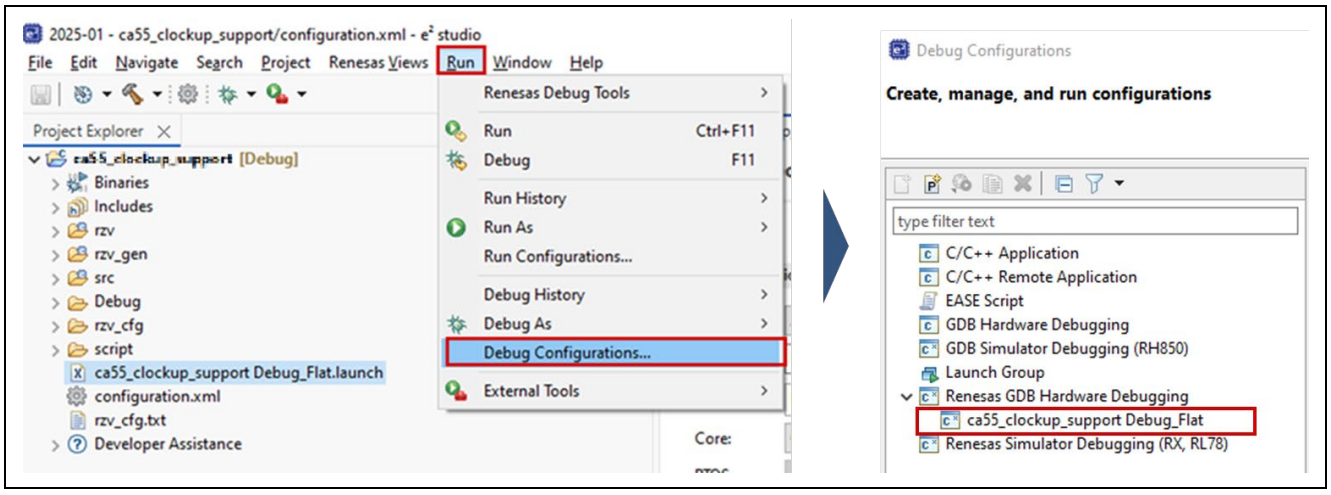


Figure 5-6. Debug Configuration Launch

7. Choose **Debugger** > **Connection Settings** and specify **Yes** to **Reset after download**.

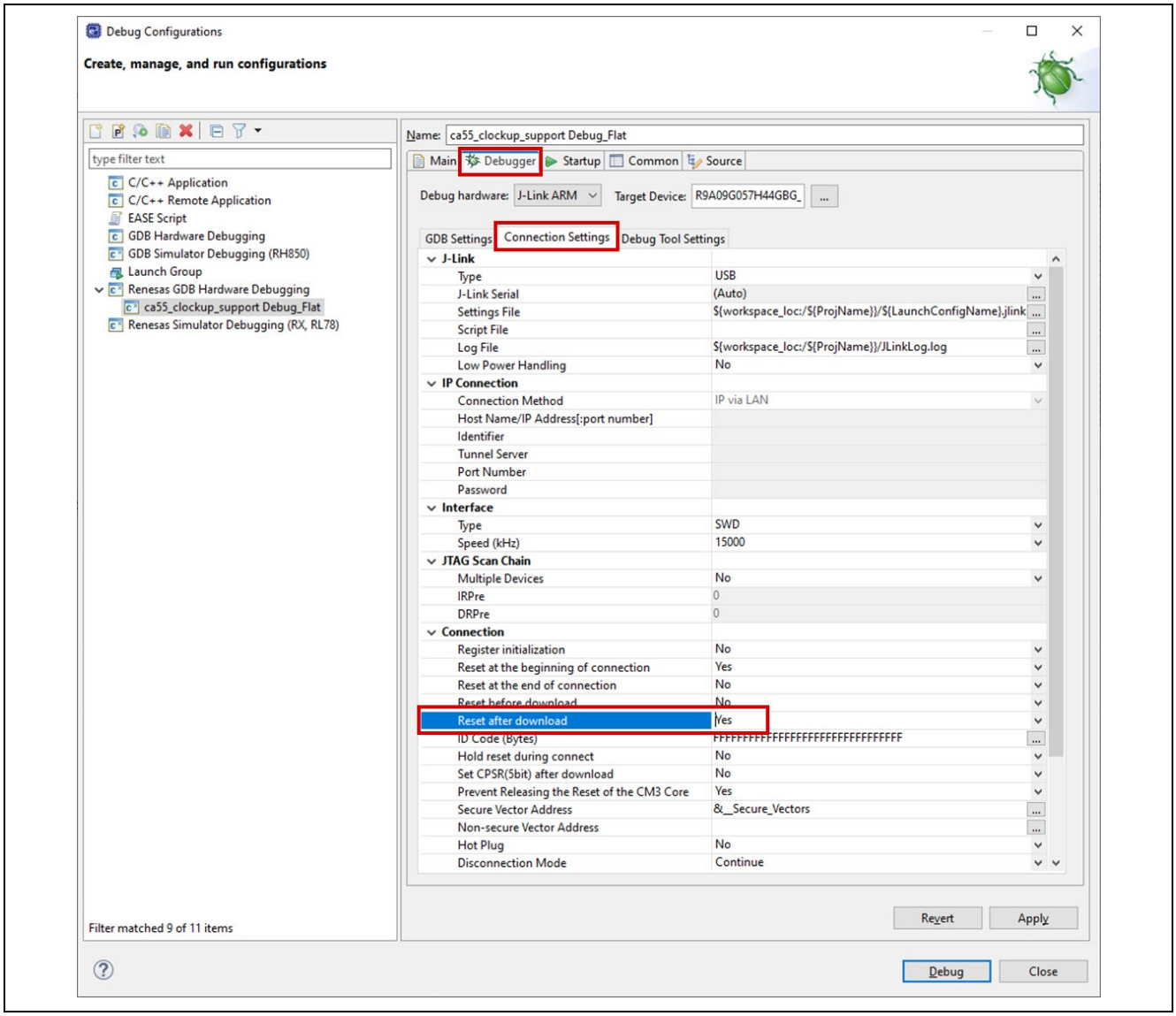


Figure 5-7. Connection Settings

8. Choose Startup and change the Load type of Program Binary to Symbols only.

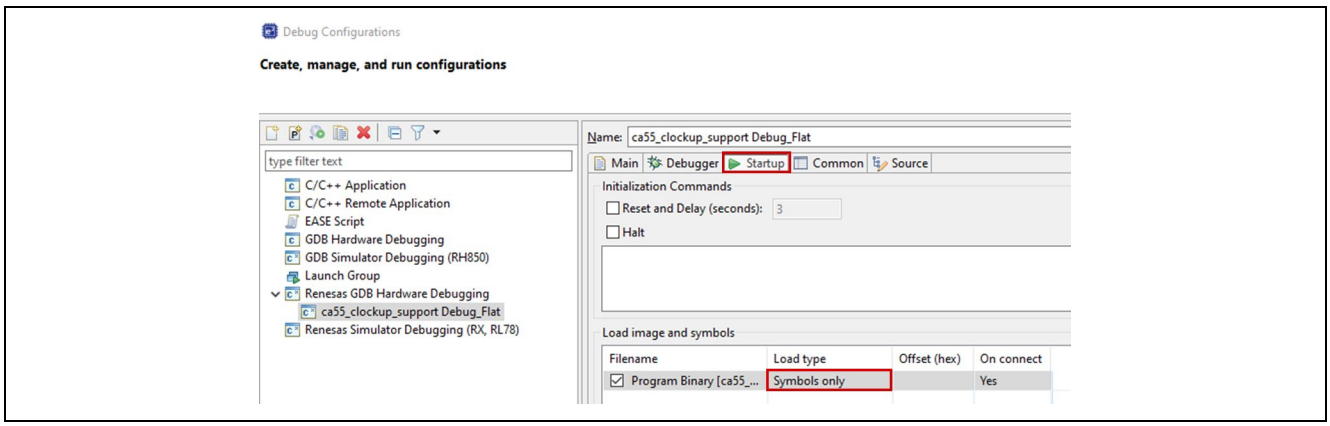


Figure 5-8. Startup Settings (1)

9. Click Add... > Workspace… , choose srec file and click OK.

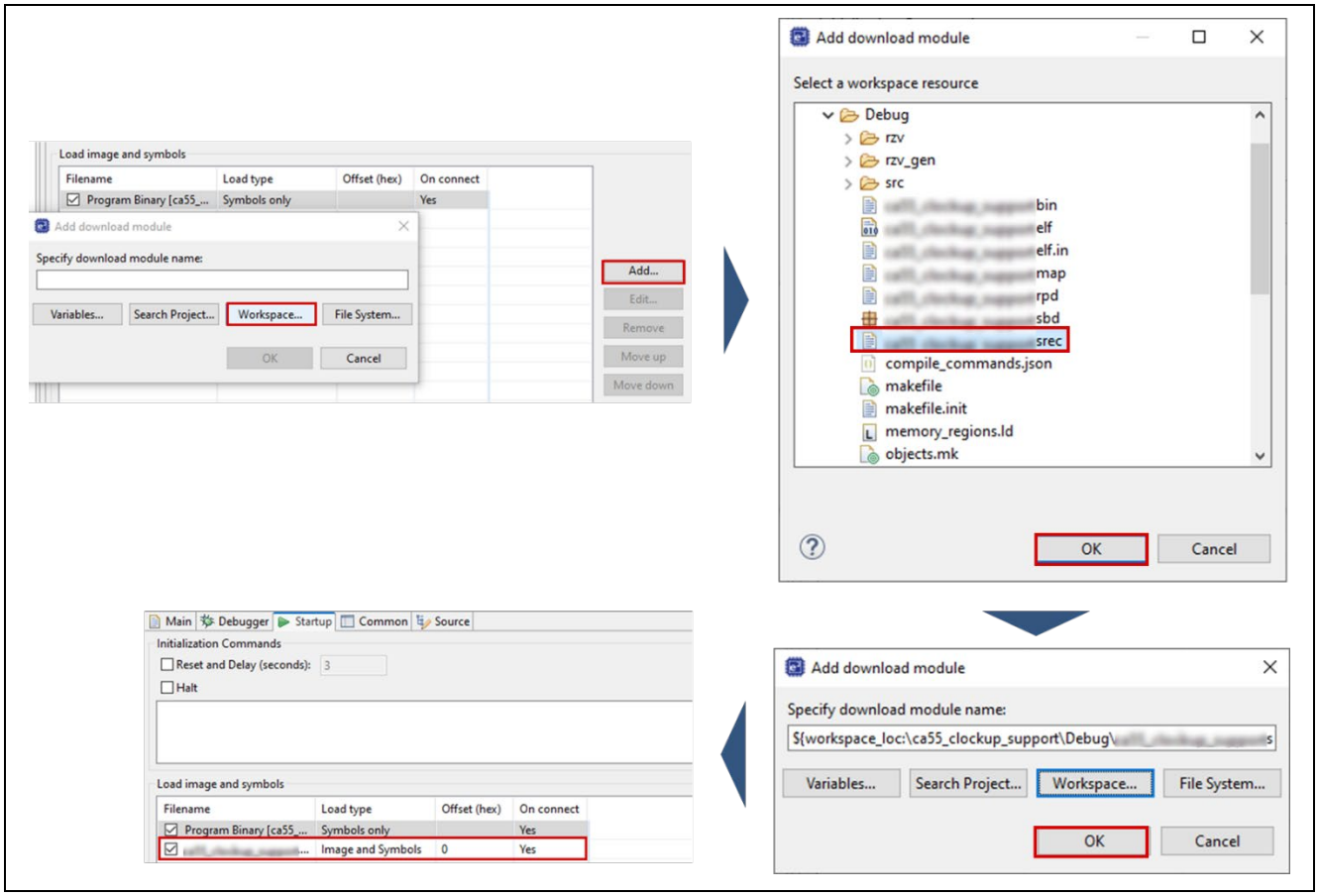


Figure 5-8. Startup Settings (2)

10. Click **Debug** to launch Debug Perspective. Note that DSW1-1, 4, 5 and 7 should be specified as OFF, OFF, OFF, ON, respectively before the launch. Then, CM33 program starts, load CA55 build artifacts from QSPI Flash ROM and kick CA55.

    For details on CM33 program invocation with e2studio, please see Getting Started with RZ/V Flexible Software Package.

7. Reference Documents

- R01AN6240 RZ/V2L, RZ/V2H, RZ/V2N Getting Started with Flexible Software Package
- R12UZ0157 RZ/V2N Evaluation Board Kit (Secure type) Hardware Manual

Revision History

Rev.	Date	Description	
		Page	Summary
3.00	Mar.11.2025	-	Migrated to RZ/V2N as per Release Note of RZ/V Multi-OS Package v2.1.0.
3.10	May.22.2025	-	Updated in align with RZ/V Multi-OS Package v3.1.0.
3.11	Jun.13.2025	-	Update Multi-OS Package version to 3.1.1.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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