

Introduction

This application note provides guidelines for thermal design of the RZ/V2N Group.

Target Device

RZ/V2N Group

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1. Purpose

This guide specifies how to calculate the junction temperature (T_j) for the RZ/V2N Group products.

Evaluate the product with a customer set to ensure that the specifications in this guide are satisfied.

2. Specification of Junction Temperature (Tj)

The specification of Tj (junction temperature) is defined as follows.

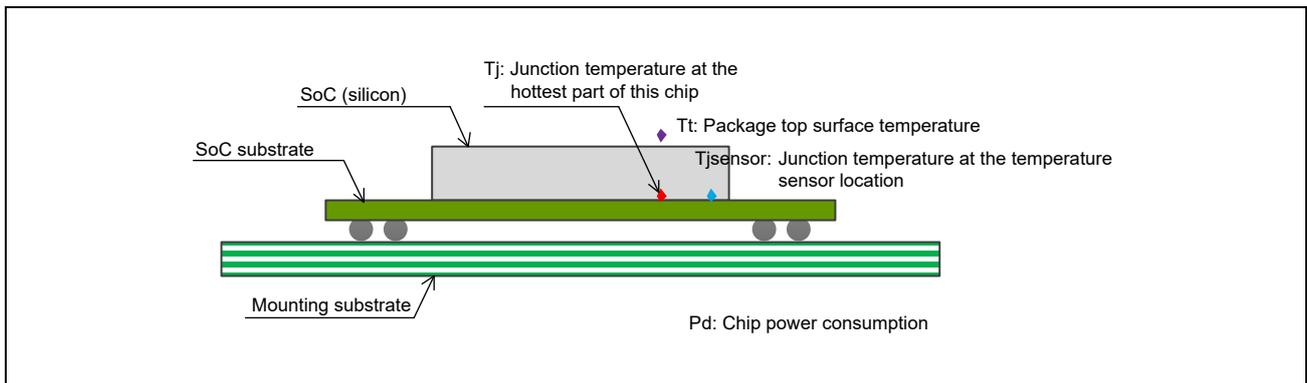
■ Operating Range

Item	Symbol	Min.	Max.	Unit
Maximum junction temperature	Tjmax	-40	125	°C

Note: The calculation method of Tjmax is shown in **4, How to Calculate Tj**. Please check Tjmax according to this calculation method. In addition, for the device lifetime, refer to the *RZ/V2N Group Lifetime Guideline*.

3. Definitions of Respective Characteristics

- The junction temperature at the hottest part inside this chip is T_j (°C).
- The junction temperature of the temperature sensors (TSU0, TSU1) are T_{jsensor0} (°C) and T_{jsensor1} (°C).
- The thermal parameters of the temperature sensors, which are calculated by the thermal distributions are Ψ_{js0} (°C/W) and Ψ_{js1} (°C/W).
- The package top surface temperature over the hottest part is T_t (°C).
- The thermal parameter of the chip surface, which is calculated by the thermal distributions is Ψ_t (°C/W).
- The chip power consumption is P_d (W).



- The formulae for calculating the thermal parameters “ Ψ_{js0} ” and “ Ψ_{js1} ” and “ Ψ_{jt} ” are given below.

$$\Psi_{\text{js0}}(\text{TSU0}) = \frac{T_j - T_{\text{jsensor0}}}{P_d}$$

$$\Psi_{\text{js1}}(\text{TSU1}) = \frac{T_j - T_{\text{jsensor1}}}{P_d}$$

$$\Psi_{\text{jt}} = \frac{T_j - T_t}{P_d}$$

4. How to Calculate T_j

4.1 How to Calculate T_j from Temperature Sensor Measurements

Since the temperatures measured by each of the temperature sensors will have some errors, use the following equations to calculate T_j with the errors in measurement by the temperature sensors taken into account.

$$T_{j0} (\text{°C}) = T_{\text{jsensor}0} (\text{°C}) + \text{Temperature sensor error} (\text{°C})^{*1} + \Psi_{\text{js}0} (\text{°C/W})^{*2} \times P_d (\text{W})$$

$$T_{j1} (\text{°C}) = T_{\text{jsensor}1} (\text{°C}) + \text{Temperature sensor error} (\text{°C})^{*1} + \Psi_{\text{js}1} (\text{°C/W})^{*3} \times P_d (\text{W})$$

The equations are used under the condition that the junction temperature of T_{j0} or T_{j1}, whichever is higher, is 125°C^{*4} or less.

Note 1. Temperature sensor error: 5°C

Note 2. Refer to the following table for the respective thermal parameters.

Note 3. Refer to the following table for the respective thermal parameters.

Note 4. Used under conditions that ensure that T_{j0} or T_{j1} does not exceed 125°C even for a moment.

Substrate and Housing	Power Consumption	Heat Sink	Air Velocity	Ψ _{js0}	Ψ _{js1}
4-layer board, Inside the housing ^{*1}	10.42 W ^{*3}	Yes	0 m/s	0.52 (°C/W)	0.10 (°C/W)
		Yes	1 m/s	0.47 (°C/W)	0.09 (°C/W)
		Yes	3 m/s	0.45 (°C/W)	0.08 (°C/W)
8-layer board, Inside the housing ^{*2}	7.30 W ^{*3}	Yes	0 m/s	0.45 (°C/W)	0.11 (°C/W)
		Yes	1 m/s	0.41 (°C/W)	0.10 (°C/W)
		Yes	3 m/s	0.39 (°C/W)	0.09 (°C/W)
	4.4 W ^{*3}	No	0 m/s	0.52 (°C/W)	0.10 (°C/W)
		No	1 m/s	0.48 (°C/W)	0.08 (°C/W)
		No	3 m/s	0.46 (°C/W)	0.07 (°C/W)

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 10.42 W use case, the AI accelerator and the CPU operate at a higher rate.

4.2 How to Calculate Tj from the Chip Surface Temperature

Measure the chip surface temperature T_t (°C), which is the highest temperature, and calculate T_j (°C) from the following formula.

$$T_j (\text{°C}) = T_t (\text{°C}) + \Psi_{jt} (\text{°C/W})^{*1} \times P_d (\text{W})$$

The equation is used under the condition that the junction temperature of Tj is 125°C*2 or less.

Note 1. Refer to the following table for the thermal parameter.

Note 2. Used under conditions that ensure that Tj does not exceed 125°C even for a moment.

Substrate and Housing	Power Consumption	Heat Sink	Air Velocity	Ψ_{jt}
4-layer board, Inside the housing*1	10.42 W*3	Yes	0 m/s	0.13 (°C/W)
		Yes	1 m/s	0.13 (°C/W)
		Yes	3 m/s	0.13 (°C/W)
8-layer board, Inside the housing*2	7.30 W*3	Yes	0 m/s	0.08 (°C/W)
		Yes	1 m/s	0.09 (°C/W)
		Yes	3 m/s	0.09 (°C/W)
	4.4 W*3	No	0 m/s	0.01 (°C/W)
		No	1 m/s	0.03 (°C/W)
		No	3 m/s	0.04 (°C/W)

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 10.42 W use case, the AI accelerator and the CPU operate at a higher rate.

5. Reference Parameters

■ Parameters (Θ_{ja} , Θ_{jc} , Θ_{jb} , Ψ_{jb})

- Θ_{ja} : Junction to ambient thermal resistance
- Θ_{jc} : Junction to case thermal resistance
- Θ_{jb} : Junction to board thermal resistance
- Ψ_{jb} : Junction to board thermal parameter

Substrate and Housing	Power Consumption	Θ_{ja}	Θ_{jc}	Θ_{jb}	Ψ_{jb}	Heat Sink
4-layer board, Inside the housing*1	10.42 (W)*3	8.1 (°C/W)	0.16 (°C/W)	4.29 (°C/W)	2.4 (°C/W)	Yes
8-layer board, Inside the housing*2	7.30 (W)*3	9.6 (°C/W)	0.15 (°C/W)	4.22 (°C/W)	2.3 (°C/W)	Yes
	4.40 (W)*3	15.8 (°C/W)	0.15 (°C/W)	4.13 (°C/W)	4.5 (°C/W)	No

Note: Air velocity: 0 m/s

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 10.42 W use case, the AI accelerator and the CPU operate at a higher rate.

■ Simulation model for thermal analysis

The model described in **Figure 5.1** is used to calculate Θ_{ja} value.

Θ_{jc} and Θ_{jb} are calculated under different conditions in **Figure 5.2**.

Θ_{jc} : Environment mimicking *Mil Std 883 Method 1012.1* of JESD51-12

Θ_{jb} : Based on JESD51-8

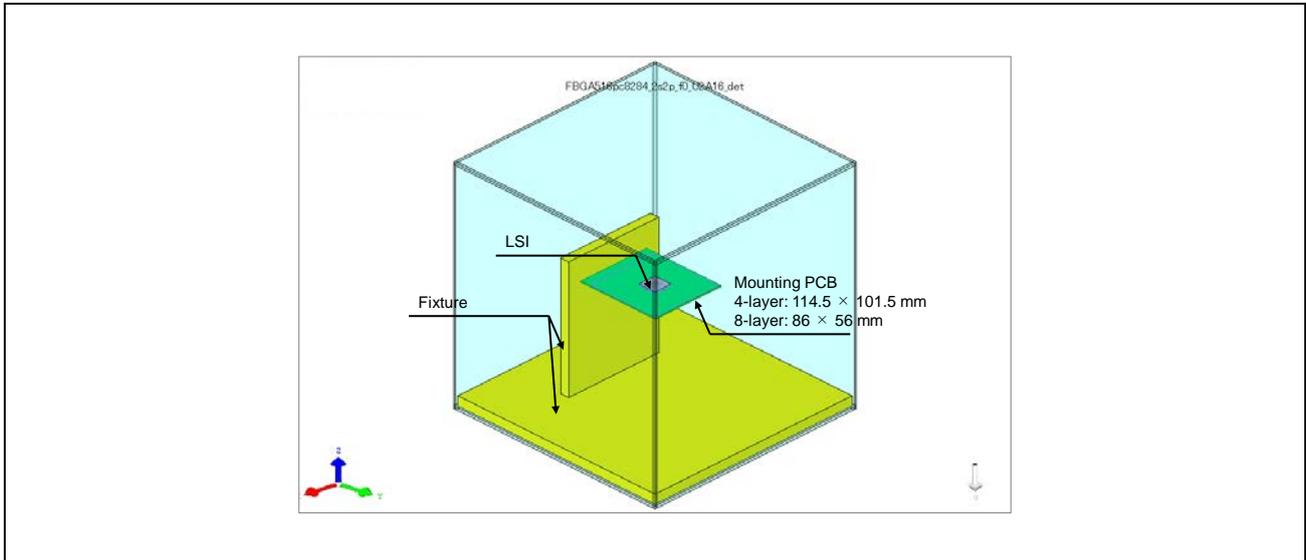


Figure 5.1 External Environment Based on JESD51-2A

Symbols	θ_{jc}	θ_{jb}
Environment	<p>Cold plate (fixed temp. @ T_c)</p> <p>Nearly all of the power dissipation flows through the top of the package.</p>	<p>Cold ring (fixed temp. @ T_a)</p> <p>Nearly all of the power dissipation flows through the bottom of the package.</p>
Definition	$\theta_{jc} = \frac{T_j - T_c}{P}$	$\theta_{jb} = \frac{T_j - T_b}{P}$

Figure 5.2 Environment for Calculating Θ_{jc} and Θ_{jb}

	SR	0.032	[mm]
L1	Cu 50%	0.05	[mm]
	FR4	0.375	[mm]
L2	Cu 95%	0.035	[mm]
	FR4	0.64	[mm]
L3	Cu 95%	0.035	[mm]
	FR4	0.375	[mm]
L4	Cu 50%	0.05	[mm]
	SR	0.032	[mm]
	Total	1.6	[mm] (excluding SR-layer)

Figure 5.3 Mounting PCB Layer Information Based on JEDEC-2S2P (4-Layer)

	SR	0.032	[mm]
L1	Cu 30%	0.035	[mm]
	FR4	0.125	[mm]
L2	Cu 80%	0.020	[mm]
	FR4	0.125	[mm]
L3	Cu 30%	0.020	[mm]
	FR4	0.135	[mm]
L4	Cu 80%	0.020	[mm]
	FR4	0.640	[mm]
L5	Cu 80%	0.020	[mm]
	FR4	0.135	[mm]
L6	Cu 30%	0.020	[mm]
	FR4	0.125	[mm]
L7	Cu 80%	0.020	[mm]
	FR4	0.125	[mm]
L8	Cu 30%	0.035	[mm]
	SR	0.032	[mm]
	Total	1.6	[mm] (excluding SR-layer)

Figure 5.4 Mounting PCB Layer Information Based on Use Case (8-Layer)

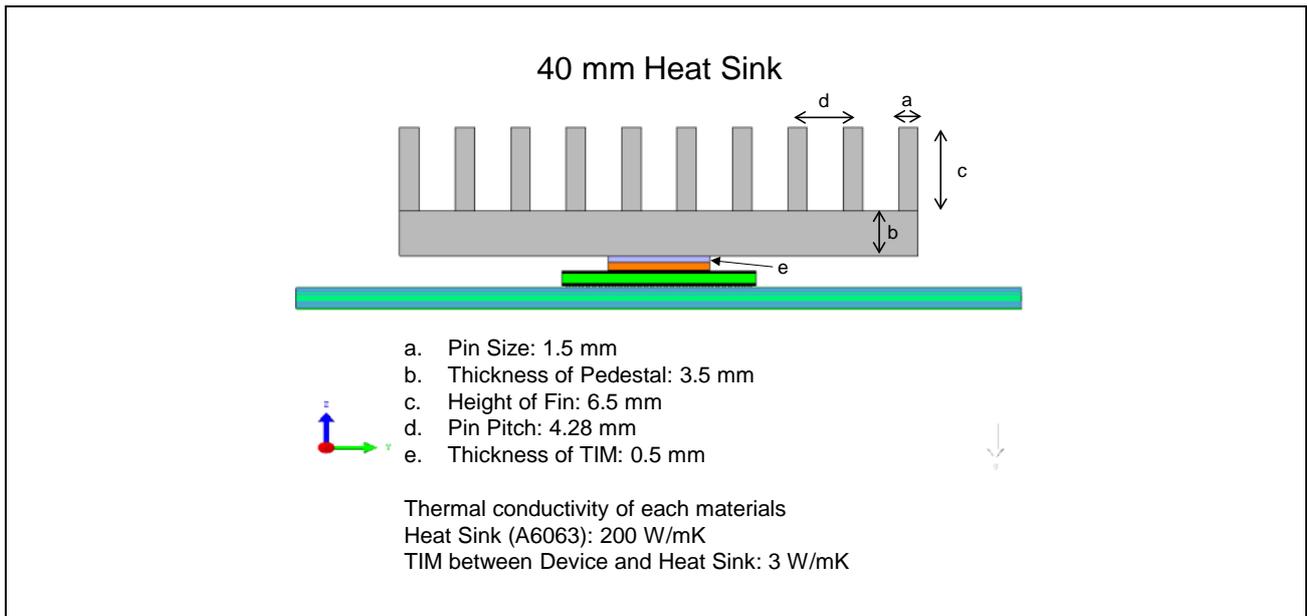


Figure 5.5 Heat Sink Information

REVISION HISTORY	RZ/V2N Group Thermal Design Guide Application Note
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 28, 2025	—	First edition issued
1.10	Oct 7, 2025	4. How to Calculate Tj	
		5	4.1 How to Calculate Tj from Temperature Sensor Measurements: Note 3 was added to the relevant table.
		6	4.2 How to Calculate Tj from the Chip Surface Temperature: Note 3 was added to the relevant table.
		5. Reference Parameters	
		7	5. Reference Parameters: Parameters (θ_{ja} , θ_{jc} , θ_{jb} , ψ_{jb}): 4-layer board, Inside the housing: θ_{ja} and ψ_{jb} : modified The Heat sink column was added to the relevant table. Note and Note 3 were added to the relevant table.
		8	5. Reference Parameters: Simulation model for thermal analysis: The main text, modified
		8	Figure 5.2 Environment for Calculating θ_{jc} and θ_{jb} , added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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