RZ/V2H Group Thermal Design Guide

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Introduction

This application note provides guidelines for thermal design of the RZ/V2H Group.

Target Device

RZ/V2H Group

Table of Contents

1. Purpose

This guide specifies how to calculate the junction temperature (Tj) for the RZ/V2H Group products.

Evaluate the product with a customer set to ensure that the specifications in this guide are satisfied.

2. Specification of Junction Temperature (Tj)

The specification of Tj (junction temperature) is defined as follows.

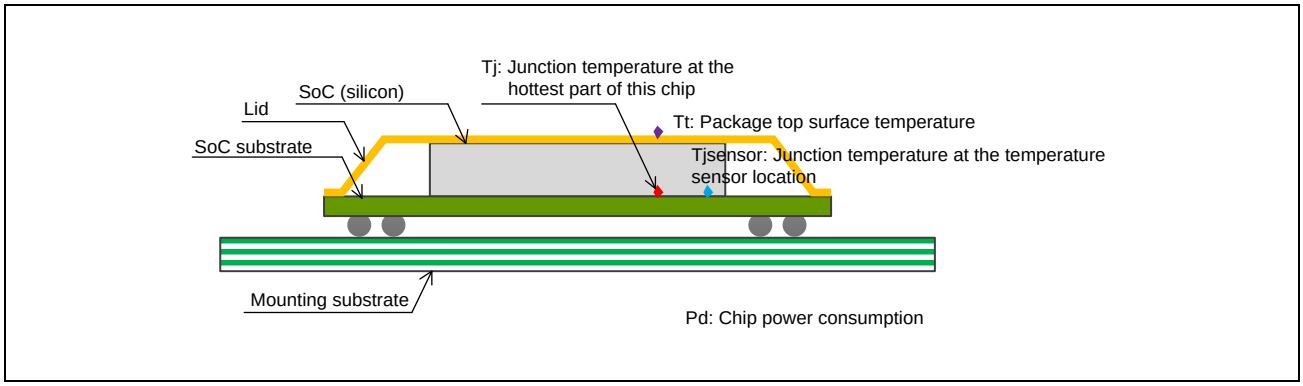
■ Operating Range

Item	Symbol	Min.	Max.	Unit
Maximum junction temperature	Tjmax	−40	125	°C

Note: The calculation method of Tjmax is shown in **4, How to Calculate Tj**. Please check Tjmax according to this calculation method. In addition, for the device lifetime, refer to the *RZ/V2H Group Lifetime Guideline*.

3. Definitions of Respective Characteristics

- The junction temperature at the hottest part inside this chip is Tj (°C).
- The junction temperature of the temperature sensors (TSU0, TSU1) are Tjsensor0 (°C) and Tjsensor1 (°C).
- The thermal parameters of the temperature sensors, which are calculated by the thermal distributions are Ψjs0 (°C/W) and Ψjs1 (°C/W).
- The package top surface temperature over the hottest part is Tt (°C).
- The thermal parameter of the chip surface, which is calculated by the thermal distributions is Ψt (°C/W).
- The chip power consumption is Pd (W).



- The formulae for calculating the thermal parameters “Ψjs0” and “Ψjs1” and “Ψjt” are given below.

$$\Psi js0(TSU0) = \frac{Tj - Tjsensor0}{Pd}$$

$$\Psi js1(TSU1) = \frac{Tj - Tjsensor1}{Pd}$$

$$\Psi jt = \frac{Tj - Tt}{Pd}$$

4. How to Calculate Tj

4.1 How to Calculate Tj from Temperature Sensor Measurements

Since the temperatures measured by each of the temperature sensors will have some errors, use the following equations to calculate Tj with the errors in measurement by the temperature sensors taken into account.

Tj0 (°C) = Tjsensor0 (°C) + Temperature sensor error (°C)*1 + Ψjs0 (°C/W)*2 × Pd (W)

Tj1 (°C) = Tjsensor1 (°C) + Temperature sensor error (°C)*1 + Ψjs1 (°C/W)*3 × Pd (W)

The equations are used under the condition that the junction temperature of Tj0 or Tj1, whichever is higher, is 125°C*4 or less.

Note 1. Temperature sensor error: 5°C

Note 2. Refer to the following table for the respective thermal parameters.

Note 3. Refer to the following table for the respective thermal parameters.

Note 4. Used under conditions that ensure that Tj0 or Tj1 does not exceed 125°C even for a moment.

Substrate and Housing	Power Consumption	Heat Sink	Air Velocity	Ψjs0	Ψjs1
4-layer board, Inside the housing*1	17.40 (W)	Yes	0 (m/s)	0.44 (°C/W)	0.22 (°C/W)
		Yes	1 (m/s)	0.41 (°C/W)	0.21 (°C/W)
		Yes	3 (m/s)	0.40 (°C/W)	0.20 (°C/W)
8-layer board, Inside the housing*2	17.40 (W)*3	Yes	0 (m/s)	0.44 (°C/W)	0.22 (°C/W)
		Yes	1 (m/s)	0.41 (°C/W)	0.21 (°C/W)
		Yes	3 (m/s)	0.40 (°C/W)	0.20 (°C/W)
	10.47 (W)*3	No	0 (m/s)	0.47 (°C/W)	0.17 (°C/W)
		No	1 (m/s)	0.41 (°C/W)	0.13 (°C/W)
		No	3 (m/s)	0.39 (°C/W)	0.12 (°C/W)

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 17.40 W use case, the AI accelerator operates at a higher rate.

4.2 How to Calculate Tj from the Chip Surface Temperature

Measure the chip surface temperature Tt (°C), which is the highest temperature, and calculate Tj (°C) from the following formula.

$$Tj\ (°C) = Tt\ (°C) + \Psi jt\ (°C/W)^{*1} \times Pd\ (W)$$

The equation is used under the condition that the junction temperature of Tj is 125°C*2 or less.

Note 1. Refer to the following table for the thermal parameter.

Note 2. Used under conditions that ensure that Tj does not exceed 125°C even for a moment.

Substrate and Housing	Power Consumption	Heat Sink	Air Velocity	Ψjt
4-layer board, Inside the housing*1	17.40 (W)	Yes	0 (m/s)	0.74 (°C/W)
		Yes	1 (m/s)	0.78 (°C/W)
		Yes	3 (m/s)	0.80 (°C/W)
8-layer board, Inside the housing*2	17.40 (W)*3	Yes	0 (m/s)	0.80 (°C/W)
		Yes	1 (m/s)	0.82 (°C/W)
		Yes	3 (m/s)	0.83 (°C/W)
	10.47 (W)*3	No	0 (m/s)	0.31 (°C/W)
		No	1 (m/s)	0.32 (°C/W)
		No	3 (m/s)	0.34 (°C/W)

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 17.40 W use case, the AI accelerator operates at a higher rate.

5. Reference Parameters

■ Parameters (Θja, Θjc, Θjb, Ψjb)

- Θja: Junction to ambient thermal resistance
- Θjc: Junction to case thermal resistance
- Θjb: Junction to board thermal resistance
- Ψjb: Junction to board thermal parameter

Substrate and Housing	Power Consumption	Θja	Θjc	Θjb	Ψjb
4-layer board, Inside the housing*1	17.40 (W)	3.5 (°C/W)	1.05 (°C/W)	3.18 (°C/W)	1.5 (°C/W)
8-layer board, Inside the housing*2	17.40 (W)*3	3.8 (°C/W)	1.05 (°C/W)	3.18 (°C/W)	1.4 (°C/W)
	10.47 (W)*3	3.6 (°C/W)	0.94 (°C/W)	3.02 (°C/W)	1.2 (°C/W)

Note: Heat sink: Yes
Air velocity: 1 m/s

Note 1. Board size: 114.5 mm × 101.5 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 3. These power consumption values are calculated based on different use cases. Since the power density differs for each use case, the thermal resistance values differ as well. In the 17.40 W use case, the AI accelerator operates at a higher rate.

■ Reference power consumption

Calculating backwards from Θja, the power consumption (Pd) at Tj = 120°C under each condition is shown below.

- Ta = 55°C

Substrate and Housing	Heat Sink	Air Velocity	Power Consumption
8-layer board, Inside the housing*1	Yes	0 (m/s)	10.32 (W)
	Yes	3 (m/s)	20.51 (W)*2
	No	0 (m/s)	5.12 (W)

Note 1. Board size: 85 mm × 56 mm
Housing size: 304.8 mm × 304.8 mm × 304.8 mm
Housing condition: Open the top and two sides for air flow.

Note 2. LSI worst case. (All units operating.)

■ Simulation model for thermal analysis

The model described in **Figure 5.1** is used to calculate Θja value.

Θjc and Θjb are calculated under different conditions in **Figure 5.2**.

Θjc: Environment mimicking *Mil Std 883 Method 1012.1* of JESD51-12

Θjb: Based on JESD51-8

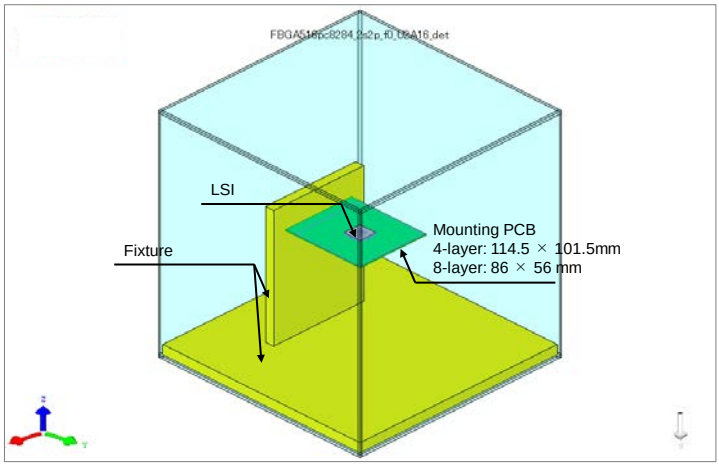


Figure 5.1 External Environment Based on JESD51-2A

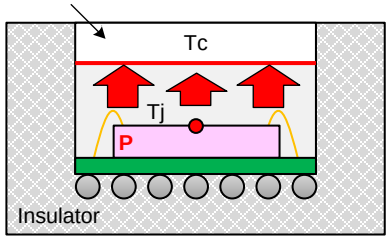
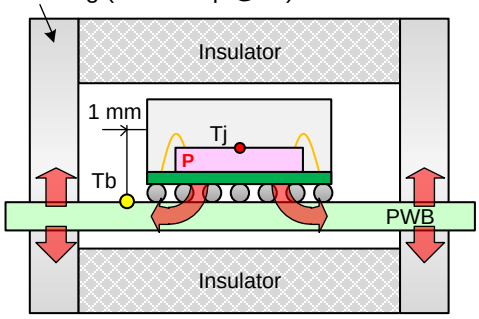
Symbols	θjc	θjb
Environment	Cold plate (fixed temp.@Ta)  Nearly all of the power dissipation flows through the top of the package.	Cold ring (fixed temp.@Ta)  Nearly all of the power dissipation flows through the bottom of the package.
Definition	$\theta_{jc} = \frac{T_j - T_c}{P}$	$\theta_{jb} = \frac{T_j - T_b}{P}$

Figure 5.2 Environment for Calculating Θjc and Θjb

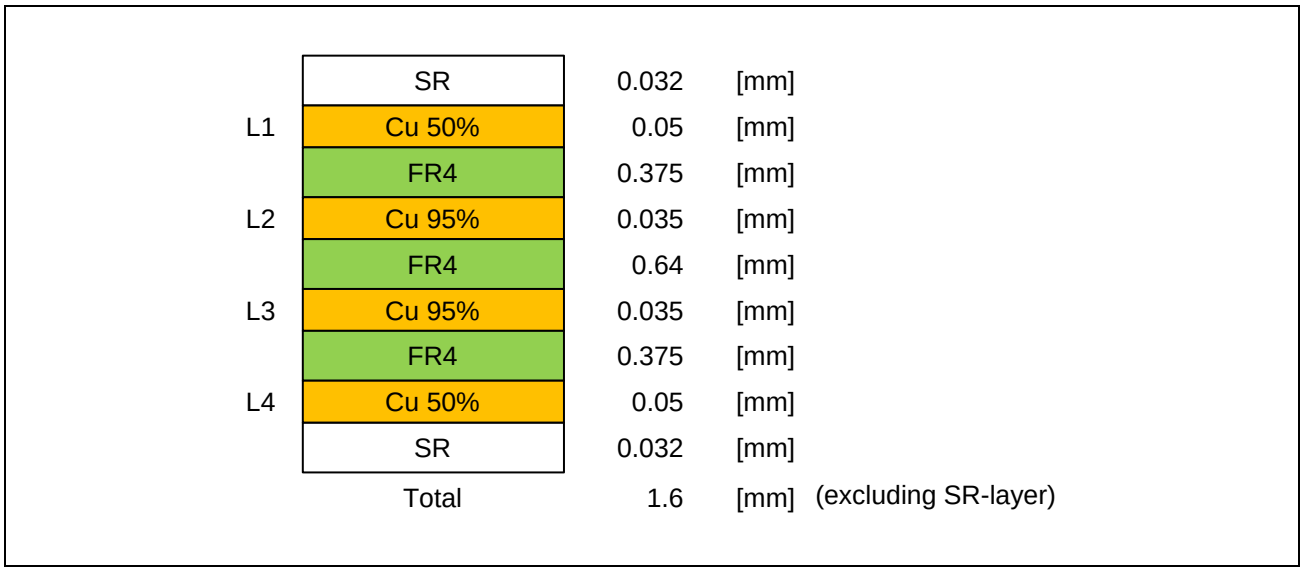


Figure 5.3 Mounting PCB Layer Information Based on JEDEC-2S2P (4-Layer)

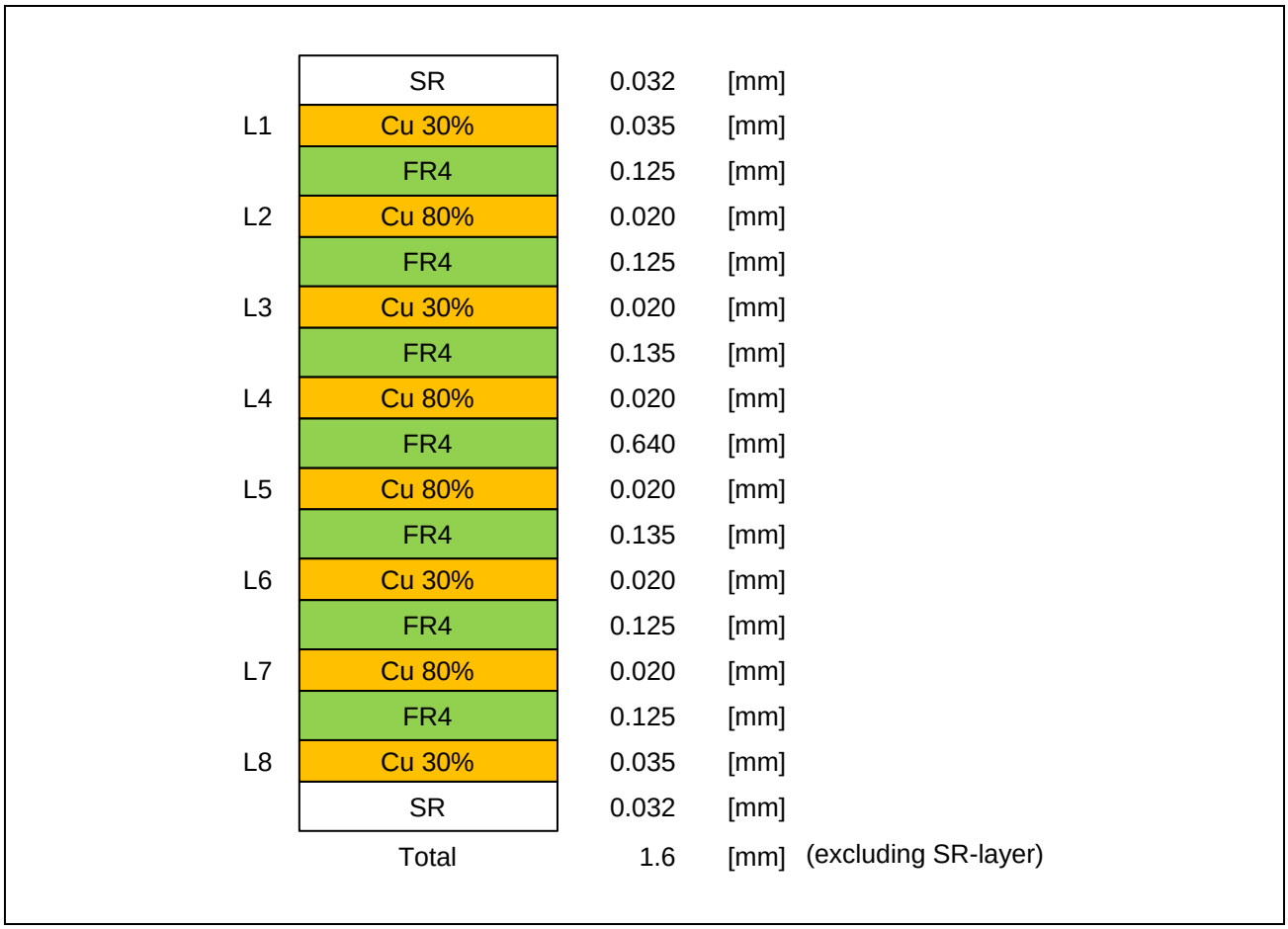
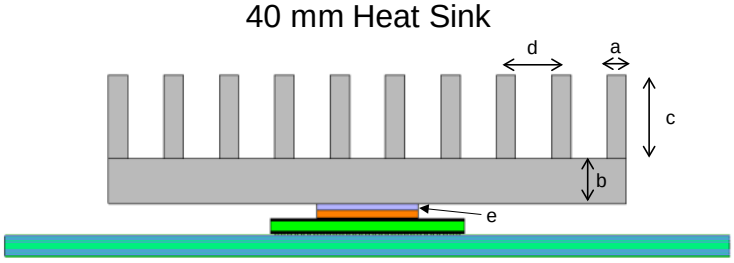


Figure 5.4 Mounting PCB Layer Information Based on Use Case (8-Layer)



a. Pin Size: 1.5 mm
b. Thickness of Pedestal: 3.5 mm
c. Height of Fin: 16.5 mm
d. Pin Pitch: 4.28 mm
e. Thickness of TIM: 0.5 mm

Thermal conductivity of each materials
Heat Sink (A6063): 200 W/mK
TIM between Device and Heat Sink: 3 W/mK

Figure 5.5 Heat Sink Information

REVISION HISTORY	RZ/V2H Group Thermal Design Guide Application Note

Rev.	Date	Description	
		Page	Summary
1.00	Dec 22, 2023	—	First edition issued
1.10	Jun 11, 2024	5	Temperature sensor error, modified
		5, 6, 7, 9	The value of 8-layer board, added
		7	Reference power consumption, added
		9	Heat sink information, added
1.20	Oct 7, 2025	4. How to Calculate Tj	
		5	4.1 How to Calculate Tj from Temperature Sensor Measurements: Note 3 was added to the relevant table.
		6	4.2 How to Calculate Tj from the Chip Surface Temperature: Note 3 was added to the relevant table.
		5. Reference Parameters	
		7	5. Reference Parameters: Parameters (Θja, Θjc, Θjb, Ψjb): Note 3 was added to the relevant table.
		8	5. Reference Parameters: Simulation model for thermal analysis: The main text, modified
		8	Figure 5.2 Environment for Calculating Θjc and Θjb, added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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