RZ/T2ME Group

IEEE 1588-2019 Sample application

Introduction

This document describes a sample application that realizes IEEE1588-2019 (PTPv2) on Renesas Starter Kit+ for RZ/T2ME (RZ/T2ME RSK)(*).

This package use the Linux PTP library created by OSS for realize PTPv2 and using Ethernet Switch(ETHSW) module provided on RZ/T2ME RSK.

This sample application realizes PTPv2 on RZ/T2ME RSK.

Note: (*): referred to as RZ/T2ME RSK

Target Device

RZ/T2ME Group

Contents

1. Overview

PTP (Precision Time Protocol) refers to a communications protocol used to synchronize clocks on the same network.

PTP for this application includes the following elements:

- IEEE1588-2019(PTPv2)
  - Achieving time synchronization

1.1 IEEE1588 2019(PTPv2)

Time synchronization using IEEE 1588-2019 (PTPv2) is achieved as follows.

- Each device runs a best master clock selection algorithm (BMCA)
- The device with the best clock is the " timeTransmitter", and the other devices are the " timeReceiver"
- The timeTransmitter device is the source of time and clock information
- A timeReceiver device synchronizes with the timeTransmitter by adjusting its own time information based on the time information received from the timeTransmitter and the network transmission delay between the timeTransmitter and the timeReceiver device.

PTPv2 has the following features:

- High-precision time synchronization
  - High-precision time synchronization down to the microsecond level is possible
- Propagation Delay Measurement
  - Since the transmission time required to send and receive time information is calculated, accurate time synchronization is possible even when the information transmission speed differs depending on the communication path.
- Automatic Selection
  - Among the PTPv2-compatible devices in the network, the device with the highest priority in clock characteristics can be automatically set as the timeTransmitter.

2. Package description

The structure of this package is as follows:

```
- RZT2ME_RSK_IEEE1588.zip                    - Project file includes sample
application
- r11an0921ejxxxx-rzt2me-ieee1588.pdf (*)    - Application note (English
version)
- r11an0921jjxxxx-rzt2me-ieee1588.pdf (*)    - Application note (Japanese
version)
```

Note: (*): YYYYMMDD: Release dates

2.1 PTPv2 sample application

This sample application is a simple application that uses PTPv2 and implemented in an RZ/T2ME RSK-to-RZ/T2ME RSK environment.

2.1.1 Information of development environment

Development environment is as follows:

- IDE
  - EWARM(IAR Embedded Workbench® for ARM)(*)
  - e² studio

Note: (*): referred to as EWARM

table 2-1 Version of IDE

Item	Version
IAR Embedded Workbench for ARM	9.60.1
Renesas e² studio	2024-04
FSP Smart Configurator	2024-04

- FSP
  - FSP2.1.0
- evaluation board
  - Renesas Starter Kit+ for RZ/T2ME (RZ/T2ME RSK)

2.1.2 Sample application Overview

PTPv2 is started by connecting the ETH ports of each RZ/T2ME RSK.

When PTPv2 is started, each RZ/T2ME RSK sends an ANNOUNCE message containing its own clock information.

When an ANNOUNCE message is received, if the Domain Numbers contained in the message are the same, the BMCA will determine timeTransmitter / timeReceiver.

When the BMCA makes the determination, it evaluates the clock information (*) in the following order.

The smaller the value, the higher the priority, and if the values are the same, it will move on to the next evaluation

Note: (*): For information on how to set clock information, see “4.1.2.3 Clock information used by BMCA”

1. Priority1
2. Clock Class
3. Clock Accuracy
4. Clock Variance
5. Priority2
6. If it cannot be evaluated 1-5, it will be evaluated using the MAC Address.

The device with the highest priority clock is the " timeTransmitter", and all other devices are " timeReceiver".

This application has two types of network transmission delay times: E2E (End to End Mechanism) and P2P (Peer to Peer Mechanism).

- In E2E, the timeReceiver sends a DELAY REQUEST message to the timeTransmitter.
  The timeTransmitter sends a DELAY RESPONSE message, which includes the time it received the DELAY REQUEST message, as a response.
  The timeReceiver calculates the transmission delay time from the time it sent its own DELAY REQUEST message and the time it received the timeTransmitter's DELAY REQUEST message.

- In P2P, both the timeTransmitter and timeReceiver send PDELAY REQUEST messages.
  When a PDELAY REQ message is received, a PDELAY RESPONSE message is sent as a response, including the reception time of the PDELAY REQUEST message.
  Immediately afterwards, a PDELAY RESPONSE FOLLOW UP message is sent, including the transmission time of the PDELAY RESPONSE message.
  Both the timeTransmitter and timeReceiver calculate the transmission delay time from the transmission and reception time of the PDELAY REQUEST and PDELAY RESPONSE messages.

For information on how to set the network transmission delay time, see “4.1.2.4 Delay mechanism”

This application has two types of time distribution methods: one step clock and two step clock.

- In one step clock, the timeTransmitter sends a SYNC message that includes its own time information and the time the message was sent.
  The timeReceiver performs time synchronization using the time information included in the SYNC message and the sending time of the timeTransmitter.
- In a two step clock, the timeTransmitter sends a SYNC message that includes its own time information. Immediately afterwards, it sends a FOLLOW UP message that includes the sending time of the SYNC message.
  The timeReceiver performs time synchronization using the time information included in the SYNC message and the sending time of the SYNC included in the FOLLOW UP message.

For information on how to set the time distribution method, see “4.1.2.5 Time distribution method”.

This application can specify Ethernet frames or UDP frames as frames for PTP.

For information on how to set the network frames, see ”4.1.2.6 Network transport”.

In addition, the following operations are implemented in this sample application as functionality for operation check.

- Displays the operating status by logging via UART.
- Uses a GPIO pin to output a clock waveform for checking PTPv2 operation.

2.1.2.1 Operation Specifications of PTPv2

The operating specifications of PTPv2 are as follows:

table 2-2 PTPv2 Specification

SYNC transmission interval	**DELAY transmission interval**	**PDELAY transmission interval**
1sec	Within 1sec (*)	1sec

Note: (*): The DELAY transmission interval is a random value within 1 second.

2.1.3 Sample application's outputs for checking operation

You can check PTPv2 operations in the following ways.

2.1.3.1 Outputs of log message

This Application outputs log messages through UART from RZ/T2ME RSK's Serial Port (CN16).

The log message shows state of application's operation.

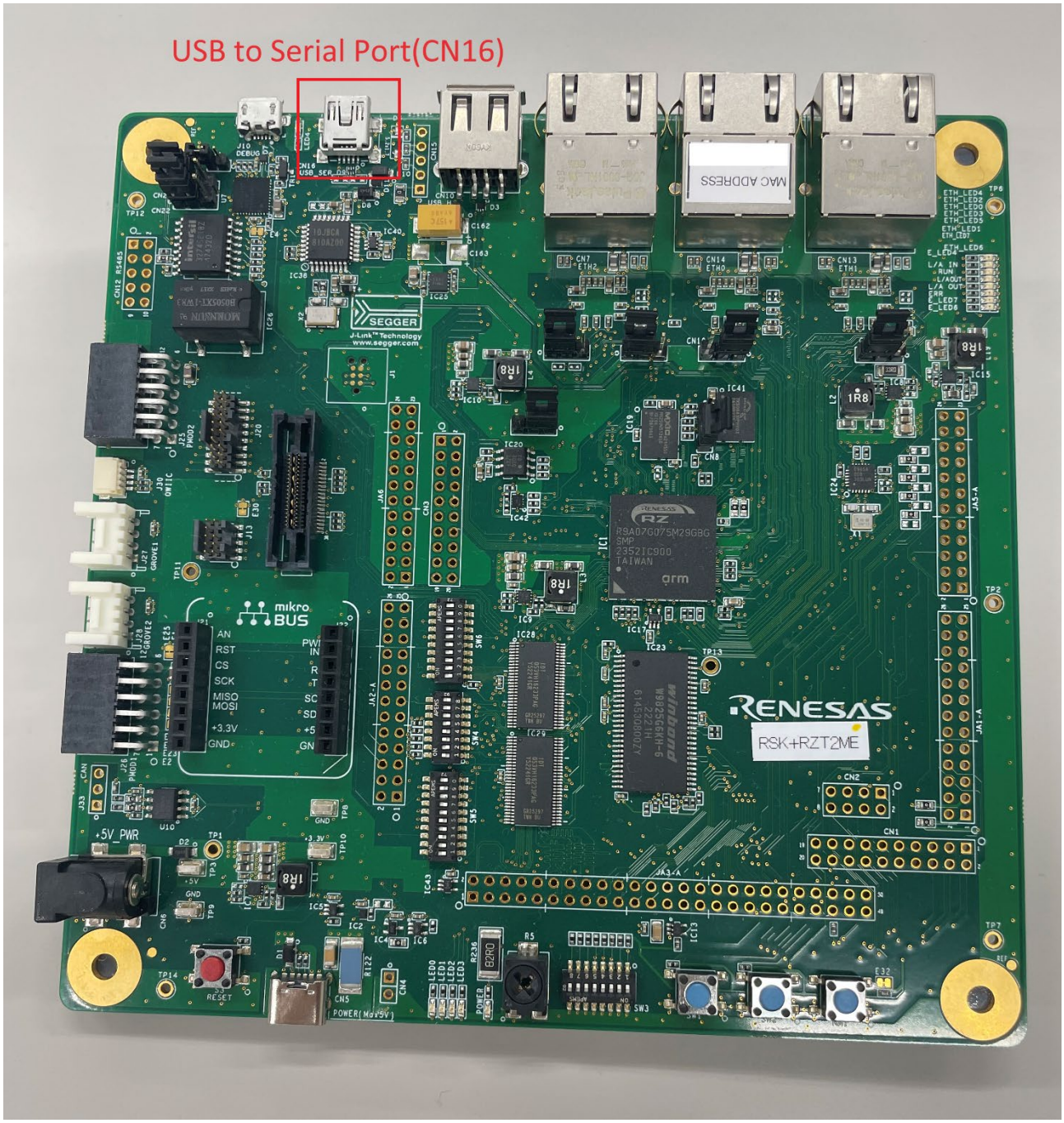

Figure2-1 RZ/T2ME RSK board layout(USB to Serial Port USB Connector)

The log message shows the following content:

- state of PTPv2

2.1.3.1.1 Log messages of PTPv2

Log messages of PTPv2 are following:

- PTPv2 log message on the " timeTransmitter" side
- >>Info : PTP notice NETDEV_UP: portIndex=0
- >>Info : PTP notice AS_CAPABLE_UP: domainNumber=0 portIndex=0
- >>Info : PTP notice GM_CHANGE: gmIdentity=74 90 50 ff fe 50 4c 3e

- PTPv2 log message on the " timeReceiver" side
- >>Info : PTP notice NETDEV_UP: portIndex=0
- >>Info : PTP notice AS_CAPABLE_UP: domainNumber=0 portIndex=0
- >>Info : PTP notice GM_CHANGE: gmIdentity=74 90 50 ff fe 50 4c 3e
- >>Info : PTP notice DEV_SYNCD:

Each log messages shows the following states.

- "`PTP notice NETDEV_UP: portIndex=0`"
  — Port 0 is link-Upped.
- "`PTP notice AS_CAPABLE_UP: domainNumber=0 portIndex=0`"
  — Port 0 is Capable.
- "`PTP notice GM_CHANGE: gmIdentity=74 90 50 ff fe 50 4c 3e`"
  — " timeTransmitter" is changed
- "`PTP notice DEV_SYNCD:`"
  — Stable synchronization with GM(GrandMaster) time".

2.1.3.2 Outputs of GPIO Pin

This Application outputs clock pulse wave (for checking time synchronization) and information of PTPv2 states from RZ/T2ME RSK GPIO Pins.

2.1.3.2.1 GPIO Pin's outputs of PTPv2

For checking time synchronization by PTPv2, clock pulse wave generated by pulse generator is outed by GPIO Pin "CN2-8".

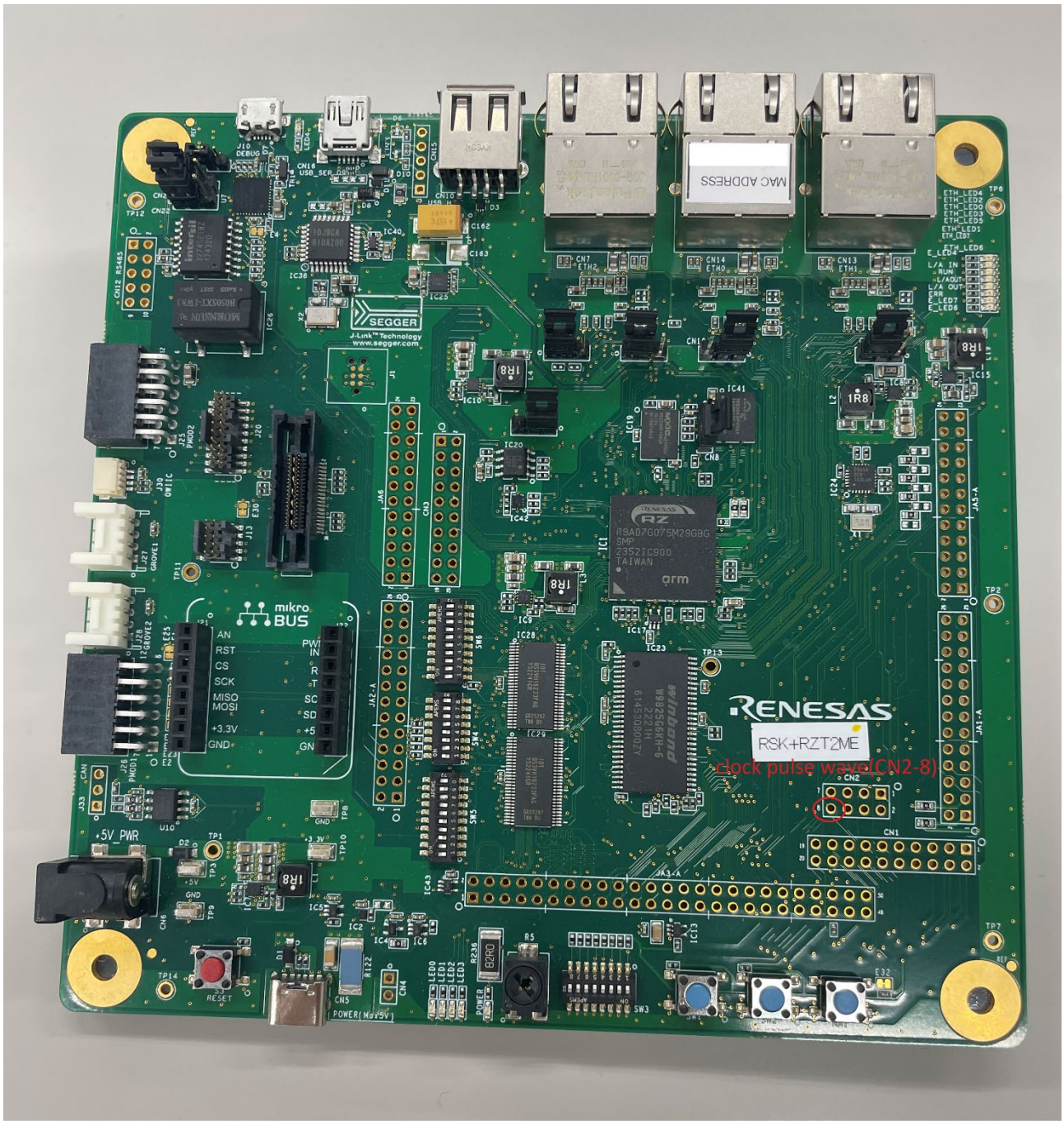

Figure 2-2 RZ/T2ME RSK board layout(GPIO)

Note: The period of the clock pulse wave is selectable from "1[ms]".

The clock pulse wave during PTPv2 synchronization is shown below.

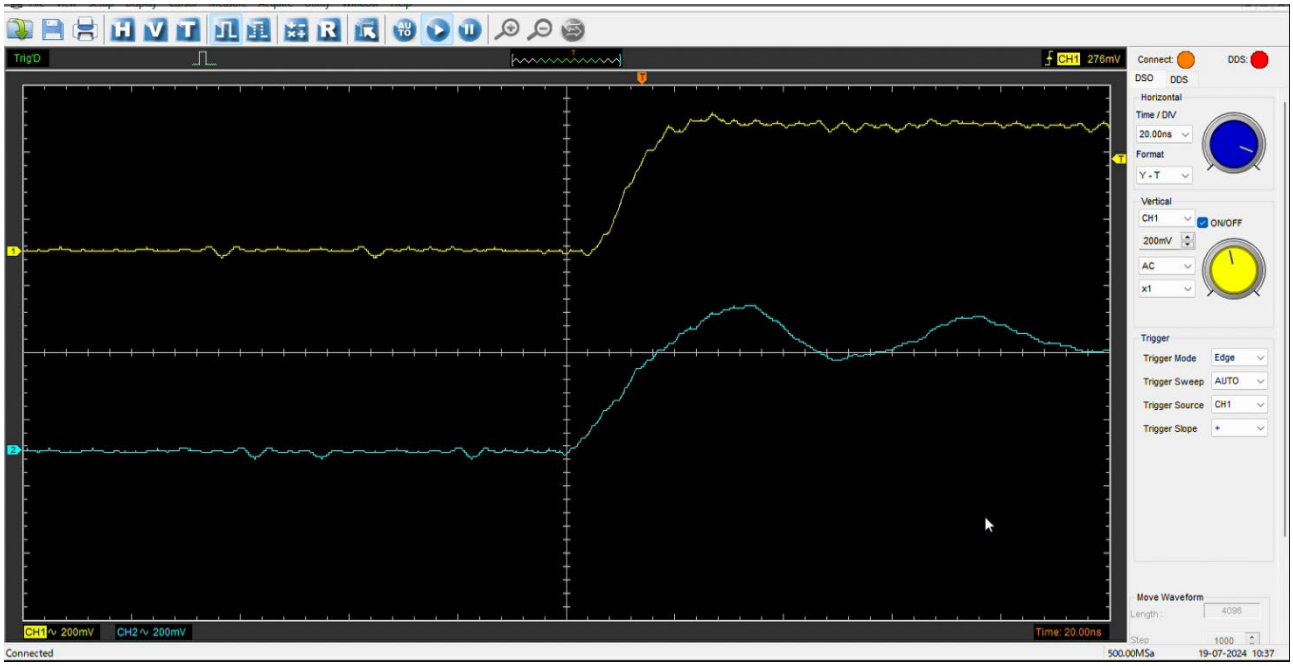

Figure 2-3 PTPv2 Clock Synchronization

Table 2-3 Description of each channel

channel	color	Pin	description
CH1	Yellow	GPIO (timeTransmitter)	timeTransmitter clock pulse wave
CH2	Blue	GPIO (timeReceiver)	It operates in sync with the timeTransmitter clock pulse wave

Each Pin in the above figure shows the following:

- `CH1 (timeTransmitter GPIO)` and `CH2 (timeReceiver GPIO)` shows the state of time synchronization.

For information on the types of packets sent and received and the timing of sending, see “2.1.2 Sample application Overview”

3. Preparation

This chapter shows tools are required to build and execute the sample application.

3.1 Hardware requirements

The following items are required for run sample application:

- Renesas Starter Kit+ for RZ/T2ME (RZ/T2ME RSK) (*1) … Evaluation Board
- I-jet debugger (*1)(*2)
- USB cable for connect to debugger (*1)
  (USB-Micro)
- USB cable for serial connection ... For getting log messages
  (USB-Mini)
- Ethernet cable ... For connection between devices and packet capturing.
- (option)oscilloscope with 2 or more channels

Notes: 1. 2 required, one for the timeTransmitter device and one for the timeReceiver device.
2. Required only if build by "EWARM".

3.1.1 Hardware-setting of RZ/T2ME RSK

The required Hardware-settings are the as follows:

- Change boot mode to 16-bit bus boot mode (NOR flash)
- Enable external emulator(*)

Note: (*):Required only if build by "EWARM".

3.1.1.1 Change boot mode

To run the sample application in RAM, external flash memory must be blank.

NOR flash memory is blank on RZ/T2ME RSK, so set the boot mode to 16-bit bus boot mode (NOR flash).

The following operation are required:

Table 3-1 Hardware-setting "Change boot mode"

Reference	**Setting**
SW4-1	ON
SW4-2	OFF
SW4-3	ON

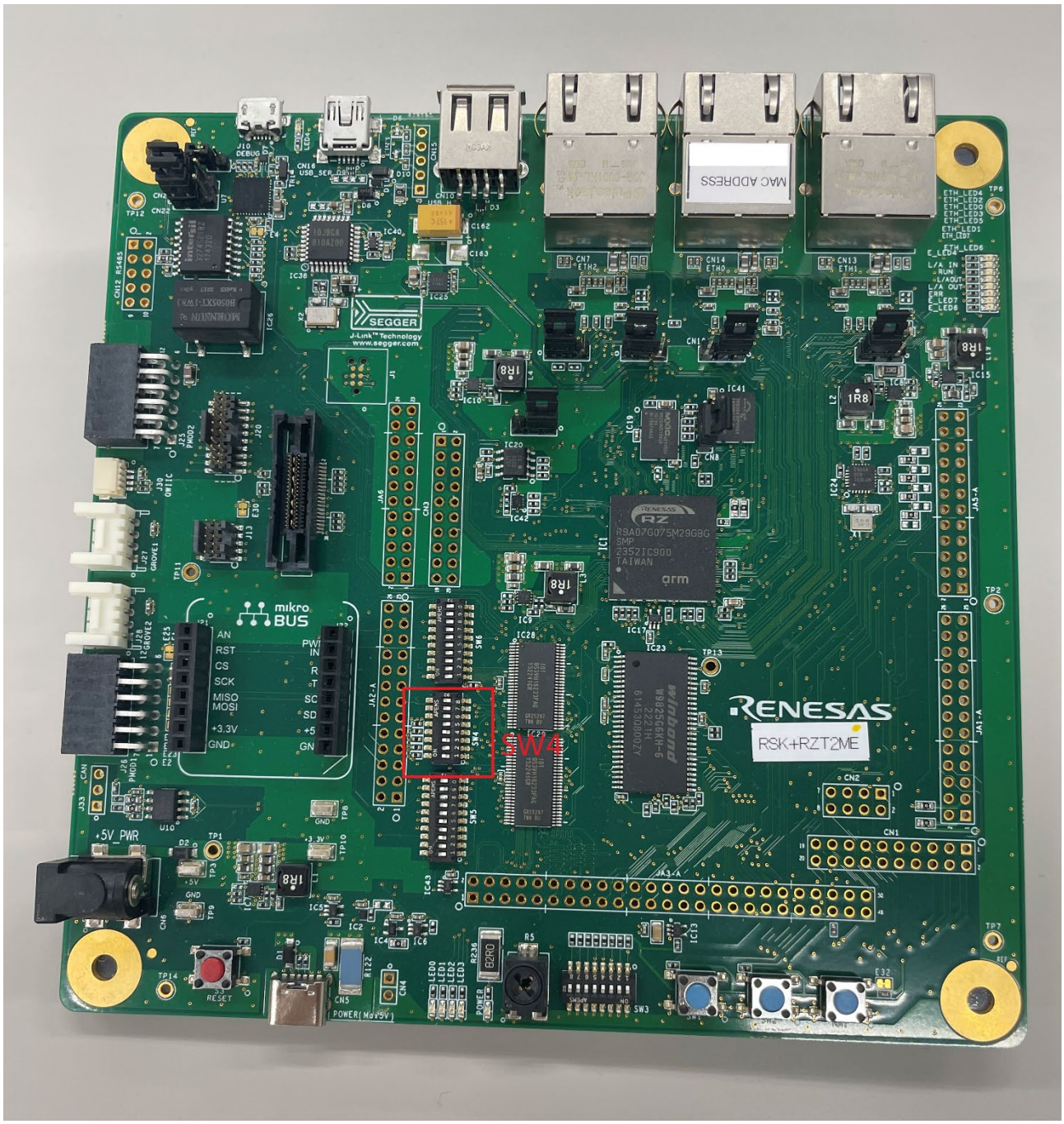

Figure 3-1 RZ/T2ME RSK board layout(SW4)

3.1.1.2 Change external-emulator enable/disable

Setting of enable/disable external-emulator depends on the IDE used.

- If using "EWARM"
  - — I-jet debugger (external-emulator) is used for debugging.
    External-emulator must be set to "enable".
- If using "e² studio"
  - — On-board debugger(J-LinkOB) is used for debugging.
    External-emulator must be set to "disable".

External-emulator enable/disable is set by "J9 jumper" on RZ/T2ME RSK.

The following operation are required:

Table 3-2 Hardware-setting "enable external-emulator"

using IDE	external-emulator	J9
EWARM	"enable"	Short
e² studio	"disable"	Open

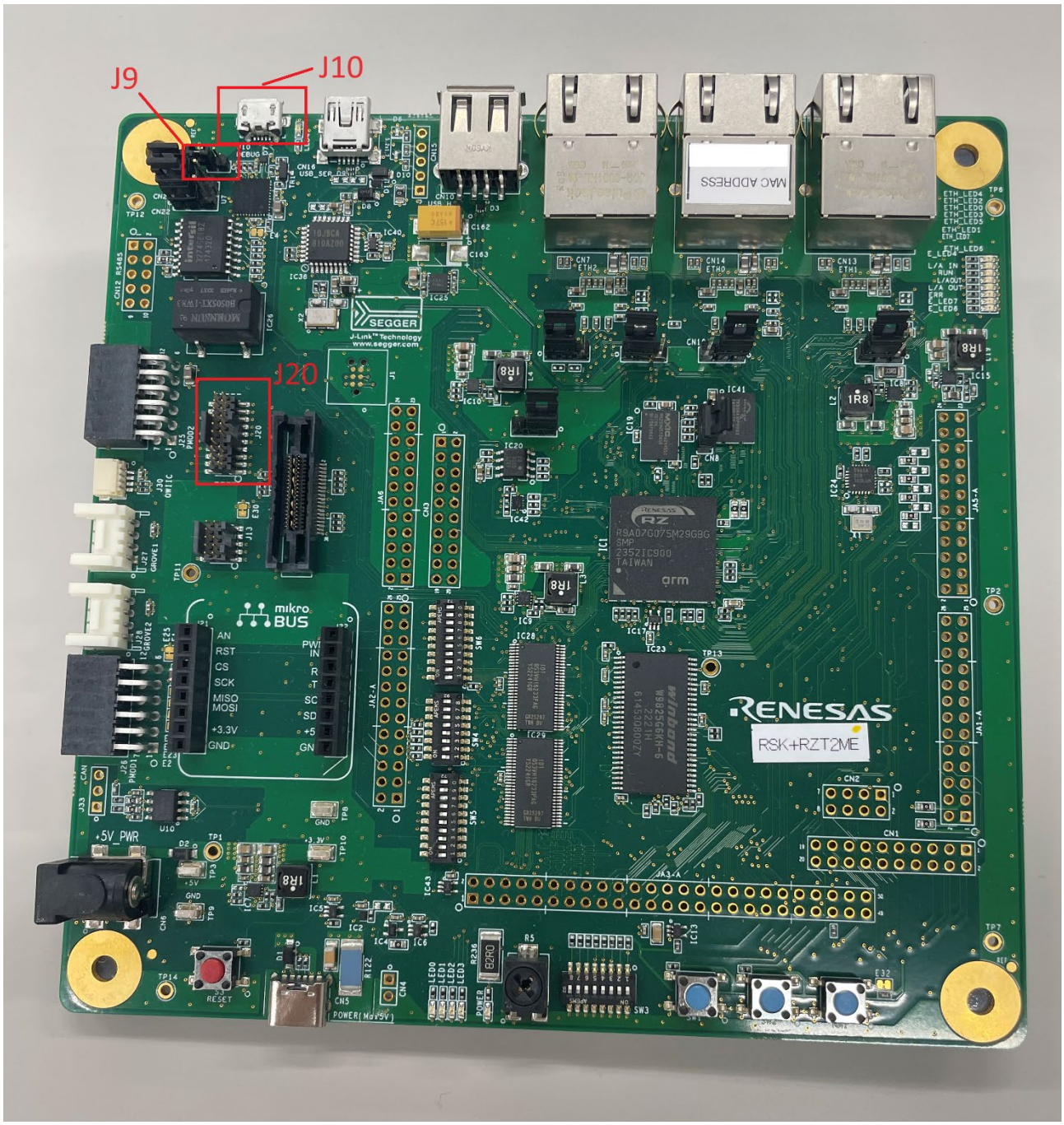

Figure 3-2 RZ/T2ME RSK board layout(J9, J10, J20)

3.1.2 Connect PC to RZ/T2ME RSK

3.1.2.1 If using "EWARM"

Connection of Host PC to RZ/T2ME RSK uses "I-jet debugger".

1. Connect Host PC and I-jet debugger.
2. Connect I-jet debugger and RZ/T2ME RSK's J20 connector.

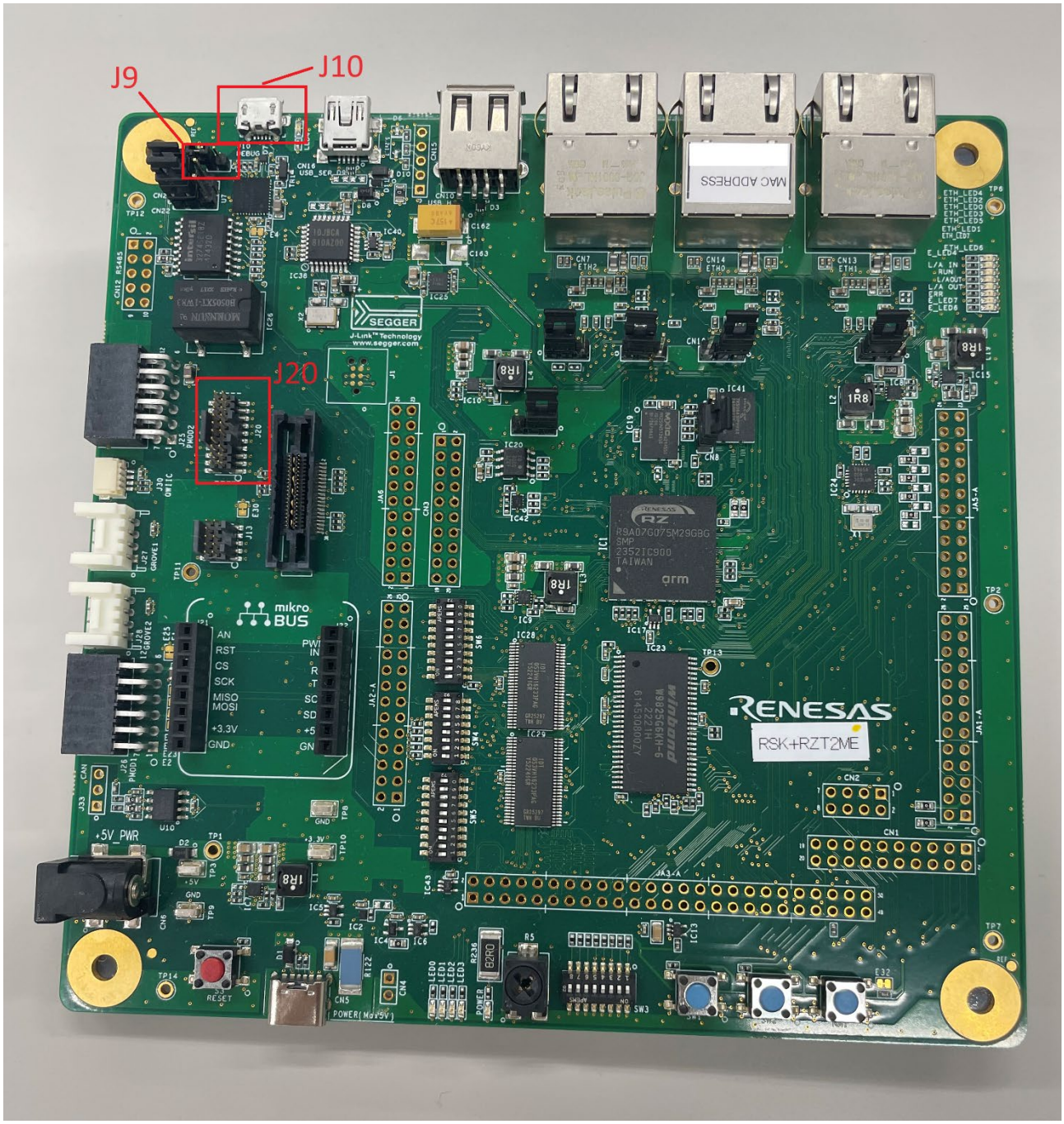

Figure 3-2(reprint) RZ/T2ME RSK board layout(J9, J10, J20)

If connection is successful, the lamps of "USB" and "DBG" on I-jet lights up.

Note: The lamps of "TPWR" must be off.

3.1.2.2 If using "e² studio"

Connection of Host PC to RZ/T2ME RSK uses "RZ/T2ME RSK's On-board debugger(J-LinkOB)".

Connect Host PC and RZ/T2ME RSK's "J-Link OB USB Connector"(J10)

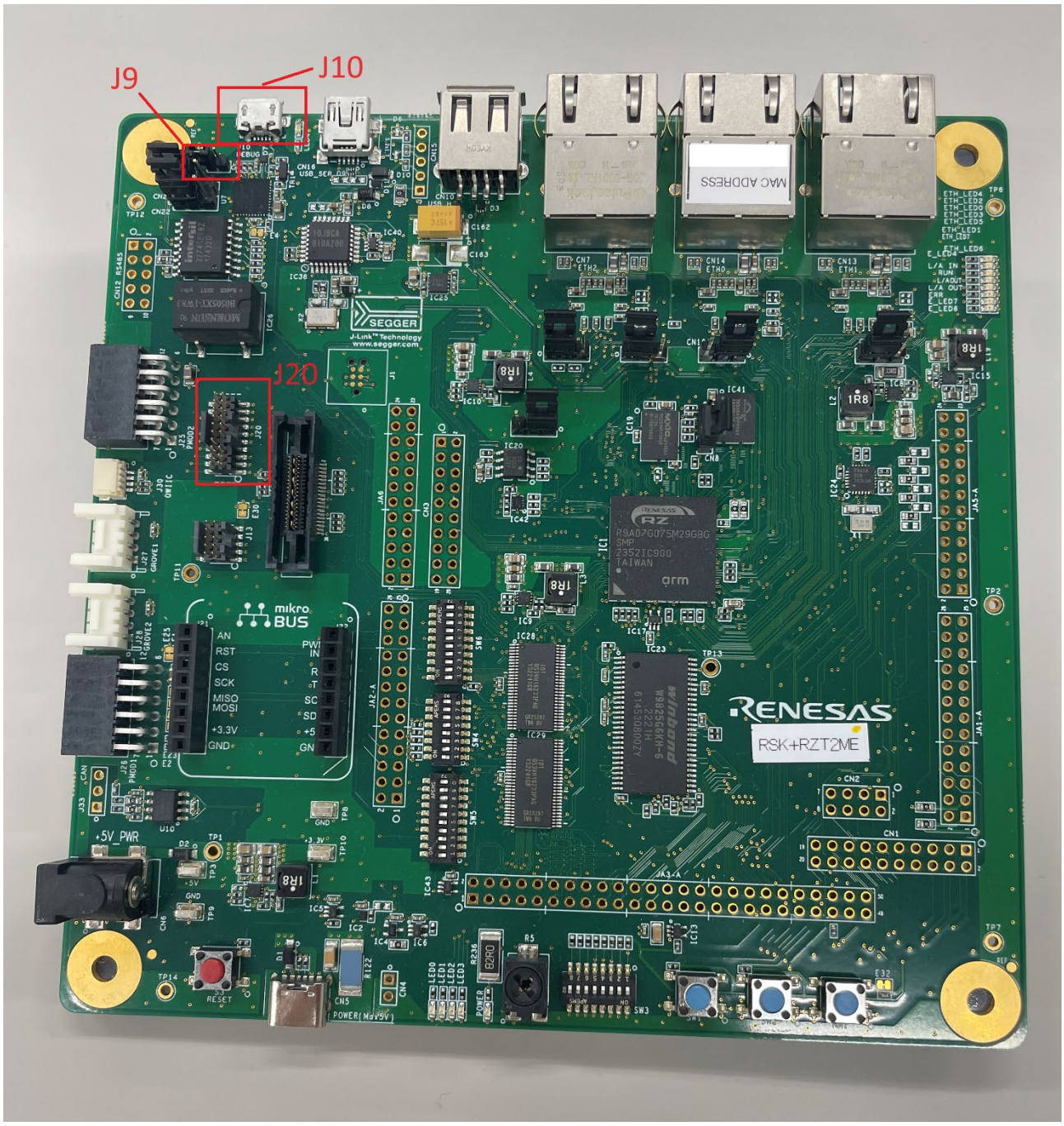

Figure 3-2(reprint) RZ/T2ME RSK board layout(J9, J10, J20)

Note: You can check connection in the following ways:
Notes: 1. On toolbar, click on the gear icon near "Launch Configuration".
2. In appeared dialog, select the "Debugger" tab.
3. In appeared screen, select the "Connection Setting" tab.
4. See the "J-Link" -> "J-Link Serial" field.
If you can select the J-Link serial number of the RZ/T2ME RSK board, the connection was completed successfully.

3.2 Software requirements

The following software are required for run sample application:

3.2.1 Required software for download sample application

The following software are required for build and download sample application:

- IDE
  IDE is selectable from "EWARM" or "e² studio".
  — EWARM (\1)(\2)

Notes: 1. License activation is required to use this software.
2. For using RZ/T2ME RSK, the following soft must be installed.
- RZ/T2 FSP SC(Smart Configurator) and FSP installer(For EWARM) (*)
  https://www.renesas.com/rskrzt2me

Note: This software is launched from above IDE.
For information on how to launch, see ”3.2.1.1.1 Launch FSP Smart Configurator from IDE”.
— e² studio
— e² studio and RZ/T2 FSP installer
https://www.renesas.com/rskrzt2me

3.2.1.1 Set-up of IDE

3.2.1.1.1 Launch FSP Smart Configurator from IDE

3.2.1.1.1.1 If using " EWARM "

On toolbar, select "Tools" -> "Configure Tools..."

In appeared dialog, select "New" button.

Fill in the fields as follow :

Table 3-3 Setting in "Configure Tools"

Field	Input
Menu Text	FSP Smart Configurator
Command	<Path for "FSP Smart Configurator"(rasc.exe)>
Argument	--compiler IAR configuration.xml
Initial Directory	$PROJ_DIR$

After setup, on toolbar, select "Tools" -> "FSP Smart Configurator".

FSP Smart Configurator will be launched.

3.2.1.1.1.2 If using "e² studio"

From the file-explorer in e² studio, open the file named "configuration.xml".

FSP Smart Configurator will be launched.

3.2.1.1.2 Select the download destination when connecting multiple RZ/T2ME RSK

3.2.1.1.2.1 If using " EWARM "

1. On toolbar, select "Project" -> "Options...".

Note: Or in IDE's file explorer, right click the project and select "Options...".

2. In appeared dialog, in "Category:"box, select "I-jet".
3. In "Setup" tab -> "Emulator", check the checkbox of "Always prompt for probe selection".

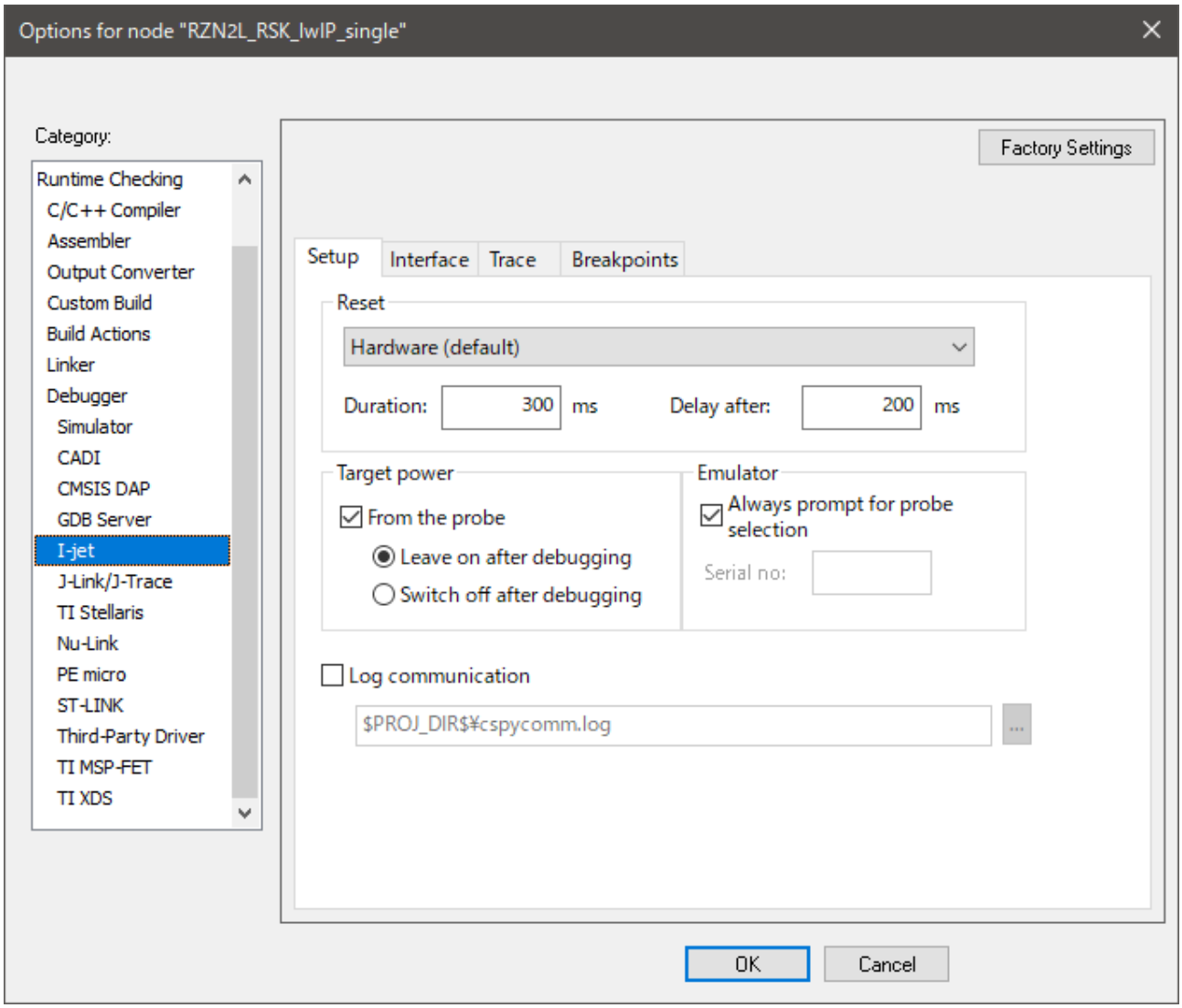

Figure 3-3 Setting dialog

After setup, the dialog of I-jet selection will appear just before application download.

In the dialog, select the I-jet connected to the RZ/T2ME RSK that you want to download the application to.

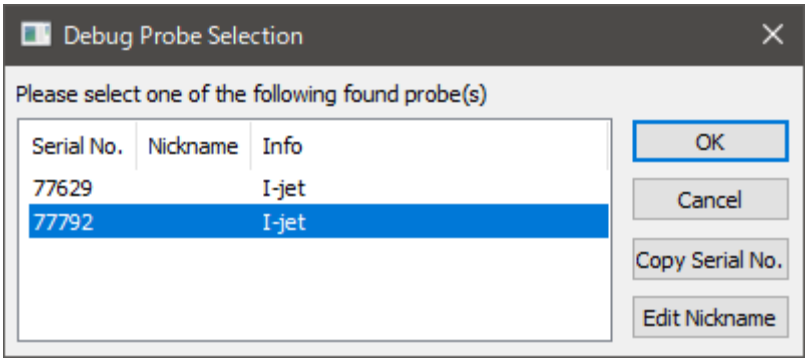

Figure 3-4 I-jet selection dialog

3.2.1.1.2.2 If using "e² studio"

1. On toolbar, click on the gear icon near "Launch Configuration".
2. From the dialog that appears, select the "Debugger" tab.
3. On the screen that appears, Select the "Connection Setting" tab.
4. On the "J-Link" -> "J-Link Serial" field, select J-Link serial number of RZ/T2ME RSK to be connected.

3.2.2 Third-Party software

3.2.2.1 Serial terminal tool

The sample application outputs log messages to "UART".

The serial terminal tool is required to check the log messages.

- TeraTerm
  Tera Term Open Source Project (teratermproject.github.io)

The serial port settings in TeraTerm are the following:

Table 3-4 Serial connection configuration

component	detail
Speed	115200
Data	8bit (default)
Parity	none (default)
Stop bits	1bit (default)
Flow control	none (default)

4. Running sample application

This chapter shows the sequence of steps from building application to running.

4.1 Build and download

4.1.1 Open project

4.1.1.1 If using " EWARM "

Unzip the zip file _"RZT2ME_RSK_IEEE1588.zip" contains the project of sample application for EWARM.

Open the follow unzipped file in EWARM.

```
/project/rzt2m_rsk/lwip_single/ewarm/RZT2ME_RSK_IEEE1588.eww
```

4.1.1.2 If using "e² studio"

Follow these steps to import the project of sample application.

1. Unzip the zip file _"RZT2ME_RSK_IEEE1588.zip" contains the project of sample application for e² studios.
2. Move unzipped directory(_"RZT2ME_RSK_IEEE1588"_) to the directory where you want to generate the project.
3. Launch e² studio and open the directory where you want to generate the project.
4. On toolbar, select "File" -> "Open Projects from fileSystem...".
5. In appeared dialog, select "Directory" button and select the unzipped directory you just moved (_"RZT2ME_RSK_IEEE1588/project/rzt2m_rsk/lwip_single/e2studio"_).
6. Select "Finish button", the project will be imported.

4.1.2 Pre-configuration for each device

Before build, each device must be configured.

The required Pre-configurations are the as follows :

- MAC address of device
- IP address of device
- Clock information used by BMCA
- Delay mechanism(*)
- Time distribution method(*)
- Network transport(*)

Note: (*): . This Configuration must be consistent across all devices.

4.1.2.1 Change MAC address of device

1. Launch "FSP Smart Configurator" from IDE.

Note: For information on how to launch, see “3.2.1.1.1 Launch FSP Smart Configurator from IDE”

2. At FSP Smart Configurator, In button of "FSP Configuration" view, open "Stack" tab.
3. From List of "threads" in upper left of the "FSP Configuration" view, select "g_ether0 Ethernet Driver on r_ether".
4. In Properties view, open "Module g_ether0 Ethernet Driver on r_ether" -> "General".
5. At "General", The value of "MAC address" is device's MAC address.
   Change the value depending to the address you want to assign.

Note: Must be set to a different value for each device.

4.1.2.2 Change IP address of device

Open "app_config.h" from project's directory.

```
/common/renesas/application/app_config.h
```

From "app_config.h", at line 7,

```
; #define NETIF_0_TCPIP_IP    LWIP_MAKEU32(192,168, 1,170)
```

IP address to be set on the Ethernet.

Note: Link-upped Ethernet is assigned the IP address defined as "NETIF_0_TCPIP_IP".

Change the value depending to the address you want to assign.

Note: Must be set to a different value for each device.

4.1.2.3 Clock information used by BMCA

Open "app_config.h" from project's directory.

```
/common/renesas/application/app_config.h
```

From "app_config.h", at line 14,

```
; // setting BMCA Clock Parameter
; // Priority1
; #define BMCA_PRIORITY_1                 12
; // Clock Class
; #define BMCA_PRIORITY_CLOCK_CLASS       248
; // Clock Accuracy
; #define BMCA_PRIORITY_CLOCK_ACCURACY    0xFE
; // Clock Variance
; #define BMCA_PRIORITY_CLOCK_VARIANCE    0xFFFF
; // Priority2
; #define BMCA_PRIORITY_2                 128
; // Domain Number
; #define BMCA_DOMAIN_NUMBER              0
```

You can set the clock information used by the BMCA by defining macros.

The following settings are available for each item:

- `#define BMCA_PRIORITY_1`
  - Value of Priority1
    The range of value is 0 to 255.
- `#define BMCA_PRIORITY_CLOCK_CLASS`
  - Value of Clock Class
    The range of value is 0 to 255.
- `#define BMCA_PRIORITY_CLOCK_ACCURACY`
  - Value of Clock Accuracy
    The range of value is 0 to 255.
- `#define BMCA_PRIORITY_CLOCK_VARIANCE`
  - Value of Clock Variance
    The range of value is 0 to 65535.
- `#define BMCA_PRIORITY_2`
  - Value of Priority2
    The range of value is 0 to 255.
- `#define BMCA_DOMAIN_NUMBER`
  - Value of Domain Number
    The range of value is 0 to 255.

Note: Devices with the same "Domain Number" on the network will synchronize their time.

4.1.2.4 Delay mechanism

Open "app_config.h" from project's directory.

```
/common/renesas/application/app_config.h
```

From "app_config.h", at line 33,

```
; // setting ptp delay mechanism
; // 0: E2E( End to End Mechanism )
; // 1: P2P( Peer to Peer Mechanism )
; #define PTP_DELAY_MECHANISM  1
```

It is possible to change the delay mechanism by defining a macro.

Note: If you want to measure the transmission delay time by E2E, set it to 0.
Note: If you want to measure the transmission delay time by P2P, set it to 1.

4.1.2.5 Time distribution method

Open "app_config.h" from project's directory.

```
/common/renesas/application/app_config.h
```

From "app_config.h", at line 38,

```
; // setting ptp time distribution
; // 0:two step clock
; // 1:one step clock
; #define PTP_ONE_STEP_FLAG    0
```

It is possible to switch the time distribution method by defining a macro.

Note: If you want to distribute the time in two steps, set it to 0.
Note: If you want to distribute the time in one step, set it to 1.

4.1.2.6 Network transport

Open "app_config.h" from project's directory.

```
/common/renesas/application/app_config.h
```

From "app_config.h", at line 28,

```
; // setting transport layer
; // 0: Layer 2: Raw packet( IEEE 802.3 )
; // 1: Layer 3: IPv4 UDP packet
; #define PTP_TRANSPORT_LAYER  1
```

It is possible to switch the transport layer by defining a macro.

Note: If you want to using Layer 2 (Ethernet Frame), set this to 0.
Note: If you want to using Layer 3 (IPv4 UDP Frame), set this to 1.

4.1.3 Build and download to RZ/T2ME RSK

4.1.3.1 Generate Project contents

Before build, generate project contents using FSP Smart Configurator.

- Launch "FSP Smart Configurator" from IDE.
  For information on how to launch, see “3.2.1.1.1 Launch FSP Smart Configurator from IDE”.
- In FSP Smart Configurator, select "Generate Project Content" in the upper right of the "FSP Configuration"view. Project content will be created.

4.1.3.2 Build and download

4.1.3.2.1 If using " EWARM "

After the creation of project content, select "Project" -> "Make" on toolbar.

The application will be built.

After building, select "Project" -> "Download and Debug" on toolbar.

The application downloading to RZ/T2ME RSK will be started.

4.1.3.2.2 If using "e² studio"

After the creation of project content, select "Project" -> "build" on toolbar.

The application will be built.

After building, select "Run" -> "Debug" on toolbar.

The application downloading to RZ/T2ME RSK will be started.

4.2 Run sample application

When the application downloading to RZ/T2ME RSK is completed, the Application becomes a standby state for running.

Follow these steps to start running application.

Note: For details on the operation check, see ”2.1.3 Sample application's outputs for checking operation”.

4.2.1 If using " EWARM "

Select "Debug" -> "Go" on toolbar.

Application will start running.

4.2.2 If using "e² studio"

Before start application, the following operations are required.

1. Open "Resisters" view.
2. Change value of "General Registers" -> "cpsr" register from "0x.....fa" to "0x.....da".(*)

Note: If the debugger connection setting "Set CPSR (5bit) after download" is "Yes", this step is not necessary.

After above operations, select "Run" -> "Resume" on toolbar.

Application will start running.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 29, 2024	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.