RZ/T2H Group

HIPERFACE DSL sample program

Introduction

This application note explains a sample program for acquiring and indicating information from an encoder in conformance with the HIPERFACE DSL® communications protocol specification by using the encoder Interface of the RZ/T2H.

The features of the program:

- Acquiring angle information, etc. from an encoder (EFM50-0KF0A023A) compliant with the HIPERFACE DSL® communications protocol specification.

Target Device

RZ/T2H

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1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications and Figure 1.1 shows the operating environment when the sample code is being executed.

Table 1.1 Peripheral Functions and Applications

Peripheral Module	Application
HIPERFACE DSL controller (HDSL)	Handling transfer to and from an absolute encoder incorporating a facility for handling the HIPERFACE DSL communications protocol
Interrupt controller (ICU)	Controlling interrupts from the HDSL controller
General PWM timer (GPT) unit 0 channel 0	Generating event cycles for input to the ELC
Event link controller (ELC)	Makes the link between events output from unit 0 channel 0 of the GPT and the HDSL module.
Serial Communication Interface (SCI) UART	Asynchronous communications of the SCI are used for COM port communications by using USB interface. It is used for console interface of the sample program.

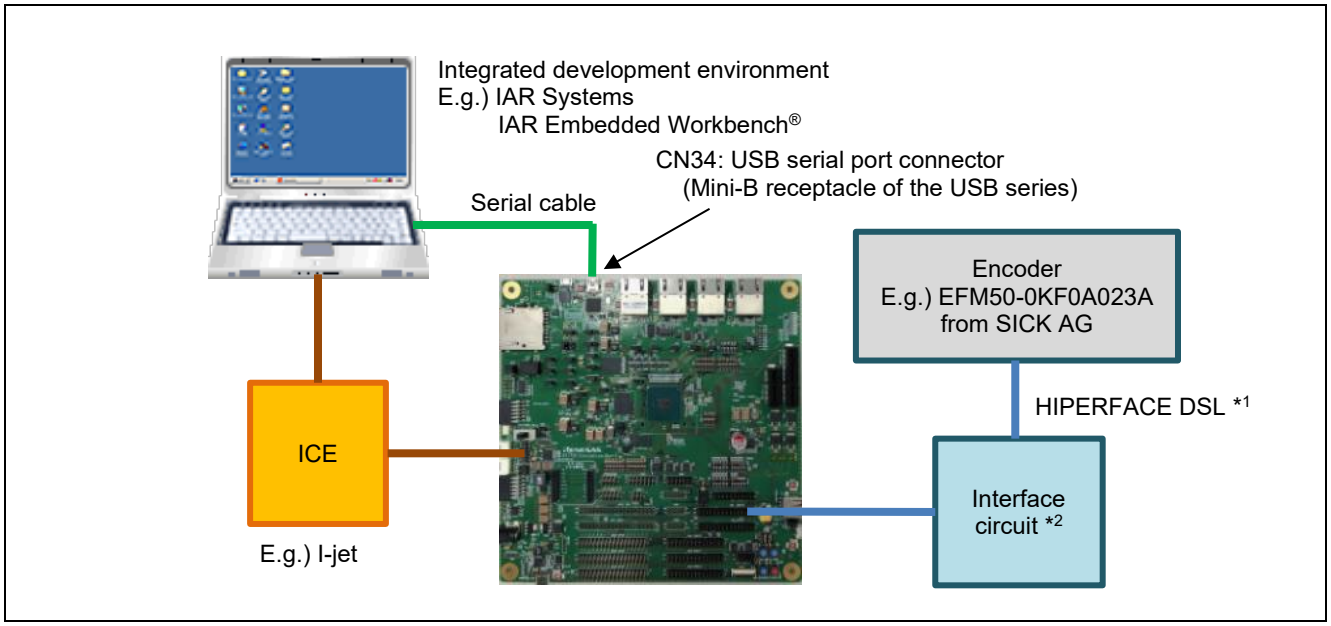

Figure 1.1 Operating Environment

Note 1. For allowable cable length, refer to the encoder manuals.
2. Refer to the “HIPERFACE DSL® MASTER Integration Manual”.

2. Operating Environment

The sample code covered in this application note is for the environment below.

Table 2.1 Operating Environment

Item		Description
MCU		RZ/T2H Group
Operating frequency *1	CR52 ver.	CPUCLK = 1000 MHz (Cortex®-R52 CPU0)
	CA55 ver.	CPUCLK = 1200 MHz (Cortex®-A55 Core0)
Operating voltage		0.8 V (Core) / 1.1 V (DDR) / 1.8 V (PLL, etc.) / 3.3 V (I/O)
Integrated development environment *2		IAR Systems: IAR Embedded Workbench® for Arm® RENESAS: e² studio
Board		RZ/T2H Evaluation Board (RTK9RZT2Hxxxxxxxxx)
Devices (function to be used on the board)		None

Note: 1. This sample program has a CR52 version that runs on the CPU core Cortex®-R52 and a CA55 version that runs on the CPU core Cortex®-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.
2. Refer to the RZ/T2H Group Encoder I/F HIPERFACE DSL sample program Release Note to check the version number of the integrated development environment.

3. Peripheral Functions

The basics of the peripheral modules, operating modes, and registers are described in the “RZ/T2H Group User’s Manual: Hardware”

3.1 Pins

The pins used and their functions are listed in the table below.

Table 3.1 Pins Used and Their Functions

Channel	Pin Name	I/O Port	Input /Output	Voltage Domain	Description
HFDSL0	ENCIFDI00 (dsl_in)	P14_5	Input	VDD33	Data input
	ENCIFDO00 (dsl_out)	P14_4	Output	VDD33	Data output
	ENCIFOE00 (dsl_en)	P14_3	Output	VDD33	Drive/receive control
HFDSL1	ENCIFDI01 (dsl_in)	P33_5	Input	VDD1833_3	Data input
	ENCIFDO01 (dsl_out)	P33_4	Output	VDD1833_3	Data output
	ENCIFOE01 (dsl_en)	P33_3	Output	VDD1833_3	Drive/receive control
HFDSL2	ENCIFDI02 (dsl_in)	P03_6	Input	VDD33	Data input
	ENCIFDO02 (dsl_out)	P03_5	Output	VDD33	Data output
	ENCIFOE02 (dsl_en)	P03_4	Output	VDD33	Drive/receive control
HFDSL3	ENCIFDI03 (dsl_in)	P05_0	Input	VDD33	Data input
	ENCIFDO03 (dsl_out)	P04_7	Output	VDD33	Data output
	ENCIFOE03 (dsl_en)	P04_6	Output	VDD33	Drive/receive control
HFDSL4	ENCIFDI04(dsl_in)	P01_1	Input	VDD1833_5	Data input
	ENCIFDO04 (dsl_out)	P01_0	Output	VDD1833_5	Data output
	ENCIFOE04 (dsl_en)	P00_7	Output	VDD33	Drive/receive control
HFDSL5	ENCIFDI05 (dsl_in)	P12_7	Input	VDD1833_6	Data input
	ENCIFDO05 (dsl_out)	P12_6	Output	VDD1833_6	Data output
	ENCIFOE05 (dsl_en)	P12_5	Output	VDD1833_6	Drive/receive control
HFDSL6	ENCIFDI06 (dsl_in)	P34_1	Input	VDD1833_3	Data input
	ENCIFDO06 (dsl_out)	P34_0	Output	VDD1833_3	Data output
	ENCIFOE06 (dsl_en)	P33_7	Output	VDD1833_3	Drive/receive control
HFDSL7	ENCIFDI07 (dsl_in)	P34_5	Input	VDD1833_3	Data input
	ENCIFDO07 (dsl_out)	P34_4	Output	VDD1833_3	Data output
	ENCIFOE07 (dsl_en)	P34_3	Output	VDD1833_3	Drive/receive control
HFDSL8	ENCIFDI08 (dsl_in)	P29_0	Input	VDD33	Data input
	ENCIFDO08 (dsl_out)	P28_7	Output	VDD33	Data output
	ENCIFOE08 (dsl_en)	P28_6	Output	VDD33	Drive/receive control
HFDSL9	ENCIFDI09 (dsl_in)	P29_4	Input	VDD1833_2	Data input
	ENCIFDO09 (dsl_out)	P29_3	Output	VDD1833_2	Data output
	ENCIFOE09 (dsl_en)	P29_2	Output	VDD1833_2	Drive/receive control
HFDSL10	ENCIFDI10 (dsl_in)	P30_0	Input	VDD1833_2	Data input
	ENCIFDO10 (dsl_out)	P29_7	Output	VDD1833_2	Data output
	ENCIFOE10 (dsl_en)	P29_6	Output	VDD1833_2	Drive/receive control
HFDSL11	ENCIFDI11 (dsl_in)	P30_4	Input	VDD1833_2	Data input
	ENCIFDO11 (dsl_out)	P30_3	Output	VDD1833_2	Data output
	ENCIFOE11 (dsl_en)	P30_2	Output	VDD1833_2	Drive/receive control
HFDSL12	ENCIFDI12 (dsl_in)	P13_3	Input	VDD1833_6	Data input
	ENCIFDO12 (dsl_out)	P13_2	Output	VDD1833_6	Data output
	ENCIFOE12 (dsl_en)	P13_1	Output	VDD1833_6	Drive/receive control

Channel	Pin Name	I/O Port	Input /Output	Voltage Domain	Description
HFDSL13	ENCIFDI13 (dsl_in)	P13_7	Input	VDD1833_6	Data input
	ENCIFDO13 (dsl_out)	P13_6	Output	VDD1833_6	Data output
	ENCIFOE13 (dsl_en)	P13_5	Output	VDD1833_6	Drive/receive control
HFDSL14	ENCIFDI14 (dsl_in)	P18_7	Input	VDD33	Data input
	ENCIFDO14 (dsl_out)	P18_6	Output	VDD33	Data output
	ENCIFOE14 (dsl_en)	P18_5	Output	VDD33	Drive/receive control
HFDSL15	ENCIFDI15 (dsl_in)	P32_1	Input	VDD33	Data input
	ENCIFDO15 (dsl_out)	P32_0	Output	VDD33	Data output
	ENCIFOE15 (dsl_en)	P31_7	Output	VDD33	Drive/receive control

4. Software

4.1 HFDSL Driver Function

The functions of the HFDSL driver are listed below.

1. Initial settings
2. Acquiring positional data
3. Transmitting and receiving messages

4.2 File Structure

For the file structure, refer to the release note for the RZ/T2H Group Encoder I/F HIPERFACE DSL sample program.

4.3 Functions

The functions to be used are listed in the table below.

Table 4.1 Functions

Category	Function Name	Page Number
HFDSL driver API functions	R_HFDSL_Open	8
	R_HFDSL_Close	8
	R_HFDSL_GetVersion	9
	R_HFDSL_Control	9
User-defined functions	hfdsl_int_nml_callback	13
	hfdsl_int_err_callback	14
	hfdsl_int_mrcv_callback	14
Interrupt handlers	hfdsl_int_isr_chn	15
	hfdsl_fpr_isr_chn	15
	hfdsl_err_isr	15

4.4 Specifications of API Functions

4.4.1 R_HFDSL_Open

R_HFDSL_Open			
Synopsis	Starts controlling operation of the encoder.		
Header	r_hfdsl_rzt2_if.h		
Declaration	int32_t R_HFDSL_Open(const int32_t id, r_hfdsl_info_t* p_info);		
Description	Call this function before using the HFDSL driver. It initializes the driver. ・Setting the interrupts ・Setting the callback functions		
Argument	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)	
		R_HFDSL0_ID	: Specifies channel 0.
		R_HFDSL1_ID	: Specifies channel 1.
		:	:
		R_HFDSL15_ID	: Specifies channel 15.
		Others	: Setting is not allowed.
	p_info	: Holder for the initial settings of the driver Set the pointer to the r_hfdsl_info_t structure which holds the information on the initial settings of the driver.	
Returned value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or the r_hfdsl_info_t structure member pointed by the p_info is not specified.) R_HFDSL_ERR_ACCESS: Abnormal termination (This function is already executed.)		
Note	Calling this API function from within a callback function is prohibited.		

4.4.2 R_HFDSL_Close

R_HFDSL_Close			
Synopsis	Ending control of the encoder		
Header	r_hfdsl_rzt2_if.h		
Declaration	int32_t R_HFDSL_Close(const int32_t id);		
Description	This function stops controlling operation of the encoder on the designated channel.		
Argument	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)	
		R_HFDSL0_ID	: Specifies channel 0.
		R_HFDSL1_ID	: Specifies channel 1.
		:	:
		R_HFDSL15_ID	: Specifies channel 15.
		Others	: Setting is not allowed.
Return Value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is not specified.)		
Note	Before calling this function, be sure to call R_HFDSL_Open. Calling this API function from within a callback function is prohibited.		

4.4.3 R_HFDSL_GetVersion

R_HFDSL_GetVersion	
Synopsis	Acquire the version number of the encoder interface driver.
Header	r_hfdsl_rzt2_if.h
Declaration	uint32_t R_HFDSL_GetVersion(void);
Description	This function acquires the version number of the HFDSL driver.
Argument	None
Return value	The major part of the version number is stored in the sixteen MSBs and the minor part of the version number is stored in the sixteen LSBs. Ex.) For ver.1.2, the value returned is 0x00010002.

4.4.4 R_HFDSL_Control

R_HFDSL_Control		
Synopsis	Controlling operation of the encoder.	
Header	r_hfdsl_rzt2_if.h	
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);	
Description	This function controls operations of the encoder by using the cmd argument. See section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands” for the operation.	
Argument	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)
		R_HFDSL0_ID : Specifies channel 0.
		R_HFDSL1_ID : Specifies channel 1.
		: :
		R_HFDSL15_ID : Specifies channel 15.
		Others : Setting is not allowed.
	cmd	: Command For details, see section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands”.
	p_buf	: Arguments corresponding to each cmd.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or cmd is not specified.) See section “4.4.4(1), Protocol Initialization Commands” and section “4.4.4(2), Control Commands” for other returned values.	

(1) Protocol Initialization Commands

(a) R_HFDSL_CMD_INIT

R_HFDSL_CMD_INIT	
Synopsis	Protocol initialization
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	Call this function after executing function R_HFDSL_Open or after a protocol reset. For how to detect a protocol reset, see section “4.5.2 hfdsl_int_err_callback”.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_INIT. p_buf : Specify NULL.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or p_buf is invalid.) R_HFDSL_ERR_ACCESS: Abnormal termination (R_HFDSL_Open has not been executed.) R_HFDSL_ERR_INIT: Abnormal termination (Link check timed out.)
Note	Calling this API function from within a callback function is prohibited.

(b) R_HFDSL_CMD_ENCID

R_HFDSL_CMD_ENCID	
Synopsis	Check encoder ID
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	Call this function after the R_HFDSL_CMD_INIT protocol initialization command. If the value returned is R_HFDSL_ERR_INIT and the protocol is to be initialized again, start over again from the protocol initialization command R_HFDSL_CMD_INIT after executing the control command R_HFDSL_CMD_RST.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_ENCID. p_buf : Encoder ID Specify the unit32_t pointer which holds the encoder ID.
Returned value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (R_HFDSL_CMD_INIT has not been executed.) R_HFDSL_ERR_INIT: Abnormal termination (The connected encoder ID does not match the specified ID.)
Note	Calling this API function form within a callback function is prohibited.

(2) Control Commands

(a) R_HFDSL_CMD_POS

R_HFDSL_CMD_POS		
Synopsis	Acquiring the fast position	
Header	r_hfdsl_rzt2_if.h	
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);	
Description	This function acquires the fast position by reading the fast position registers (POS4 to POS0).	
Argument	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)
		R_HFDSL0_ID : Specifies channel 0.
		R_HFDSL1_ID : Specifies channel 1.
		: :
		R_HFDSL15_ID : Specifies channel 15.
		Others : Setting is not allowed.
	cmd	: Specify R_HFDSL_CMD_POS.
	p_buf	: Fast position Specifies the pointer to the r_hfdsl_pos_t structure which holds the fast position value. For details, see section “4.10.1(2) r_hfdsl_pos_t”.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG： Abnormal termination (The id is invalid or p_buf is null.)	

(b) R_HFDSL_CMD_VPOS

R_HFDSL_CMD_VPOS		
Synopsis	Acquiring the safe position	
Header	r_hfdsl_rzt2_if.h	
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);	
Description	This function acquires the safe position by reading the safe position registers (VPOS4 to VPOS0), and safe position CRC registers (VPOSCRC_H, VPOSCRC_L).	
Argument	id	: Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.)
		R_HFDSL0_ID : Specifies channel 0.
		R_HFDSL1_ID : Specifies channel 1.
		: :
		R_HFDSL15_ID : Specifies channel 15.
		Others : Setting is not allowed.
	cmd	: Specify R_HFDSL_CMD_VPOS.
	p_buf	: Safe position Specifies the pointer to the r_hfdsl_vpos_t structure which holds the safe position value. For details, see section “4.10.1(3) r_hfdsl_vpos_t”.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.)	

(c) R_HFDSL_CMD_VEL

R_HFDSL_CMD_VEL	
Synopsis	Acquiring the rotational velocity of the motor.
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function acquires the rotational velocity of the motor by reading the velocity registers (VEL2 to VEL0).
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_VEL. p_buf : Rotational velocity of the motor Specifies the pointer to uint32_t which holds the rotational velocity of the motor.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.)

(d) R_HFDSL_CMD_MSG

R_HFDSL_CMD_MSG	
Synopsis	Transmitting messages
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control(const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function transmits messages. The data received is indicated by function hfdsl_int_mrcv_callback. For details of the function, see section “4.5.3 hfdsl_int_mrcv_callback”.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_MSG. p_buf : Message data for transmission Specifies the pointer to the r_hfdsl_send_msg_t structure which holds message data for transmission. For details, see section “4.10.1(4) r_hfdsl_send_msg_t”.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id is invalid or p_buf is null.) R_HFDSL_ERR_ACCESS: Abnormal termination (The protocol initialization function described in section “4.4.4(1) Protocol Initialization Commands”, has not been executed.)
Note	Calling this API function from within a callback function is prohibited. To proceed with the next transmission, execute this function following the hfdsl_int_mrcv_callback function.

(e) R_HFDSL_CMD_RST

R_HFDSL_CMD_RST	
Synopsis	Protocol reset
Header	r_hfdsl_rzt2_if.h
Declaration	int32_t R_HFDSL_Control (const int32_t id, const r_hfdsl_cmd_t cmd, void *const p_buf);
Description	This function resets the protocol. After this function is called. An HDSLn_INT interrupt is generated in response to the PRST bit in the EVENT_H being set to 1. To resume communications, call the functions described in section “4.4.4(1), Protocol Initialization Commands”.
Argument	id : Specifies the ID to be used. (It is defined in r_hfdsl_rzt2_dat.h.) R_HFDSL0_ID : Specifies channel 0. R_HFDSL1_ID : Specifies channel 1. : : R_HFDSL15_ID : Specifies channel 15. Others : Setting is not allowed. cmd : Specify R_HFDSL_CMD_RST. p_buf : Specify NULL.
Return value	R_HFDSL_SUCCESS: Normal termination R_HFDSL_ERR_INVALID_ARG: Abnormal termination (The id or p_buf is invalid.)

4.5 Specification of User-defined Functions

4.5.1 hfdsl_int_nml_callback

hfdsl_int_nml_callback	
Synopsis	Indicating the generation of HDSLn_FPR interrupt
Header	-
Declaration	void hfdsl_int_nml_callback(uint8_t event);
Description	This callback function is registered with the member variable p_cb_nml of the argument r_hfdsl_info_t structure of the R_HFDSL_Open function. It is called when an HDSLn_FPR interrupt is generated. This interrupt shows that the fast position registers (POS4 to POS0) have been updated. The fast position can be acquired by executing the function R_HFDSL_Control (R_HFDSL_CMD_POS) from within this function. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
Argument	event : Source of the interrupt Holds the value POS_RDY_BIT. The value of this argument is only valid within this function.
Return value	None

4.5.2 hfdsl_int_err_callback

hfdsl_int_err_callback	
Synopsis	Indicating the generation of HDSLn_INT interrupt
Header	-
Declaration	void hfdsl_int_err_callback(uint32_t event_err);
Description	This callback function is registered with the member variable p_cb_err of the argument r_hfdsl_info_t structure of the R_HFDSL_Open function. It is called when an HDSLn_INT interrupt is generated in response to the SUM, POS, DTE or PRST bits in the EVENT_H register, or the MIN, ANS or QMLW bits in the EVENT_L register being set to 1. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
Argument	event_err : Source of the HDSLn_INT interrupt Holds the value of the EVENT_H, EVENT_L registers. The value of this argument is only valid within this function.
Return value	None
Note	This function is not called when an HDSLn_INT is generated in response to the FREL bit in the EVENT_L register being set to 1.

4.5.3 hfdsl_int_mrcv_callback

hfdsl_int_mrcv_callback	
Synopsis	Indicating that the HDSLn_INT interrupt by the FREL bit in the EVENT_L register has occurred.
Header	-
Declaration	void hfdsl_int_mrcv_callback(uint8_t* msg_data);
Description	This callback function is registered with the R_HFDSL_Control (R_HFDSL_CMD_MSG) function. It is called when the HDSLn_INT interrupt by the FREL bit in the EVENT_L register occurs, and data storage of the received message is completed. This function is the context of the interrupt handler. To ensure interrupt responsiveness, return immediately. The function name is an example and can be set freely.
Argument	msg_data[] : Message address and PC_BUFF register values (long messages) Two bytes of the message address (PC_ADD_H, PC_ADD_L) and the values of the PC_BUF0 to PC_BUF7 registers (long messages) are stored. The fifth bit LOFF of the message address PC_ADD_H holds the message reception error flag. The value of this argument remains valid until the next HDSLn_INT interrupt caused by the FREL bit is generated.
Return value	None

4.6 Interrupt Handler

4.6.1 hfdsl_int_isr_ch*n* (n=0 to 15)

hfdsl_int_isr_ch*n*	
Synopsis	Interrupt handler for the HDSL*n*_INT
Header	-
Declaration	static void hfdsl_int_isr_ch*n*(void);
Description	An interrupt handler for the HDSL*n*_INT interrupt. If the source of an interrupt is the FREL bit of the EVENT_L register, function hfdsl_int_mrcv_callback is called as a callback function. If the source of an interrupt is other bits of the EVENT_H register and the EVENT_L register, function hfdsl_int_err_callback is called as a callback function.
Argument	None
Return value	None

4.6.2 hfdsl_fpr_isr_ch*n* (n=0 to 15)

hfdsl_fpr_isr_ch*n*	
Synopsis	Interrupt handler for the HDSL*n*_FPR
Header	-
Declaration	static void hfdsl_fpr_isr_ch*n*(void);
Description	An interrupt handler for the HDSL*n*_FPR interrupt. If the interrupt is generated, function hfdsl_int_nml_callback is called as a callback function.
Argument	None
Return value	None

4.6.3 hfdsl_err_isr

hfdsl_err_isr	
Synopsis	Interrupt handler for the PERI_ERR0
Header	-
Declaration	static void hfdsl_err_isr(void);
Description	An interrupt handler for the PERI_ERR0 interrupt. If the interrupt is generated, this function reads error events from ENCIFERR_STAT*n* (n=1 to 4) register and clear interrupt.
Argument	None
Return value	None

4.7 Interrupts

Table 4.2 lists the interrupts for the HFDSL driver.

Table 4.2 Interrupts for the HFDSL Driver

Interrupts	ID *		Description
	CR52 ver.	CA55 ver.	
HDSL0_INT	388	716	Generated when the value of any bit in the ch0 EVENT_L, EVENT_H registers is updated to 1.
HDSL0_FPR	389	718	Generated when the fast position value of the ch0 is ready to read.
HDSL1_INT	390	720	Generated when the value of any bit in the ch1 EVENT_L, EVENT_H registers is updated to 1.
HDSL1_FPR	391	722	Generated when the fast position value of the ch1 is ready to read.
HDSL2_INT	392	724	Generated when the value of any bit in the ch2 EVENT_L, EVENT_H registers is updated to 1.
HDSL2_FPR	393	726	Generated when the fast position value of the ch2 is ready to read.
HDSL3_INT	394	728	Generated when the value of any bit in the ch3 EVENT_L, EVENT_H registers is updated to 1.
HDSL3_FPR	395	730	Generated when the fast position value of the ch3 is ready to read.
HDSL4_INT	396	732	Generated when the value of any bit in the ch4 EVENT_L, EVENT_H registers is updated to 1.
HDSL4_FPR	397	734	Generated when the fast position value of the ch4 is ready to read.
HDSL5_INT	398	736	Generated when the value of any bit in the ch5 EVENT_L, EVENT_H registers is updated to 1.
HDSL5_FPR	399	738	Generated when the fast position value of the ch5 is ready to read.
HDSL6_INT	400	740	Generated when the value of any bit in the ch6 EVENT_L, EVENT_H registers is updated to 1.
HDSL6_FPR	401	742	Generated when the fast position value of the ch6 is ready to read.
HDSL7_INT	402	744	Generated when the value of any bit in the ch7 EVENT_L, EVENT_H registers is updated to 1.
HDSL7_FPR	403	746	Generated when the fast position value of the ch7 is ready to read.
HDSL8_INT	404	748	Generated when the value of any bit in the ch8 EVENT_L, EVENT_H registers is updated to 1.
HDSL8_FPR	405	750	Generated when the fast position value of the ch8 is ready to read.
HDSL9_INT	406	752	Generated when the value of any bit in the ch9 EVENT_L, EVENT_H registers is updated to 1.
HDSL9_FPR	407	754	Generated when the fast position value of the ch9 is ready to read.
HDSL10_INT	408	756	Generated when the value of any bit in the ch10 EVENT_L, EVENT_H registers is updated to 1.
HDSL10_FPR	409	758	Generated when the fast position value of the ch10 is ready to read.
HDSL11_INT	410	760	Generated when the value of any bit in the ch11 EVENT_L, EVENT_H registers is updated to 1.
HDSL11_FPR	411	762	Generated when the fast position value of the ch11 is ready to read.
HDSL12_INT	412	764	Generated when the value of any bit in the ch12 EVENT_L, EVENT_H registers is updated to 1.
HDSL12_FPR	413	766	Generated when the fast position value of the ch12 is ready to read.
HDSL13_INT	414	768	Generated when the value of any bit in the ch13 EVENT_L, EVENT_H registers is updated to 1.
HDSL13_FPR	415	770	Generated when the fast position value of the ch13 is ready to read.

Interrupts	ID *		Description
	CR52 ver.	CA55 ver.	
HDSL14_INT	416	772	Generated when the value of any bit in the ch14 EVENT_L, EVENT_H registers is updated to 1.
HDSL14_FPR	417	774	Generated when the fast position value of the ch14 is ready to read.
HDSL15_INT	418	776	Generated when the value of any bit in the ch15 EVENT_L, EVENT_H registers is updated to 1.
HDSL15_FPR	419	778	Generated when the fast position value of the ch15 is ready to read.
PERI_ERR0	420	417	Generated when the value of any bit indicating HDSL ch0 to ch15 error in the ENCIFERR_STATn (n=1 to 4) register is updated to 1.

Note: This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

4.8 Constants and Error Codes

The tables below list the constants and error codes. For the definitions, see the respective tables.

Table 4.3 User-defined Constants for the HFDSL Driver (r_hfdsl_rzt2_config.h)

Constant Name	Setting	Description
R_HFDSL_SYNC_CTRL	3	Setting of the SYNC_CTRL register
R_HFDSL_ACC_ERR	31	Setting of the ACC_ERR register
R_HFDSL_MASK_H	4Bh	Setting of the MASK_H register *1
R_HFDSL_MASK_L	36h	Setting of the MASK_L register *1

Note: 1. To change R_HFDSL_MASK_H and R_HFDSL_MASK_L, change processing of the hfdsl_int_isr_ch*n* (n=0 to 15) function in accord with the settings in the R_HFDSL_MASK_H and R_HFDSL_MASK_L.

Table 4.4 Error Codes

Constant Name	Setting	Description
R_HFDSL_SUCCESS	0	Normal termination
R_HFDSL_ERR_INVALID_ARG	-1	Argument error
R_HFDSL_ERR_ACCESS	-2	API execution order error
R_HFDSL_ERR_INIT	-3	Failure in initialization of the HFDSL controller and encoder

4.9 Fixed-width Integers

Table 4.5 lists the fixed-width integers for the sample code. The fixed-width integers used in the sample code are defined in the standard library.

Table 4.5 Fixed-width Integers for the Sample Code

Symbols	Description
int8_t	8-bit signed integer
int16_t	16-bit signed integer
int32_t	32-bit signed integer
int64_t	64-bit signed integer
uint8_t	8-bit unsigned integer
uint16_t	16-bit unsigned integer
uint32_t	32-bit unsigned integer
uint64_t	64-bit unsigned integer

4.10 Structures, Unions, and Enumerated Types

The major structures, unions, and enumerated types are listed below.

4.10.1 Structures

(1) r_hfdsl_info_t

Information on initialization of the HFDSL driver

```
typedef struct
{
    r_hfdsl_int_nml_cb_t    p_cb_nml;   Pointer to the callback function to be called when an
                                        HDSLn_FPR interrupt is generated.
                                        For details, see section “4.5.1, hfdsl_int_nml_callback”. *1 *2
    r_hfdsl_int_err_cb_t    p_cb_err;   Pointer to the callback function to be called when an
                                        HDSLn_INT interrupt is generated.
                                        For details, see section “4.5.2, hfdsl_int_err_callback”.  *1
} r_hfdsl_info_t
```

Note: 1. This function is not called if NULL is specified.
2. This function is not called when an HDSLn_INT interrupt is generated in response to the FREL bit in the EVENT_L register being set to 1.

(2) r_hfdsl_pos_t

For storing fast position

```
typedef struct
{
    bool                    all;        Enables the member variable posh.
                                        (true: The member variable posh is enabled,
                                         false: The member variable is disabled)
    uint8_t                 posh;       Holds bits [39:32] of the fast position.
                                        The value is updated when the member variable all is true.
    uint32_t                pos;        Holds bits [31:0] of the fast position.
} r_hfdsl_pos_t
```

(3) r_hfdsl_vpos_t

For storing the safe position

```
typedef struct
{
    uint8_t                 vposh;      Holds bits [39:32] of the safe position.
    uint32_t                vpos;       Holds bits [31:0] of the safe position.
    uint16_t                crc;        Holds the CRC of the vertical channel.
} r_hfdsl_vpos_t
```

(4) r_hfdsl_send_msg_t

For storing message data for transmission.

```
typedef struct
{
    uint8_t             *p_data;    Pointer to the array which holds message data for transmission
                                    Set the pointer to the array which holds message data for
                                    transmission.
    r_hfdsl_msg_cb_t    p_cb_msg;   Pointer to the callback function to be called when a message is
                                    received.
                                    For details, see section “4.5.3, hfdsl_int_mrcv_callback”.
                                    Be sure to set the address of hfdsl_int_mrcv_callback.
} r_hfdsl_send_msg_t
```

4.10.2 Unions

Not used.

4.10.3 Enumerated Types

Not used.

4.11 Description of the Sample Program

4.11.1 Outline of Operations

This sample program supports the encoder (EFM50-0KF0A023A from SICK AG) compliant with the HIPERFACE DSL communications protocols specification. It handles the following processing.

1) Indicates the following information by using a command input from the console.
   A) Fast and safe positions
   B) Rotational velocity of the motor
   C) Results of transmission and reception of long messages (the type of the encoder from resources)
2) Runs in SYNC mode.
3) This sample program ends by detecting a protocol reset.

(1) System Block Diagram

Figure 4.1 shows a block diagram of the system.

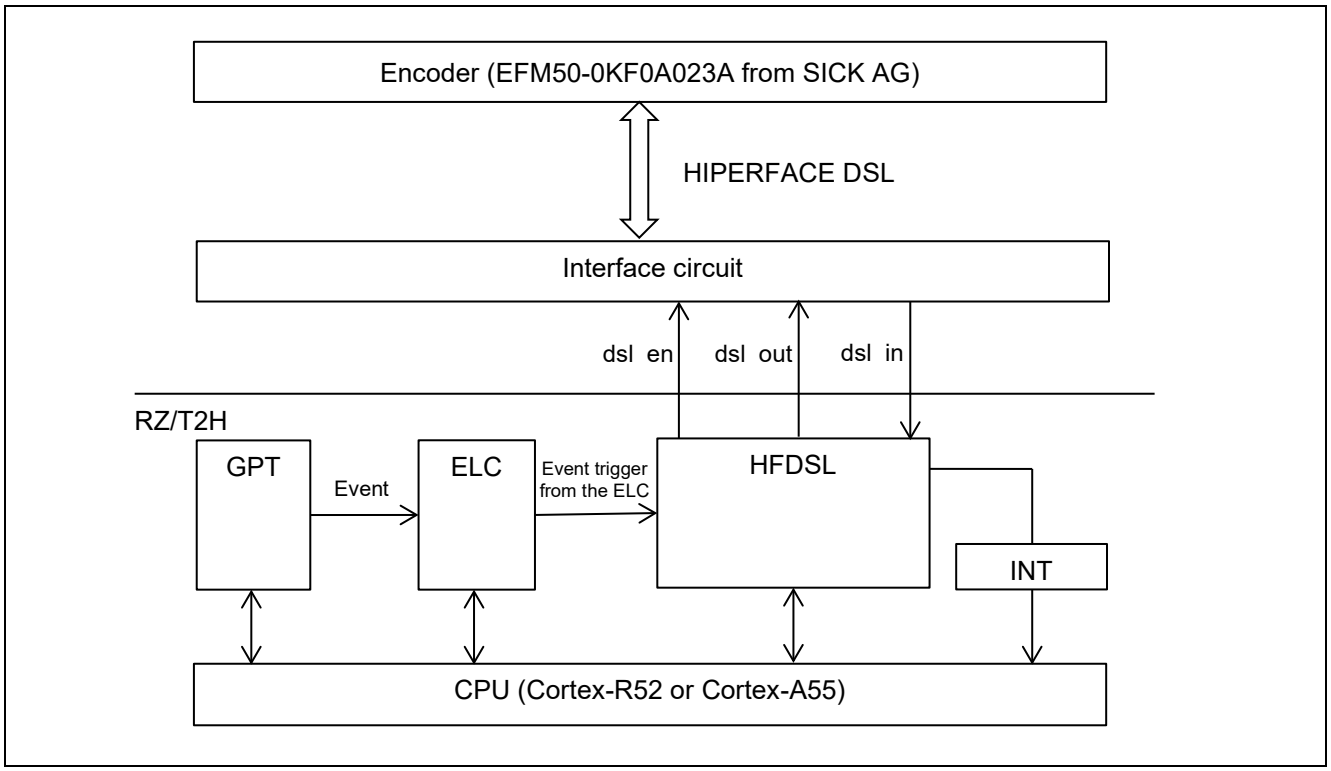

Figure 4.1 System Block Diagram

(2) Software Configuration

Figure 4.2 is a block diagram of the software.

The HFDSL driver has six sections: the opening process part configured of function R_HFDSL_Open, the closing process part configured of function R_HFDSL_Close, the protocol initialization, positional value acquisition, and message transmission parts configured of function R_HFDSL_Control, and the data reception part (interrupt handler) configured of the callback function.

The HFDSL driver controller section of the sample program controls the HFDSL driver, acquires the positional value, and sends messages. The results indication section (callback) displays the results of data reception.

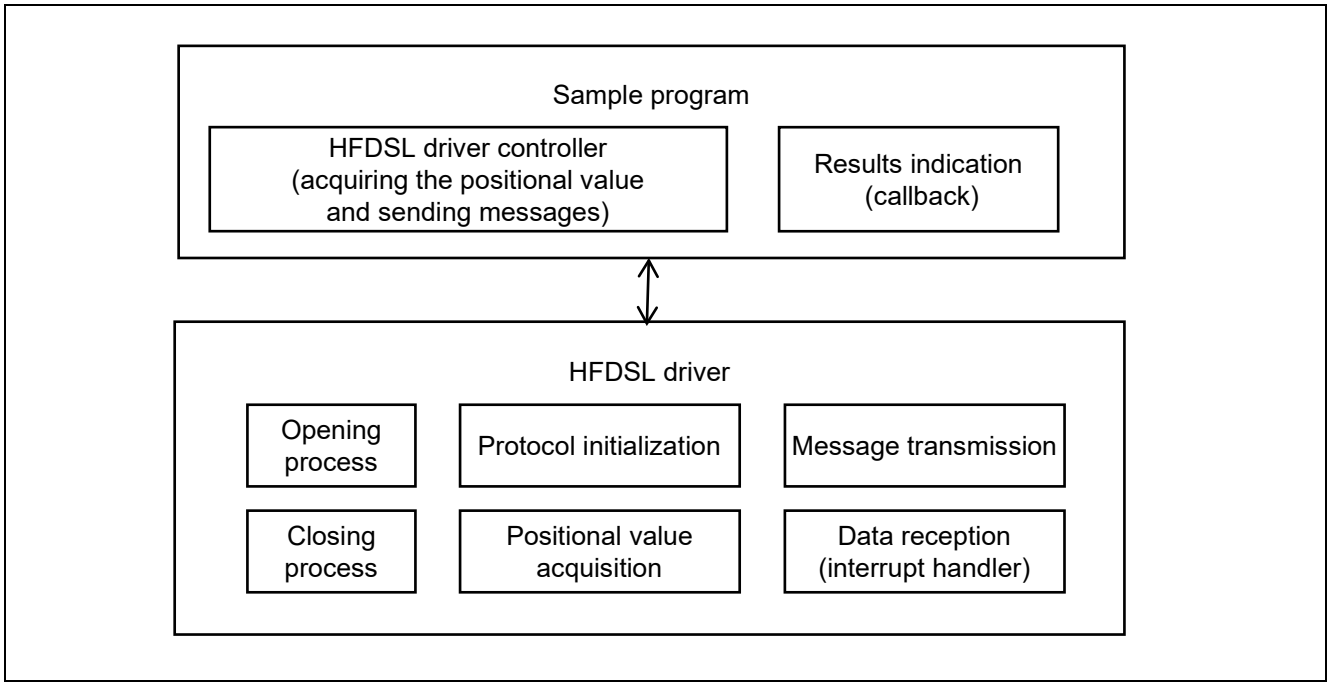

Figure 4.2 Software Configuration

4.11.2 Variables for the Sample Program

Table 4.6 lists the major static variables.

Table 4.6 Major Static Variables

Type	Variable Name	Description
bool	mrcv_flg	Message transfer completed flag (true: Transfer of messages has been completed false: Transfer of messages is in progress)
bool	prst_found	Protocol reset warning detection flag (true: Protocol reset warning is detected false: Protocol reset warning is not detected)
uint32_t	err_info	Holds the HDSLn_INT interrupt source.
uint32_t	pos_rot	Holds the number of rotations with the fast position.
uint32_t	pos_res	Holds the angle of the fast position.
uint32_t	vpos_rot	Holds the number of rotations with the safe positions.
uint32_t	vpos_res	Holds the angle of the safe position.
uint32_t	vel	Holds the rotational velocity of the motor.
uint8_t	lmsg_recv[LMSG_RECV_SIZE]	Holds received data in long messages.

4.11.3 Constants for the Sample Program

Table 4.7 lists the major constants for the sample program.

Table 4.7 Major Constants

Constant Name	Setting	Description
ENC_ID	00000183h	Encoder ID of EFM50-0KF0A023A *1 *2
RES_BIT	0	Position of the least significant bit of the positional information in the POS4 to 0 registers *1
RES_MASK	007FFFFFh	Masking of the positional information in the POS3 to 0 registers *1
RES_MASK_H	00000000h	Masking of the positional information in the POS4 register *1
ROT_BIT	23	Position of the least significant bit of the rotational information in the POS4 to 0 registers *1
ROT_MASK	000001FFh	Masking of the number of rotations in the POS3 to 0 registers *1
ROT_MASK_H	00000E00h	Masking of the number of rotations in the POS4 register *1
LMSG_RECV_SIZE	10	Maximum size of received data in long messages
TIMEOUT_UNIT	1000	Setting of timeout unit (1 ms)
TIMEOUT_COUNT	1000	Setting of timeout (1 ms x 1000)
INIT_RETRY_COUNT	10	Retry times of initialization error

Note: 1. To run the sample program with an encoder other than an EFM50-0KF0A023A, change the settings to suit the specifications of the connected encoder.
2. Refer to the “HIPERFACE DSL® MASTER Integration Manual” for details.

The figure below shows the mechanism for storing the positional and rotational information.

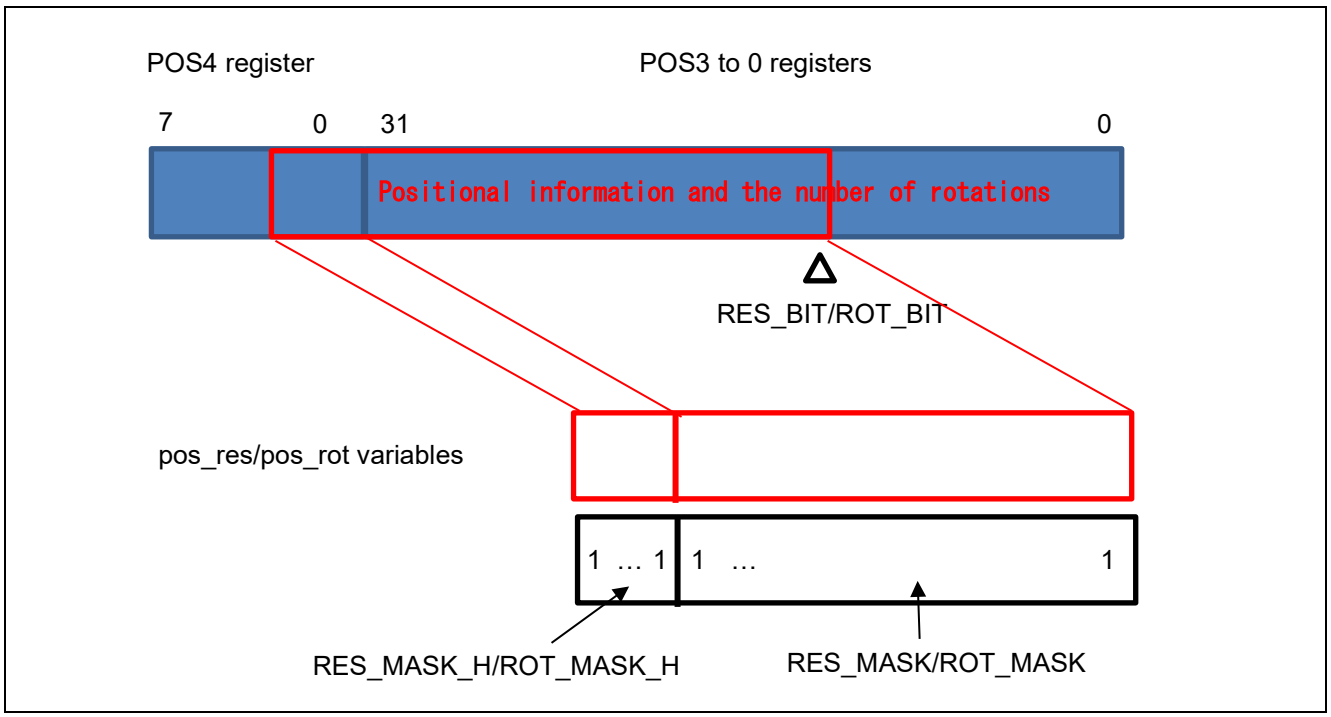

Figure 4.3 Mechanism for Storing the Positional and Rotational Information

4.11.4 Flowchart of Main Processing

The flowchart below shows processing by the main function.

Processing marked with * in the figure is shown separately in a subsequent flowchart.

(1) Flowchart of enc_main

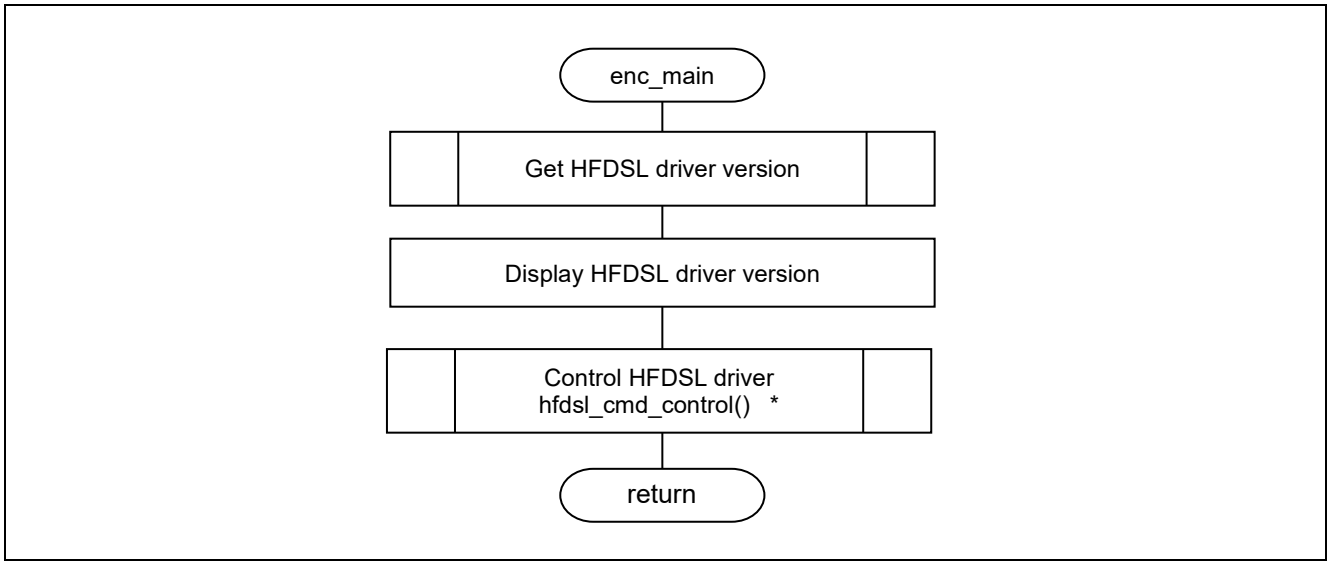

Figure 4.4 Flowchart of the enc_main Function

(2) Flowchart of hfdsl_cmd_control

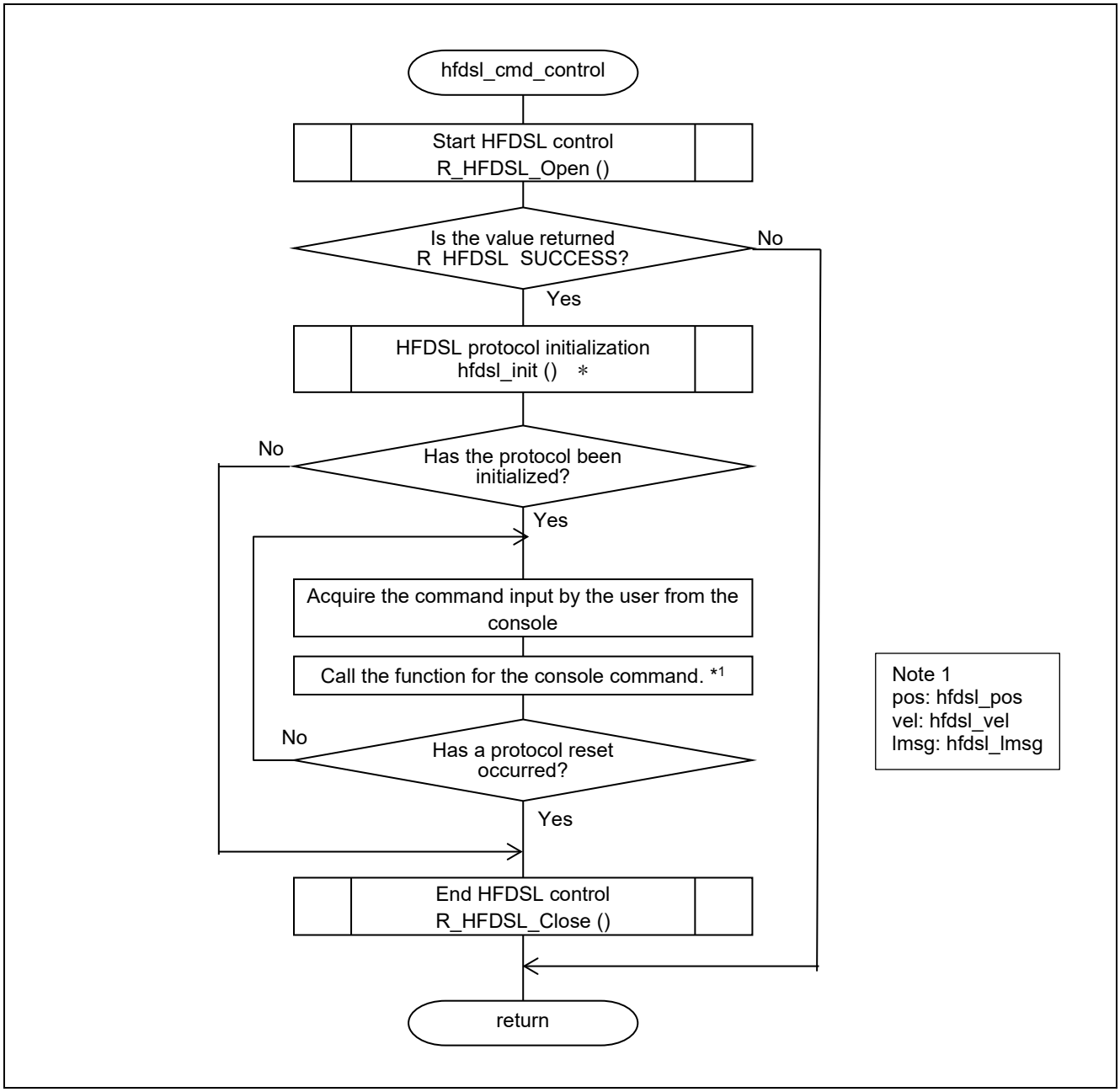

Figure 4.5 Flowchart of the hfdsl_cmd_control

(3) Flowchart of hfdsl_init

This function initializes the protocol.

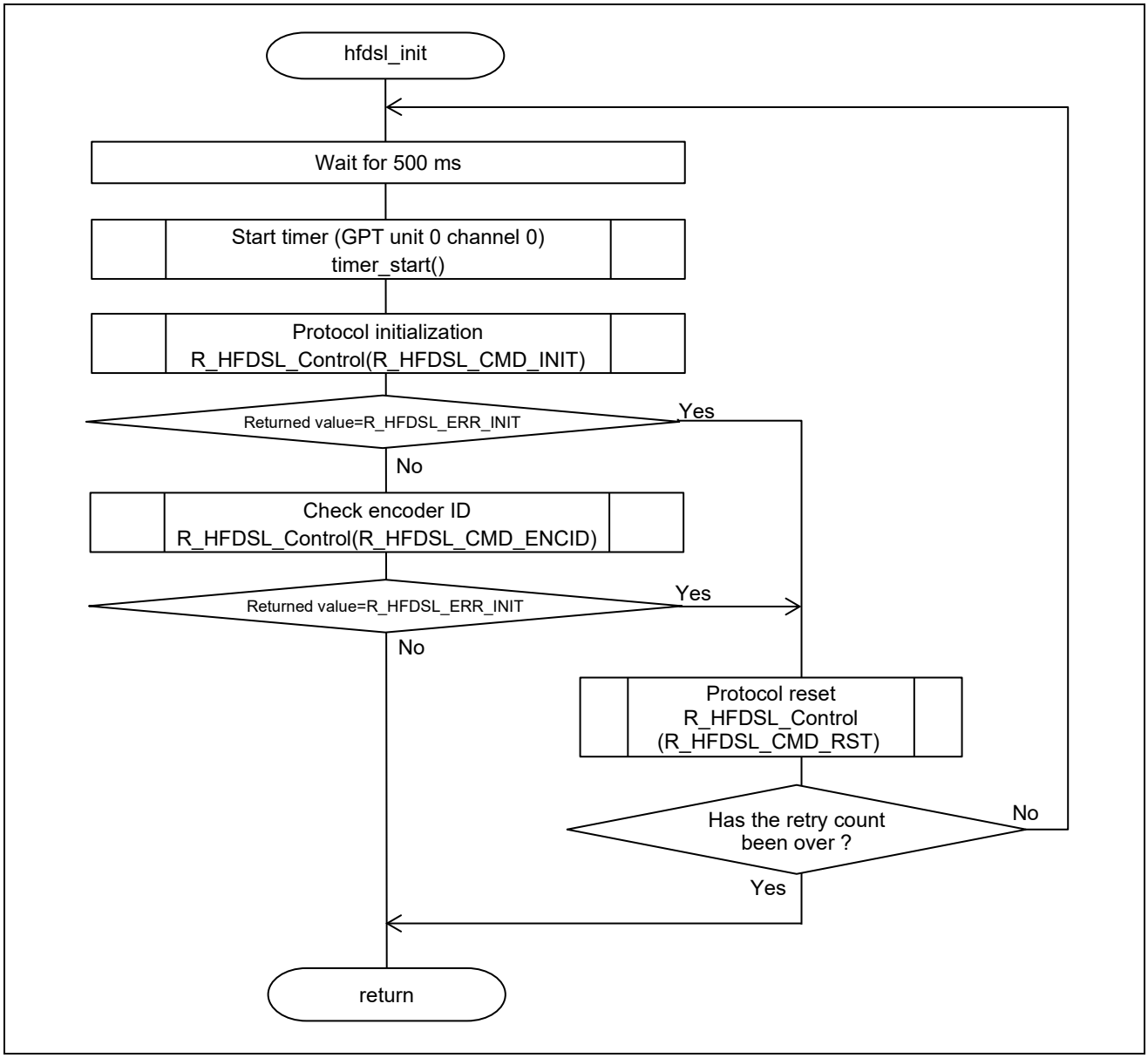

Figure 4.6 Flowchart of the hfdsl_init

(4) Flowchart of hfdsl_pos, hfdsl_vel

These functions are executed in response to input of the console commands “pos” and “vel”, and indicate the acquired data. The functions corresponding to the respective console commands and details of the items displayed are below.

Table 4.8 Functions Corresponding to the Console Commands “pos”, “vel”

Console Command	Corresponding Function	Items Displayed
pos	hfdsl_pos	pos_rot, pos_res vpos_rot, vpos_res err_info
vel	hfdsl_vel	vel, err_info

Since the procedures for processing of the hfdsl_pos and hfdsl_vel functions are similar, they are shown in the same flowchart.

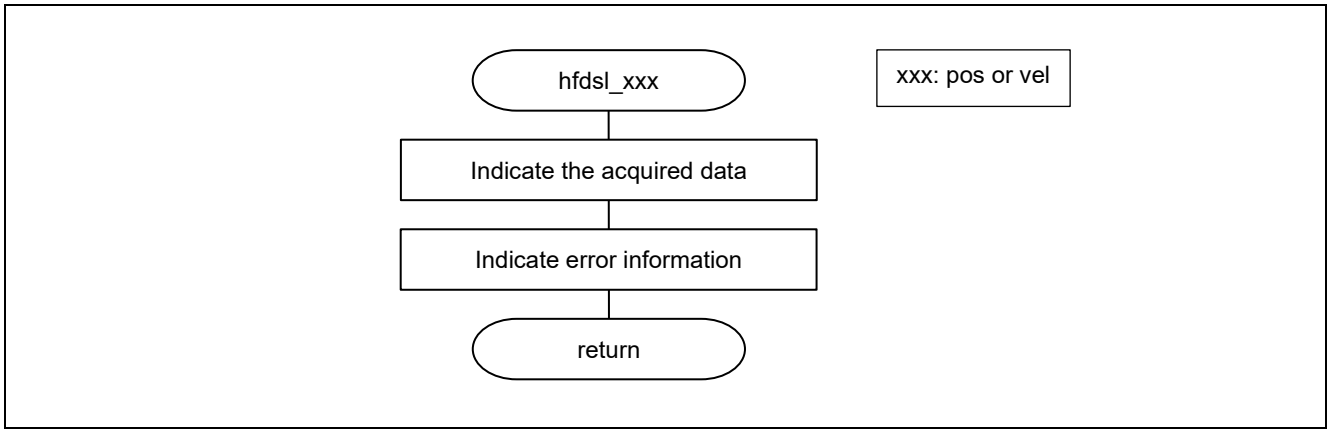

Figure 4.7 Flowchart of the hfdsl_pos, hfdsl_vel

(5) Flowchart of hfdsl_lmsg

This function is executed in response to input of the console command “lmsg”.

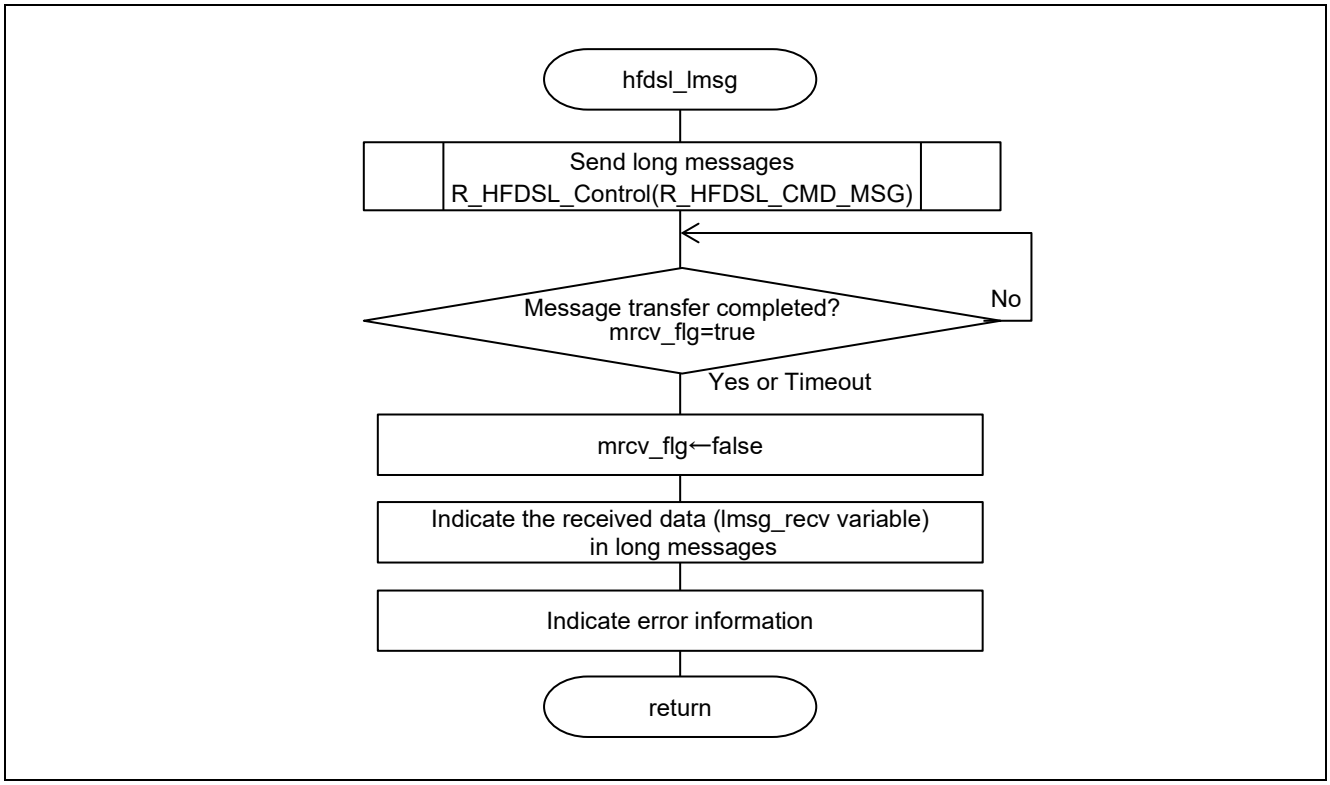

Figure 4.8 Flowchart of the hfdsl_lmsg

(6) Flowchart of hfdsl_int_nml_callback

This callback function is called in response to generation of an HDSLn_FPR interrupt.

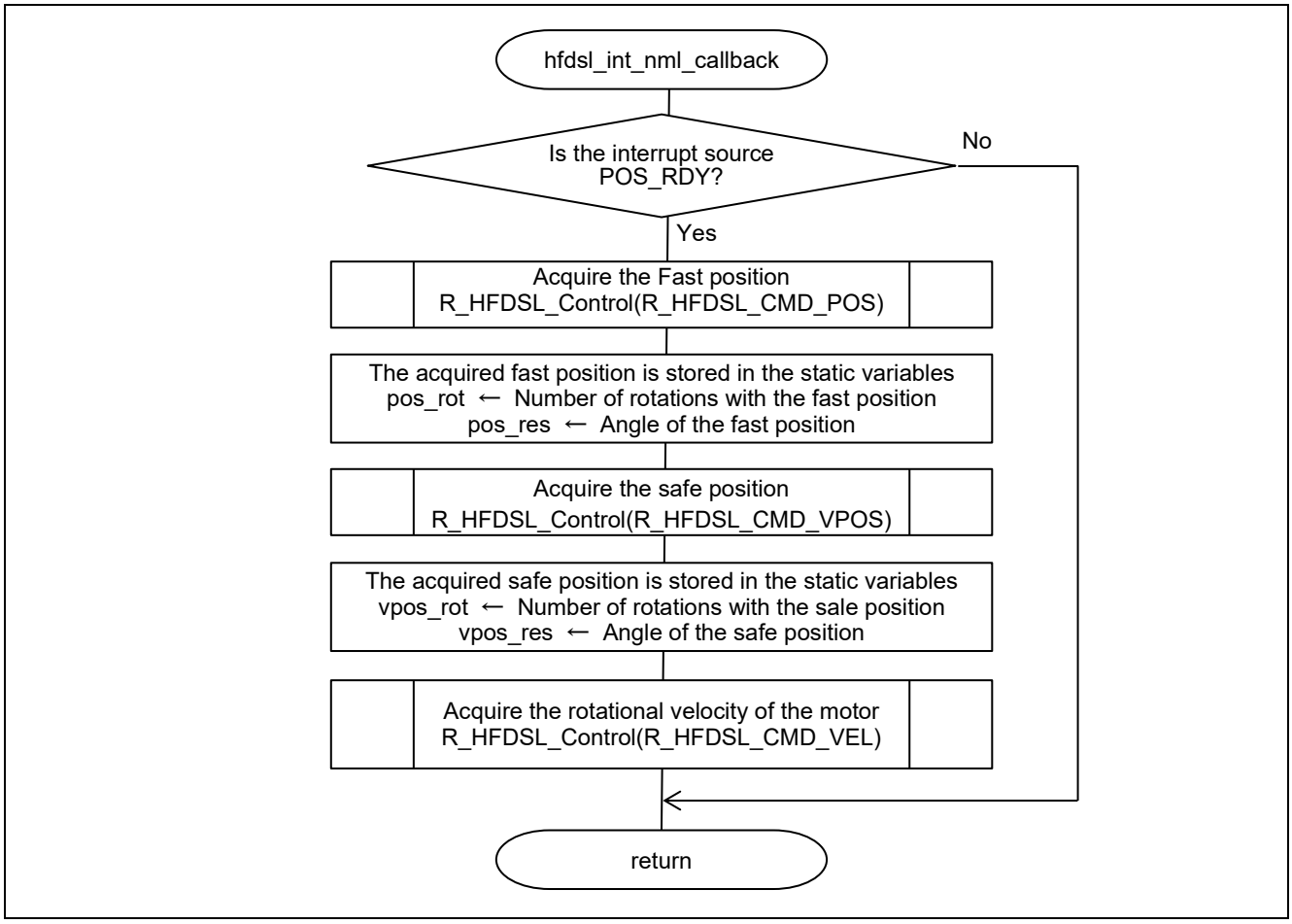

Figure 4.9 Flowchart of the hfdsl_int_nml_callback

(7) Flowchart of hfdsl_int_err_callback

This callback function is called in response to generation of an HDSLn_INT interrupt.

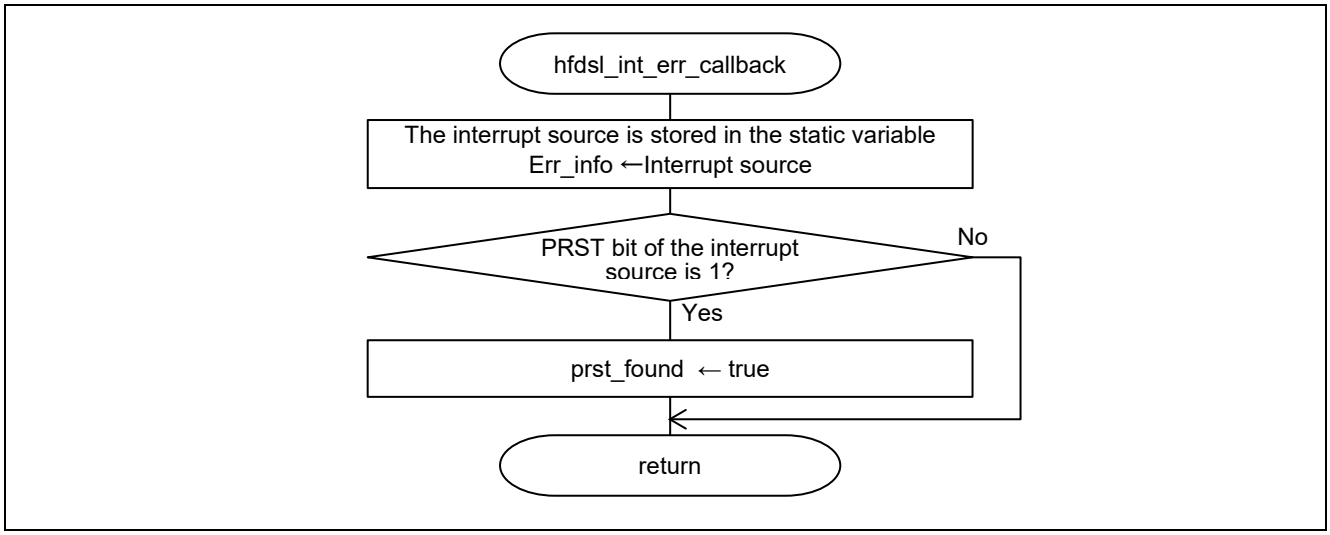

Figure 4.10 Flowchart of the hfdsl_int_err_callback

(8) Flowchart of hfdsl_int_mrcv_callback

This callback function is called when the HDSLn_INT interrupt by the FREL bit in the EVENT_L register occurs and data storage of the received message is completed.

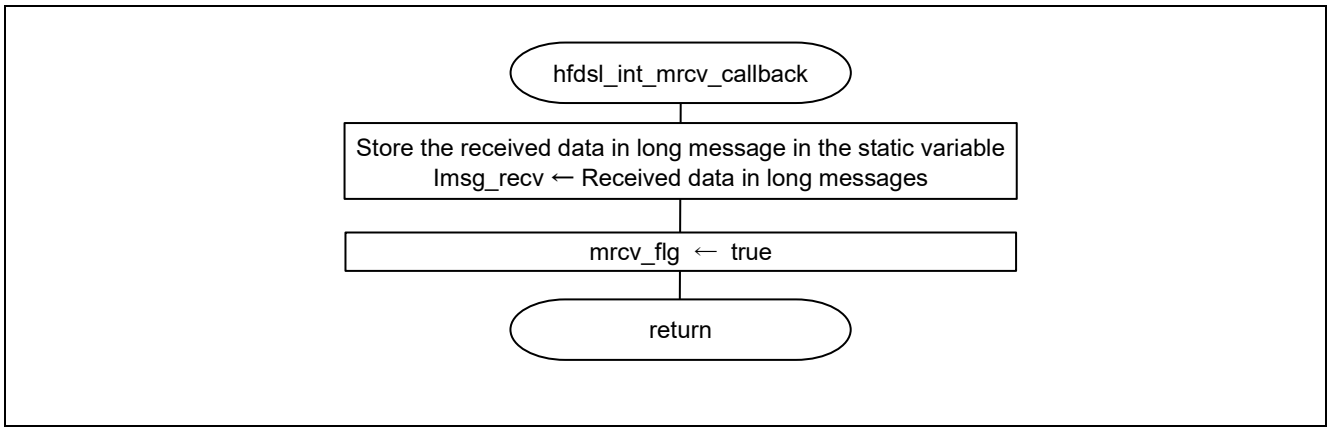

Figure 4.11 Flowchart of the hfdsl_int_mrcv_callback

4.11.5 Operation Sequence

(1) Startup Sequence

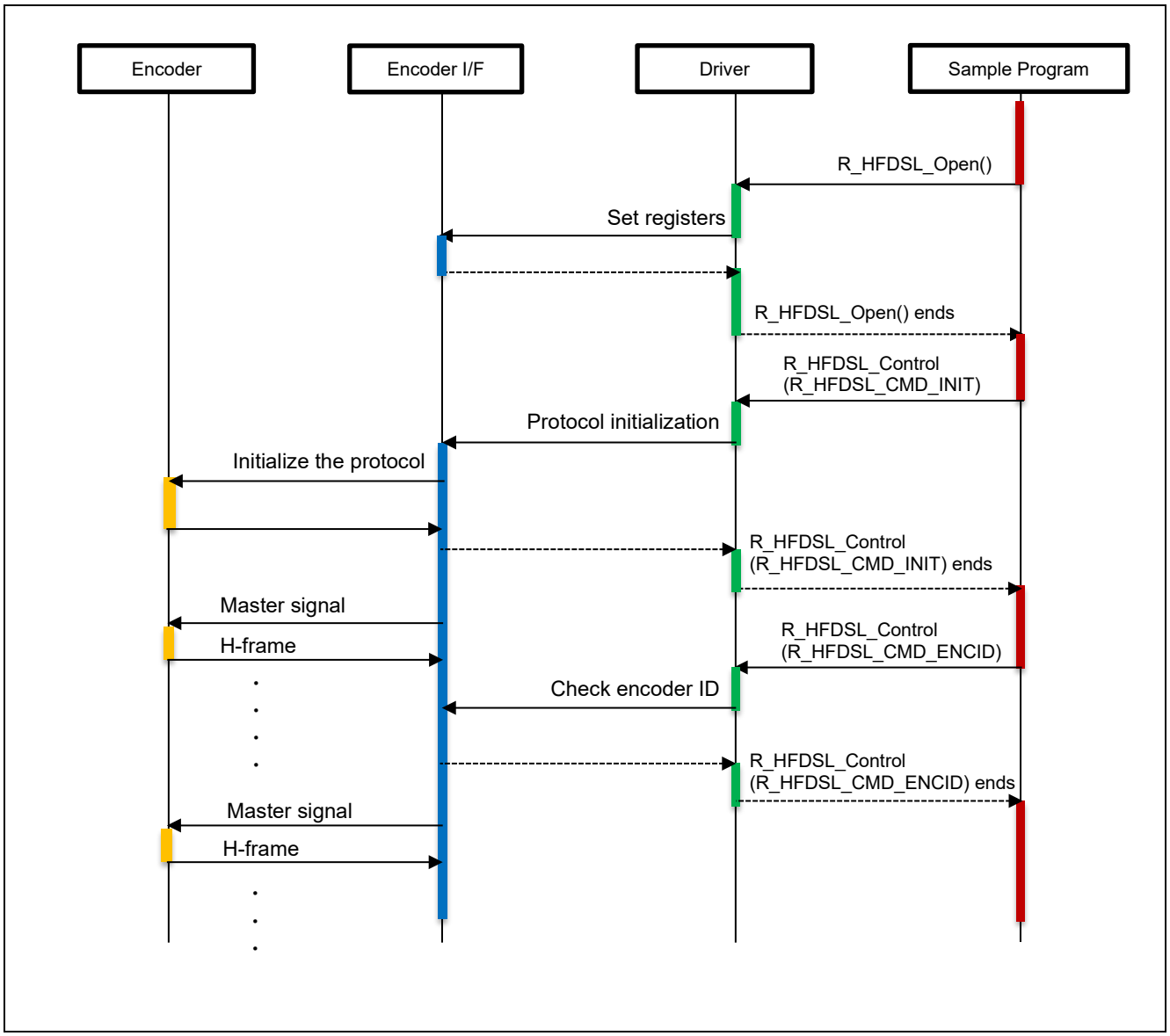

Figure 4.12 Startup Sequence Diagram

(2) Fast Position in SYNC Mode Acquisition Sequence

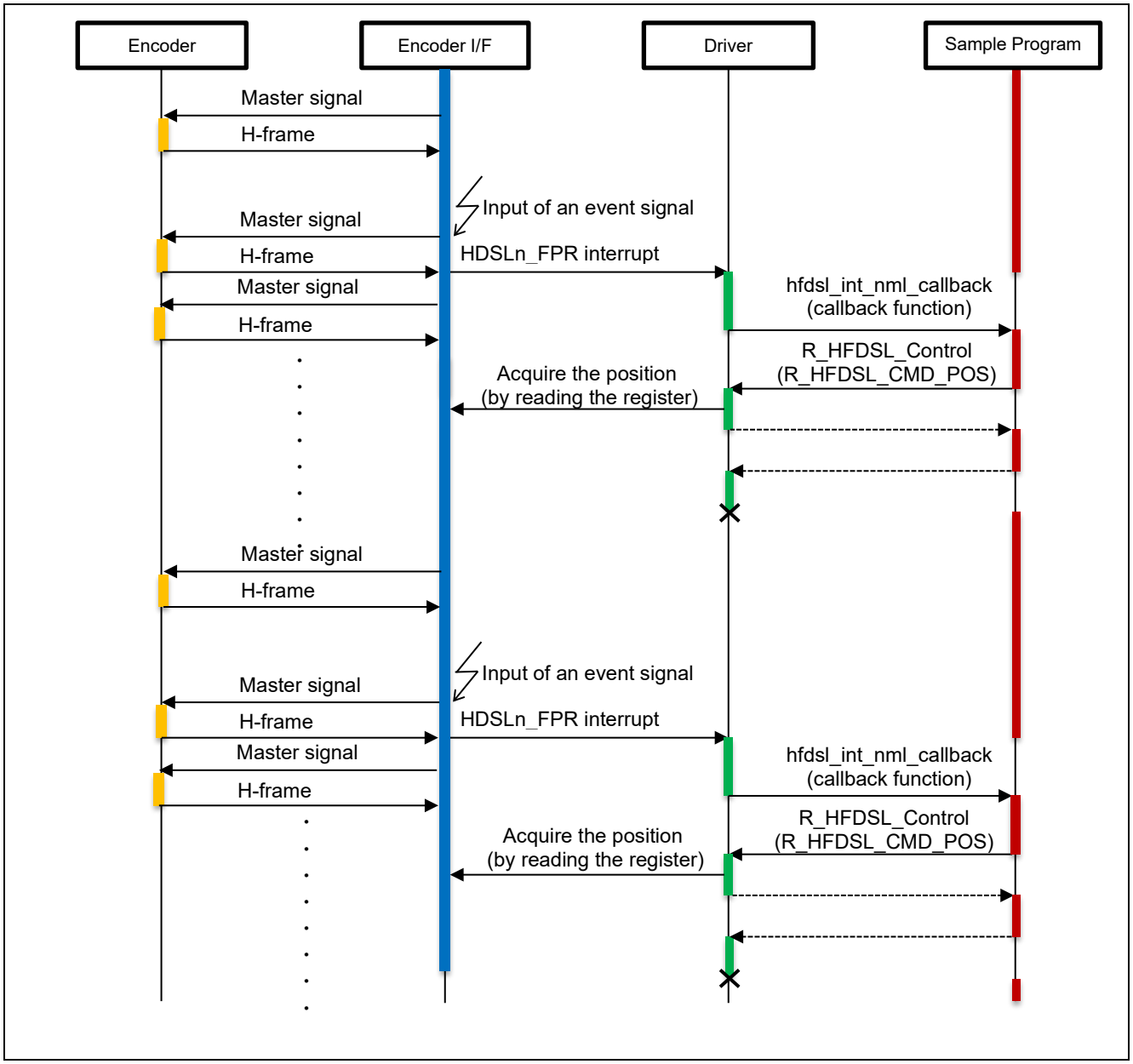

Figure 4.13 Fast Position in SYNC Mode Acquisition Sequence Diagram

(3) Message Transfer Sequence

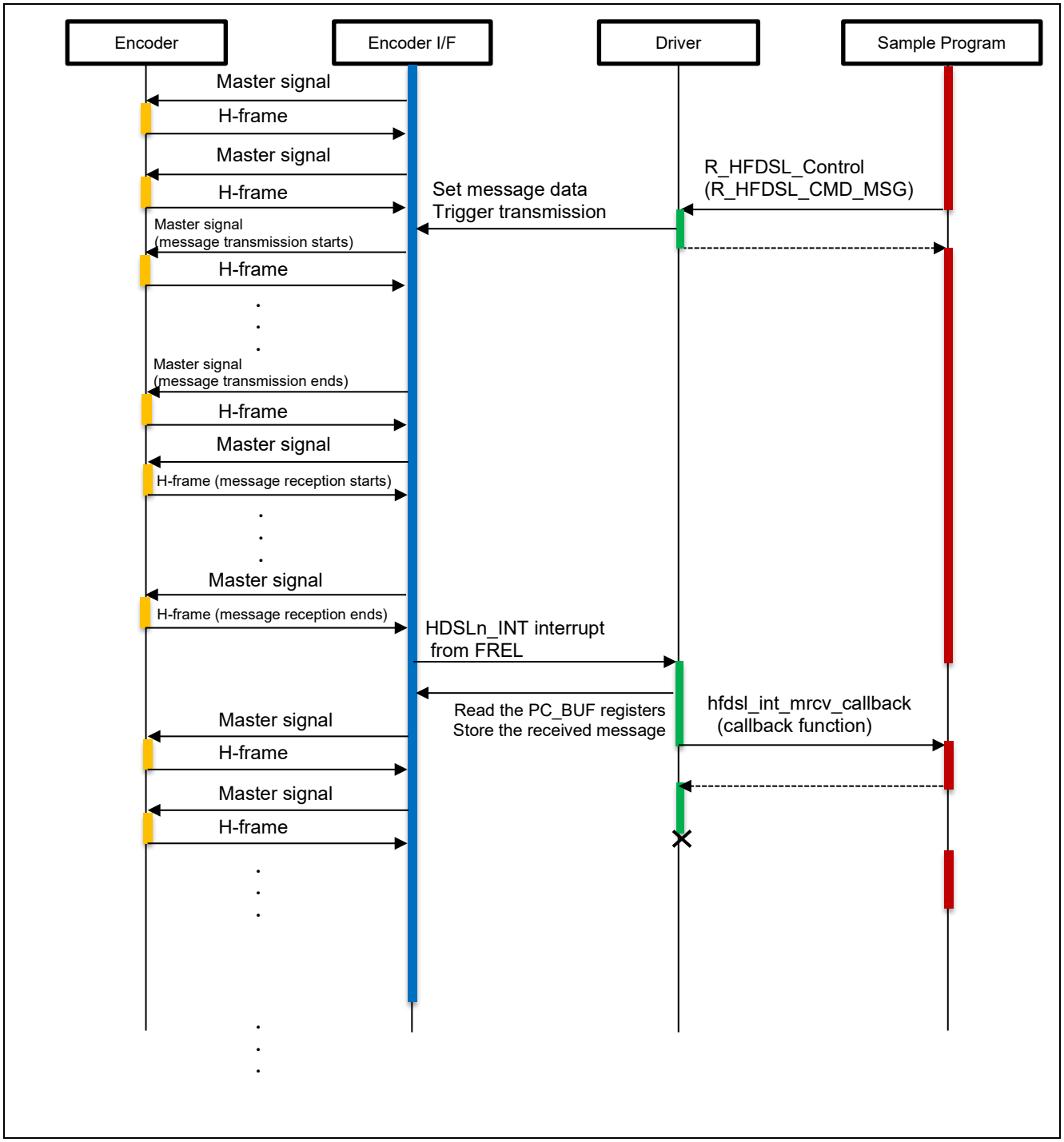

Figure 4.14 Message Transfer Sequence Diagram

(4) Stop Sequence

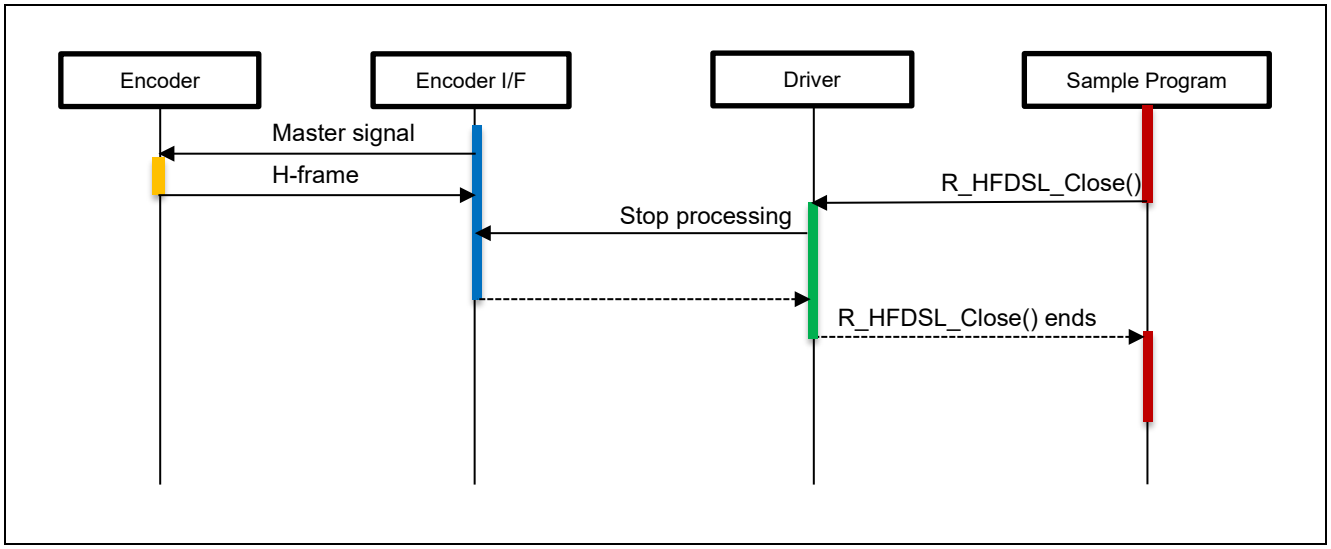

Figure 4.15 Stop Sequence Diagram

4.11.6 Console Commands

The commands available for input from the console are listed below.

Table 4.9 Console Commands

Command	Description
pos	Indicates the fast and safe positions
vel	Indicates the rotational velocity of the motor.
lmsg	Among the encoder resources, acquire the type of encoder as a long message.

(1) Result of Running

After running, it will display the command prompt following the version. Enter the command after “hfdsl >”.

```
HFDSL sample program start
R_HFDSL_GetVersion = 4.0


hfdsl >
```

(2) Example of Command Execution

It is an example of executing pos command. Fast position, Safe position and Error information are reported as the response from the encoder.

```
hfdsl >pos
Fast position
    Rotations   : 0x00000997
    Angle       : 0x00028AF4
Safe position
    Rotations   : 0x00000997
    Angle       : 0x00028AF4
Error information
    EVENT_EER   : 0x00000000
```

5. Sample Code

The sample code can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
0.50	Sep.29.23	-	First Edition issued.
0.60	Feb.22.24	-	Added operation with Cortex-A55.
2.00	Nov.21.24	3 19 22 22 28 34	Update table 1.1 by supporting ELC (Event link controller). Update table 4.3 by supporting ELC. Update 4.11.1 Outline of Operations by supporting SYNC mode. Figure 4.1 Add GPT and ELC. Figure 4.6 Add Start timer (GPT unit 0 channel 0) to hfdsl_init. Figure 4.13 Add Input of an event signal.
3.00	Aug 20.25	1, 3, 4 3, 24	Change description for trademarks. Update notes of HIPERFACE DSL MASTER Integration Manual. Revise to unify description for functions.
4.00	Apr 24.26	4 8 to 14, 19, 20 13, 14 24	Change frequency of the Cortex-A55 Core0 to 1200MHz. Change prefix of pointer variables to “p_”. Revise header column of the specifications of user-defined functions. Correct variable name of position in fig. 4.3.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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