RZ/T2, **RZ/N2**

Quick Start Guide: Renesas PROFINET IRT DEVKIT

Introduction

This document describes the setup procedure of the sample program for RZ/T2M, RZ/N2L of PROFINET.

Target Device

RZ/T series: RZ/T2M RZ/N series: RZ/N2L

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1. Overview

This document describes the setup procedure of the sample program for RZ/T2M, RZ/N2L of PROFINET and explains the procedure for connecting the CODESYS software programmable logic controller (PLC) and Siemens PLC.

For demonstration, this application includes standard I/O and PROFIdrive operations. This document explains the procedure for writing application firmware and connecting to the PLC.

1.1 Abbreviations / Definitions

Table 1-1 Abbreviations/Definitions

Index	Abbreviations/Definitions	Description
1	IP	Internet Protocol
3	USB	Universal Serial Bus
4	PC	Personal Computer
5	SW	Switch
6	RSK+	Renesas Starter Kit+
7	l-jet	IAR debug probe
8	J-Link	SEGGER debug probe
9	J-Link OB	SEGGER On-board debug probe

1.2 Reference

1.2.1 About RZ/T2M and RZ/N2L

Technical information about RZ/T2M and RZ/N2L is available via Renesas.

Table 1-2 Technical Inputs for RZ/T2M

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+RZT2M hardware.	Renesas Starter Kit+ for RZ/T2M User's Manual	<u>r20ut4939eg****</u>
User's Manual	Provides technical details of the RZ/T2M microprocessor.	RZ/T2M Group User's Manual Hardware	<u>r01uh0916eg****</u>

Table 1-3 Technical Inputs for RZ/N2L

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+RZN2L hardware.	Renesas Starter Kit+ for RZ/N2L User's Manual	r20ut4984eg****
User's Manual	Provides technical details of the RZ/N2L microprocessor.	RZ/N2L Group User's Manual Hardware	<u>r01uh0955eg****</u>

1.2.2 About the API for user applications of the PROFINET stack

For more information about the API for user applications of the PROFINET stack, please refer to Chapter 4 "Interface description" in the document linked below.

Interface description PROFINET IO Development Kits V4.7.0 10/2020

1.2.3 About the PROFIdrive application

For more information about the PROFIdrive application, please refer to the document at the link below.

PROFIDrive Application Example AC4.pdf



2. Features

This package includes the firmware for the PROFINET stack on Renesas' RZ/T and RZ/N series processors.

The package includes the following firmware:

- Standard Application firmware encompasses essential features required in industrial equipment communication, including PROFINET RT (Real-Time) and IRT (Isochronous Real-Time) communication.
- PROFIdrive Application firmware includes a certified PROFIdrive application example implemented in compliance with Application Class 4 and 1.
- PROFIsafe firmware includes safety communication functionality using the Functional Safety Reference Board.

2.1 Package folder structure

The folder structure of the sample application is shown in Table 2-1 Folder structure.

Folders	Files	Descriptions
/	Renesas PROFINET IRT DEVKIT -	This is the sample software license
	SOFTWARE LICENSE AGREEMENT.txt	agreement.
/	r01an7819ej0110-rzt2-n2-profinet.pdf	This guide explains the procedure for the
		demo.
/ Document / Release Note	Change_Log.pdf	This document is the change log of the
/ Change Log		sample program.
/ Document / Release Note	Feature_list.pdf	This document is the list of sample
/ Feature List		program features.
/ Firmware	Renesas_PROFINET_IRT_DEVKIT_	This is the installer for the sample program.
	V1.10.0.exe	
/ GSDML / RZT2M	GSDML-02C7-0003-RZT2-RSK.bmp	Bitmap used in the GSDML files
	GSDML-V2.43-RENESAS-RZT2-	GSDML file for RZ/T2M Standard
	VSC8541-20250516.xml	Application
/ GSDML / RZN2L	GSDML-02C7-0003-RZN2-RSK.bmp	Bitmap used in the GSDML files
	GSDML-V2.43-RENESAS-RZN2-	GSDML file for RZ/N2L Standard
	VSC8541-20250516.xml	Application
/ PLC_Project / CODESYS	RZT2M_PROFINET_Sample_	CODESYS project for RZ/T2M Standard
	App1_STANDARD.projectarchive	Application
	RZT2M_PROFINET_Sample_	CODESYS project for RZ/T2M PROFIdrive
	PROFIdrive_AC1_App.projectarchive	Application
	RZN2L_PROFINET_Sample_	CODESYS project for RZ/N2L Standard
	App1_STANDARD.projectarchive	Application
	RZN2L_PROFINET_Sample_	CODESYS project for RZ/N2L PROFIdrive
	PROFIdrive_AC1_App.projectarchive	Application
/ PLC_Project / TIA_Portal	RZT2M_PROFINET_RT_Sample_	TIA Portal project for RT communication of
	App1_STANDARD.zap18	RZ/T2M Standard Application
	RZT2M_PROFINET_IRT_Sample_	TIA Portal project for IRT communication of
	App1_STANDARD.zap18	RZ/T2M Standard Application
	RZT2M_PROFINET_RT_Sample_	TIA Portal project for RT communication of
	PROFIdrive_AC1_App.zap18	RZ/T2M PROFIdrive AC1 Application
	RZT2M_PROFINET_IRT_Sample_	TIA Portal project for IRT communication of
	PROFIdrive_AC4_App.zap18	RZ/T2M PROFIdrive AC4 Application
	RZT2M_PROFINET_RT_Sample_App5_	TIA Portal project for RT communication of
	FAILSAFE_PSD.zap18	RZ/T2M PROFIsafe Application
	RZT2M_PROFINET_IRT_Sample_App5	TIA Portal project for IRT communication of
	_FAILSAFE_PSD.zap18	RZ/T2M PROFIsafe Application
	RZN2L_PROFINET_RT_Sample_	TIA Portal project for RT communication of
	App1 STANDARD.zap18	RZ/N2L Standard Application

Table 2-1 Folder structure



RZN2L_PROFINET_IRT_Sample_	TIA Portal project for IRT communication of
App1_STANDARD.zap18	RZ/ N2L Standard Application
RZN2L_PROFINET_RT_Sample_	TIA Portal project for RT communication of
PROFIdrive_AC1_App.zap18	RZ/N2L PROFIdrive AC1 Application
RZN2L_PROFINET_IRT_Sample_	TIA Portal project for IRT communication of
PROFIdrive_AC4_App.zap18	RZ/N2L PROFIdrive AC4 Application
RZN2L_PROFINET_RT_Sample_App5_	TIA Portal project for RT communication of
FAILSAFE_PSD.zap18	RZ/T2M PROFIsafe Application
RZN2L_PROFINET_IRT_Sample_App5_	TIA Portal project for IRT communication of
FAILSAFE_PSD.zap18	RZ/T2M PROFIsafe Application

3. Requirements

This RZ/T2M, RZ/N2L project has been developed and tested on these environments using the following boards and tools.

Table 3-1 RZ/T2M Requirements

Item	Vender	Description
Board	Renesas Electronics	RZ/T2M RSK Board
		RTK9RZT2M0S00000BE
		(Built in J-Link OB)
IDE	IAR Systems	Embedded Workbench® for ARM Version 9.50.1
	Renesas Electronics	e ² studio 2024-01.1
		FSP Smart Configurator 2024-01.1
		RZ/T Flexible Software Package (FSP) v2.0.0
		Please download from the link below.
		https://github.com/renesas/rzt-fsp/releases/tag/v2.0.0
Utility tool	IAR Systems	I-jet
	SEGGER	J-Link

Table 3-2 RZ/N2L Requirements

Item	Vender	Description
Board	Renesas Electronics	RZ/N2L RSK Board
		RTK9RZN2L0S00000BE
		(Built in J-Link OB)
IDE	IAR Systems	Embedded Workbench® for ARM Version 9.50.1
	Renesas Electronics	e² studio 2024-01
		FSP Smart Configurator 2024-01
		RZ/N Flexible Software Package (FSP) v2.0.0
		Please download from the link below.
		https://github.com/renesas/rzn-fsp/releases/tag/v2.0.0
Utility tools	IAR Systems	l-jet
	SEGGER	J-Link



 Table 3-3 Common Requirements

Item	Vender	Description
Evaluation Software	CODESYS GmbH	CODESYS v3.5 SP20 64-bit or later
	Siemens	TIA portal V18 or later
Evaluation Hardware	Siemens	SIMATIC S7-1500 6ES7 516-3AN02-0AB0
PROFIsafe Evaluation	Siemens	SIMATIC S7-1500 6ES7 516-3FN02-0AB0
		PROFIsafe Driver V2.2.3 for F-Slaves
	Renesas Electronics	RZ/T2L Safety Network Reference Kit

4. Hardware Setup

4.1 RZ/T2M RSK Board

4.1.1 Jumper and Switch configuration

This document describes the major hardware. Refer to Renesas Stater Kit+ for RZ/T2M user's manual and schematic for more board details.



Figure 4-1 RZ/T2M RSK board layout



Table 4-1 Jumper pin settings

Reference	Jumper Position	Description
CN8	Shorted Pin 2-3	Enable QSPI (IC21).
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2.
		(When using SDRAM)
CN18	Shorted Pin 1-2	When using 3 ports in the same PHY mode
CN19	Shorted Pin 1-2	When using 3 ports in the same PHY mode
CN20	Open	Not use Ethernet port2.
J9	Open	Enable the J-Link® OB.

Table 4-2 SW4 Settings

SW4	Setting	Description
SW4-1	ON	xSPI0 boot mode (x1 boot serial flash)
SW4-2	ON	
SW4-3	ON	
SW4-4	ON	JTAG Authentication by Hash is disabled.
SW4-5	OFF	ATCM 1 wait

Table 4-3 SW5 Settings

SW5	Setting	Description
SW5-3	ON	Enable SCI_RTS
SW5-4	OFF	
SW5-5	ON	Enable SCI_RXD
SW5-6	OFF	
SW5-7	OFF	
SW5-8	OFF	Enable SCK3
SW5-9	ON	
SW5-10	OFF	

Table 4-4 SW6 Settings

SW6	Setting	Description
SW6-1	ON	Enables the external bus signal
SW6-3	ON	Enable TRACE_CTL
SW6-4	OFF	
SW6-5	OFF	Enable SCI_TXD
SW6-6	ON	
SW6-7	OFF	Enable MB_RST
SW6-8	ON	
SW6-9	OFF	Enable CAN_RX_OB
SW6-10	ON	

Other SW settings refer to r20ut4939egxxxx-rskplus-rzt2m-v1-um.pdf.



4.1.2 Setup RZ/T2M RSK Board

Setting the board for running sample program is shown below.

- 1. Connect an emulator.
 - When you use I-jet or J-Link emulator, connect it to J20 on RZ/T2M RSK board.
 - When you use J-Link On-Board emulator, connect USB micro-B to J10 on RZ/T2M RSK board. (Please disconnect J9 for powering up J-Link OB.



Figure 4-2 Setup RZ/T2M RSK board

- 2. Connect to a USB serial port.
 - Connect the USB cable (Type-A to type Mini B) to the USB connector "CN16" on the RZ/T2M RSK board.
- 3. Power is supplied using USB cable (Type-C) or AC / DC adapter.
 - When using USB cable (Type-C), connect it to the USB connector "CN5" on the RZ/T2M RSK board.
 - When using AC/DC adapter, connect it to the connector "CN6" on the RZ/T2M RSK board.
- 4. Connect Ethernet Cable to the Ethernet Connector "ETH0".



4.2 RZ/N2L RSK Board

4.2.1 Jumper and Switch configuration

This document describes the major hardware. Refer to Renesas Stater Kit+ for RZ/N2L user's manual and schematic for more board details.



Figure 4-3 RZ/N2L RSK board layout

Table 4-5 Jumper pin settings

Reference	Jumper Position	Description			
CN8	Shorted Pin 2-3	Enable QSPI (IC21).			
CN17	Shorted Pin 1-2	Connect 3.3V Power rail to VCC1833_2.			
		(When using an external bus etc.)			
CN20	Shorted Pin 2-3	When ports 0 and 1 use the same PHY mode and port 2			
CN21	Shorted Pin 2-3	uses different PHY modes			
CN22	Shorted Pin 2-3				
CN24	Shorted Pin 2-3	Connect 1.8V Power rail to VCC1833_3.			
		(When using QSPI Flash IC21)			
J9	Open	Enable the J-Link® OB.			



Table 4-6 SW4 Settings

SW4	Setting	Description
SW4-1	ON	xSPI0 boot mode (x1 boot serial flash)
SW4-2	ON	
SW4-3	ON	
SW4-4	ON	JTAG Authentication by Hash is disabled.
SW4-6	OFF	Enables signals other than the trace signal.
		(Motor, RS485, etc.)
SW4-7	OFF	Enable the external bus signal.
SW4-8	OFF	Enable SW3.

Table 4-7 SW8 Settings

SW5	Setting	Description
SW8-1	OFF	Enable the "LED_GREEN" signal.
SW8-2	ON	
SW8-3	OFF	
SW8-4	ON	Enable the "LED5" signal.
SW8-5	OFF	

Table 4-8 SW11 Settings

SW6	Setting	Description
SW11-1	ON	Enable the " LED_RED2" signal.
SW11-2	OFF	
SW11-3	OFF	

Other SW settings refer to r20ut4984egxxxx-rskplus-rzn2l-v1-um.pdf.



4.2.2 Setup RZ/N2L RSK Board

Setting the board for running sample program is shown below.

- 1. Connect an emulator.
 - When you use I-jet or J-Link emulator, connect it to J20 on RZ/N2L RSK board.
 - When you use J-Link On-Board emulator, connect USB micro-B to J10 on RZ/N2L RSK board. (Please disconnect J9 for powering up J-Link OB.)



Figure 4-4 Setup RZ/N2L RSK board

- 2. Connect to a USB serial port.
 - Connect the USB cable (Type-A to type Mini B) to the USB connector "CN16" on the RZ/T2M RSK board.
- 3. Power is supplied using USB cable (Type-C) or AC / DC adapter.
 - When using USB cable (Type-C), connect it to the USB connector "CN5" on the RZ/N2L RSK board.
 - When using AC/DC adapter, connect it to the connector "CN6" on the RZ/N2L RSK board.
- 4. Connect Ethernet Cable to the Ethernet Connector "ETH0".



5. Set up the Host Device

5.1 Configuration the Host IP Address

Set an IP address that can communicate with the device in the Ethernet adapter settings on the PC side. For example, set as follows on the PC side.

- Example setting on the PC side.
 - IP address: 192.168.0.111
 - Subnet mask: 255.255.255.0

5.2 Set up the CODESYS Software

This chapter describes the setup of the CODESYS software.

5.2.1 How to get CODESYS

CODESYS Development system is available from the following web sites.

- Please open the <u>CODESYS Store</u> on the <u>CODESYS</u> website
 - Create an account, log in, and then download the CODESYS Installer.
 - ♦ When creating an account as a business customer, you need:
 - VAT Number if you are European VAT registered Customers.
 - Certificate of Registration as Taxpayer (entrepreneur) if you are non-EU customers.

5.2.2 Startup CODESYS Tools

After the installation is complete, launch the CODESYS Installer.

Click the "Add Installation" button, select the Platform, then choose "CODESYS 3.5 SP20" or a later version in the Setup, and click "OK" to proceed with the installation.

CODESYS Installer	New Installation		×
Installations	New Installation	Add Installation ~	=
	Platform x64		
	Setup CODESYS 3.5 SP20 (64 bit)		
	Version CODESYS 3.5 SP20 (64 bit) Patch 5		
	Create separate repositories	1	
	Update Mode All		
	Import Add-ons		
	From an existing installation		
	or from an Add-on Configuration file		
	OK Cancel		

Figure 5-1 CODESYS Installer

After installing the CODESYS, please launch the CODESYS tools shown below

Table 5-1 CODESYS tools

Name	Description	Note
CODESYS V3.5 SP20	IDE	CODESYS V3.5 SP20 or later is required.
CODESYS Gateway V3	Software Gateway	This might already be running from Windows startup.
CODESYS Control Win V3	Software PLC	This might already be running from Windows startup.



If the CODESYS is launched properly, the following window is shown



Figure 5-2 CODESYS Initial Window

If the CODESYS Gateway and Control Win SysTray is launched properly, the following icons are shown in notification area of Windows Tool Bar. (The left icon is of the CODESYS Gateway, and the right one is of the CODESYS Control Win SysTray)



Figure 5-3 CODESYS Icons



5.2.3 Install GSDML File into CODESYS

In the CODESYS, please open "tools" > "Device Repository" in tool bar.

CODESYS			
File Edit View Project Build Online Debug	Tools Wi	ndow Help	T
🛯 🍽 📓 🗠 🖉 🖉 🖓 🖄 🖓 👘 🖏 🖄 👘	CODES	YS Installer	= ※[目記言言》 ◆ 第 章 ◇
	Library	Repository	
evices	Device	Repository	
	Visuali	zation Element Repository	SP20 Patch 5
	🛃 Visuali	zation Style Repository	
	Licens	Repository	Latest powe
	OPC U	A Information Model Repository	Latest news
	Licens	Manager	
	Device	License Reader	
	Custor	nize	CODESYS
	Option	S	
	Import	and Export Options	
	Scripti	ng 🕨	·
	Edge G	ateway	·
	Autom	ation Server	
	Miscel	aneous •	
			A constraint of the second sec
		Close page after project	:load
		Show page on startup	
Messages - Total 0 error(s), 0 warning(s), 0 message(s)			
			Last build: 🔿 0 🕐 0 Precompile 🖌 Protect user: (nobody)

Figure 5-4 Device Repository in CODESYS

Click "Install" and select "PROFINET GSDML" as the file type in the "Install Device Description" dialog. Refer to the table below to select the GSDML that corresponds to the device.

Table 5-2 Device and GSDML File

Device	GSDML File
RZ/T2M	GSDML-V2.43-RENESAS-RZT2-VSC8541-20250516.xml
RZ/N2L	GSDML-V2.43-RENESAS-RZN2-VSC8541-20250516.xml



5.2.4 Change GSDML File

When changing the RSK board to be operated to be operated, you also need to change the GSDML installed in CODESYS. Please follow the steps below to uninstall the installed GSDML.

Open "Tools" > "Device Repository" from the toolbar again.

Enter "Renesas" in the search field, select all three devices that appear, and click the Uninstall button. Click the Install button and select the GSDML file to be used next.

Location	System Repository			~	Edit Locations
	(C:\ProgramData\CODESYS\Devi	ices)			
Installed D	Device Descriptions				
Renesas		Vendor <all td="" v<=""><td>endors></td><td>~</td><td>Install</td></all>	endors>	~	Install
Name			Vendor	Version	Uninstall
8- 🖬 F	Fieldbuses				Exports.
B. #	PROFINET IO				
6	PROFINET IO Slave				
	- Car RZT2 PROFINET	IRT DEVKIT			
	🔤 Failsafe_2_6	5_1_Standard, MRP	Renesas Electronics	SW=V1.4.2, HV	
	- Standard, M	RP	Renesas Electronics	SW=V1.4.2, H	
	- Standard, M	RP, S2 redundancy	Renesas Electronics	SW=V1.4.2, H	
	🚟 🚟 Standard, M	RP, S2 redundancy	DR Renesas Electronics	SW=V1.4.2, HV	
<				>	
					Class

Figure 5-5 Uninstall Devices



5.3 Setup the TIA portal Software

5.3.1 How to get TIA portal

Table 5-3 lists the recommended equipment used in the demonstration.

Table 5-3 List of equipment used for demonstration

Name	Description	Order Number	Webpage
PROFINET	SIEMENS CPU 1516-	6ES7 516-	https://mall.industry.siemens.com/mall/en/WW/Catalog/Pr
Controller	3 PN/DP *1	3AN02-0AB0	oduct/6ES7516-3AN02-0AB0
	SIEMENS CPU	6ES7 516-	https://mall.industry.siemens.com/mall/en/WW/Catalog/Pr
	1516F-3 PN/DP *1 *2	3FN02-0AB0	oduct/6ES7516-3FN02-0AB0
TIA Portal	Configuration	6ES7822-	Product Details - Industry Mall - Siemens WW
Software	software PLC	1AA24-0YA5	

Notes: 1. Please purchase a memory card together. It is required for the controller to operate.

2. Required when using PROFIsafe application.



Figure 5-6 Demo configuration



TIA portal can be purchased from the following website.

Product Details - Industry Mall - Siemens WW

🕼 🗖 🔄 Produ	ict Details - Industry Mall - S 🗙 🕂				- o	×
← C A ●	https://mall.industry.siemens.com/mall/en/WV	V/Catalog/Product/6ES7822-	1AA24-0YA5	at A de	@	. 🧳
SIEMENS				SiePortal The integrated platform for your information, buying an workflow – bringing together Industry Mall and Online S	> Log in d ordering Support.	
SiePortal	d language	► Contact ► Help	 Support Request 	Search for products	Q	
6ES7822-1AA24-C	VYA5 SIMATIC STEP 7 Professional V20, floating license; en Portal; software and documentation on DVD, license ke languages: de on zh included, fresi, tru ja ko as downin Sr.1200/150, Sr.300400/wnAC, SiMATIC Beise Panels. – for system requirements specification, see w content: set (3x DVD + 1x USB) List Price Customer Price DataSheet in PDF	gineering software in the TIA yr on USB fiash drive; class A; 9 wel; for configuration of SIMATIC www.siemens.com/compation - Show prices Show prices Show prices Show prices Show prices	Buy product Quantity 1 1 Pi		a _{1 ••} Car	
Image similar Image gallery and data for N 	Service & Support (Manuals, Certificates, FAQs) I-CAD and E-CAD (1) (1)	↗ Download				
Product Article Number (Market Facin	a Number) 6ES7922 10424 0V45					
Product Description	SIMATIC STEP 7 Professi engineering software in th documentation on DVD; lii class A; 9 languages: de download; for condiguratio 300/400WinAC, SIMATIC 300/400WinAC, SIMATIC	onal V20, floating license; e TIA Portal; software and sense key on USB flash drive; in,zh included, fr,es,it,ru,ja,ko as n of SIMATIC S7-1200/1500, S7- Basic Panels, SIMATIC Unified				

Please install the software according to the TIA Portal manual.



6. Running the Sample Application

This chapter describes how to download and run the program.

6.1 Install of EWARM environment

- 1) Run the installer file (EWARM-9501-69506.exe).
- 2) Click "Install IAR Embedded Workbench® for Arm", and follow the instructions to install.
- 3) Download the FSP Smart Configurator installer file. Only available for FSP V2.0.0.
 RZT2M: <u>setup_rztfsp_v2_0_0_rzsc_v2024-01.1.exe</u>
 RZN2L: <u>setup_rznfsp_v2_0_0_rzsc_v2024-01.1.exe</u>
- 4) Run the installer file, and follow the instructions to install.

6.2 Install of e2 studio environment

- Download the installer file. Only available for FSP V2.0.0.
 RZT2M:<u>setup rztfsp v2 0 0 e2s v2024-01.1.exe</u>
 RZN2L: <u>setup rznfsp v2 0 0 e2s v2024-01.1.exe</u>
- 2) Run the installer file, and follow the instructions to install.



6.3 Debugging with EWARM

This section shows the debug method for the sample program in the following steps.

- 1) Install and extract the project.
- 2) For dual-core debugging, open the CPU0 configuration file (configuration.xml) in Smart Configurator. Click "Generate Project Content" and repeat the same steps for the CPU1 configuration file.
- 3) Open the sample project file *.eww. For dual-core debugging, open CPU1 project.
- 4) Select the application to run

* Application overview





Figure 6-1 Select Single-core Application

Figure 6-2 Select Dual-core Application

Table 6-1 Application and Core Support

Application Name	Description	Core Support
Debug_App1_STANDARD	Standard Application (Use SDRAM)	Single, Dual
Debug_App1_STANDARD_hram	Standard Application (Use HyperRAM)	Single, Dual
Debug_App3_ IsoApp	Isochronous Application (Use SDRAM)	Single, Dual
Debug_App3_IsoApp_hram	Isochronous Application (Use HyperRAM)	Single, Dual
Debug_App5_FAILSAFE_PSD	PROFIsafe Application (Use SDRAM)	Single, Dual
Debug_App5_FAILSAFE_PSD_hram	PROFIsafe Application (Use HyperRAM)	Single, Dual
Debug_App6_SharedMemory	Shared Memory Application (Use SDRAM)	Dual
Debug_App6_SharedMemory_hram	Shared Memory Application (Use HyperRAM)	Dual
Debug_App44_PROFIdrive	PROFIdrive Application (Use SDRAM)	Single, Dual
Debug_App44_PROFIdrive_hram	PROFIdrive Application (Use HyperRAM)	Single, Dual



5) Select the device mode. Set the preprocessor options according to the device mode you want to use.

Regoly:	I ⊡ Multi-file Cor	milation			Factory Setting
atic Analysis	Discard	Unused Publics			
untime Checking	Language		2 Code	Ontimization	c Output
C/C++ Compiler	Language	Deserves	2 Code	opumization	is Output
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ustom Build	□ Ignore st	tandard include dir	ectories		
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Figure 6-3 Set the preprocessor options

Update the preprocessor to match the device mode you want to use.

Table 6-2 Preprocessor Option

Device Mode	Function	Preprocessor Option
DAP3(Default) ¹	Standard, MRP	IOD_INCLUDE_S2_REDUNDANCY=0
		IOD_INCLUDE_DR=0
DAP7	Standard, MRP, System Redundancy	IOD_INCLUDE_S2_REDUNDANCY=1
		IOD_INCLUDE_DR=0
DAP8	Standard, MRP, System Redundancy, CiR	IOD_INCLUDE_S2_REDUNDANCY=1
		IOD_INCLUDE_DR=1
DAP9 (Only use with	Standard, MRP, PROFIsafe	IOD_INCLUDE_S2_REDUNDANCY=0
PROFIsafe Application)		IOD_INCLUDE_DR=0

1 When PROFIsafe Application (DebugApp5_FAILSAFE_PSD), DAP9 is used instead of DAP3.

- 6) Select the "Rebuild All" item from the "Project" menu to rebuild the project.
- 7) For dual-core debugging, set the reset mode "Software" in the Reset section under Options > I-Jet > Setup tab. Save the changes and close CPU1 project.

Category: General Options 🔨 Static Analysis		Factory Settings
Runtime Checking C/C++ Compiler Assembler Output Converter Custom Build Linker	Setup Interface Trace Breakpoints Reset Software	
Build Actions Debugger Simulator CADI CMSIS DAP E2/E2 Lite GDB Server	Luration: 340 ms Delay after: 240 ms Target power Emulator ☑ From the probe ■ Always prompt for probe ④ Leave on after debugging ○ Switch off after debugging	
G+LINK I-jet J-Link/J-Trace TI Stelaris Nu-Link PE micro V	Log communication SPROL_DIR\$4cspycomm.log	

Figure 6-4 Set the reset mode



- 8) For dual-core debugging, open CPU0 project file. Select the same application as for CPU1 and then select the "Rebuild All".
- 9) For dual-core debugging, select "Simple" in the Asymmetric Multicore section under Options > Debugger > Multicore tab.

ategory:		Factory Setting
Seneral Options		
itatic Analysis		
untime Checking	Satura Devertand Income Multicore Authoration	tion Friter Ontions Division
C/C++ Compiler	Setup Download Images Multicore Authentica	ation Extra Options Plugins
Assembler	Symmetric multicore	
Dutput Converter		-
Custom Build	Number of cores: 1	
inker	Asymmetric multicare	
Ruild Actions	Asymmetric multicore	
lebugger	O Disabled	
Simulator	Simple	
CADI	C Simple	
CMSIS DAP	Partner workspace: \$PROJ_DIR\$¥¥xspi_t	oot_dual_cpu1¥RZ
E2/E2 Lite	Partner project: RZT2M_PROFINET_IR	T_XSPI_BOOT_DUA
G+LINK	Partner configuration: Debug_App1_STAND	ARD
I-jet 1+ ink/1-Trace	Attach partner to running target Par	tner cores: 1
TI Stellaris	Override partner debugger location	
Nu-Link	Partner debugger:	
PE micro	Advanced	
	Session configuration:	

Figure 6-5 Enable the Asymmetric multicore

10) Press the "RESET" switch of the RSK + RZT2M or RSK + RZN2L board.



Figure 6-6 RESET switch

In case you will see this kind of error message, please ignore them and press the "Skip" button.

Get Alternative File	×
Could not find the following source file: C:\Users\a5122373\Desktop\Esyse\io-com4\RZT2\rzt2_sdk\src\ext\EK47\pn_ioddevkits\sr\clrpc_cfq_lib.c	
Suggested alternative:	
Use this file Skip	
☑ If possible, do not show this dialog again	

Figure 6-7 Error message



11) While the board and I-jet are connected, click on the "Download and debug" button in the "Project" toolbar.

The CPU0 or CPU1 project will start. Please note that the initial startup will take longer than usual because the build process needs to be executed.

RZT2_BSP_beta1 - IAR Embedded Workbench IDE - Arm 8.50.	0.4	- a ×
File Edit View Project 1-jet Tools Window Help		
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Add Project Connection	MPGRT SystemCoreClockDpdate	
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He Compone		
-B Program 2 and English Project	27 OPEINLEION	
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đ Ciran	L_smoor_ini dda dwoddoddi / smaore droupi internupt velue TLR ded dwoddoddi / Scalar i used for Groupi internupt	
Satch build	76	
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C-STAT Static Analysis	ne VECT_ADDR 0x30000000 ; Vector address	
Stop Build Ctrl+8	Break me MODE MSR OwlF / Bit mask for mode bits in CPSR	
O Download and Debug Ct	20-0	
Debug without Downloading		
Attach to Rynning Target	citor same : ayatma_ant	
G Make & Restart Debugger CP	LIN-R LUBERTS I DODE	
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an adapt	WVW FO, #EACTLE BIT L / Set BACTLE Dits(L)	
CMSIS-Pack Manager	OVI 10, #0	
Open Device Description File	FCR p15, #4, FO, c1, c0, #1 / WFISE FO TO MACTLR	
Save List of Registers	eri	
	MBC pl5, 44, rl, cl, cl, 40 / Read Ryp Configuration Register	
	MCR pl5, #4, rl, cl, cl, #0 / Frite Ryp Configuration Register	
	The second	
ZT2_BSP_beta1 <	APP VIGT	>
suglog		* 0
Log		
Wed Jan 27, 2021 06:42:18 IAB Embedded Workbr	ench 8.50.4 (CVProcram Files (x85))AR Systems/Embedded Workbench 8.4am/bin/amoroc.dl)	
Wed Jan 27, 2021 06:42:18: Loading the Hjet driver		
alld Debug Log		

Figure 6-8 Download and debug

12) After the debug connection is established, the program will break at the first code line of "system_init" in the file "startup_core.c".

> RZT2M_PROFINET_IRT_XSPI_BOOT - IAF	Embedded Workbench IDE - Arm 9.50.1	– 🗗 🗙
File Edit View Project Debug Di	assembly J-Link Tools Window Help	
i n n 🖻 🖻 🔒 🕹 🗈 🗅 i) C	5 - 8 E E C
Workspace 🗸 🗸 🗙	startup_core.c x	Disassembly • 4 ×
Debug_App1_STANDARD ~	system_init() f	0 Go to:
Files	<pre>175 BSP_IAGET_ARW void system_init (void) 176 Bif 1// Software loops are only needed when debugging. 177 Bif 1 // Software loops are only needed when debugging. 178 Bif 28 void 11 (* * * * * * * * * * * * * * * * *</pre>	Disassembly
Log Tue Dec 03, 2024 13:36:43: Enabli Tue Dec 03, 2024 13:36:43: Reset	ig debug mode argel() end - Took 220ms	<u>^</u>
Build Debug Log	a Marana a Constantina a Constantina di Constantina di Constantina di Constantina di Constanti di Constanti di	
Ready	Errors 0, Warnings 0 Lr	180, Col 47 System CAP NUM 上書き

Figure 6-9 After debug connection



13) Press the "Go" button to start the program.

For dual-core debugging, press "Start Core" on CPU0, then press "Start Core" on CPU1 to start the program.

> RZT2M_PROFINET_IRT_XSPI_BOOT	_DUAL_CPU0 - Master - IAR Embedded Workbench IDE - Arm 9.50.1		– ø ×
File Edit View Project Debug	Disassembly I-jet Tools Window Help		
i 🗅 🖄 🔛 🕋 🔒 i 🕹 🛍 🗂	- く Q > 集 栏 く Q > G D D D = 0 個 G C D A T P H H M M M の 白 + 8]	etm suo 🛛 🚛	📮 j 🔳 0 🔹 💷 1 🔹
Workspace 👻 🕈 🗙	startup_core.c x bsp_delay_core.c	Disassembly	Start Core
Debug_App1_STANDARD ~	system_init() fo	Go to:	Stop Core
Files	199 BSP_CFG_HANDLE_UNRECOVERABLE_ERROR(0); 170 } 171 * After boot processing, LSI starts executing here. 173 * After boot processing, LSI starts executing here. 174 ** 175 BSP_TARGET_ARM void system_init (void) 176 #if 1 // Software loops are only needed when debugging. 177 #if 1 // Software loops are only needed when debugging. 178 = 179 = 170 #if 1 // Software loops are only needed when debugging. 176 #if 1 // Software loops are only needed when debugging. 178 = 179 = 180 = 181 = 182 = 183 = 184 = 185 = 186 = 187 = 188 = 188 = 189 = 180 = 181 = 182 = 183 = 184 =	Disasser a 0x1 0x1 0x1 0x1	bby sm volatile (" mov r(movt r: "software_loc " adds r(" cmp r("
	199 - ::[DSp_mactir_Dit_1] 1 (DSP_maclik_Dil_C) : memory); 194		" MOVU r(" MOVT r(
RZT2M_PROFINET_IRT_XSPI_B		4	
Debug Log			★ å ×
Log Tue Dec 03, 2024 16:11:16: Tr Tue Dec 03, 2024 16:11:16: Tr Tue Dec 03, 2024 16:11:16: W Tue Dec 03, 2024 16:11:16: W Tue Dec 03, 2024 16:11:16: M Tue Dec 03, 2024 16:11:16: Tr	ace: ETM-4 is already powered-up (TRCPDSR=0x23) ace: Using ETF at address 0x800110000, RAM size 0x1000 words (16KB) ace: Configured as 'ETM-4 to ETB' (SW ver: Trace2=1.40 ETM=1.02 ETB=1.05 Deco=1.45) aming: Power and SWO trace are not possible in multi-core debugging. JflCore: Synchronous core execution DISABLED iere were 3 wamings during the initialization of the debugging session.		*
Build Debug Log Ready	Errors 0, Warnings 4 I. Ln 178, Col 5	System	CAP NUM 上書き

Figure 6-10 Start the program

- 14) When reconfiguration: Open the Smart Configurator.
- 15) Close the "New Renesas RZ/T Project" window.

🔞 New Renesas RZ/T Project	(<u>1811</u>)		×
New Renesas RZ/T Project			
Project Name and Location			
Project name			
FSP_Project			
✓ Use <u>d</u> efault location			
Location: C:¥Users¥a5144133¥RASmartConfigurator¥FSP_Project		Brov	vse
You can download more Renesas packs here			
< <u>B</u> ack <u>Next</u> > Einist	1	Cancel	

Figure 6-11 Create New Project window



16) Open the configuration.xml from iar_project. To do this, select File > Open from the toolbar.

					B	
ganize ▼ New folder						
me	Date modified	Туре	Size			
.settings	5/8/2025 5:17 PM	File folder				
Debug_App1_STANDARD	5/8/2025 7:14 PM	File folder				
Debug_App3_IsoApp	5/9/2025 3:16 PM	File folder				
Debug_App3_IsoApp_hram	5/9/2025 2:54 PM	File folder				
rzt	5/8/2025 5:17 PM	File folder				
rzt_cfg	5/8/2025 5:17 PM	File folder				
rzt_gen	5/8/2025 5:17 PM	File folder				
script	5/8/2025 5:17 PM	File folder				
settings	5/8/2025 7:53 PM	File folder				
src	5/8/2025 5:17 PM	File folder				
configuration.xml	5/8/2025 5:00 PM	XML File		148 KB		
File name: configuration	n.xml		~	FSP Config	uration XML	File (cor

Figure 6-12 Open the configuration.xml

17) This allows reconfiguration. When reconfiguring ram_debug_dual_cpu1 project, build Debug_App1_STANDARD in the CPU0 project before opening the configuration.xml.



6.4 Debugging with e2 studio

This section describes how to debug the sample program in the e2 studio environment using the following steps.

- 1) Open e² studio.
- 2) Import "gcc_project" folder from "File" tab.

Select the import wizard to "Projects from Folder or Archive".



Figure 6-13 Import the project

3) Select only the projects compatible with the installed e2 studio.

RZ/T2M: ram_debug_dual_cpu0, 1 / ram_debug_single / xspi_boot_single / xspi_boot_dual_cpu0, 1 RZ/N2L: rzn2l_ram_debug / rzn2l_shost_host / rzn2l_shost_xspi_boot / rzn2l_shost_remote / rzn2l_xspi_boot

nport source:	¥Renesas_PROFINET_IRT_DEVKIT_V ~	Directory	Archive
ype filter text			Select All
older	Import as		Deselect All
gcc_project			Deselect Pill
gcc_project¥ram_debug_dual_cpu0	Eclipse project		
gcc_project¥ram_debug_dual_cpu1	Eclipse project		
gcc_project¥ram_debug_single	Eclipse project		
gcc_project¥rzn2l_ram_debug	Eclipse project		
<pre>gcc_project¥rzn2l_shost_host</pre>	Eclipse project		
gcc_project¥rzn2l_shost_host_xspi_boot	Eclipse project		
<pre>gcc_project¥rzn2l_shost_remote</pre>	Eclipse project		
gcc_project¥rzn2l_xspi_boot	Eclipse project		
gcc_project¥xspi_boot_dual_cpu0	Eclipse project		
gcc_project¥xspi_boot_dual_cpu1	Eclipse project	6 of '	12 selected
gcc_project¥xspi_boot_single	Eclipse project	Пн	ide already open proje
se installed project configurators to:] Search for nested projects] Detect and configure project natures Working sets			
Add project to working sets			New
Wedding			Colore .
manning sed.			20/0Ct

Figure 6-14 Select the project



- 4) Select the application to run from "Build Configurations". For dual-core debugging, select the CPU1 project.
- * Single-core project

🍐 Project Explorer 🗡 🛛 🔚 🖏 🖔	8	Show In	Alt+Shift+W >			
<pre>> \$ ram_debug_dual_cpu0 > \$ ram_debug_dual_cpu1 > \$ ram_debug_single > \$ ram_debug_single > \$ xspi_boot_dual_cpu0 > \$ xspi_boot_dual_cpu1</pre>		Copy Paste Delete Source	Ctrl+C Ctrl+V Delete >			
State (Debug_App1_STA	AN C	Rename	F2			
		Import Export Renesas FSP Export	,			
	Ð	Build Project Clean Project Refresh Close Project Close Unrelated Projects	F5			
		Build Targets Index	>			
		Build Configurations	>	Set Active	> ~	1 Debug_App1_STANDARD
		Source	>	Manage		2 Debug_App1_STANDARD_hram
	0 #	Run As Debug As Team	>	Build All Clean All Build Selected		3 Debug_App3_IsoApp 4 Debug_App3_IsoApp_hram 5 Debug_App44_PROFIdrive
		Compare With Restore from Local History	,			6 Debug_App44_PROFIdrive_hram 7 Debug_App5_FAILSAFE_PSD 8 Debug_App5_FAILSAFE_PSD_hram

Figure 6-15 Select Single-core application

* Dual-core project

🍋 Project Explorer 🗡 🛛 📄 🔩		Show In	Alt+Shift+W >				
> 🚰 ram_debug_dual_cpu0 > 🚰 ram_debug_dual_cpu1 > 🚰 ram_debug_single > 🚰 xspi_boot_dual_cpu0		Copy Paste Delete Source	Ctrl+C Ctrl+V Delete				
> 🚰 xspi_boot_dual_cpu1 [Debug_App1		Move					
> 💕 xspi_boot_single		Rename	F2				
	22	Import Export Renesas FSP Export	>				
	Ð	Build Project Clean Project Refresh Close Project Close Unrelated Projects	F5				
		Build Targets	>				
		Index	>				
		Build Configurations	>	Set Active	>	~	1 Debug_App1_STANDARD
		Source	>	Manage			2 Debug_App1_STANDARD_hram
	0	Run As Debug As Team	> >	Build All Clean All Build Selected			3 Debug_App3_IsoApp 4 Debug_App3_IsoApp_hram 5 Debug_App44_PROFIdrive
		Compare With Restore from Local History MISRA-C	>				6 Debug_App44_PROFIdrive_hram 7 Debug_App5_FAILSAFE_PSD 8 Debug_App5_FAILSAFE_PSD_hram
	10	C/C++ Project Settings Renesas C/C++ Project Settings	Ctrl+Alt+P				9 Debug_App6_SharedMemory 10 Debug_App6_SharedMemory_hram

Figure 6-16 Select Dual-core application

Table 6-3	Application	and Core	Support
-----------	-------------	----------	---------

Application Name	Description	Core Support
Debug_App1_STANDARD	Standard Application (Use SDRAM)	Single, Dual
Debug_App1_STANDARD_hram	Standard Application (Use HyperRAM)	Single, Dual
Debug_App3_ IsoApp	Isochronous Application (Use SDRAM)	Single, Dual
Debug_App3_IsoApp_hram	Isochronous Application (Use HyperRAM)	Single, Dual
Debug_App5_FAILSAFE_PSD	PROFIsafe Application (Use SDRAM)	Single, Dual
Debug_App5_FAILSAFE_PSD_hram	PROFIsafe Application (Use HyperRAM)	Single, Dual
Debug_App6_SharedMemory	Shared Memory Application (Use SDRAM)	Dual
Debug_App6_SharedMemory_hram	Shared Memory Application (Use HyperRAM)	Dual
Debug_App44_PROFIdrive	PROFIdrive Application (Use SDRAM)	Single, Dual
Debug_App44_PROFIdrive_hram	PROFIdrive Application (Use HyperRAM)	Single, Dual



5) Select the device mode. Set the preprocessor options according to the device mode you want to use.



Figure 6-17 Set the preprocessor options

Update the preprocessor to match the device mode you want to use.

Table 6-4 Preprocessor Option

Device Mode	Function	Preprocessor Option
DAP3(Default) ¹	Standard, MRP	IOD_INCLUDE_S2_REDUNDANCY=0
		IOD_INCLUDE_DR=0
DAP7	Standard, MRP, System Redundancy	IOD_INCLUDE_S2_REDUNDANCY=1
		IOD_INCLUDE_DR=0
DAP8	Standard, MRP, System Redundancy, CiR	IOD_INCLUDE_S2_REDUNDANCY=1
		IOD_INCLUDE_DR=1
DAP9 (Only use with	Standard, MRP, PROFIsafe	OD_INCLUDE_S2_REDUNDANCY=0
PROFIsafe Application)		IOD_INCLUDE_DR=0

1 When PROFIsafe Application (DebugApp5_FAILSAFE_PSD), DAP9 is used instead of DAP3.

6) Select the "Build project" item from the "Project" menu to build the project.



Figure 6-18 Build the project



- 7) For dual-core debugging, open the CPU0 project file. Select the same application as for CPU1, then select "Build project".
- 8) Press the "RESET" switch of the RSK + RZT2M or RSK + RZN2L board.
- 9) While the board and J-link OB are connected, click on the "Debug Configurations..." button in the toolbar. For dual-core debugging, start the debugging process from the CPU0 project.

e2_manual - e ² studio								- a ×
File Edit Source Refactor Navigate Search Project Reness	as Views Run Window Help							
🐔 💿 🔳 🗣 Debug 🛛 🗸 🖾 ram_debug_single_App ~	0 [] + [] 0] 0 + 5 + [] 0 0 + 6 + 3	• @ • 💩 🖉 • 🕼 🗉 🐐 🔖	🐵 😵 💩 🕶 💁 🕶 0,	*花田*田学家:	古(の)別 * 羽 * つ	00+0+10		Q. 1 ₪ Q/C+-
Project Explorer ×	1 - D		(no launch	history)		- 0	₿ Outline ×	
> 💋 ram debug dual cpu0			Debug As	· · · · ·			There is no active edite	ir that provides an outline
> 💋 ram_debug_dual_cpu1			Debug Co	infigurations				
> 💋 ram_debug_single			Organize	Favorites				
sspi_boot_single [Debug_App3_IsoApp]					1			
> & Binaries								
> 🕫 Includes								
> 🥴 rzt								
> 🕮 rzt_gen								
> @ src								
> & Debug_App3_IsoApp								
> le rzt_ctg								
> is script								
ter configuration.xml								
Runni heet siegle Apet kom elijiek								
E vroi boot single Apot bram elf laurch								
R vsni hont single Annt elfilink								
8 xspi boot single App1 elf launch								
ii xspi boot single App3 hram.elf.link								
8 xspi boot single App3 hram.elf.launch								
xspi_boot_single_App3.elf,link								
R xspi boot single App3.elfJaunch								
	P Desklams X D Canada D Deserties	Connect Resources (1) Connect Manual						71-1
	Derror 25 warpiege 0 other	Smart browser - Smart Manual						
	Description	Perourre	Dath	Location	Tuno			
	Warnings (25 items)	resource	Four	Location	ijpe			
	· · · · · · · · · · · · · · · · · · ·							

Figure 6-19 Open Debug Configurations

10) In the "Debug Configurations" window, double-click the configuration of the application you want to run.

Debug Configurations					×
Create, manage, and run configurations				X	Ş
🖹 🖻 🍋 🗎 🗶 🖻 🏹 🗝		Name: xspi_boot_single_App3.elf			
type filter text		📄 Main 🕸 Debugger 🕨 Startup 🦆 Source 🔳	Common		
xspi_boot_dual_cpu1_App5_hram.elf	^	Project:			
spi_boot_dual_cpu1_App6_hram.elf		xspi_boot_single		Browse	
xspi_boot_dual_cpu1_App6.elf		C/C++ Application:			
xspi_boot_single_App1_hram.elf		Debug App3 IsoApp/yspi boot single App3 elf			
xspi_boot_single_App1.elf		bebug_r.pps_isor.ppr.spi_bool_single_r.pps.eii			
xspi_boot_single_App3_hram.elf		Variables Search Proje	ect	Browse	
c xspi_boot_single_App3.elf		Build (if required) before launching			
xspi_boot_single_App44_fifam.en		Build Configuration: Use Active			~
xspi boot single App5 hram.elf					
┏x xspi_boot_single_App5.elf		C Enable auto build Disable a	uto build		
xspi_boot_single_rphy_App1_hram.elf		Use workspace settings <u>Configure V</u>	/orkspace S	Settings	
xspi_boot_single_rphy_App1.elf					
xspi_boot_single_rphy_App3_hram.elf					
xspi_boot_single_rphy_App3.elf					
xspi_boot_single_rphy_App44_hram.elf					
xspi_boot_single_rphy_App44.elf					
spi_boot_single_rpny_App5_hram.elf					
Panasas Simulator Dobugging (PX, PL79)	~				
Filter matched 79 of 81 items		Revert		Apply	
(?)		Debu		Close	

Figure 6-20 Debug Configurations window

Click "Switch" in the "Confirm Perspective Switch" dialog box.





Figure 6-21 Confirm Perspective Switch dialog box

- 11) The CPU0 or CPU1 project is started.
- 12) After the debug connection is established, the program will break at the first code line of "system_init" in the file "startup.c".
- 13) Press the "Resume" button, the program will break at the first code line of "main". To run the program completely, press the "Resume" button again.



14) For dual-core debugging, run the CPU1 project debugging while the CPU0 project is halted at the first line of "system init".

Click "No" when the following dialog appears when you start debugging the project cpu1.



Figure 6-23 Appearing dialog box



Click Yes to "proceed with launch?" dialog box.



Figure 6-24 Proceed with launch? dialog box

15) When reconfiguration: Double-click configuration.xml in the Project Explorer.



Figure 6-25 Open the configuration.xml

16) This allows you to reconfigure settings. When reconfiguring CPU1 in the Dual Core project, build Debug_App1_STANDARD in the CPU0 project before opening the configuration.xml.



7. Demonstration of the application

Before starting this chapter, power on the RSK board and then connect the PC/PLC to either the ETH0 connector. For details, please refer to Chapter 4.

7.1 Application Behavior

The connections between the RZ/T2M, RZ/N2L application and PLC application are shown below.



Figure 7-1 Application Overview

7.2 Board Configuration

7.2.1 MAC Address Configuration

The default MAC address is set to 74:90:50:10:e9:07. If you need to change the MAC address, connect the PC to the RSK board via the USB connector "CN16" and use the serial console to change the MAC address. Follow the steps below to change the MAC address.

First, turn off the board. Disconnect the Ethernet cable from the "ETH0" port and connect a USB cable to the "CN16" port. Then, turn the board back on.

Next, use the terminal software with the following settings to connect to the COM port of the RSK board.

- Baud Rate: 115200bps
- Local Echo: OFF
- TX New Line: CR or CR+LF

In the terminal software, type N and press ENTER.



Figure 7-2 MAC Address Change Command



After that, follow the instructions displayed in the output and enter each byte of the new MAC address in order, pressing ENTER after each one. The process is complete when "***Bsp_nv_data_store: Completed ***" is displayed.

To apply the new MAC address to the RSK board, press the RESET button "S3" on the RSK board and connect the Ethernet cable to "ETH0".



Figure 7-3 MAC Address Change Complete



7.3 Start CODESYS Connection

7.3.1 Open CODESYS project

Select "File" > "Open Project..." from the menu in the CODESYS toolbar. Then, open the project file corresponding to the PROFINET application.

Table 7-1 PROFINET application and CODESYS project

PROFINET Applications	CODESYS Project
xspi_boot_single / Debug_App1_STANDARD	RZT2M_PROFINET_Sample_App1_STANDARD.projectarchive
xspi_boot_single / Debug_App44_PROFIdrive	RZT2M_PROFINET_Sample_PROFIdrive_AC1_App.projectarchive
rzn2l_xspi_boot / Debug_App1_STANDARD	RZN2L_PROFINET_Sample_App1_STANDARD.projectarchive
rzn2l_xspi_boot / Debug_App44_PROFIdrive	RZN2L_PROFINET_Sample_PROFIdrive_AC1_App.projectarchive

If the project is opened properly, the opened project is shown in "Device" section located at left in the following window.



Figure 7-4 Open a CODESYS Project



7.3.2 Start PLC

Start the software PLC. Click on the CODESYS Gateway and CODESYS Control icons in the system tray, then click "Start Gateway" and "Start PLC".



Figure 7-5 Start Gateway and PLC

If the Gateway and PLC is started properly, the icons pigment like the following image.



Figure 7-6 Icons with Gateway and PLC successfully started



7.3.3 Network Configuration

Please double-click "Device (CODESYS Control Win V3)" to open "Communication Settings" at center section, and please click "Scan Network..." to open "Select Device" window.

			$=$ $=$ $-\phi$ $ $, $ $ hus $ $ \cdots $ $ ϕ
← 및 > T2M_PROFINET_Sample_Standard_App	Communication Settings	Network Gateway - Device -	
Device (CODESYS Control Win V3 x64)	Applications		
- INOUT - 🎒 GVL	Backup and Restore		••
Library Manager	Files	Gateway	•
Task Configuration MainTask (TEC Tasks)	Log	Gateway-1	✓ [] (active) ✓
PLC_PRG	PLC Settings	IP-Address: localhost	Device Name: REL-0063305
Profinet_CommunicationTask (IEC-Tasks PN_Controller.CommCycle	PLC Shell	Port 1217	Target ID: 0000 0004
Profinet_IOTask (IEC-Tasks) Ethernet (Ethernet)	Users and Groups		Target Type:
PN_Controller (PN-Controller)	Access Rights		4096
	Symbol Rights		3S - Smart Software Solutions GmbH
	Software metrics for license determination		Target Version: 3.5.20.50
	IEC Objects		
	Task Deployment		
	Status		

Figure 7-7 Communication Settings

If the software PLC is found after scanning network, the device name (here, PC name) is shown under Gateway tree. Please double-click this device name (in blue portion).

		_
Select Device	X	
Select the Network Path to the Controller		
Gateway-1 (Scanning)	Device Name: Scan Network	
[0115]	Wink	
	Device Address:	
	0115	
	Block driver:	
	UDP	
	Encrypted Communication	
	TLS supported	
	Number of descela	
	4	
	Serial number:	
Uide see metaking devices filtes by Target TD	OK Cased	
	OK Cancel	

Figure 7-8 Select Device

When starting CODESYS for the first time, the user management activation prompt appears. Click "Yes" and add a Device User.





Figure 7-9 Add Device User Dialog

In the "Add Device User" dialog, enter the desired Username and Password, then click OK to add the Device User." When logging in next time, you will need to enter the Username and Password you specified here.

Add Device User	×	-
Name Default group	Administrator V	
Password Confirm password Password strength	Very weak	
Password policy	Password can be changed by user Password must be changed at first login Zero-length passwords are not allowed.	
	· · · · · · · · · · · · · · · · · · ·	
	OK Cancel	

Figure 7-10 Add Device User

Click the pull-down button next to the PLC name and select the device name (in this case, the PC name) displayed in Scan Network. If the network is configured properly, its configuration is shown in "Communication Settings" tab, and there are the green marks at gateway and device portions.



Communication Settings	Scan Network Gateway -	Device •			
Applications					
Backup and Restore			· · · · · · · · · · · · · · · · · · ·		
Files		_			•
Log		Cateway-1	Gateway	~	· · · · · · · · · · · · · · · · · · ·
PLC Settings		IP-Address:		*	Device Name:
PLC Shell		Port:			Device Address:
Users and Groups		1217			0115
Access Rights					Target ID: 0000 0004
Symbol Rights					Target Type: 4096
Software metrics for license					Target Vendor: 3S - Smart Software Solutions GmbH
IEC Objects					Target Version:

Figure 7-11 Green Marks at Gateway and Device Portions

7.3.4 Interface and IP address configuration

Please click "Ethernet (Ethernet)" in left section to open "Ethernet" tab in center section.

After that, please select "Browse..." button to select network interface ethernet which is connected with RSK board, and please configure the IP address and related address values of the ethernet network interface.

RZT2M_PROFINET_Sample_Standard_App.project* - CODESYS					- 0 ×
File Edit View Project Build Online Debug	loois Window Help		AN (11)		₹ 2
🗉 🖙 💾 🕼 🗠 🖉 🖉 🐨 🐘 🗶 🌆 🖓 🕼 🦉	비 게 게 게 네 믑 @* 더 @	Application [Device	: PLC Logic] 🔹 👒 🗐 🕨 🔳	🖌 (1 +1 +1 +1 + 1 + 1 + 1 + 1 + 1 + 1 + 1	3 \ampi */~
Devices 👻 🕈 🗙	Device i Ethernet X				
RZT2M_PROFINET_Sample_Standard_App Standard_App Device (CODESYS Control Win V3 x64)	General	Network interface	イーサネット 16	Browse	
PLC Logic Application	Ethernet Device I/O Mapping	IP address	192 . 168 . 0 . 111		
	Ethernet Device IEC Objects	Subnet mask	255 . 255 . 255 . 0		
library Manager	Log	Default gateway			
ILC_PRG (PRG) Idsk Configuration	Status		g system settings		
■ 参 MainTask (IEC-Tasks) □ ● PLC PRG	Information				
Profinet_CommunicationTask (IEC-Tasks)					
PN_Controller.CommCycle Profinet_IOTask (IEC-Tasks)		1			
Ethernet (Ethernet)					
PN_Controller (PN-Controller)					
Standard_MRP (Standard, MRP)					
64 bytes O (64 bytes O)					
>	<				
Messages - Total 0 error(s), 0 warning(s), 0 message(s)					
			💫 🛛 Last build: 😋 0 😗) Precompile 🧹 🛛 🚰	Project user: (nobody)

Figure 7-12 Open Ethernet tab

To modify the device configuration from the default, double-click "Standard_MRP (Standard, MRP)" in the left section. The configuration can be modified from the "Standard_MRP (Standard, MRP)" tab.



e Edit View Project Build Online Debug 🖆 🔜 🕼 🗠 🖙 🔏 🖿 🛍 🗙 👫 🏰 🌿	Tools Window Help	' 🎬 Application [Device:	PLC Logic] • 😋 🥨 🕨 🔳 💘 🗔 🖘 🖆 🏭 😂 🗢 🧱 🛫	₹
Construction C	Device Ethern General Port data IOXS Log PNIO I/O Mapping PNIO I/O Mapping PNIO IEC Objects Status	Application [Device: Application [Device: Station name	PLC Logic] • ♥ ♥ ■ ♥ [] • 1 • 1 & • ₩ ₩ • Standard_MRP × 2 192.168.0.2 255.255.0 0.0.0.0.0	
Pri_Controller_CommCyde Profinet_IOTask (IEC-Tasks) Pri_Controller (PN-Controller) PN_Controller (PN-Controller) Standard_MRP (Standard, MRP) J_64_bytes_I (64 bytes I) _64_bytes_O (64 bytes O)	Information	Send clock (ms) Reduction ratio Phase RT class Options Fast Startup	1 Vlan ID 12 - 4 Vlan ID 0 - - Vlan ID 0 -	
tessages - Total 0 error(s), 0 warning(s), 0 message(s)	¢	Shared device		

Figure 7-13 Standard_MRP Configurations

7.3.5 Build Project and Start Application

Follow the following steps and figure to build the project and start the application.

- 1. Click "Build" button in the tool bar to build the CODESYS project.
- 2. Click "Login" button in the tool bar to login the network.
- 3. Click "Start" button in the tool bar to run network and application.

🎦 🚅 📕 🎒 い つ ぶ 🗈 🛍 🗙 構 🌿 🐴 🌿 🔳	🛛 🐄 🦄 🖄 🛗 🍈 🖆 📋 Application [Device: PLC Logic] 🔹 🧐 🛞 🕞 💼 🔍 📜 🕾 🔤 🖄 🗢 🛒 😓	
🗎 🖆 🖶 🎒 🗠 🗠 🐰 酯 🛍 🗙 🛤 🌿 📥 🚰 📕	【 🐄 🦄 🎽 🛗 🋅 • 🚰 Application [Device: PLC Logic] - 😻 🥨 🕟 📄 🔏 📮 🕾 🗐 👘 👘 👘 👘 👘	
🎦 🖆 📕 🏉 🗠 🗠 🐰 酯 🛍 🗙 🖊 🌿 📕	【 🐄 🦄 🖄 🔚 🋅 + 📋 🛗 Application [Device: PLC Logie] 🔹 🧐 🥳 📄 🔍 [三 🕾 🤤 💷 🖄 中 那 デ 🏷	

Figure 7-14 Build Project and Start Application



7.3.6 Set Station Name

Set the station name for the device.

Right-click on "PN_Controller" and select "Scan for Devices..".

RZT2M_PROFINET_Sample_App1_STANDARD.project - CODESYS					o x
File Edit View Project Build Online Debug Tools	Window	Help			₹6
🗎 🚔 🖬 🚳 외 여 🖇 🐚 🛍 🗙 構 🌾 🐴 🌿 제 1	別別省	🛱 🏪 - 🗳 🏙 Ap	oplication [Device: PLC Logic] 🔹 🧐 👹 🕞 🔳 🖎 🗊 🖓 🖄 🚽 🖓 🌩 🛒 🦿		
Devices	• • ×	Ethernet	PN_Controller X Standard_MRP Device		•
RZT2M_PROFINET_Sample_App1_STANDARD S Off Device [connected] (CODESYS Control Win V3 x64)	•	General	Station name controller		^
PLC Logic		Overview			
Application [run]			Default Slave IP Parameter		
- PLC_PRG (PRG)		Topology			
E Task Configuration		Media Redundancy	Last IP address 192 . 168 . 0 . 254		
AinTask (IEC-Tasks)		PNIO I/O Mapping	Subnet mask 255 . 255 . 0		
🖃 😏 🍪 Profinet_CommunicationTask (IEC-Taski)		Piero yo Piepping	Default gateway 0.0.0.0		
PN_Controller.CommCyde	Cut		I/O Provider / Consumer Status		
Profinet_IOTask (IEC-Tasks)	Paste		Application stop> Substitute values		
O PN Controller (PN-Controller)	Delete		✓ Add to I/O mapping		~
Standard_MRP (Standard, MRP)	Refactoring				>
▲ <u> </u>	Desertion	y ,	varning(s), 37 message(s)		→ ∓ X
△	Properties.		▼ O error(s) O warning(s) 37 message(s) × ×		
111	Add Objec	t	Proj	ect Object	Position ^
	Add Folder	r	IGBEFORETASK_4		
	Acknowled	evices			
	Acknowled	dge Diagnosis Subtree			
L, L	Edit Object	t	16 bytes		
	Edit Object	t With	tot used for licensing purposes:		
	Edit IO ma	pping) warnings : Ready for download		
👷 Devices 👔 POUs	Import ma	ppings from CSV	0 warning(s), 37 message(s) 🐹 Watch 1 🏟 Breakpoints		•
∑ Device user: device_user Last build: O ●	Export ma	ppings to CSV	Program loaded Program unchanged Pro	oject user: (nob	ody) 🖗

Figure 7-15 Set Station Name

Enter the device name (rzt2 or rzn2) in the "Station Name" field and click the "Set Name and IP" button.

Device name	Device type	Station Name	ID number
$\sim\!\!\!\sim$ The identification data is not available. Check the IP address.	Vendor-ID: 0x02C7, Device-ID: 0x0003	rzt2	Error: A valio
c			
k kM Auto-IP <> Reset Blink LED Set Name and IP] Show only unnamed stations	Show differe	ences to projec
د کلا Auto-IP <> Reset Blink LED Set Name and IP] Show only unnamed stations	Show differe	ences to project



If the CODESYS application on PC connects with PROFINET application on RZ/T2M(RZ/N2L) properly, "Device", "Ethernet", "PN_Contoroller", and "Standard_MRP" in left section are marked with green cycle mark.



Figure 7-17 Check Network Connection



7.4 Start PLC Connect

7.4.1 Select TIA Portal project

Select the project you want to demonstrate.

See Table 7-2 for the correspondence between the PROFINET application and the TIA Portal project file.

Table 7-2 PROFINET applications and TIA Portal project files

PROFINET applications	TIA Portal project file
xspi boot single / Debug App1 STANDARD	RZT2M_PROFINET_RT_Sample_App1_STANDARD.zap18
	RZT2M_PROFINET_IRT_Sample_App1_STANDARD.zap18
xspi boot single / Debug App44 PROFIdrive	RZT2M_PROFINET_RT_Sample_PROFIdrive_AC1_App.zap18
······································	RZT2M_PROFINET_IRT_Sample_PROFIdrive_AC4_App.zap18
rzn2l xspi boot/Debug App1 STANDARD	RZN2L_PROFINET_RT_Sample_App1_STANDARD.zap18
······································	RZN2L_PROFINET_IRT_Sample_App1_STANDARD.zap18
rzn2l xspi boot / Debug App44 PROFIdrive	RZN2L_PROFINET_RT_Sample_PROFIdrive_AC1_App.zap18
······································	RZN2L_PROFINET_IRT_Sample_PROFIdrive_AC4_App.zap18

7.4.2 Open TIA Portal project

This section describes the procedure to download a project file to the PLC.

- 1. Launch TIA Portal V18 or later.
- 2. Select "Open existing project" and click "Browse".

Via Siemens				_ • ×
				Totally Integrated Automation PORTAL
Start			Open existing project	
Devices & networks	1	Open existing project	Recently used Project Path	Last change
PLC programming		Migrate project		
Motion & technology	*	Close project		
Visualization	1	Welcome Tour		
Online & Diagnostics	10	First steps		
		Installed software	Activate basic integrity check	
		Melp	Browse	Open
		🐼 User interface language		
Project view				

Figure 7-18 Open TIA Portal V18



3. Open the project you want to demonstrate in the "Open an existing project" window.

Open an existing pr	roject			×
← → • ↑ 🖊	> My PC: > Downloads	~	ප Search Downloads	Q
Organize 👻 New	v folder			
🖈 Quick access	Name ~ Today (6)	Date modified	Type Siz	re .
OneDrive - Rene	esas Ele	2/25/2025 1:04 PM	Siemens TIA Portal V	344 KB
My PC:	RZT2M_PROFINET_RT_Sample_PROFIDrive_AC1_App.zap18	2/25/2025 1:04 PM	Siemens TIA Portal V	601 KB
3D Objects	RZT2M_PROFINET_IRT_Sample_Standard_App.zap18	2/25/2025 1:04 PM	Siemens TIA Portal V	345 KB
Desktop	RZT2M_PROFINET_IRT_Sample_PROFIDrive_AC4_App.zap18	2/25/2025 1:04 PM	Siemens TIA Portal V	645 KB
	RZN2L_PROFINET_RT_Sample_Standard_App.zap18	2/25/2025 1:04 PM	Siemens TIA Portal V	344 KB
	RZN2L_PROFINET_IRT_Sample_Standard_App.zap18	2/25/2025 1:04 PM	Siemens TIA Portal V	345 KB
Music Pictures Videos (C:) Windows Network				
	File name: RZT2M_PROFINET_RT_Sample_Standard_App.zap18		 All supported files (*.a Open 	ap18;*.ap1 ~ Cancel

Figure 7-19 Open an existing project

- 4. Select any directory where you want to deploy the project in the "Select target directory" window.
- 5. The GSDML file will be installed automatically.



Figure 7-20 Install GSD files automatically



6. Click "Open the project view".

Siemens - C:\TIA_Porta	l_Project\demo\R	ZT2M_PROFINET_RT_Sample_Standard_Ap	p\RZT2M_PROFINET_RT_Sample_Standard	_Арр		_ # X
					Totally	Integrated Automation PORTAL
Start		Onon evicting project	First steps Project: "RZT2M_PROFINET_RT_Samp	le_Standard_App" was o	opened successfully. I	Please select the next step:
PLC programming	** *	Create new project Migrate project	Start			^
Motion & technology	*	Close project	Devices &	Configure a	device	
Visualization Online & Diagnostics		 Welcome Tour First steps 	PLC programming	Write PLC pro	ogram	=
		Installed software	Motion & .	Configure technology o	bjects	
		Help	Visualization	Configure an	HMI screen	
		🕜 User interface language	Project view	Open the pro	oject view	
Project view		Opened project: C:\TIA_Portal_Proje	ect\demo\RZT2M_PROFINET_RT_Sample	Standard_App\RZT2M_	PROFINET_RT_Sample	e_Standard_App

Figure 7-21 Open the project view

7. The project opens. Figure 7-22 shows the screen when "Device & networks" is selected.

Siemens - C:\TIA_Portal_Project\demo\R2	ZT2M_PROFINET_RT_Sample_Standard_AppIRZT2M_PROFINET_RT_Sample_Standard_App	_ #X
Project Edit View Insert Online Optio	ngs Iools Window Help Total Sp ± (# ± 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	lly Integrated Automation PORTAL
Project tree 🛛 🔳 🖣	RZT2M_PROFINET_RT_Sample_Standard_App → Devices & networks	Hardware catalog 🔳 🛙 🕨
Devices	🛃 Topology view 🛛 🛔 Network view 🚺 Device view	Options 😐
1 III III III III III III III III III I	💦 Network 🔛 Connections 🔣 HM connection 💌 💆 🖫 🖀 🔛 🛄 🍳 ± 🔤 🚺 Network overvi (4 🕨	
RZT2M_PROFINET_RT_Sample_Sta Add new device Add new device ProfileT_RT_Sample_Sta Add new device Constant Sample_Sta ProfileState ProfileStateStateStateStateStateStateStateSta	PLC_1 rzt2 rzt2 rzt2 * S7-1500/ET200 PLC_1 Standard, MRP RZ/T2 * G5D device_1 PLC_1 * rzt2 * rzt2 PN/IE_1 * rzt2 * rzt2 Q Properties * Info & Diagnostics * rzt2	✓ Catalog ✓ Catalog
<pre> Construction matrixity Construction matrixity Details view Name Name </pre>	Compare Compa	Tasks
Portal view Overview	🚠 Devices & ne	ROFINET_RT_Sample

Figure 7-22 Device & network



7.4.3 Compile the project

To compile the project, please click on the icon "Compile"

After the project has been compiled, the compilation result is displayed on the Compile tab at the lower part of the window.

Make sure that the compilation has been successfully completed.



Figure 7-23 Compile the project



7.4.4 Download the project to the PLC

On the Device tab, right-click PLC in the tree and select Download to device > Hardware configuration.

	Device	Device type	Slot Interfac	e type Address	Subnet
	PLC_1	CPU 1516-3 PN/DP	1 X3 PROFIB	US 2	
		CPU 1516-3 PN/DP	1 X1 PN/IE	192.168.0.1	00 PN/IE_1
		CPU 1516-3 PN/DP	1 X2 PN/IE	192.168.1.1	
		Type of the PG/PC inter PG/PC inter Connection to interface/sul 1st gate	face: PN/IE face: Masix A bnet: PN/IE_1	.X88179 USB 3.0 to Gi	gabit Ethernet A ▼ ♥ ☑ ▼ ♥
	Select target de	vice:		Show all com	patible devices 🗸
	Device	Device type	Interface type	Address	Target device
and the second se	PLC 1	CPU 1516-3 PN/DP	PN/IE	192.168.0.100	PLC_1
1			DILLIE	Enter address he	
	-	-	PN/IE	Enter address he	re —
Flash LED	-	-	PN/IE	Enter address he	re –
Flash LED	-		PN/IE	Enter address he	re –
Flash LED	ion:		ΡΝΛΕ	Enter address he	re – <u>S</u> tart search y error messages
Flash LED e status informat ttempting to con	ion: nect to the device w		PN/IE	Enter address he	re – <u>S</u> tart search y error messages
Flash LED e status informat ttempting to con can and informa onnection estab	ion: nect to the device w tion retrieval comple		ΡΝΛΕ	Enter address he	re – <u>S</u> tart search y error messages

Figure 7-24 Extended download to device

Search the PLC to download the project.

- 1) In the "Type of the PG/PC interface" field, select "PN/IE".
- 2) In the "PG/PC interface" field, select the network connected to the PLC.
- 3) In the "Connection to subnet" field, select "PN/IE_1".
- 4) Click the [Start search] button to search PLCs and select the target PLC.
- 5) Click the [Load] button.



Click "Continue without synchronization" if "Software synchronization before loading to a device" appears.

Software synchronization	Status	Action	
▼ PLC_1			
 'Program blocks' 			
Main [OB1]		Upload and overwrite in the project	
 'PLC tags' 			
Tags	•	Manual synchronization required	
		III	

Figure 7-25 Software synchronization before loading to a device

The Load Preview window opens.

If the action status of "Stop modules" and "Device configuration" indicates "No action", select "Stop all" for "Stop modules" and select "Download to device" for "Device configuration" from each drop-down list.

When no error is present, click the [Load] button.

Image: Weight of the second	1
Protection Protection from unauthorized access Devices connected to an enterprise network or directly to the internet must be appropriately protected against unauthorized access, e.g. by use of firewalls and network segmentation. For	
Devices connected to an enterprise network or directly to the internet must be appropriately protected against unauthorized access, e.g. by use of firewalls and network segmentation. For	
more information about industrial security, please visit http://www.siemens.com/industrialsecurity	
Different modules Differences between configured and target modules (online)	
Stop modules The modules are stopped for downloading to device. Stop all	
 Device configurati Delete and replace system data in target Download 	o device

Figure 7-26 Load preview



If "Start all" checkbox appears, check it. And then click the [Finish] button.

Load res	sults				×
? s	Status	and actions after download	ding to device		
Status	1	Target	Message	Action	
4	%	▼ PLC_1	Downloading to device completed without error.		
	▲	Start modules	Start modules after downloading to device.	🛃 Start all	
<					>
			Finish	Load	Cancel

Figure 7-27 Load results

Connect the real PLC to the real device in accordance with the topology configuration.

Load res	sults			×
? s	Status a	and actions after downl	pading to device	
Status	1	Target	Message	Action
+1	0	PLC_1	Downloading to device completed without error.	Load 'PLC_1'
	•	Start modular Download	Start moduler after downloading to device to device Finish loading Start PLC_1 (current mode: STARTUP)	<+art module
			Can	cel
<			111	
			Finish	Load Cancel

Figure 7-28 Finish loading



7.4.5 Assign device name

Assign the Station name to the device.

Click on the interface to which the PLC is connected under "Online Access". Then double-click "Update accessible devices".

oject tree	RZT2M_PROFINET_RT_Sample_App1_STANDARD → Devices & networks	Hardware catalog 📰 🔳
Devices	🛃 Topology view 💼 Network view 🛐 Device view	Options
Add new device Devices & networks Puc_1 [CPU 1516-3 PN/DP] CUngrouped devices Se Security settings Common data Common da	Image: Network Image: Connections Image: Connec	Catalog Cearch> Catalog Cearch> Catalog Controller Filter Profile: Catl> Catalo Filter Fordite: Fordit
Name		

Figure 7-29 Update accessible devices

Double-click "Online & diagnostics" under "Accessible device".

oject tree	II (ZT2M_PROFINET_RT_Sample_App1_STANDARD Devices & networks	. • • <u>×</u>	Hardware catalog 👘 🔳
Devices		🛃 Topology view 🛛 🏭 Network view 🛛 🕅 Device	e view	Options
Gamma Control Con	■ ■	Network 1 Connections HM connection Connection	ervi ▲ ►	✓ Catalog ✓earch> ✓ Filter ✓ Frofile: colls
 We Cross-device functions Image: Image: Image	=	CPU 1516-3 PN/ Standard, MRP RZ/T2 CONSISTENT CONSIS	device_1 2	Controllers MM Coystems Orives & starters
	₩ 2 5 6.30 % 9	Image: Second) 	A Detecting & Monitoring Distributed I/O Power supply and distribution Field devices
 ASIX AX88179 USB 3.0 to Gigabit Ethe Update accessible devices Display more information 	met	Compile C	to 2	• 🛅 Other field devices
Lpronnet interface_1 [192.168 LAccessible device [74-90-50-10-E9- LAonine & diagnostics Details view	-07]	Project RZT2M_PROFINET_RT_Sample_App1_STANDARD opened. Scanning for devices on interface ASIX AX88179 USB 3.0 to Gigabit Ethernet Adapter was st Scanning for devices completed for interface ASIX AX88179 USB 3.0 to Gigabit Ethernet Ada		





Click "Assign PROFINET device name" under "Functions".

Enter the device name (rzt2 or rzn2) in the "PROFINET device name" field and click the "Assign name" button.

Diagnostics General	Assign PROFINET dev	vice name				*
▼ Functions						
Assign IP address		Configured	PROFINET dev	ice		
Reset to factory settings		PROFINE	Tdevice name:	rzt2		
		Co	nverted name:			
			Device type:	RSK-RZT2		
		Device filter				
		Only	show devices of	the same type		
4		Only	show devices wi	th bad parameter settings		
		Only	show devices wi	thout names		
	Accessible de	vices in the network	:			
	IP address	MAC address	Device	PROFINET device name	Status	
						- 11
						- 11
						- 11
						- 11
			LED flas	hes Upda	te list Assign name	

Figure 7-31 Assign PROFINET device name

When the ERROR indicator on the real PLC does not light and the RUN/STOP indicator lights green, the PROFINET connection has been successfully established.



8. Annex

8.1 Shared memory Application

The shared memory application separates application processing and network communication, exchanging necessary data via shared memory. The host handles application processing, while the remote handles network communication.







8.1.1 API

API used by the host in the implementation of the application

- (1) PNIO_SHM_Read_PnStatus
- Macro Definition: PNIO_SHM_Read_PnStatus (data)
- Location: PnUsr_SharedMemory.h
- Description: Get communication establishment status.

(2) PNIO_SHM_Read_Output

- Macro Definition: PNIO_SHM_Read_Output(slot , subslot , data)
- Location: PnUsr_SharedMemory.h
- Description: Get Output data, data stored by Remote.

(3) PNIO_SHM_Read_Input

- Macro Definition: PNIO_SHM_Read_Input(slot , subslot , data)
- Location: PnUsr_SharedMemory.h
- Description: Get Input data, which is used to determine the effective data size of Input.

(4) PNIO_SHM_Write_Input

- Macro Definition: PNIO SHM Write Input(slot , subslot , data)
- Location: PnUsr SharedMemory.h
- Description: Set Input data, data stored by Host.

(5) PNIO_SHM_Input_SwitchBank

- Macro Definition: PNIO_SHM_Input_SwitchBank()
- Location: PnUsr SharedMemory.h
- Description: Flush input data for remote reference.

8.1.2 API usage example

See the MainAppl function in the following file

profinet_sdk\src\ext\EK47\pn_ioddevkits\src\application\App5_SharedMemory_Host\usriod_main_host.c

8.1.3 Core to Core communication

The dual-core project is realizing shared-memory applications through inter-core communication. In core-to-core communication, CPU0 is the host and CPU1 is the remote.

8.1.4 Access to shared memory using the Serial Host Interface (SHOSTIF)

The projects in Table 8-1 are sample programs using the RZ/N2L's Serial Host Interface (SHOSTIF). The host accesses remote shared memory using SHOSTIF.

 Table 8-1 SHOSTIF sample project

Projects	Description
rzn2l_shost_remote	N2L Serial Host Interface Project for Remote
rzn2l_shost_host	N2L Serial Host Interface Project for Host (RAM Debug Mode)
rzn2l_shost_host_xspi_boot	N2L Serial Host Interface Project for Host (xSPI Boot Mode)



8.1.4.1 How the SHOSTIF sample project works

(1) Hardware Configurations

The host reads and writes remote shared memory, by communicating with the remote SHOSTIF by SPI communication. The remote generates an interrupt signal in the communication after initialization.

The remote reflects the data in the shared memory to the PROFINET frame, which is transmitted to the PLC.



Figure 8-1 Hardware Configuration

(2) Jumper Settings

Table 8-2 Jumper Settings

Jumpers	Host settings	Remote settings
CN8	Shorted Pin 2-3	Shorted Pin 2-3
CN17	Shorted Pin 1-2	Shorted Pin 1-2
CN20	Shorted Pin 1-2	Shorted Pin 2-3
CN21	Shorted Pin 1-2	Shorted Pin 2-3
CN22	Shorted Pin 1-2	Shorted Pin 1-2
CN24	Shorted Pin 2-3	Shorted Pin 2-3
CN25	Shorted Pin 1-2	Shorted Pin 1-2
CN27	Shorted Pin 1-2	Shorted Pin 2-3
CN29	Shorted Pin 1-2	Shorted Pin 1-2

(3) Switch Settings

Table 8-3 SW4 Settings

SW4	1	2	3	4	5	6	7	8
Host (RAM Debug Mode)	ON	OFF	ON	ON	OFF	OFF	ON	OFF
Host (xSPI Boot Mode)	ON	ON	ON	ON	OFF	OFF	ON	OFF
Remote	ON	ON	ON	ON	OFF	OFF	OFF	OFF

Table 8-4 SW8 Settings

SW8	1	2	3	4	5	6	7	8	9	10
Host	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
Remote	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF

Table 8-5 SW11 Settings

SW11	1	2	3	4	5	6	7	8	9	10
Host	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
Remote	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF



(4) Connecting Host and Remote

Connect the host to the remote.

Host			Remote	
J26.1	SPI_SSL20(P21_1)	⇔*	CN4.4	HSPI_CS#(P16_0
J26.2	SPI_MOSI2(P18_5)	⇔*	CN4.5	HSPI_IO0(P14_1)
J26.3	SPI_MISO2(P18_6)	⇔*	CN4.6	HSPI_IO1(P14_3)
J26.4	SPI_RSPCK2(P18_4)	⇔*	CN4.3	HSPI_CK(P14_2)
J26.6	3.3V	⇔*	CN17.3	3.3V
J21.8	GND	⇔*	J22.8	GND
JA5-A.9	IRQ14(P2_2)	\Leftrightarrow	CN22.3	MBX_HINT#(P12_4)

*Since the host SPI is 3.3V and the remote SHOSTIF is 1.8V, a level shifter is required to connect them.

(5) Operation Check

Let the remote and the PLC communicate first, and then start the host. If the data of the remote transmission frame is "a3", the connection is correct.

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53248 55.876919	RenesasE 10:e9:07	Siemens 49:9d:d1	PNIO	86 RTC1		0x8000.	Len:	66.	Cvc	le:476	80 (Vali	d. Pi	rimar	v.Ok.Ru	n
53249 55.879001	Siemens 49:9d:d1	RenesasE 10:e9:07	PNIO	90 RTC1		0x8000.	Len:	66.	Cvc	le:583	04 (Vali	d. Pi	rimar	v.Ok.Ru	n)
53250 55.879006	RenesasE 10:e9:07	Siemens 49:9d:d1	PNIO	86 RTC1		0x8000,	Len:	66,	Cyc	le:477	44 (Vali	d, Pi	rimary	,Ok,Ru	n)
53251 55.881101		RenesasE 10:e9:07	PNIO	90 RTC1	I. ID:0	0x8000,	Len:	66,	Cvc	le:583	68 (Vali	d, Pi	rimary	,Ok,Ru	n)
53252 55.881105	RenesasE 10:e9:07		PNIO	86 RTC1	, ID:0	0x8000,	Len:	66,	Cyc	le:478	08 (Vali	d, Pi	rimary	,Ok,Ru	n)
53253 55.883006		RenesasE 10:e9:07	PNIO	90 RTC1	, ID:0	0x8000,	Len:	66,	Cyc	le:584	32 (Vali	d, Pi	rimary	,Ok,Ru	n)
53254 55.883029	RenesasE 10:e9:07	Siemens 49:9d:d1	PNIO	86 RTC1	I, ID:0	0x8000,	Len:	66,	Cyc	le:478	72 (Vali	d, Pi	rimary	,Ok,Ru	n)
53255 55.885053	Siemens 49:9d:d1	RenesasE 10:e9:07	PNIO	90 RTC1	I, ID:0	0x8000,	Len:	66,	Cyc	le:584	96 (Vali	d, Pi	rimary	,Ok,Ru	n)
53256 55.885062	RenesasE 10:e9:07	Siemens 49:9d:d1	PNIO	86 RTC1	I, ID:0	0x8000,	Len:	66,	Cyc	le:479	36 (Vali	d, Pi	rimary	,Ok,Ru	n)
53257 55.886942	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1	I, ID:0	0x8000,	Len:	66,	Cyc	le:585	60 (Vali	d, Pi	rimary	,Ok,Ru	n)
53258 55.886947			PNIO	86 RTC1	I, ID:0	0x8000,	Len:	66,	Cyc	le:480	00 (Vali	d, Pi	rimary	,Ok,Ru	n)
53259 55.888523			PNIO	90 RTC1	., ID:0	0x8000,	Len:	66,	Cyc	le:586	24 (Vali	d, Pi	rimary	,Ok,Ru	n)
53260 55.888528	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1	L, ID:0	0x8000,	Len:	66,	Cyc	le:480	64 (Vali	d, Pi	rimary	,Ok,Ru	n)
53261 55.890640	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1	L, ID:0	0x8000,	Len:	66,	Cyc	le:586	88 (Vali	d, Pi	rimary	,Ok,Ru	n)
53262 55.890649	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1	l, ID:0	0x8000,	Len:	66,	Cyc	le:481	28 (Vali	d, Pi	rimary	,Ok,Ru	n)
<					·	[*]	•		-		/			•		
> Frame 53254: 86 b	ytes on wire (688 bi	its), 86 bytes captu	ired (0000 ec	1c 5d	d 49 9d	d1 74	90	50 1	0 e9 0	7 8	8 92	80	00	··]I··t	• P••
> Ethernet II, Src:	RenesasE_10:e9:07 ((74:90:50:10:e9:07),	Dst:	0010 a3	<u>00 00</u>	00 00	00 00	00	00 e	0 00 0	0 00	0	00	00	• • • • • • •	• • • •
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PROFINET IO Cycli	c Service Data Unit:	: 66 bytes		0030 00	00 00	00 00	00 00	00	00 e	0 00 0	0 00	ə 00	00	00	•••••	• • • • •
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Figure 8-2 Remote transmit frames when the host starts



The data in the remote transmitted frame changes by pressing SW1 or SW2 on the host.

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	73648 77.147120	Stemens_49:90:01	Reflesase_10:e9:07	PNIO	90 KTC	. , L , L ,		3000,	Len:	66,	Cyci	.e:528	40	Vali	רק וו. רק ווי	rimary	/, UK, K	uri)	
	73649 77.14/123	Kenesase_10:e9:07	Stemens_49:90:01	PNIO		.L, 1		3000,	Len:	66,	Cyci	.e:422	40 (Vali	רק ויי.	rimary	/, UK, K	uri)	
	73650 77.149230	Stemens_49:90:01	Refiesase_10:e9:07	PNIO	90 KTC	.L, 1		3000,	Len:	66,	Cyci	.e:529	28 (vali	רקים. חו⊳	rimary	/, UK, K	un)	
	73651 77.149235	RenesasE_10:e9:07	Siemens_49:9d:dl	PNIO	86 KTC	.l, 1	TD:0X	3000,	Len:	66,	Cyci	.e:423	04 (vali	a, P	rimary	/, UK, K	un)	
	/3652 //.152252	Siemens_49:9d:dl	Renesase_10:e9:07	PNIO	90 RTC	. 1, 1	ID:0X	3000,	Len:	66,	Cycl	.e:529	92 (vali	a, P	rimary	/,UK,K	un)	-
	/3653 //.152256	RenesasE_10:e9:07	Siemens_49:9d:dl	PNIO	86 RTC	.1, 1	ID:0X8	3000,	Len:	66,	Cyci	.e:423	68 (vali	a, P	rimary	/, UK, K	(un)	
	/3654 //.155114	Siemens_49:9d:dl	RenesasE_10:e9:07	PNIO	90 RTC	.1, 1	TD:0X	3000,	Len:	66,	Cyci	.e:530	56 (vall	a, P	rimary	/, UK, K	un)	
	/3655 //.155119	RenesasE_10:e9:0/	Siemens_49:9d:d1	PNIO	86 RTC	1, 1	1D:0X8	3000,	Len:	66,	Cycl	.e:424	32 (Vali	d,P	rimary	/,0K,R	lun)	
	/3656 //.158111	Siemens_49:9d:d1	RenesasE_10:e9:0/	PNIO	90 RTC	1, 1	1D:0X8	3000,	Len:	66,	Cycl	.e:531	20 (Vali	d,P	rimary	/,OK,R	lun)	
	/365///.158120	RenesasE_10:e9:0/	Siemens_49:9d:d1	PNIO	86 RTC	1, 1	1D:0x8	3000,	Len:	66,	Cycl	.e:424	96 (Vali	d,P	rimary	/,OK,R	lun)	
	/3658 //.160194	Siemens_49:9d:d1	RenesasE_10:e9:0/	PNIO	90 RTC	1, 1	1D:0x8	3000,	Len:	66,	Cycl	.e:531	84 (Valı	d,P	rimary	/,OK,R	lun)	
	7365977.160201	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC	1, 1	ID:0x8	3000,	Len:	66,	Cycl	.e:425	60 (Vali	d,P	rimary	/,Ok,R	un)	
	7366077.163029	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC	1, 1	ID:0x8	3000,	Len:	66,	Cyc1	.e:532	48 (Vali	d,P	rimary	/,Ok,R	un)	
	7366177.163034	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC	1, 1	ID:0x8	3000,	Len:	66,	Cyc]	.e:426	24 (Vali	d,P	rimary	/,Ok,R	un)	
	7366277.165054	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC	1, 1	ID:0x8	3000,	Len:	66,	Cyc]	.e:533	12 ((Vali	d,P	rimary	/,Ok,R	un)	
	7366377.165059	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC	1, 1	ID:0x8	3000,	Len:	66,	Cyc]	e:426	88 ((Vali	d,P	rimary	/,Ok,R	un)	
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> E	thernet II, Src:	RenesasE_10:e9:07	(74:90:50:10:e9:07)	, Dst:	0010 a2	2 00	00 0	0 00	00 00	00	00 0	0 00 0	<u>30</u> 0	0 00	00	00	••••	•••	••••
> P	ROFINET cyclic Re	eal-Time, RTC1, ID:0	0x8000, Len: 66, Cy	/cle:4	0020 00	0 00	00 0	0 00	00 00	00	00 0	0 00 0	<u> 90</u> 0	0 00	00	00	••••	•••	••••
Ρ	ROFINET IO Cyclic	c Service Data Unit	: 66 bytes		0030 00	0 00	0000	0 00	00 00	00	00 0	0 00 0	30 0	0 00	00	00	••••	•••	• • • •
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	86609 90.400362	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1,	, ID:0x80	300,	Len:	66,	Cycle	e: 7744	(Va	lid,	Primar	y,Ok,	Run)	
	8661090.400367	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1,	, ID:0x80	300,	Len:	66,	Cycle	:62656	(Va	lid,	Primar	y,Ok,	Run)	
	86611 90.402379	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1,	, ID:0x80	<i>300,</i>	Len:	66,	Cycle	e: 7808	(Va	lid,	Primar	y,Ok,	Run)	
	86612 90.402387	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1,	, ID:0x80	300,	Len:	66,	Cycle	:62720	(Va	lid,	Primar	y,Ok,	Run)	
	8661390.404368	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1,	, ID:0x80	300,	Len:	66,	Cycle	e: 7872	(Va	lid,	Primar	y,Ok,	Run)	
	86614 90.404373	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1,	ID:0x8	300,	Len:	66,	Cycle	e:62784	(Va	lid,	Primar	y,Ok,	Run)	
	86615 90.406364	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1,	ID:0x8	<i>300,</i>	Len:	66,	Cycle	e: 7936	(Va	lid,	Primar	y,Ok,	Run)	
	86616 90.406368	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1,	, ID:0x80	<i>300,</i>	Len:	66,	Cycle	:62848	(Va	lid,	Primar	y,Ok,	Run)	
	8661790.408361	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1,	ID:0x8	<i>900,</i>	Len:	66,	Cycle	e: 8000	(Va	lid,	Primar	y,Ok,	Run)	
	86618 90.408369	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1,	ID:0x80	<i>300,</i>	Len:	66,	Cycle	:62912	(Va	lid,	Primar	y,Ok,	Run)	
	86619 90.410338	Siemens_49:9d:d1	RenesasE_10:e9:07	PNIO	90 RTC1	ID:0x80	<i>300,</i>	Len:	66,	Cycle	: 8064	(Va	lid,	Primar	y,Ok,	Run)	
	86620 90.410343	RenesasE_10:e9:07	Siemens_49:9d:d1	PNIO	86 RTC1	ID:0x80	300,	Len:	66,	Cycle	:62976	(Va	lid,	Primar	y,Ok,	Run)	
	86621 90.411989	Siemens 49:9d:d1	RenesasE 10:e9:07	PNIO	90 RTC1	ID:0x8	300,	Len:	66,	Cycle	e: 8128	(Va	lid,	Primar	y,Ok,	Run)	
	86622 90.411992	RenesasE 10:e9:07	Siemens 49:9d:d1	PNIO	86 RTC1	ID:0x8	200,	Len:	66,	Cycle	:63040	(Va	lid,	Primar	v.Ok.	Run)	
	86623 90.413510		RenesasE 10:e9:07	PNIO	90 RTC1	ID:0x8	200.	Len:	66.	Cvcle	e: 8192	(Va	lid.	Primar	v.Ok.	Run)	
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>	PROFINET cyclic R	al-Time RTC1 TD:	av8000 len: 66 ()	cle:6	0020 00	00 00 00	00	00 00	00	00 00	00 00	00 (00 00	00			
	PROFINET TO Cyclic	c Service Data Unit	· 66 bytes	/	0030 00	00 00 00	00	00 00	00	00 00	00 00	00 (90 00	00			
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Figure 8-4 Remote transmission frame when SW2 is pressed



8.2 **PROFIsafe Application**

The PROFIsafe application connects to the RZ/T2L x2 Functional Safety Reference Board (Safety Board), which is included in the RZ/T2L Safety Network Reference Kit, and processes safety communication by sending PROFIsafe parameters and PDU. As shown in Figure 8-5, the RSK board exchanges safety related communication with the Safety Board via UART interface. To verify functional safety, please refer to the manual included with the RZ/T2L Safety Network Reference Kit for setup of the Safety Board.



Figure 8-5 PROFIsafe Hardware Configuration

Figure 8-6 shows the sequence of PROFIsafe communication with Safety Board. To verify functional safety using PROFIsafe, a PROFIsafe-compatible PLC is required. Verification cannot be performed with CODESYS.



Figure 8-6 PROFIsafe Communication Sequence



8.2.1 API

Main APIs used by the application in communication with the Safety Board.

- (1) psdInterfaceF_App_Cycle
- Function Prototype: void psdInterfaceF_App_Cycle(void)
- Location: psd_interface.c
- Description: Processes PROFIsafe communication events and controls communication with the Safety Board through state machine management.

(2) psdInterfaceReceiveRecord

- Function Prototype: PNIO_UINT32 psdInterfaceReceiveRecord(PNIO_UINT32 RecordIndex, unsigned char *pBuffer,PNIO_UINT32 *pBufLen)
- Location: psd interface.c
- Description: Stores F-Parameters received from the PLC into a buffer and manages them based on the record index.
- (3) psdInterfaceProcessDataReceived
- Function Prototype: void psdInterfaceProcessDataReceived(PNIO_UINT32 slot_num, PNIO UINT32 subslot num, PNIO IOXS Iops)
- Location: psd interface.c
- Description: Stores Output PDU in buffer and sets transmission events.

(4) psdInterfaceSendProcessData

- Function Prototype: void psdInterfaceSendProcessData(PNIO_UINT8 *InDataArray, unsigned short telLen)
- Location: psd interface.c
- Description: Stores Input PDU received from Safety Board in buffer for cyclic communication.
- (5) plsw_parse_cmd_thread_entry
- Function Prototype: void plsw_parse_cmd_thread_entry(void* pvParameters)
- Location: plsw_parse_cmd_thread_entry.c
- Description: Processes UART command reception from the Safety Board and executes command parsing operations.

(6) plsw_rxcmd_start_req

- Function Prototype: void plsw_rxcmd_start_req(void)
- Location:plsw_parse_cmd_thread_entry.c
- Description: Processes start request from Safety Board and sets startup event.

(7) plsw_rxcmd_fparack

- Function Prototype: void plsw_rxcmd_fparack(void)
- Location: plsw_parse_cmd_thread_entry.c
- Description: Processes F-Parameter acknowledgment from Safety Board and stores parameters in buffer.

(8) plsw_rxcmd_inpdu

- Function Prototype: void plsw_rxcmd_inpdu(void)
- Location: plsw_parse_cmd_thread_entry.c
- Description: Processes Input PDU received from Safety Board and stores data in buffer.
- (9) plsw_send_cmd_thread_entry
- Function Prototype: void plsw_send_cmd_thread_entry (void* pvParameters)
- Location: plsw_send_cmd_thread_entry.c
- Description: Handles UART command transmission to the Safety Board.

(10) PLSW_txcmd_start_ack

• Function Prototype: PNIO_UINT8 PLSW_txcmd_start_ack(void)



RZ/T2, RZ/N2

- Location: plsw_send_cmd_thread_entry.c
- Description: Queues start request acknowledgment command for transmission to Safety Board.

(11) PLSW_txcmd_fpram

- Function Prototype: PNIO_UINT8 PLSW_txcmd_fpram(PNIO_UINT8* pBuf)
- Location: plsw_send_cmd_thread_entry.c
- Description: Queues F-Parameter data transmission command to Safety Board.

(12) PLSW_txcmd_run

- Function Prototype: PNIO_UINT8 PLSW_txcmd_run(void)
- Location: plsw send cmd thread entry.c
- Description: Queues run request command for transmission to Safety Board.

(13) PLSW_txcmd_stop

- Function Prototype: PNIO_UINT8 PLSW_txcmd_stop(void)
- Location: plsw_send_cmd_thread_entry.c
- Description: Queues stop request command for transmission to Safety Board.

(14) PLSW_txcmd_outpdu

- Function Prototype: PNIO UINT8 PLSW txcmd outpdu (PNIO UINT8* pBuf)
- Location: plsw_send_cmd_thread_entry.c
- Description: Queues Output PDU transmission command to Safety Board.

8.2.2 Connection Verification

Following the completion of PLC setup as outlined in Section 7.4, the operational verification of Safety communication within the PROFIsafe application may be performed using the procedures detailed below.

- 1) Disconnect the Ethernet cable between the RSK board and the PLC, then set the PLC to STOP mode.
- 2) With power turned OFF, connect the J25 connector on the RSK board to the CON14 connector on the RZ/T2L x2 Functional Safety Reference Board (Safety Board) as follows:

Table 8-7 UART Connection

RSK Boa	rd		RZ/T2L x2 Fu	nctional Safety Reference Board
J25.3	SCI_RXD (P17_7)	⇔*	CON14.3	CON_TXD_A (P18_0)
J25.2	SCI_TXD (P18_0)	⇔*	CON14.2	CON_RXD_A (P17_7)
J25.5	GND	⇔*	CON14.1	GND

Note: For Safety Board connections, please refer to section 4.1 in r30uz0202jj0100.pdf.

- 3) Power ON the RSK board first, then power ON the Safety Board.
- 4) Reconnect the Ethernet cable between the PLC and the RSK board.
- 5) Once the LED on the Safety Board shows "Parameter state", switch the PLC to RUN mode.

When the LED on the Safety Board changes to "I/O Data Processing state", the PROFINET connection has been successfully established.



8.3 How to adapt to a different vendor's PHY chip

Ethernet PHYs introduce delays during receiving and transmitting due to internal data processing. These delays, known as PHY latency or PHY delay, vary depending on the vendor's PHY chip. To adapt to a different PHY chip, it is necessary to apply these delays in the GSDML and software. There are two types of delays: transmission delay and Receive delay. Please obtain the values for each delay from the PHY chip vendor's documentation and official website.

8.3.1 Adaptation of GSDML

In GSDML, please change the attribute values that define transmission delay and receive delay according to the specifications of the PHY chip you want to adapt.

- Target element: PortSubmoduleItem
- Target attributes:
 - MaxPortTxDelay : Transmission delay
 - MaxPortRxDelay : Receive delay

8.3.2 Adaptation of Software

In the software, please change the macro definition values that define transmission delay and receive delay according to the specifications of the PHY chip you want to adapt.

- Target file: profinet_sdk\src\pns\eddp\eddp_llif.h
- Target attributes:
 - EDDP_LL_PHY_PHY_TX_DELAY : Transmission delay
 - EDDP_LL_PHY_PHY_RX_DELAY : Receive delay



Revision History

		Description			
Rev.	Date	Page	Summary		
1.00	May 14, 2025	-	First issued		
1.10	Jun 30, 2025	-	Add PROFIsafe Related.		



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power is supplied until the power reaches the level at which reseting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
- 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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