Renesas RZ Family

RZN2H-EVK Example Project Bundle

Introduction

This RZN2H-EVK Example Project Bundle introduces practical examples projects for the RZN2H-EVK Kit. The Example Projects contained within the bundle show how to write code for the various Renesas Flexible Software Package (FSP) modules supported by the RZN2H-EVK Kit.

Flexible Software Package is an optimized software package designed to provide easy to use, scalable, high-quality software for embedded system design. The primary goal is to provide lightweight, efficient drivers that meet common use cases in embedded systems. FSP code quality is enforced by peer reviews, automated requirements-based testing, and automated static analysis. FSP provides uniform and intuitive APIs that are well documented. Each module is supported with detailed user documentation including example code. FSP modules can be used on any MPU in the RZ family, provided the MPU has any peripherals required by the module. FSP modules can be configured at build-time to optimize the size of the module for the feature set required by the application.

Supported Kit

RZN2H-EVK

Supported FSP Version

FSP v4.3.0

Supported Toolchains

For the latest version of each Integrated Development Environment (IDE) and toolchain listed below, please refer to the FSP release notes:

- e² studio with GCC Arm Embedded (GCC)
- IAR EWARM with IAR toolchain for Arm

1. Using the Example Projects

To use RZN2H-EVK Example Projects, follow the steps mentioned in the following documents:

- Example Project Usage Guide
  rz-fsp-examples/blob/main/example_projects/Example Project Usage Guide.pdf

Users who are new to the FSP are recommended to refer to the section **Starting Development** in the RZ FSP Documentation prior to attempting to program or debug an example project.

2. List of Example Projects Supported on Different Toolchains in the Bundle

The following table lists example projects supported by each IDE. These are ready to import using the import process for each IDE.

Note:

1. Additional example projects other than those mentioned above, may be available in the example project repository. However, they are supported with older version of FSP. Please refer the example_projects/version_info_table.md file in the repository to identify the appropriate FSP version for the example project of interest.
2. All projects supported by e^2 studio/GCC are supported with e^2 studio via port from GCC.

Table 1. IDE Support for the Example Project

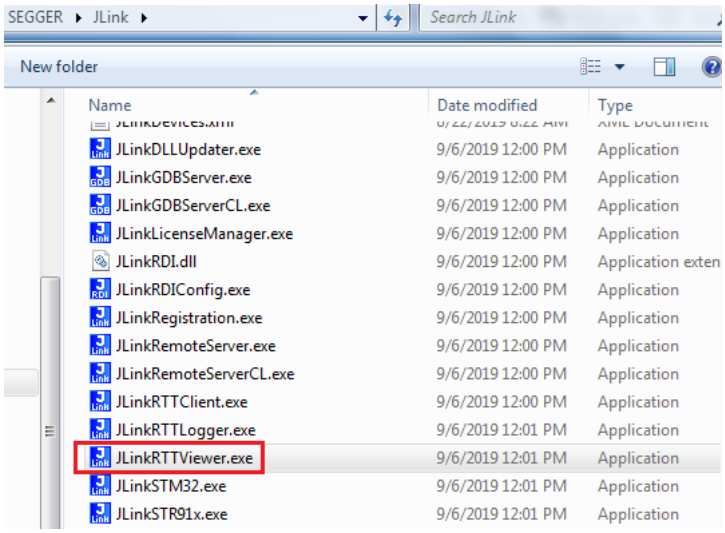
	IDE Support	
Example Project	**e² studio**	**IAR**
FreeRTOSplusTCP	Supported	
adc	Supported	
bsp	Supported	
bsp_multi	Supported	
cmt	Supported	
cmtw	Supported	
crc	Supported	
dmac	Supported	
elc	Supported	
ethernet	Supported	
freertos	Supported	
gpt_phase_count	Supported	
iic_master	Supported	
mtu3_phase_count	Supported	
rtc	Supported	
sci_uart	Supported	
xspi_qspi	Supported	

3. Running the Project

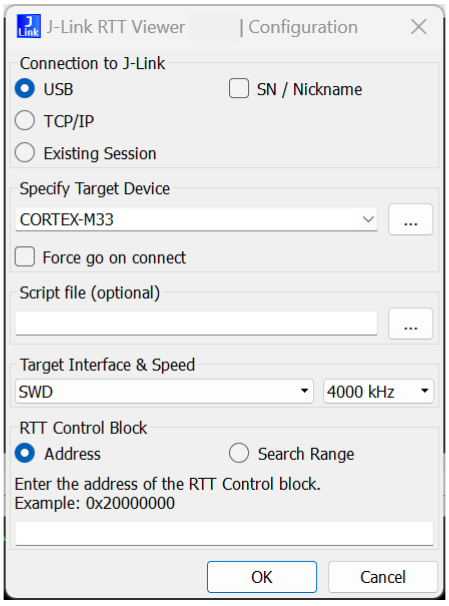
3.1 Connecting with J-Link RTT Viewer

This section is designated for example projects running on Arm Cortex-R as they support J-Link RTT Viewer as terminal console application.

1. Open RTT Viewer by double clicking `JLinkRTTViewer.exe` in the downloaded `/Segger/JLink` folder**.**

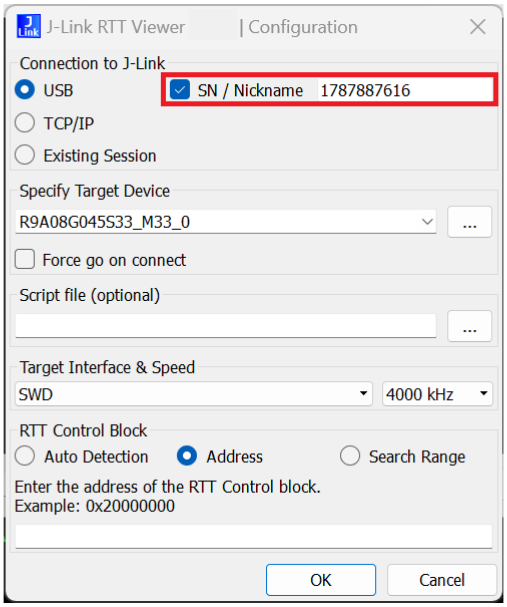


2. On opening, the field **Specify Target Device** shows up as **unspecified**. With USB selected, click on the … tab and select the desired Renesas RZ device. Keep a note of the Core type.

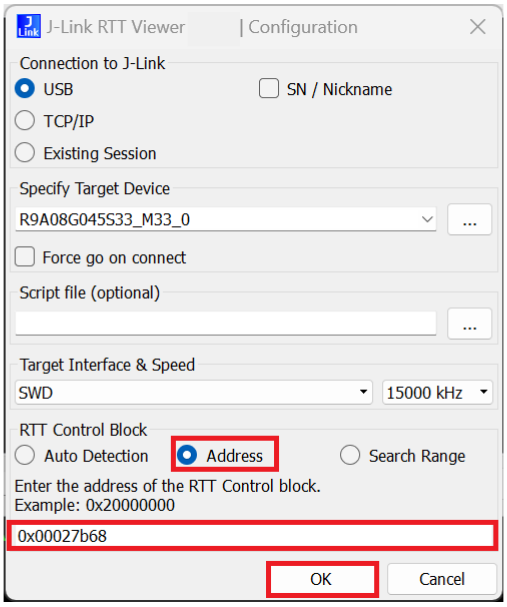


3. If multiple kits are connected to the PC, make sure to choose the corresponding serial number (SN/ Nickname.

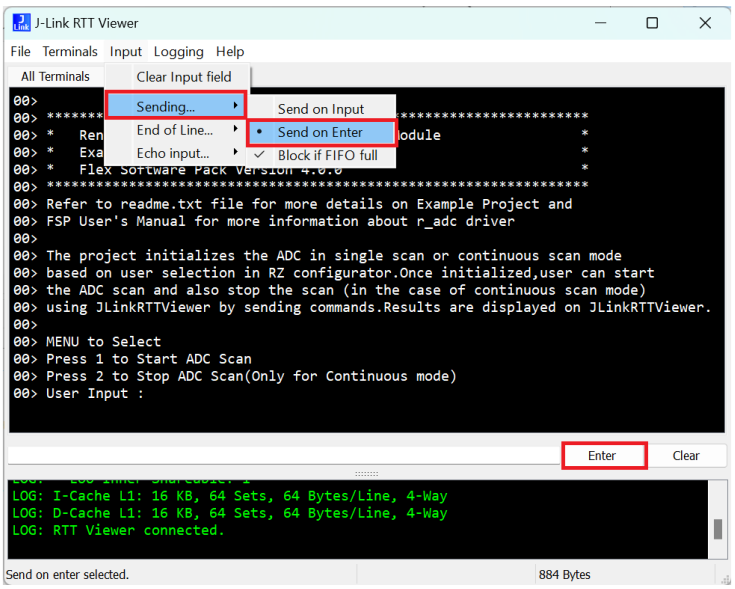
Note: For MPUs, the exact address of the RTT Control Block must be specified. When Auto Detection is used, RTT Viewer parses all RAM memory to find the RTT Block. As TrustZone boundaries are configured for all projects for these MPUs, RTT Viewer will encounter access failures, and you will not see the output logs in RTT viewer. The exact address for the SEGGER_RTT data structure in RAM is found in the readme.txt file associated with the module under evaluation or in the map file when a binary is built. (Refer Appendix for an example).



4. To enter the exact address of the variable into the Address of RTT Control Block, refer the Appendix. Then click **OK**.



5. Click on the **Input** tab and change **Sending** option to **Send on Enter**. Every time input in entered, you must either press the **Enter** or **Enter** tab on the RTT viewer.

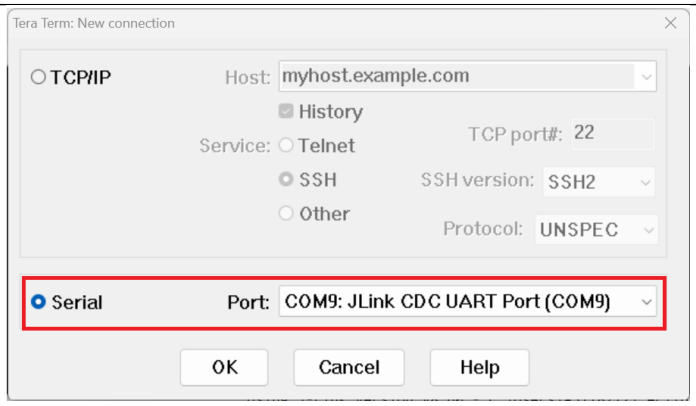


Follow the instructions displayed on the RTT Viewer as shown above. Also refer to `readme.txt` file in the project folder (downloaded.zip file or in https://github.com/renesas/rz-fsp) to run the project.

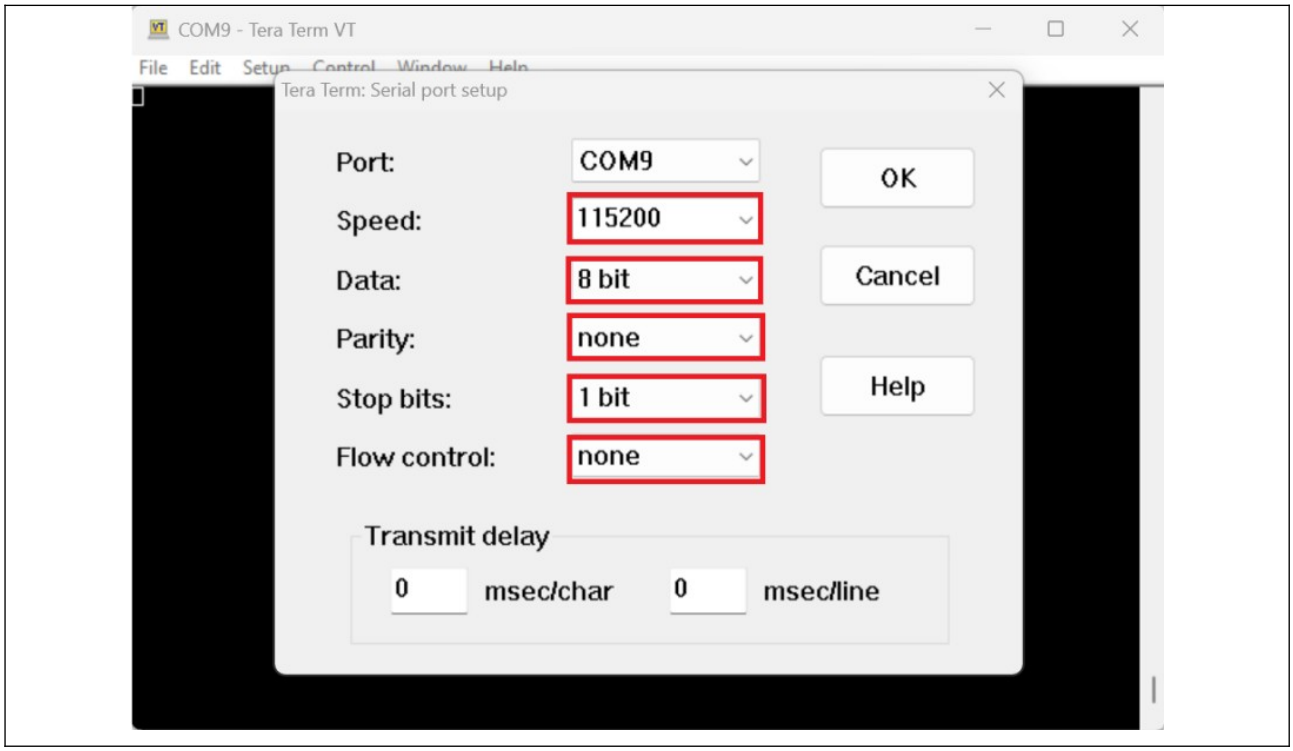
3.2 Connecting with Tera Term

This section is designated for example projects running on Arm Cortex-A as they support Tera Term as terminal console application.

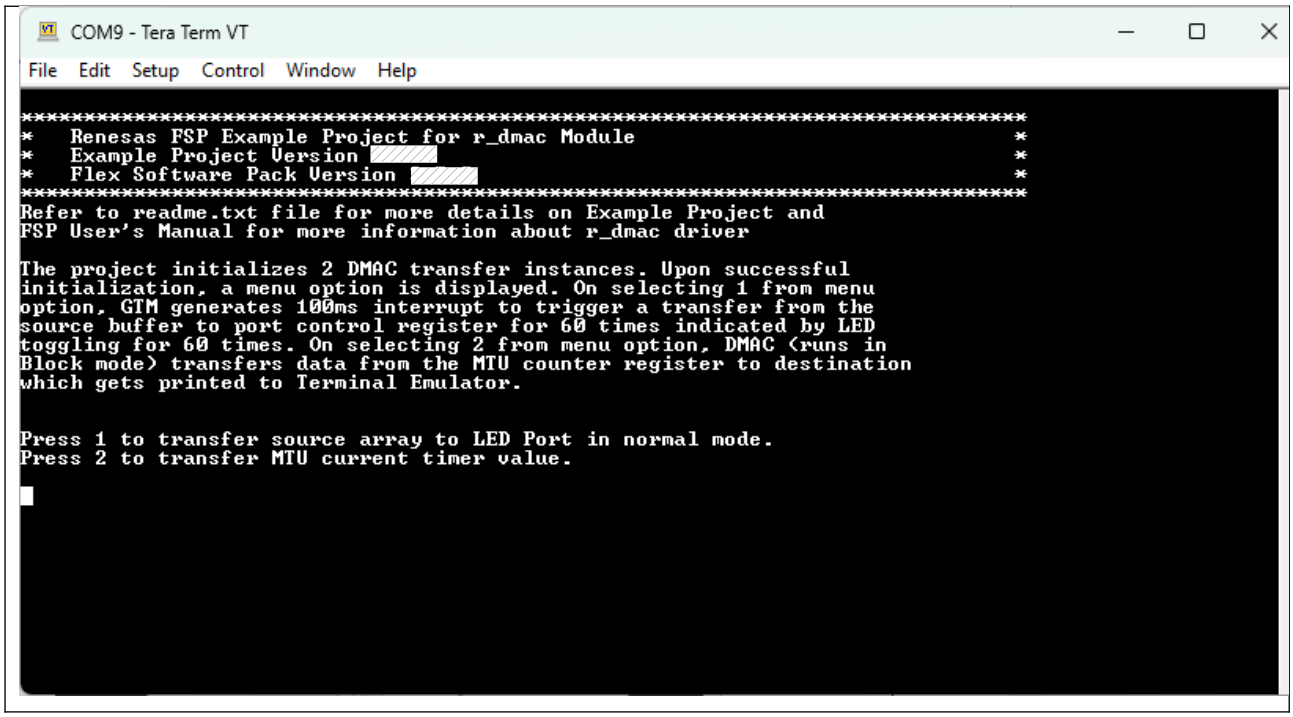
1. Open **Tera Term** by double clicking **ttermpro.exe** in the downloaded folder.
2. Select **Serial port**.



3. Set up **Serial port**.



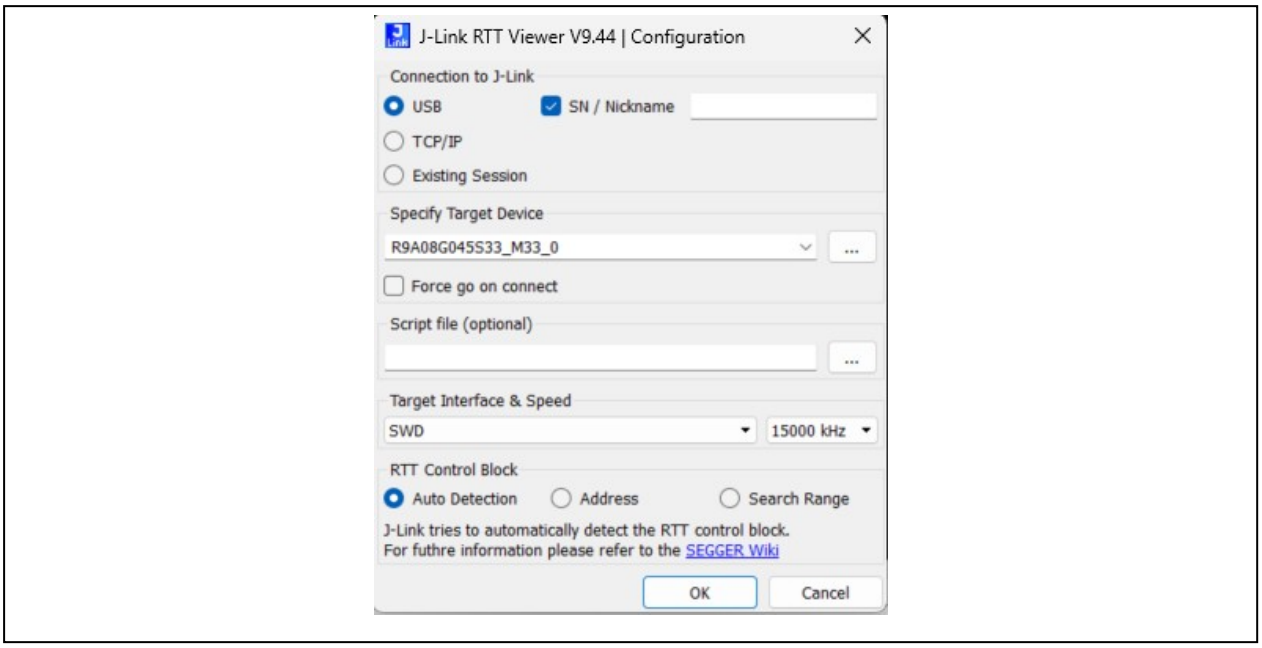
4. Check log in Tera Term.



Appendix

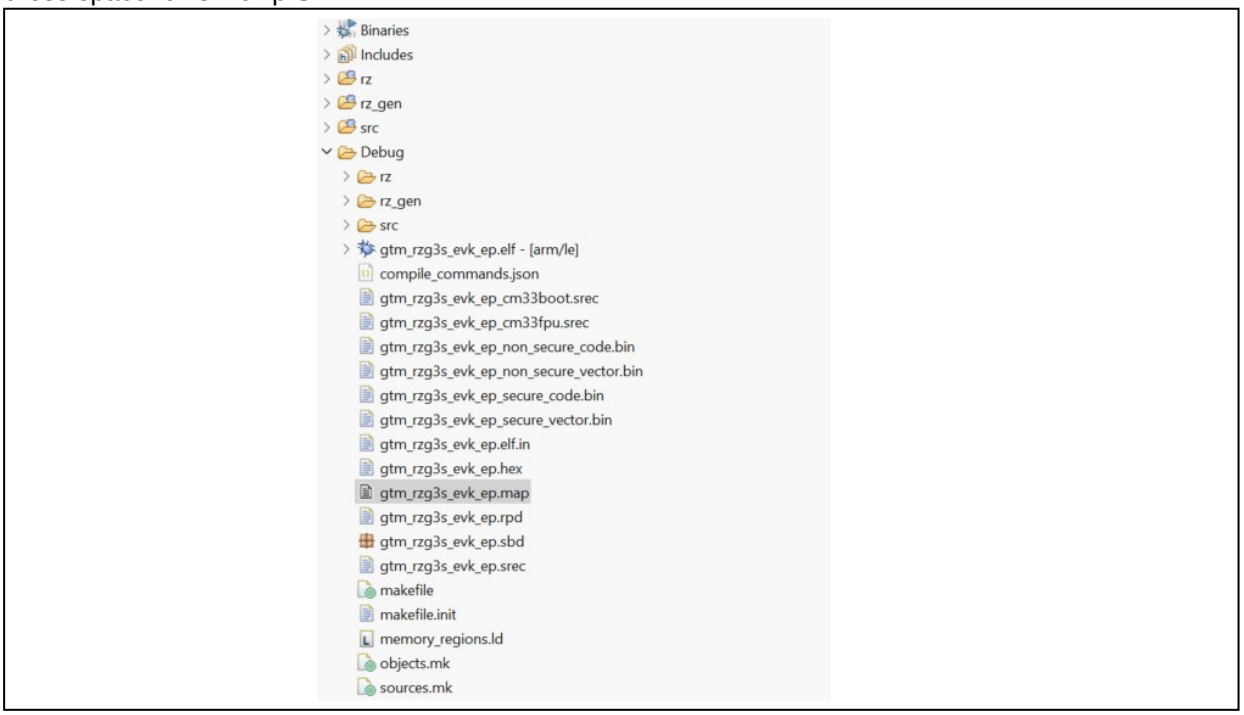
a. Limitations in connecting with J-Link RTT Viewer v9.44 or later

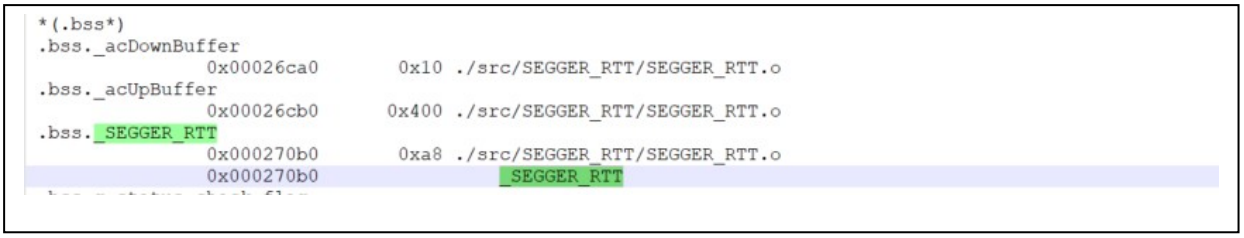
When using Auto Detection option for the RTT Control Block, J-Link RTT Viewer may not be able to find the SEGGER_RTT variable in RAM memory due to restrictions on memory access imposed by TrustZone settings made by the Renesas Device Partition Manager. Restrictions are typically applied for TrustZone Example Projects If the RTT Control Block cannot be found by RTT Viewer, then output from an Example Project may not be visible in the RTT Viewer Console with Auto Detection.



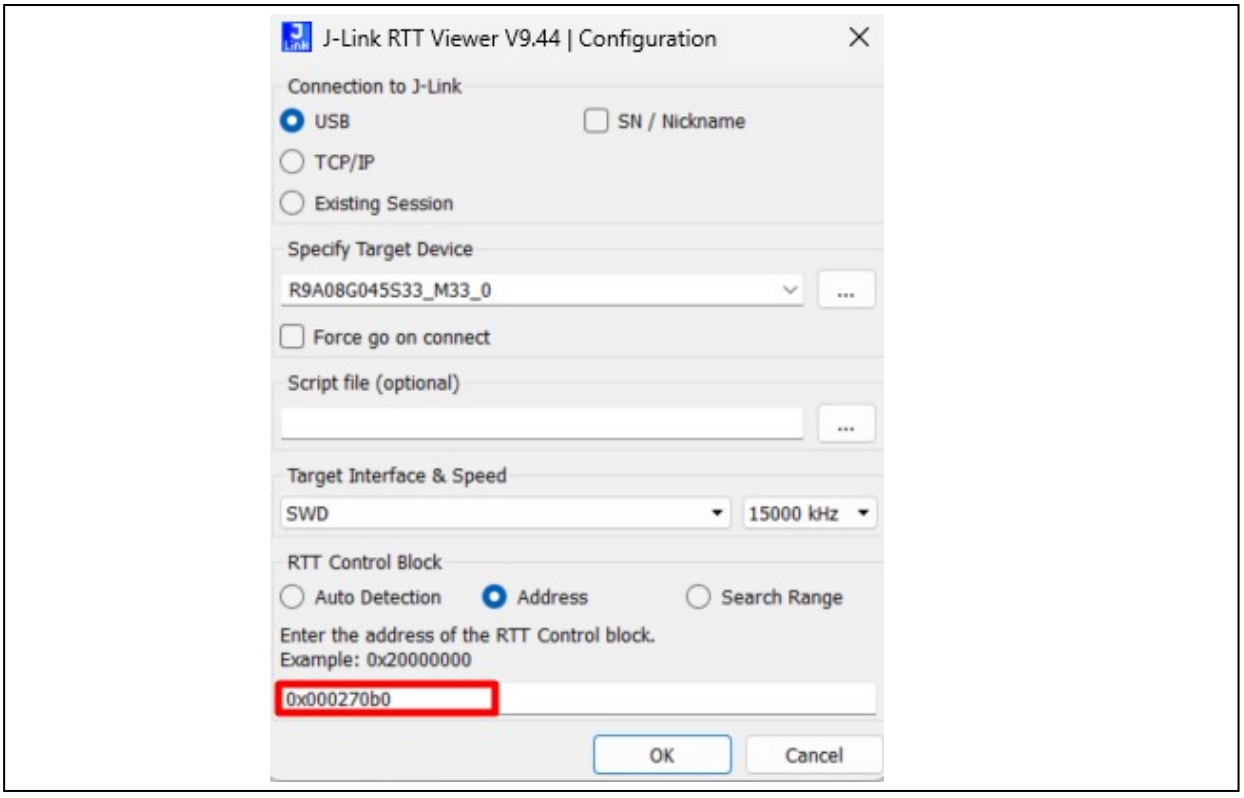
To mitigate this situation, you may use any one of the following approaches:

1. **Method 1:** The recommended approach is to search _SEGGER_RTT variable in the map file, generated upon successfully building a configuration of an Example Project, which is by default located in the address space for On-chip SRAM.

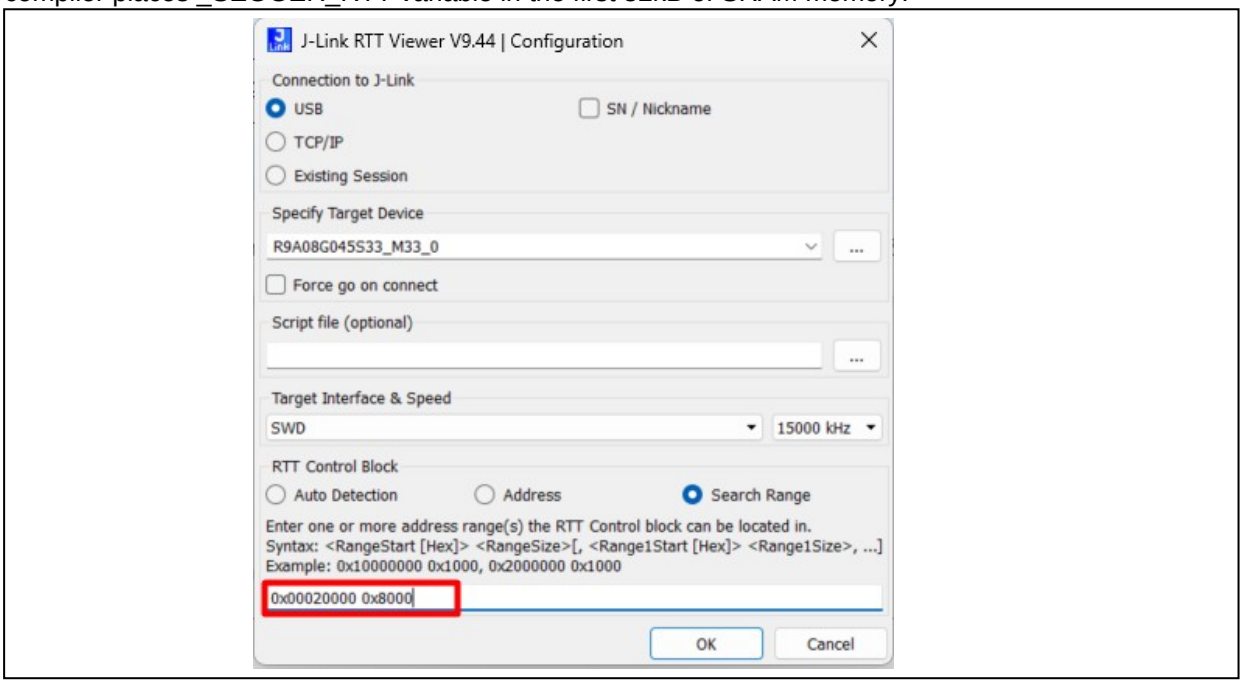




And input the exact address of the variable into the Address Input.



2. **Method 2:** Apply a search range within the first 32kB of SRAM Memory. This approach works when the compiler places _SEGGER_RTT variable in the first 32kB of SRAM memory.



Website and Support

Visit the following URLs to learn about key elements of the RZ family, download components and related documentation, and get support.

RZ Product Information	renesas.com/rz
RZ Product Support Forum	renesas.com/rz/forum
RZ Flexible Software Package	renesas.com/rz-fsp
Renesas Support	renesas.com/support

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
4.00	Mar.04.26	—	First release document on FSPv4.0.0.
4.01	May.08.26	—	Added support on FSPv4.1.0.
4.02	Aug.07.26	—	Added support on FSPv4.2.0.
4.03	Nov.12.26	—	Added support on FSPv4.3.0.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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