RZ/N1D, RZ/N1S, RZ/N1L group

External Bus Interface (MSEBI) configuration guide

Introduction

The application note is described about two examples of use case for Medium Speed External Bus Interface (MSEBI) of RZ/N1 group device. The first example is 8-bit synchronous connection and second one is 16-bit asynchronous connection.

The 8-bit synchronous connection is explained by direct connection of two RZ/N1S or RZ/N1D CPU (hereinafter refer to as “RZ/N1x”). Two set of RZ/N1x CPU boards and RZ/N1 expansion boards are used in the explanation.

The 16-bit asynchronous connection is explained by connection of RZ/N1x and external SRAM. However, user need to prepare boards which has SRAM connected to MSEBI of RZ/N1x by own because it’s not on the RZ/N1x CPU board or RZ/N1 expansion board.

Target Device

RZ/N1D

RZ/N1S

Contents

1. Specification 3
2. Operation confirmation conditions 5
3. Related application note 5
4. Hardware described 6
4.1 Hardware construction 6
4.1.1 8-bit synchronous connection 6
4.1.2 16-bit asynchronous connection 6
4.2 List of target pins 7
4.2.1 8-bit synchronous connection 7
4.2.2 16-bit asynchronous connection 8
5. Software description 8
5.1 Operation summary 8
5.1.1 8-bit synchronous connection 8
5.1.2 16-bit asynchronous connection 8
5.2 Register configuration 9
5.2.1 8-bit synchronous connection 9
5.2.1.1 Burst access by CPU 9
5.2.1.2 Burst access by DMA 11
5.2.2 16-bit asynchronous connection 14
5.3 Constants 15

5.4 Variables 15
5.5 Functions 16
5.6 Function specification 16
5.7 Flowchart 17
5.7.1 Main processing 17
5.7.2 Initialization processing 19
5.7.3 Writing and reading processing 21
5.8 Setting of drive strength 24

6. Sample program 25

7. Reference documents 25

Revision History 26

1. Specification

The connecting configuration used in this application note is shown in Table 1.1.

Table 1.1 Connecting configuration

	8-bit synchronous connection		16-bit asynchronous connection
Master device	RZ/N1x		RZ/N1x
Slave device	RZ/N1x		External SRAM
Bus width	8bit		16bit
Sync/Async	Synchronous		Asynchronous
Access mode	Burst access		Single access
Bus master	CPU	DMA	CPU

The master device writes and reads the data to/from the slave device via MSEBI. The two types of connecting configurations are described below.

1) 8-bit synchronous connection

One of the two RZ/N1x is MSEBI master and the other is MSEBI slave. The MSEBI master is connected to the MSEBI slave with the 8-bit bus width. The block diagram for 8-bit synchronous connection is shown in Figure 1.1. The MSEBI master and the MSEBI slave communicates with synchronous mode. In this application note, MSEBI burst access by CPU and the MSEBI burst access by DMA are explained.

2) 16-bit asynchronous connection

The RZ/N1x as MSEBI master is connected to the external SRAM, which is as a slave device, with the 16-bit bus width. The block diagram for 16-bit asynchronous connection is shown in Figure 1.2. The MSEBI master communicates with asynchronous mode. In this application note, MSEBI single access by CPU is explained. Regarding DMA access, please refer to relevant section of 8-bit synchronous connection.

Figure 1.1 Block diagram (8-bit synchronous connection)

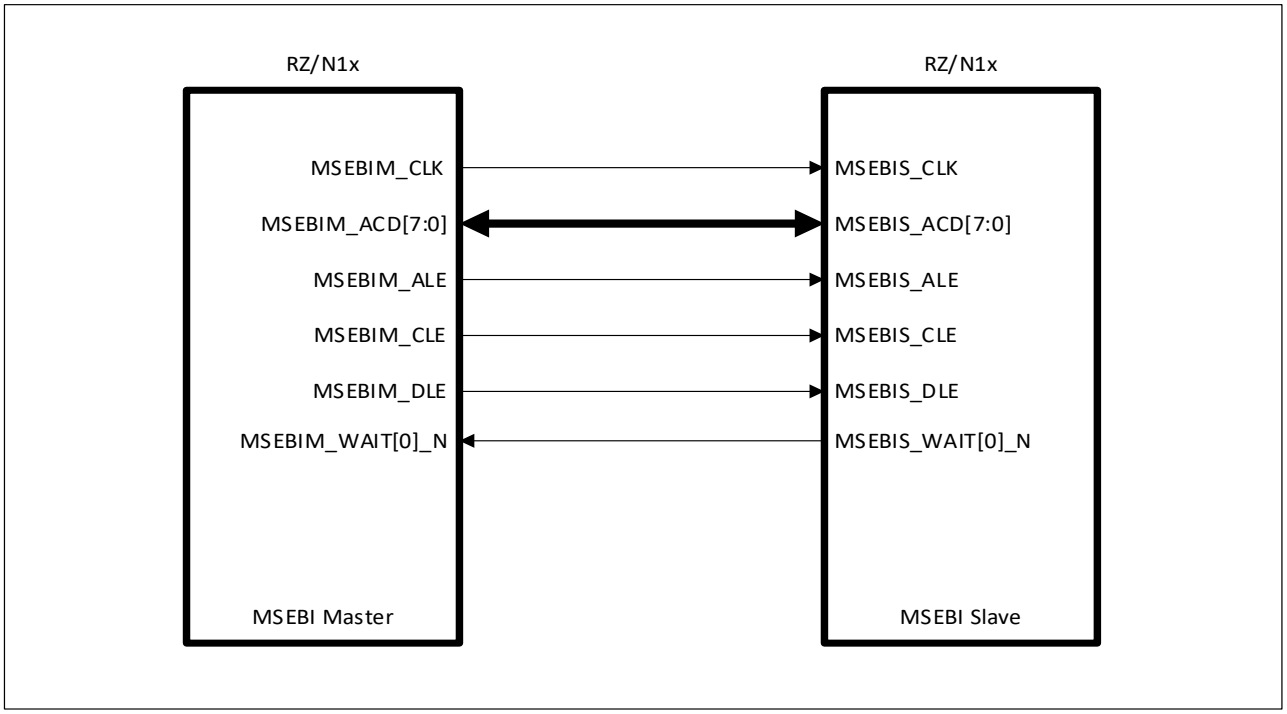

Figure 1.2 Block diagram (16-bit asynchronous connection)

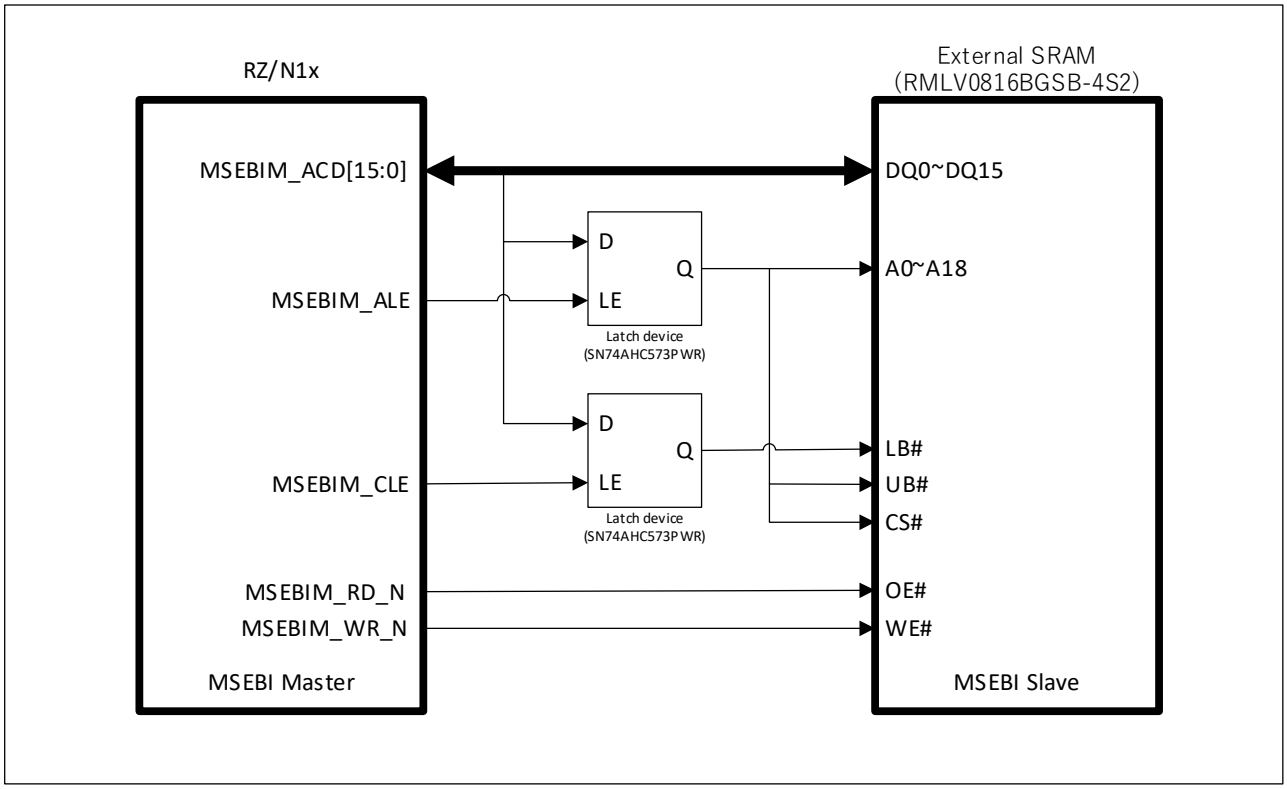

Table 1.2 shows the peripheral functions and usages.

Table 1.2 Peripheral functions and usages

Peripheral functions	Usages
MSEBI	Connected with RZ/N1x or external SRAM
DMAC	Data transfer between MSEBI and internal RAM

Table 1.3 shows the specification of the external SRAM.

Table 1.3 Specification of the external SRAM (RMLV0816BGSB-4S2)

Items	Contents
Product name	RMLV0816BGSB-4S2 (Made by Renesas Electronics)
Construction	512K words x 16bit
Capacity	8Mbits
Access time	45ns (max.)

2. Operation confirmation conditions

The sample program is confirmed to operate under the conditions shown in Table 2.1.

Table 2.1 Operation confirmation conditions

Items	Contents
Target microcomputer	R9A06G032NGBG (RZ/N1D) R9A06G033NGBG (RZ/N1S)
CPU	Arm® Cortex®-A7 Arm® Cortex®-M3
Operating frequency	Main clock: 40MHz System clock: 125MHz Cortex-A7: 500MHz (4 multiplication of the system clock) Cortex-M3: 125MHz MSEBI_HCLK: 125MHz
Drive strength	MSEBI clock pin: 8mA Pins other than the clock: 4mA
Operating voltage	3.3V
Integrated development environment	IAR Embedded Workbench for ARM 8.30.2
Version of bare metal driver	MSEBI driver: 1.7 DMAC driver: 1.11 (See solution kit V1.4.4)
Version of sample program	Version 2.00
Target board	RZ/N1x CPU board RZ/N1 expansion board External SRAM connection board (not sale)
External SRAM	Renesas RMLV0816BGSB-4S2(512K word x 16bit)

3. Related application note

The application notes related to this application note are shown below. Please see also.

RZ/N1xGroup (D, S, L) Bare Metal Drivers Rev.0.19 (R11AN0282EJ0019)

In the sample program of this application note, bare metal drivers in the above application note are used. Revision of the drivers are as of the writing of this application note and may not be latest.

Please find the latest revision on the Renesas Electronics website and replace with it.

4. Hardware described

4.1 Hardware construction

4.1.1 8-bit synchronous connection

First, please set a dip switch and a boot loader in refer to “RZ/N1x Group CONNECT IT! – ETHERNET RZ/N1x Quick Start Guide”.

One RZ/N1x CPU board, which is as the MSEBI master device, is connected to the other board, which is as the MSEBI slave device, with the CN7 connector in RZ/N1 expansion board as Figure 4.1. Regarding to the pin configuration, please refer to “List of target pins”. In addition, the SW5 dip switch 3 should be set to “ON”.

Note: The drive strength and the MSEBI clock frequency (MSEBI_CLK) should be adjusted depending on the length of writing between boards. Please refer to Section 5.8 for details regarding to the drive strength. In addition, the length of wiring when this sample program was tested is about 15cm.

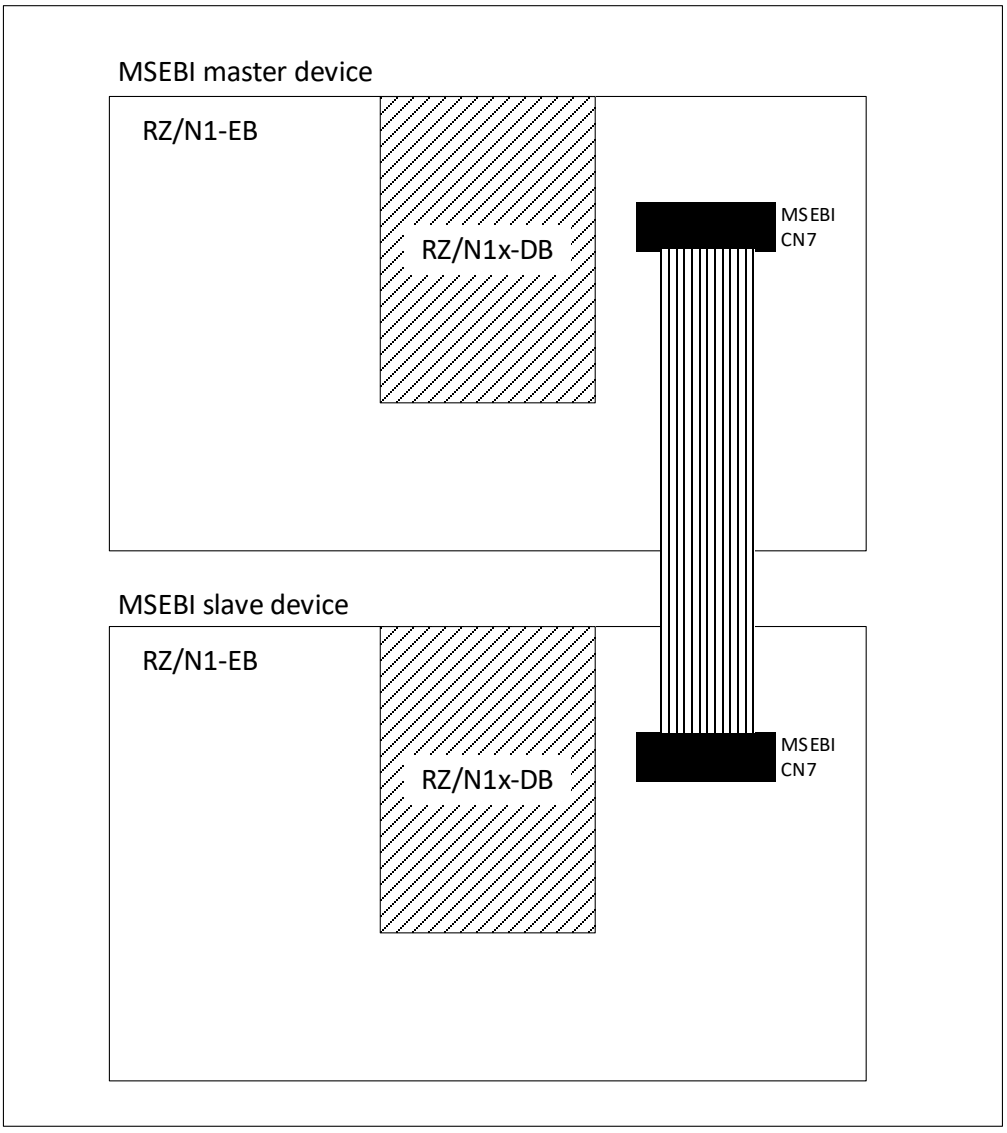

Figure 4.1 Connection construction using RZ/N1x-DB

4.1.2 16-bit asynchronous connection

Since the specification of address data multiplex of MSEBI is unique, a dedicated latch circuit should be implemented for connection with devices with a parallel bus. Please contact support for more information.

4.2 List of target pins

4.2.1 8-bit synchronous connection

Table 4.1 shows the target signals and functions for MSEBI master.

Table 4.1 Target signals and functions (MSEBI master)

signal name	I/O	Description
MSEBIM_CLK	Output	Clock
MSEBIM_ACD[7:0]	Input/output	Multiplexing of Address, control data and data
MSEBIM_ALE	Output	Address latch enable
MSEBIM_CLE	Output	Address and control latch enable
MSEBIM_DLE	Output	Data latch enable
MSEBIM_WAIT[0]_N	Input	Input of waiting signal by slave device

Table 4.2 shows the target signals and functions for MSEBI slave.

Table 4.2 Target signals and functions (MSEBI slave)

signal name	I/O	Description
MSEBIS_CLK	Input	Clock
MSEBIS_ACD[7:0]	Input/output	Multiplexing of Address, control data and data
MSEBIS_ALE	Input	Address latch enable
MSEBIS_CLE	Input	Address and control latch enable
MSEBIS_DLE	Input	Data latch enable
MSEBIS_WAIT[0]_N	Output	Output of waiting signal by slave device

Table 4.3 shows the correspondence of the connected pins in RZ/N1 expansion board for the master and slave devices.

Table 4.3 Correspondence of the connected pins

signal name	Connector: CN7	
	MSEBI master	MSEBI slave
MSEBI(y)_ACD[0]	Pin 3	Pin 3
MSEBI(y)_ACD[1]	Pin 4	Pin 4
MSEBI(y)_ACD[2]	Pin 5	Pin 5
MSEBI(y)_ACD[3]	Pin 6	Pin 6
MSEBI(y)_ACD[4]	Pin 7	Pin 13
MSEBI(y)_ACD[5]	Pin 8	Pin 11
MSEBI(y)_ACD[6]	Pin 9	Pin 15
MSEBI(y)_ACD[7]	Pin 10	Pin 17
MSEBI(y)_CLK	Pin 11	Pin 8
MSEBI(y)_ALE	Pin 13	Pin 7
MSEBI(y)_CLE	Pin 15	Pin 9
MSEBI(y)_DLE	Pin 17	Pin 10
MSEBI(y)_WAIT[0]_N	Pin 19	Pin 19

For MSEBI master interface, MSEBI(y) represents MSEBIM. Whereas for MSEBI slave interface, MSEBI(y) represents MSEBIS.

4.2.2 16-bit asynchronous connection

Table 4.4 shows the target signal and functions for MSEBI master.

Table 4.4 Target signal and functions (MSEBI master)

signal name	I/O	Description
MSEBIM_ACD[15:0]	Input/output	Multiplexing of Address, control data and data
MSEBIM_ALE	Output	Address latch enable
MSEBIM_CLE	Output	Address and control latch enable
MSEBIM_WR_N	Output	Write enable
MSEBIM_RD_N	Output	Read enable

5. Software description

5.1 Operation summary

The master device writes 32K bytes data to the RAM area of slave device and then reads the written data from slave device. Finally, the master device compares the written data and the read data and confirms whether correctly write and read.

5.1.1 8-bit synchronous connection

This subsection describes about the software operation for the MSEBI burst access by CPU and DMA.

One MSEBI burst access can write or read 1K bytes data maximally and repeats ALE phase, CLE phase and DLE phase for each access.

(1) Burst access by CPU

The master device writes data in the base address area of the chip select 0 (CS0). The master device sends the end of block event (CPUTX) to the slave device after sent all data. Next, after waiting for a second, the master device reads the data from the CS0 base address area. When all data is completed to be received, the master device sends the end of block event (CPURX) to the slave device.

Whereas the slave device waits until detecting the end of block event from the master device. When the end of block event is detected by the MSEBI slave interrupt, the slave device finishes the waiting processing.

(2) Burst access by DMA

For write access from the master device to slave device using DMA, the DMA transmit FIFO address is set as DMA transfer destination. For read access, the DMA receive FIFO address is set as DMA transfer source.

The master device starts the DMA transfer by setting DMA transmit enable bit of MSEBI. When all data is completed to be sent, the master device sends the end of block event (DMATX) to the slave device. Next, after waiting for a second, the master device starts the DMA transfer by setting the DMA receive enable bit of MSEBI. When all data is completed to be received, the master device sends the end of block event (DMARX) to the slave device.

Whereas the slave device performs the same processing as the burst access by CPU.

5.1.2 16-bit asynchronous connection

This subsection describes about the software operation for MSEBI single access by CPU

One MSEBI single access repeats ALE phase, CLE phase and DLE phase for each access.

The master device writes the data to the CS0 base address area. When all data is completed to be sent, the master device waits for a second. Next, the master device reads the data from the CS0 base address area. When all data is completed to be received, the master device performs the comparing processing.

5.2 Register configuration

5.2.1 8-bit synchronous connection

5.2.1.1 Burst access by CPU

Table 5.1 to Table 5.4 shows the register configuration of MSEBI master and Table 5.5 to Table 5.8 shows the one of MSEBI slave.

Table 5.1 Common Config Register（rMSEBIM_CONFIG）

Bit name	Value	Function
bMSEBIM_BURST_SIZEMAX_CPUREAD	4	Not limited
bMSEBIM_BURST_SIZEMAX_CPUWRITE	4	Not limited
bMSEBIM_CLKENABLE	1	Enable clock generation
bMSEBIM_CLKH	3	4 MSEBIM_HCLK
bMSEBIM_CLKL	3	4 MSEBIM_HCLK

Table 5.2 Chip Select CycleSize Register（rMSEBIM_CYCLESIZE_CS[n]_N）

Bit name	Value	Function
bMSEBIM_WRDLEDATA_NB	1	2 MSEBIM_CLK
bMSEBIM_RDDLEDATA_NB	1	2 MSEBIM_CLK
bMSEBIM_WRDLEDATA_B	1	2 MSEBIM_CLK
bMSEBIM_RDDLEDATA_B	1	2 MSEBIM_CLK
bMSEBIM_CLEDATA	1	2 MSEBIM_CLK

Table 5.3 Chip Select SetHold Register（rMSEBIM_SETUPHOLD_CS[n]_N）

Bit name	Value	Function
bMSEBIM_WRDLEHOLD	1	1 MSEBIM_CLK
bMSEBIM_RDDLEHOLD	1	1 MSEBIM_CLK
bMSEBIM_WRDLESETUP	1	1 MSEBIM_CLK
bMSEBIM_RDDLESETUP	1	1 MSEBIM_CLK

Table 5.4 Chip Select Config Register（rMSEBIM_CONFIG_CS[n]_N）

Bit name	Value	Function
bMSEBIM_ALE_MODE	0	Serial mode
bMSEBIM_ALE_NUMBER	2	2 MSEBIM_ALE used
bMSEBIM_BURST_ENABLE	1	Burst enable
bMSEBIM_MODE_WAIT	2	Wait management on MSEBIM_WAIT0_N pin
bMSEBIM_CONFIG	5	Synchronous, 8 bits, multiplexed, Mode8, Burst available

Table 5.5 Common Config Register（rMSEBIS_CONFIG）

Bit name	Value	Function
bMSEBIS_AHB_MASTER_BUF	0	Buffer disable
bMSEBIS_BURST_SIZEMAX_CPUWRITE	3	16 words
bMSEBIS_BURST_SIZEMAX_CPUREAD	3	16 words

Table 5.6 Chip Select CycleSize Register（rMSEBIS_CYCLESIZE_CS[n]_N）

Bit name	Value	Function
bMSEBIS_WRDLEDATA_NB	1	2 MSEBIS_CLK
bMSEBIS_RDDLEDATA_NB	1	2 MSEBIS_CLK
bMSEBIS_WRDLEDATA_B	1	2 MSEBIS_CLK
bMSEBIS_RDDLEDATA_B	1	2 MSEBIS_CLK
bMSEBIS_CLEDATA	1	2 MSEBIS_CLK

Table 5.7 Chip Select SetHold Register（rMSEBIS_SETUPHOLD_CS[n]_N）

Bit name	Value	Function
bMSEBIS_WRDLESETUP	1	1 MSEBIS_CLK
bMSEBIS_RDDLESETUP	1	1 MSEBIS_CLK

Table 5.8 Chip Select Config Register（rMSEBIS_CONFIG_CS[n]_N）

Bit name	Value	Function
bMSEBIS_CS_ENABLE	1	Ready to receive request from the master
bMSEBIS_ADDR_MODE	1	MMU mode
bMSEBIS_BURST_ENABLE	1	Burst enable
bMSEBIS_MODE_WAIT	2	Wait management on MSEBIS_WAIT0_N pin
bMSEBIS_WEN	1	Write on device is enabled
bMSEBIS_CONFIG	2	Synchronous, 8 bits, multiplexed, Mode8, Burst available

5.2.1.2 Burst access by DMA

The burst access by DMA needs the MSEBI register configurations for DMA transfer in addition of the register configurations shown in the section 5.2.1.1. Table 5.9 to Table 5.14 shows the register configurations of MSEBI master and Table 5.15 to Table 5.18 shows the one of MSEBI slave.

Table 5.9 DMA Transmit Control and Status Register（rMSEBIM_TDMACR_CS[n]_N）

Bit name	Value	Function
bMSEBIM_DEST_BLOCK_SIZE	Data size / 8	Block transfer size
bMSEBIM_DEST_BURST_SIZE	1	4 Single transactions
bMSEBIM_TDMAE1	1	Enable the DMA in Transmit mode

Table 5.10 DMA Receive Control and Status Register（rMSEBIM_RDMACR_CS[n]_N）

Bit name	Value	Function
bMSEBIM_SRC_BLOCK_SIZE	Data size / 8	Block transfer size
bMSEBIM_SRC_BURST_SIZE	1	4 Single transactions
bMSEBIM_RDMAE1	1	Enable the DMA in Transmit mode

Table 5.11 DMA Transmit Data Level Register（rMSEBIM_DMATDLR_CS[n]_N）

Bit name	Value	Function
bMSEBIM_USE_EXT_WRDMA_REQ	0	Disable DMA control by External pins
bMSEBIM_BURST_SIZEMAX_DMAWRITE	5	Not limited
bMSEBIM_DMATDLR	28	28 or less data entries

Table 5.12 DMA Receive Data Level Register（rMSEBIM_DMARDLR_CS[n]_N）

Bit name	Value	Function
bMSEBIM_USE_EXT_RDDMA_REQ	0	Disable DMA control by External pins
bMSEBIM_BURST_SIZEMAX_DMAREAD	5	Not limited
bMSEBIM_DMARDLR	28	28 or less data entries

Table 5.13 DMA Read Address Register（rMSEBIM_ADDRDMA_READ_CS[n]_N）

Bit name	Value	Function
bMSEBIM_ADDRDMA_READ	0x80200000	Address DMA read access

Table 5.14 DMA Write Address Register（rMSEBIM_ADDRDMA_WRITE_CS[n]_N）

Bit name	Value	Function
bMSEBIM_ADDRDMA_READ	0x80200000	Address DMA write access

Table 5.15 DMA Transmit Request Register（rMSEBIS_DMATX_REQ_CS[n]_N）

Bit name	Value	Function
bMSEBIS_DMATX_ENABLE	1	Ready to receive request
bMSEBIS_DMATX_FORCE	0	MSEBIS_DMA_WR[n]_N is set to 0

Table 5.16 DMA Receive Request Register（rMSEBIS_DMARX_REQ_CS[n]_N）

Bit name	Value	Function
bMSEBIS_DMARX_ENABLE	1	Ready to receive request
bMSEBIS_DMARX_FORCE	0	MSEBIS_DMA_RD[n]_N is set to 0

Table 5.17 DMA Transmit Data Level Register（rMSEBIS_DMATDLR_CS[n]_N）

Bit name	Value	Function
bMSEBIS_DMATX_FLOW_CTRL	0	DMA flow control is disabled
bMSEBIS_DMATX_OPT_BURST	1	Enable burst size optimization
bMSEBIS_DMATX_MAX_BURST	3	16 words max

Table 5.18 DMA Receive Data Level Register（rMSEBIS_DMARDLR_CS[n]_N）

Bit name	Value	Function
bMSEBIS_DMATX_FLOW_CTRL	0	DMA flow control is disabled
bMSEBIS_DMATX_OPT_BURST	1	Enable burst size optimization
bMSEBIS_DMATX_MAX_BURST	3	16 words max

In addition, Table 5.19 to Table 5.22 shows the register configuration of DMA controller.

Table 5.19 Source Address Register for Channel [n]（SAR[n]）

Bit name	Value	Function
SAR	0x80100000 0x40080000	When writing: Transmit data stored address When reading: DMA receive FIFO address

Table 5.20 Destination Address Register for Channel [n]（SAR[n]）

Bit name	Value	Function
DAR	0x40090000 0x80200000	When writing: DMA transmit FIFO address When reading: Receive data stored address

Table 5.21 Destination Address Register for Channel [n]（SAR[n]）

Bit name	Value	Function
TT_FC	4 6	When writing: From peripheral to memory Flow controller is peripheral When reading: From memory to peripheral Flow controller is peripheral
SRC_MSIZE	1	4 burst transactions for SRC
DEST_MSIZE	1	4 burst transactions for DST
SINC	0 2	When writing: Increment When reading: Fixed
DINC	2 0	When writing: Fixed When reading: Increment
SRC_TR_WIDTH	3	64 bits
DST_TR_WIDTH	3	64 bits
INT_EN	0	Interrupt enable

Table 5.22 Configuration Register for Channel [n]（CFG[n]）

Bit name	Value	Function
DEST_PER	11	When writing: Request interface 11 MSEBI1 (CS0_N TX)
SRC_PER	10	When reading: Request interface 10 MSEBI9 (CS0_N RX)
HS_SEL_SRC	0	When reading: Hardware request interface
HS_SEL_DST	0	When writing: Hardware request interface

5.2.2 16-bit asynchronous connection

Table 5.23 to Table 5.26 shows the register configuration of MSEBI master for 16-bit asynchronous connection.

Table 5.23 Common Config Register（rMSEBIM_CONFIG）

Bit name	Value	Function
bMSEBIM_BURST_SIZEMAX_CPUREAD	0	1 word
bMSEBIM_BURST_SIZEMAX_CPUWRITE	0	1 word
bMSEBIM_CLKENABLE	0	Disable clock generation
bMSEBIM_CLKH	0	1 MSEBIM_HCLK
bMSEBIM_CLKL	0	1 MSEBIM_HCLK

Table 5.24 Chip Select CycleSize Register（rMSEBIM_CYCLESIZE_CS[n]_N）

Bit name	Value	Function
bMSEBIM_WRDLEDATA_NB	1	2 MSEBIM_CLK
bMSEBIM_RDDLEDATA_NB	1	2 MSEBIM_CLK
bMSEBIM_WRDLEDATA_B	1	2 MSEBIM_CLK
bMSEBIM_RDDLEDATA_B	1	2 MSEBIM_CLK
bMSEBIM_CLEDATA	1	2 MSEBIM_CLK

Table 5.25 Chip Select SetHold Register（rMSEBIM_SETUPHOLD_CS[n]_N）

Bit name	Value	Function
bMSEBIM_WRDLEHOLD	1	1 MSEBIM_CLK
bMSEBIM_RDDLEHOLD	1	1 MSEBIM_CLK
bMSEBIM_WRDLESETUP	1	1 MSEBIM_CLK
bMSEBIM_RDDLESETUP	1	1 MSEBIM_CLK

Table 5.26 Chip Select Config Register（rMSEBIM_CONFIG_CS[n]_N）

Bit name	Value	Function
bMSEBIM_ALE_MODE	0	Serial mode
bMSEBIM_ALE_NUMBER	1	1 MSEBIM_ALE used
bMSEBIM_BURST_ENABLE	0	Burst disable
bMSEBIM_MODE_WAIT	0	Wait management on MSEBIM_WAIT0_N pin
bMSEBIM_CONFIG	0	Asynchronous, 16 bits, multiplexed, Mode8, No Burst

5.3 Constants

Table 5.27 shows the constants.

Table 5.27 Constants used in sample program

Constant name	Value	Description
MSEBI_DATA_SIZE	0x00008000	Data size: 32KB
MSEBIM_WRITE_ADDR	0x80100000	Write data address
MSEBIM_READ_ADDR	0x80200000	Read data address
MSEBIM_DMA_FIFOREAD_CS0	0x40080000	MSEBIM DMA receive FIFO (CS0) address
MSEBIM_DMA_FIFOWRITE_CS0	0x40090000	MSEBIM DMA transmit FIFO (CS0) address
MSEBIS_DATA_ADDR	0x80200000	Receive data address
MSEBIS_INT_CPURX_SET	0x00000001	CPURX value in rMSEBIS_INT register
MSEBIS_INT_CPUTX_SET	0x00000010	CPUTX value in rMSEBIS_INT register
MSEBIS_INT_DMARX_SET	0x00000100	DMARX value in rMSEBIS_INT register
MSEBIS_INT_DMATX_SET	0x00001000	DMATX value in rMSEBIS_INT register
MSEBIS_MMU_MASK_SIZE	0x00007FFF	MMU mask size
MSEBIS_EOB_ADDR	0x20000000	Block transfer descriptor writing address
MSEBI_DMA_DIR_READ	0	DMA transfer direction: reading
MSEBI_DMA_DIR_WRITE	1	DMA transfer direction: writing

Table 5.28 shows the variable type.

Table 5.28 Variable type used in sample program

Type	Type name	Description
typedef enum	msebi_opeation_t	Operation mode CPU_SYNC_8 = 0, DMA_SYNC_8 = 1, CPU_ASYNC_16 = 2

5.4 Variables

Table 5.29 shows the global variables.

Table 5.29 Global variables

Type	Variable name	Description
static uint32_t *	msebim_wr_buf	Write data pointer
static uint32_t *	msebim_rd_buf	Read data pointer
static uint32_t *	msebis_int	rMSEBIS_INT register pointer
static bool	dma_memtomem_completed	DMA transfer completion flag

Table 5.30 shows the local variables.

Table 5.30 Local variables

Type	Variable name	Description
msebi_opeation_t	msebim_op	Operation mode for MSEBI master
msebi_opeation_t	msebis_op	Operation mode for MSEBI slave

5.5 Functions

Table 5.31 shows the list of functions.

Table 5.31 Functions

Function	Description
msebim_main	Main function for MSEBI master
mesbis_main	Main function for MSEBI slave
msebim_set_init	Initialization for MSEBI master
msebis_set_init	Initialization for MSEBI slave

5.6 Function specification

The function specifications of the sample program are shown below.

msebim_main	
Summary	Main function for MSEBI master
Header	None
Declaration	static void msebim_main(void)
Description	After select the operation mode, the initialization, writing and reading is run in each mode.
Argument	None
Returned value	None

msebis_main	
Summary	Main function for MSEBI slave
Header	None
Declaration	static void msebis_main(void)
Description	After select the operation mode, the initialization, writing and reading is run in each mode.
Argument	None
Returned value	None

msebim_set_init	
Summary	Initialization for MSEBI master
Header	None
Declaration	static void msebim_set_init(msebi_opeation_t operation)
Description	Execute the initialization of MSEBI slave.
Argument	msebi_opeation_t type operation: Operation mode
Returned value	None

msebis_set_init	
Summary	Initialization for MSEBI slave
Header	None
Declaration	static void msebis_set_init(msebi_opeation_t operation)
Description	Execute the initialization of MSEBI slave.
Argument	msebi_opeation_t type operation: Operation mode
Returned value	None

5.7 Flowchart

5.7.1 Main processing

Figure 5.1 shows a flowchart of main processing of MSEBI master.

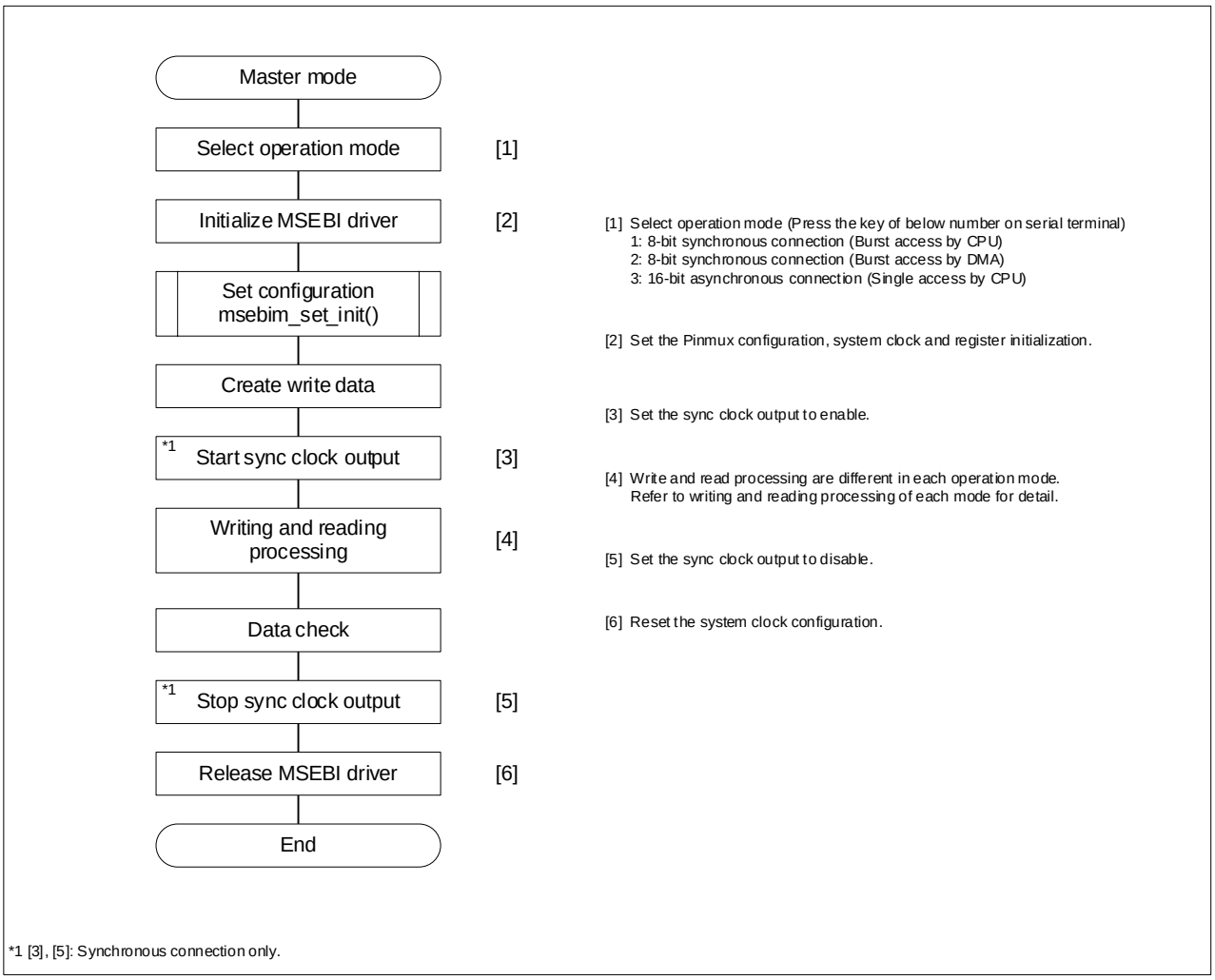

Figure 5.1 Main processing of MSEBI master

Figure 5.2 shows that of main processing of MSEBI slave.

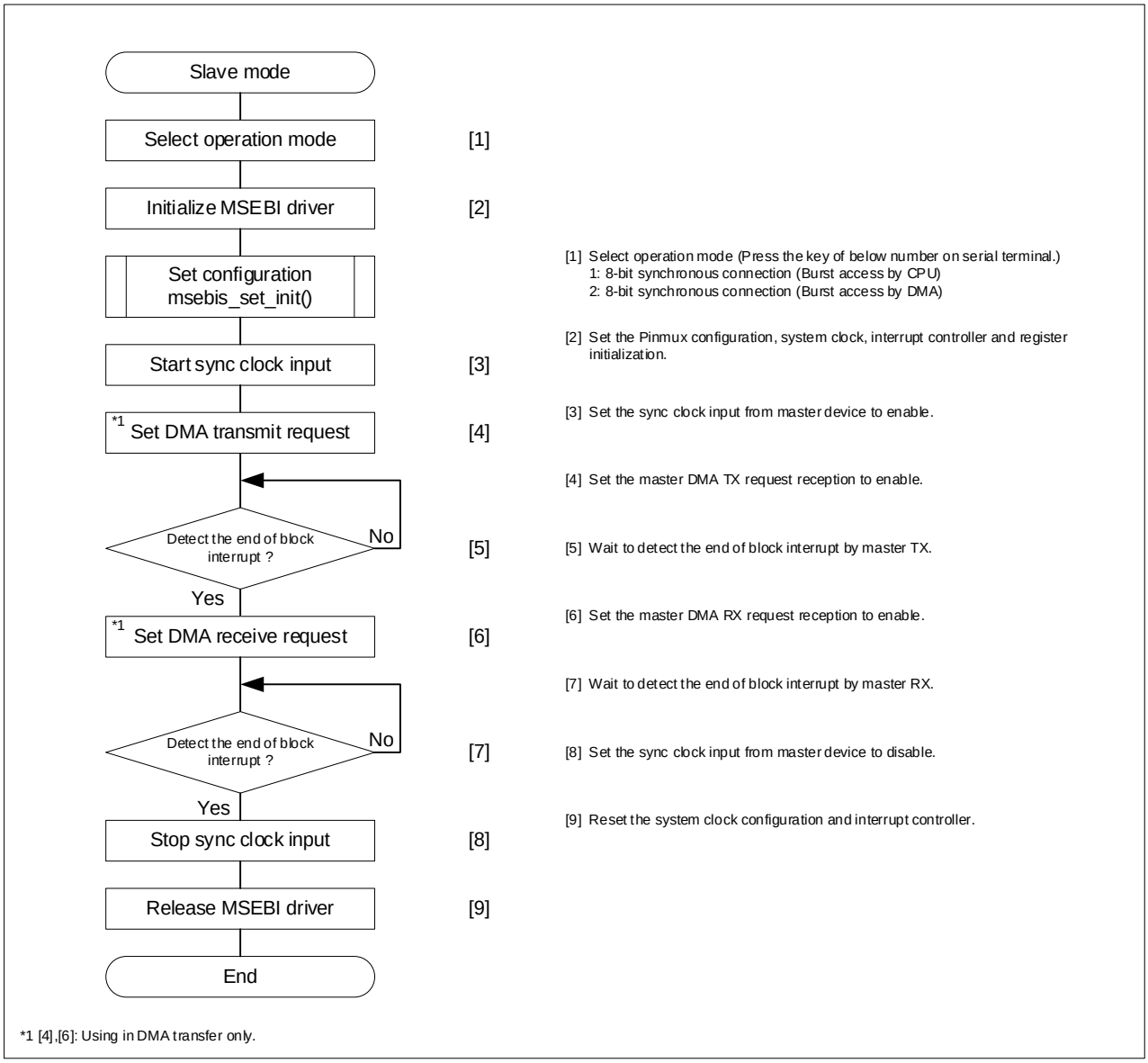

Figure 5.2 Main processing of MSEBI slave

5.7.2 Initialization processing

Figure 5.3 shows a flowchart of Initialization of MSEBI master.

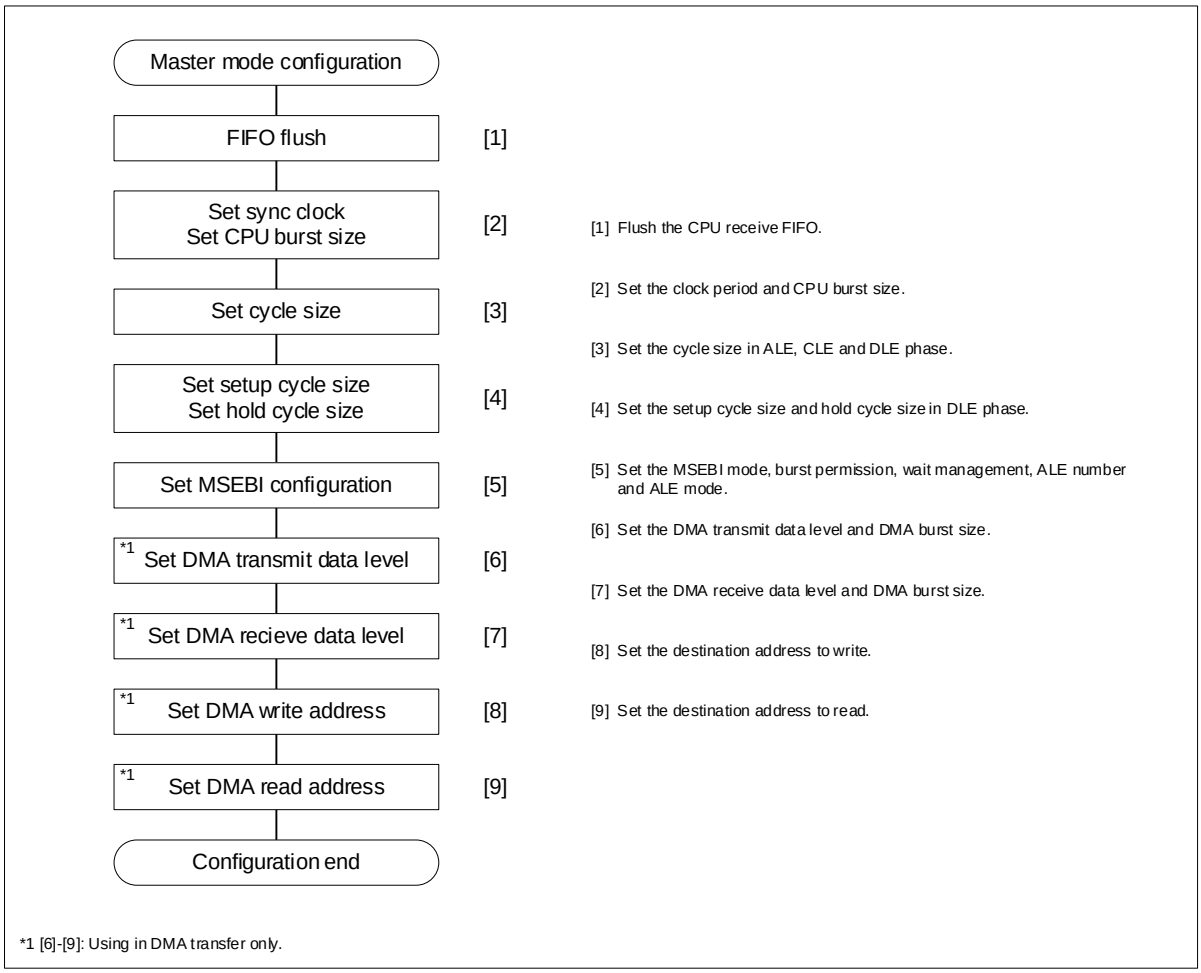

Figure 5.3 Initialization of MSEBI master

Figure 5.4 shows that of Initialization of MSEBI slave.

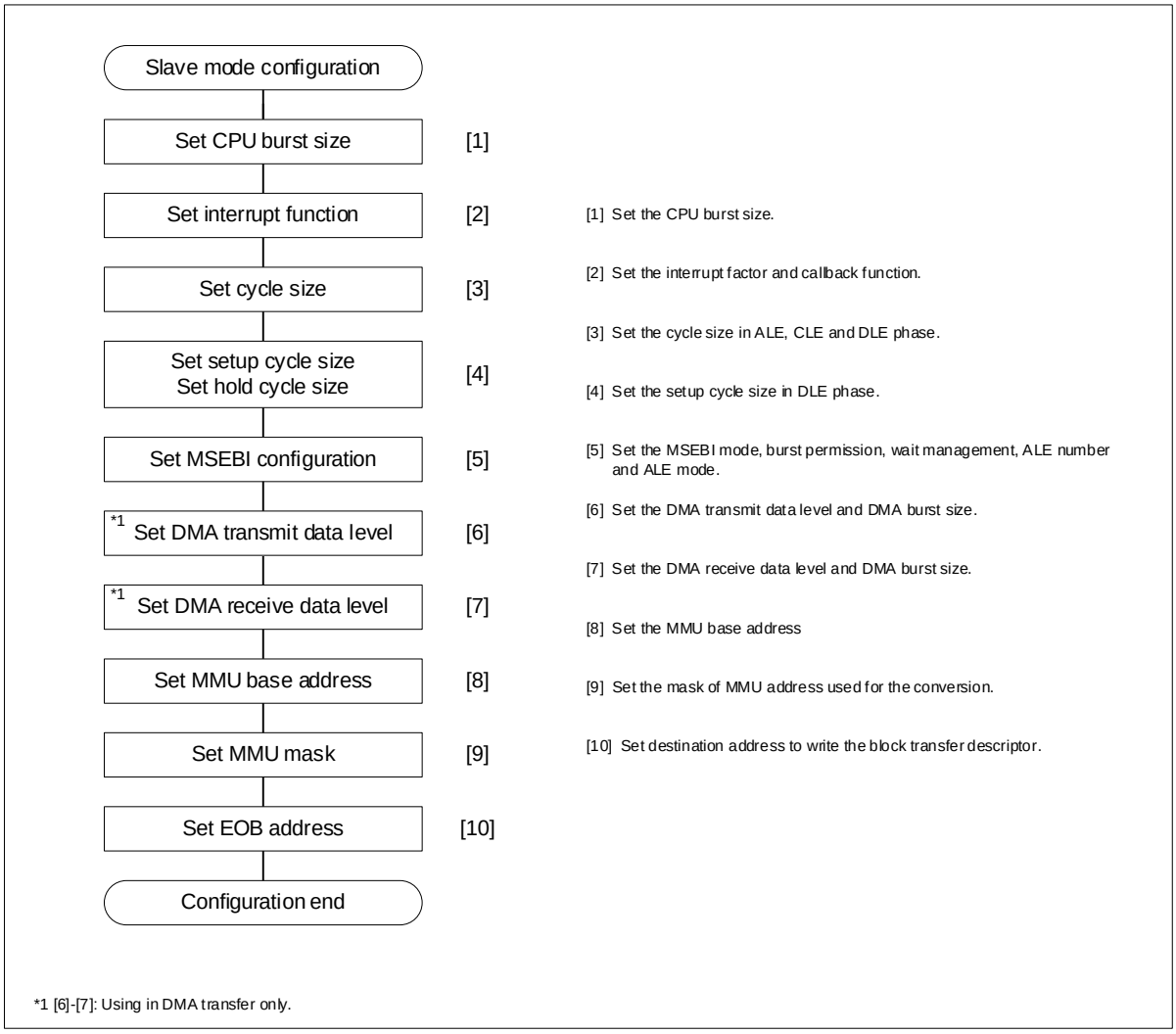

Figure 5.4 Initialization of MSEBI slave

5.7.3 Writing and reading processing

Figure 5.5, Figure 5.6 and Figure 5.7 shows the flowcharts of writing and reading processing of MSEBI master in each operation mode.

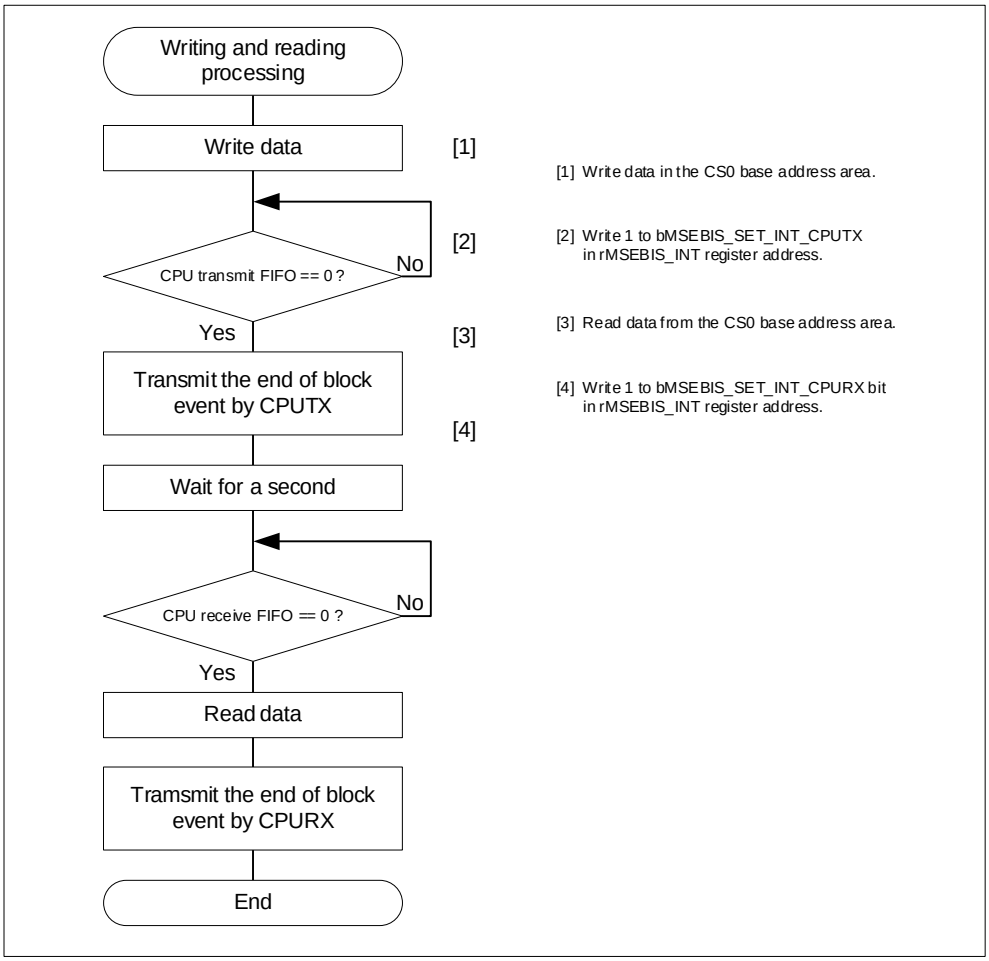

Figure 5.5 Writing and reading processing of 8-bit synchronous connection (Burst access by CPU)

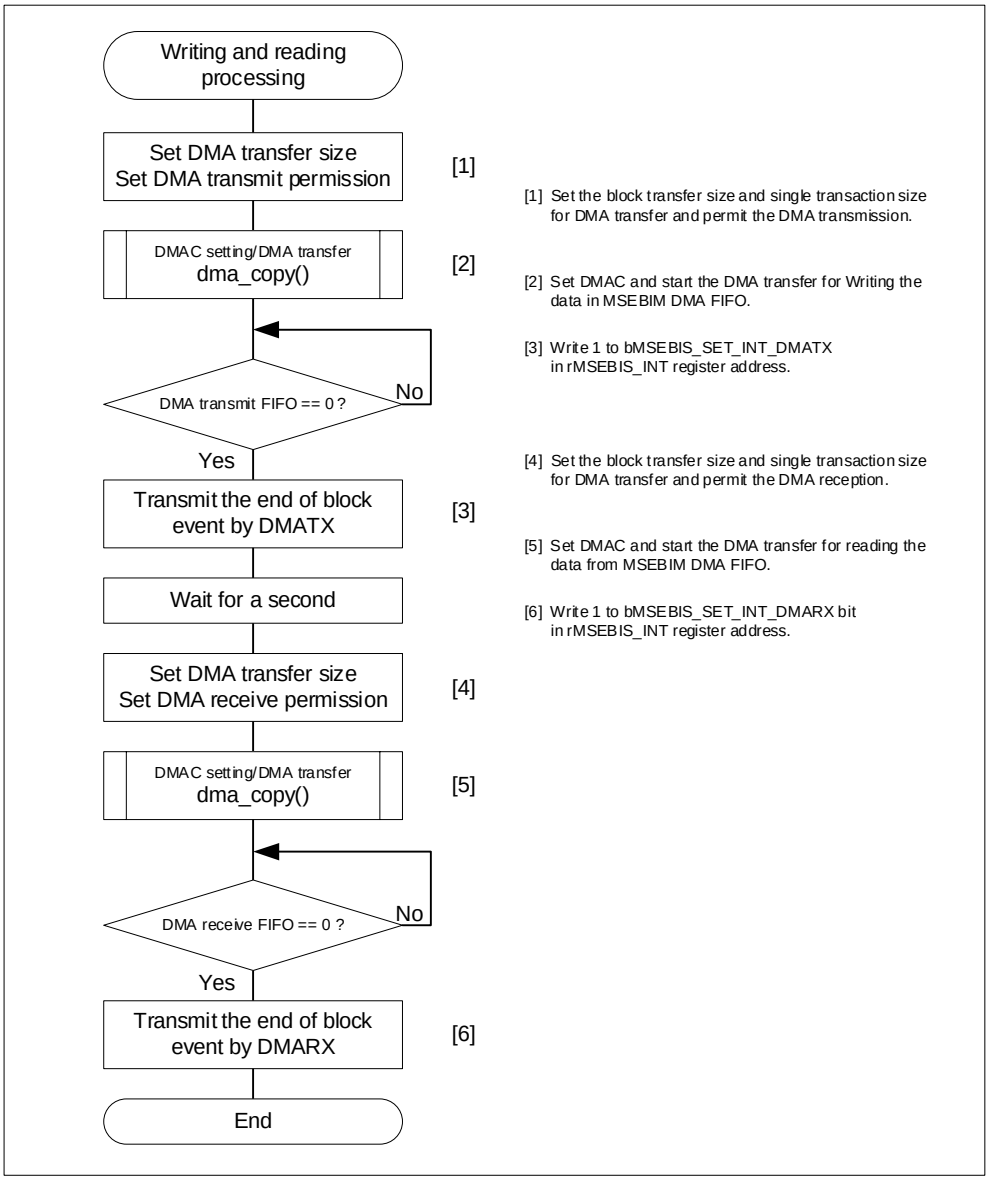

Figure 5.6 Writing and reading processing of 8-bit synchronous connection (Burst access by DMA)

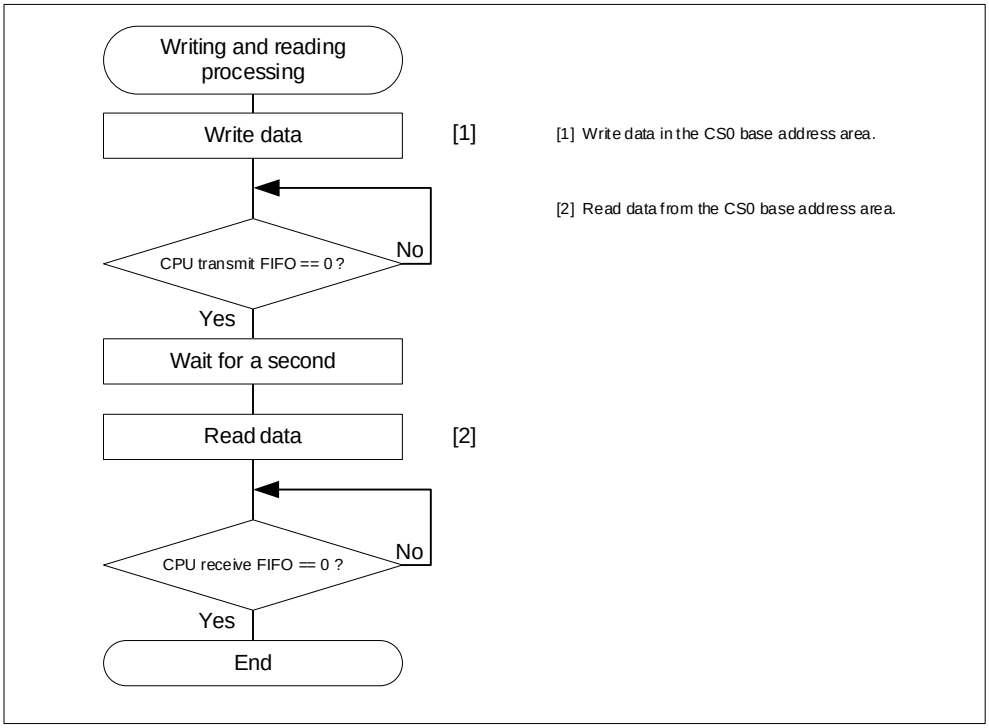

Figure 5.7 Writing and reading processing of 16-bit asynchronous connection (Single access by CPU)

5.8 Setting of drive strength

When connecting two sets RZ/N1x CPU boards by wires, the drive strength of the connected pins should be adjusted because MSEBI may not be able to capture the data depending on the length of wiring between the boards.

The drive strength of MSEBI(y)_CLK is set to 8mA in this application note. Whereas, in the sample program, the drive strength is set by the following code in “r_msebi_rzn1.c”.

```
1740
1741 /*****************************************************************************************************************************************************
1742  *  Function Name:MSEBI_PinMux
1743  *****************************************************************************************************************************************************/
1744 ER_RET MSEBI_PinMux (bool master)
1745 {
1746     ER_RET ret_val = ER_OK;
1747     iomux_pin_properties_t pin_mux =    {
1748                                             .function       = RZN1_FUNC_MSEBIS,
1749                                             .drive_strength = RZN1_MUX_DRIVE_4MA,
1750                                             .pull_level     = RZN1_MUX_PULL_NONE
1751                                         };
1752
1753     /* First pin at 105. 14 sequential to match CN7 connection */
1754     if (master)
1755     {
1756         /* Master */
1757         pin_mux.function = RZN1_FUNC_MSEBIM;
1758     }
1759
1760     for (uint8_t pin = 105; pin <= 118; pin++)
1761     {
1762         ret_val = R_IOMUX_PinCtrl(pin, IOMUX_CONTROL_SET_PIN_PROPERTIES, &pin_mux);
1763     }
1764
1765     pin_mux.pull_level = RZN1_MUX_PULL_UP; /* Pull the two wait pins down to flag as not ready  */
1766     ret_val |= R_IOMUX_PinCtrl(117, IOMUX_CONTROL_SET_PIN_PROPERTIES, &pin_mux); /* MSEBIS_WAIT_N[0] */
1767     ret_val |= R_IOMUX_PinCtrl(118, IOMUX_CONTROL_SET_PIN_PROPERTIES, &pin_mux); /* MSEBIS_WAIT_N[1] */
1768
1769     /* Change drive strength of MSEBI_CLK */                    PinMux setting for the clock pins
1770     pin_mux.drive_strength = RZN1_MUX_DRIVE_8MA;
1771     pin_mux.pull_level = RZN1_MUX_PULL_NONE;
1772
1773     if(master)
1774     {
1775       /* MSEBIM_CLK @GPIO110 */
1776         ret_val |= R_IOMUX_PinCtrl(110, IOMUX_CONTROL_SET_PIN_PROPERTIES, &pin_mux);
1777     }
1778     else
1779     {
1780       /* MSEBIS_CLK @GPIO114 */
1781         ret_val |= R_IOMUX_PinCtrl(114, IOMUX_CONTROL_SET_PIN_PROPERTIES, &pin_mux);
1782     }
1783     /***************/
1784
1785     return ret_val;
1786 }
1787 /*****************************************************************************************************************************************************
1788  End of function MSEBI_PinMux
1789  *****************************************************************************************************************************************************/
```

Figure 5.8 Changing point of MSEBI_PinMux function

6. Sample program

Please get the sample program from Renesas electronics websites.

7. Reference documents

User's Manual: Hardware

RZ/N1D group, RZ/N1S group, RZ/N1L group

User's Manual: System Introduction, Multiplexing, Electrical and Mechanical Information

User's Manual: System Control and Peripheral

User's Manual: Peripherals

User's Manual: Quick Start Guide

RZ/N1S Group CONNECT IT! – ETHERNET RZ/N1S Quick Start Guide

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2020/07/01		First edition issued
2.00	2020/12/14	All pages 5 6 21,22,23 24	Full revision “Drive strength” item was appended in Table 2.1. The version of solution kit was updated. The version of sample program was updated. “Note” was appended in 4.1.1. Figure 5.5, Figure 5.6, and Figure 5.7 in 5.7.3 were modified. 5.8 “Setting of drive strength” was appended.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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