RZ/G3S
Power Consumption Measurement

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Information

This application note provides measurement results of power consumption of RZ/G3S in some use cases.

Target Device

RZ/G3S

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1. Power Rail Overview

The RZ/G3S has three power domains (AWO, ISO, VBATT). A power system example with a power management IC (PMIC) and programable LDO devices (GreenPAK), is depicted in the following figure. The 0.9 V power supply to the core logic of this SoC is aggregated to the VDD. Thus, current flow on the VDD changes along with computationally demands. Current flows on other power rails also change along with each function demands.

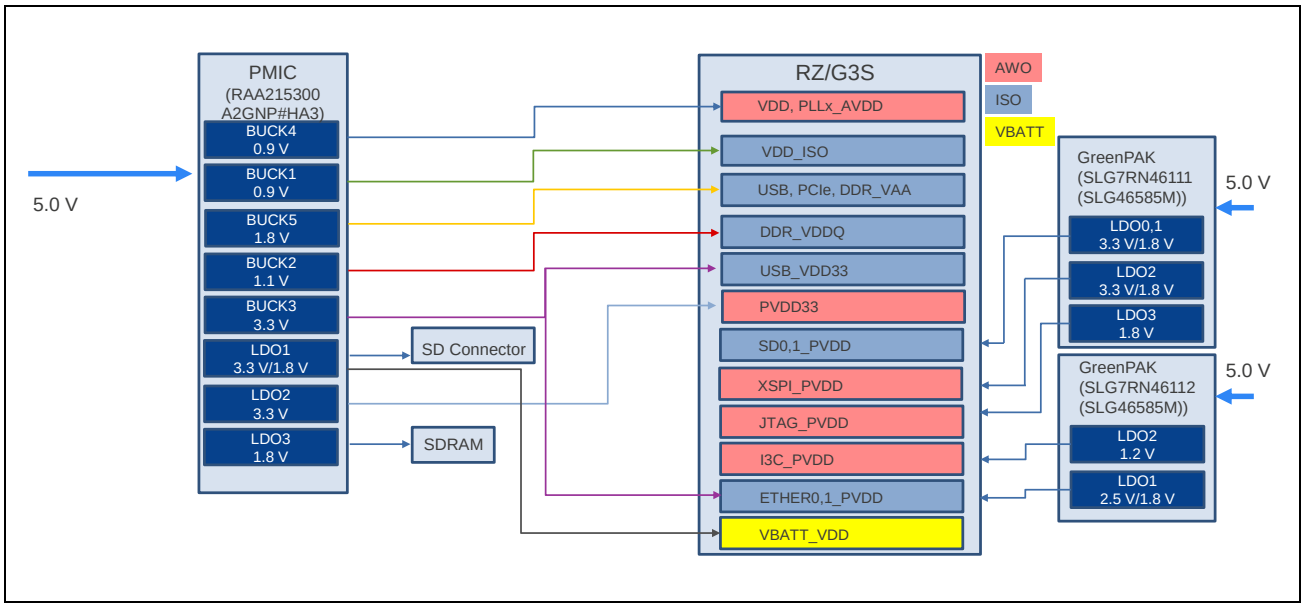

Figure 1.1 A power system example

2. Measurement Condition

- Device condition
  - Process TYP
  - VDD TYP
  - Temperature Room (Ta ≈ 25°C)
- DRAM configuration
  One to one connection to the SoC
- Target power rails

  Power rails for core supplies; 0.9 V for VDD of RZ/G3S, VDD_ISO of RZ/G3S and 1.1 V for VDDQ, VDD2 of DRAM and DDR_VDDQ of RZ/G3S.
- Use cases
  - VBATT
  - AWO
  - AWO (Power Reduction)
  - Linux Idle
  - 1-Core Dhrystone
  - Himeno Bench

3. Measurement Results

This chapter provides measurement results of power consumption in six use cases;

- VBATT
- AWO
- AWO (Power Reduction)
- Linux Idle
- 1-Core Dhrystone
- Himeno Bench

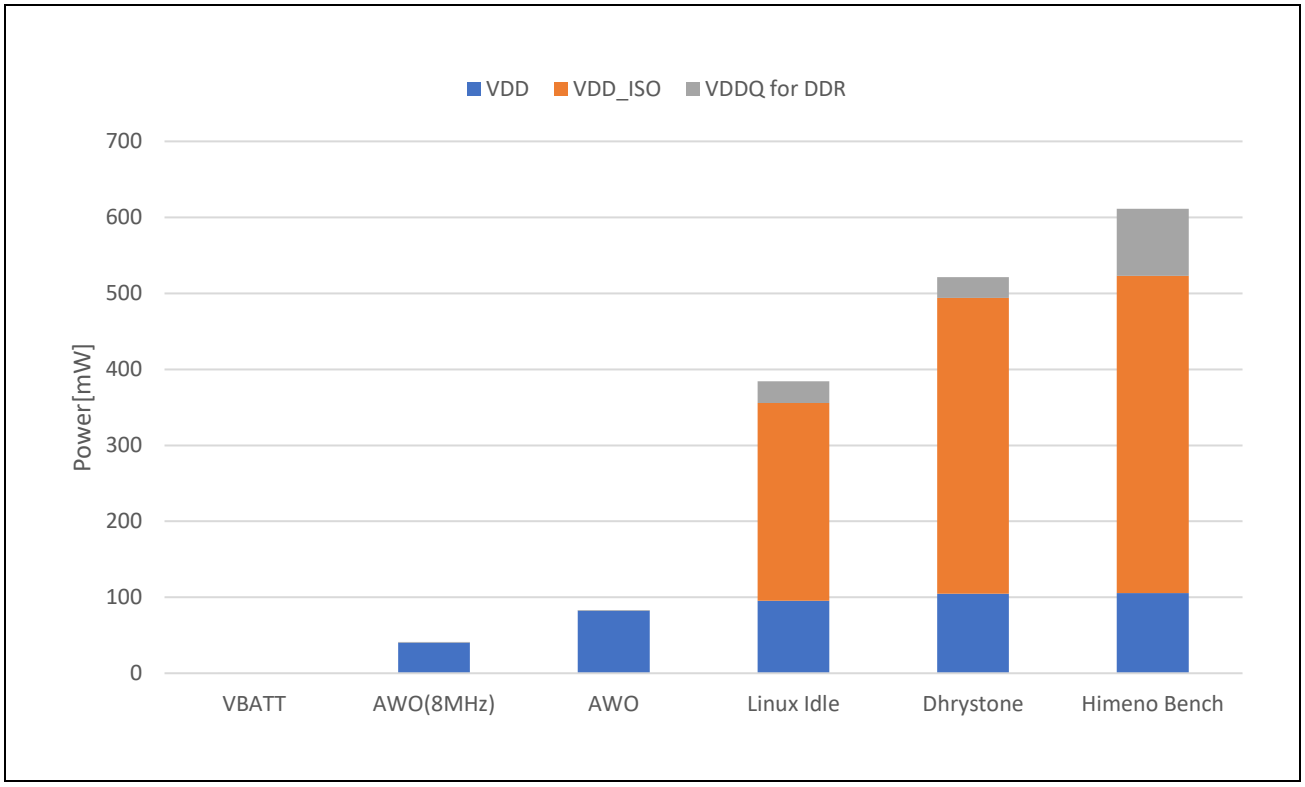

Figure 3.1 Power consumption graph for each use case

3.1 VBATT

In this use case, “VBATT”, CA55 core and CM33 core are power off with DDR retention, supplying power only to the VBATT area.

Table 3.1 Measurement result in VBATT

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	0	0
VDD_ISO	0.9	0	0
VDDQ for DDR	1.1	0.45*1	0.49
Total Power	—	—	0.49

Note 1. The VDDQ for DDR supplies both the G3S and the DRAM. However, the DRAM consumes the most part of the current.

3.2 AWO

In this use case, “AWO”, CA55 core is power off and CM33 core is running at 250 MHz with DDR retention.

Table 3.2 Measurement result in AWO

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	91.7	82.6
VDD_ISO	0.9	0	0
VDDQ for DDR	1.1	0.74	0.81
Total Power	—	—	83.4

3.3 AWO (Power Reduction)

In this use case, “AWO (Power Reduction)”, CA55 core is power off and CM33 core is running at 8 MHz with DDR retention.

Active IP under CM33 Bus: DMAC, I2C, SCIF, OSTM, GPIO. Other modules are in standby.

Table 3.3 Measurement result in AWO (Power Reduction)

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	44.8	40.3
VDD_ISO	0.9	0	0
VDDQ for DDR	1.1	0.74	0.81
Total Power	—	—	41.1

3.4 Linux Idle

In this use case, “Linux Idle”, Linux is executed on one CA55 core with 1.1 GHz clock.

Table 3.4 Measurement result in Linux Idle

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	106.3	99.9
VDD_ISO	0.9	288.8	271.5
VDDQ for DDR	1.1	26.1	28.7
Total Power	—	—	400.1

3.5 1-Core Dhrystone

In this use case, “Dhrystone”, well-known CPU benchmark program, is executed on one core with 1.1 GHz clock.

Table 3.5 Measurement result in 1-Core Dhrystone

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	116.3	104.6
VDD_ISO	0.9	432.5	389.2
VDDQ for DDR	1.1	25.0	27.5
Total Power	—	—	521.3

3.6 Himeno Bench

In this use case, “Himeno Bench”, a benchmarking software published by RIKEN.

https://i.riken.jp/supercom/documents/himenobmt/

Table 3.6 Measurement result in Himeno Bench

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD	0.9	117.5	105.8
VDD_ISO	0.9	463.8	417.4
VDDQ for DDR	1.1	80.0	88.0
Total Power	—	—	611.2

REVISION HISTORY	RZ/G3S Power Consumption Measurement

Rev.	Date	Description	
		Page	Summary
1.00	Nov 29, 2023	—	First edition issued
1.01	Mar 26, 2024	6	Table 3.1 Measurement result in VBATT: Note 1, added

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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