RZ/G3E
Power Consumption Measurement

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Information

This application note provides measurement results of power consumption of the RZ/G3E in some use cases.

Target Device

RZ/G3E

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1. Power Rail Overview

The RZ/G3E has three power domains (PD_AWO, PD_OTHER, and PD_CA55). A power system example with a power management IC (PMIC) and programmable LDO device (GreenPAK) is depicted in the following figure.

The 0.8 V/0.9 V power supply to the core logic of this SoC is aggregated to the VDD.

Thus, current flow on the VDD changes with a computational demand. Current flows on other power rails change with each function demand.

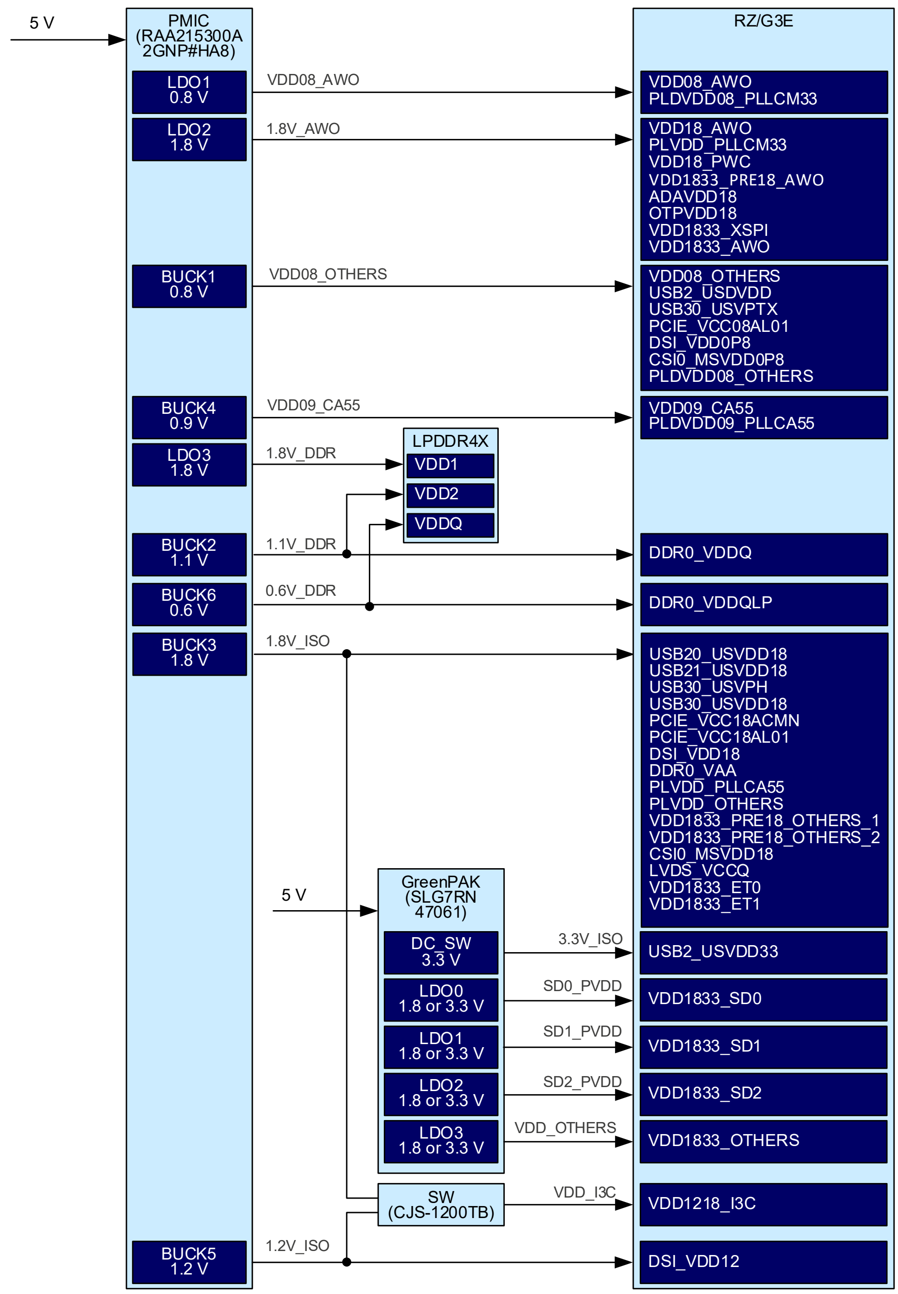

Figure 1.1 Power System Example

2. Measurement Condition

- Device conditions
  - Process TYP
  - VDD TYP (for use cases except DDR_RETENTION (low-power mode))
    MAX (for the use case of DDR_RETENTION (low-power mode))
  - Temperature Room (Ta ≈ 25°C)

- DRAM configuration
  One-to-one connection to the SoC
  DRAM: LPDDR4X-3200, 32-bit × 1 ch

- Target power rails
  Power rails for core supplies:
  - VDD09_CA55: 0.9 V for VDD09_CA55 and PLDVDD09_PLLCA55 of the RZ/G3E
  - VDD08_AWO: 0.8 V for VDD08_AWO and PLDVDD08_PLLCM33 of the RZ/G3E
  - VDD08_OTHERS: 0.8 V for VDD08_OTHERS, USB2_USDVDD, PCIE_VCC08AL01, DSI_VDD0P8, CSI0_MSVDD0P8, PLDVDD08_OTHERS, and USB30_USVPTX of the RZ/G3E
  - 1.1V_DDR: 1.1 V for VDD2 of DRAM and DDR0_VDDQ of the RZ/G3E
  - 0.6V_DDR: 0.6 V for VDDQ of DRAM and DDR0_VDDQLP of the RZ/G3E

- Use cases
  - Linux Idle
  - 1-core Dhrystone
  - 2-core Dhrystone
  - 4-core Dhrystone
  - 3D graphics rendering and multi-display output
  - Multi-stream decoding and multi-display output
  - DDR_RETENTION (low-power mode)

3. Measurement Results

This section provides measurement results of power consumption in seven use cases:

- Linux Idle
- 1-core Dhrystone
- 2-core Dhrystone
- 4-core Dhrystone
- 3D graphics rendering and multi-display output
- Multi-stream decoding and multi-display output
- DDR_RETENTION (low-power mode)

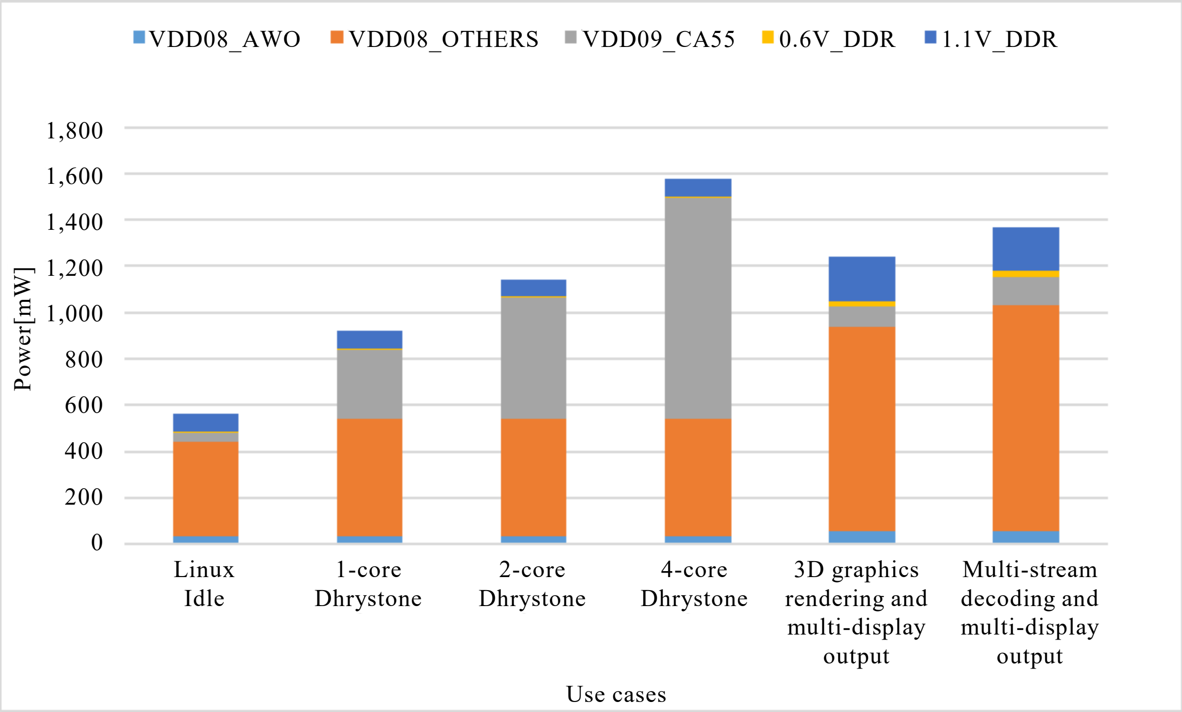

Figure 3.1 Power Consumption Graph for Use Cases except DDR_RETENTION (Low-Power Mode)

3.1 Linux Idle

In this use case, "Linux Idle", Linux is executed on four cores of CA55 with 1.8 GHz clock.

Table 3.1 Measurement Result in Linux Idle

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	44	35.2
VDD08_OTHERS	0.8	510	408.0
VDD09_CA55	0.9	40	36.0
0.6V_DDR*[1]	0.6	11	6.6
1.1V_DDR*[1]	1.1	69	75.9
Total Power	—	—	561.7

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.2 1-Core Dhrystone

In this use case, “Dhrystone”, a well-known CPU benchmark program, is executed on one core of CA55 with 1.8 GHz clock.

Table 3.2 Measurement Result in 1-Core Dhrystone

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	45	36.0
VDD08_OTHERS	0.8	630	504.0
VDD09_CA55	0.9	330	297.0
0.6V_DDR*1	0.6	11	6.6
1.1V_DDR*1	1.1	69	75.9
Total Power	—	—	919.5

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.3 2-Core Dhrystone

In this use case, "Dhrystone", a well-known CPU benchmark program, is executed on two cores of CA55 with 1.8 GHz clock.

Table 3.3 Measurement Result in 2-Core Dhrystone

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	45	36.0
VDD08_OTHERS	0.8	630	504.0
VDD09_CA55	0.9	580	522.0
0.6V_DDR*1	0.6	11	6.6
1.1V_DDR*1	1.1	69	75.9
Total Power	—	—	1,144.5

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.4 4-Core Dhrystone

In this use case, “Dhrystone”, a well-known CPU benchmark program, is executed on four cores of CA55 with 1.8 GHz clock.

Table 3.4 Measurement Result in 4-Core Dhrystone

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	45	36.0
VDD08_OTHERS	0.8	630	504.0
VDD09_CA55	0.9	1060	954.0
0.6V_DDR*[1]	0.6	11	6.6
1.1V_DDR*[1]	1.1	69	75.9
Total Power	—	—	1,576.5

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.5 3D Graphics Rendering and Multi-Display Output

In this use case, the four cores of CA55 operate at a clock frequency of 1.8 GHz. The 3D graphics function renders 3D graphics using two instances of glmark2. The multi-display function outputs two Full-HD displays at 60 fps via MIPI-DSI and dual LVDS.

Table 3.5 Measurement Result in 3D Graphics Rendering and Multi-Display Output

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	74	58.9
VDD08_OTHERS	0.8	1,098	878.2
VDD09_CA55	0.9	99	89.1
0.6V_DDR*1	0.6	38	23.0
1.1V_DDR*1	1.1	177	194.2
Total Power	—	—	1,243.4

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.6 Multi-Stream Decoding and Multi-Display Output

In this use case, the four cores of CA55 operate at a clock of 1.8 GHz. The multi-stream function decodes one stream at Full-HD at 60 fps with H.265 and four streams at Full-HD at 60 fps with H.264. The multi-display function outputs two Full-HD displays at 60 fps via MIPI-DSI and dual LVDS.

Table 3.6 Measurement Result in Multi-Stream Decoding and Multi-Display Output

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.8	73	58.7
VDD08_OTHERS	0.8	1,218	974.6
VDD09_CA55	0.9	133	120.0
0.6V_DDR*1	0.6	47	27.9
1.1V_DDR*1	1.1	172	189.0
Total Power	—	—	1,370.2

Note 1. The 0.6V_DDR and 1.1V_DDR supply power to both the RZ/G3E and the DRAM.

3.7 DDR_RETENTION (Low-Power Mode)

In this use case, power is supplied only to the PD_DDR0_IO area. This low-power mode enables LPDDR4/4X self-refresh, allowing for a quick return to Linux applications.

Please note that the measurement values in the table below represents the power consumption of the SoC only (the power consumption of the DRAM is not included).

Table 3.7 Measurement Result in DDR_RETENTION (Low-Power Mode) of LPDDR4

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.00	0.00	0.00
VDD08_OTHERS	0.00	0.00	0.00
VDD09_CA55	0.00	0.00	0.00
0.6V_DDR	0.00	0.00	0.00
1.1V_DDR	1.17	1.03	1.20
Total Power	—	—	1.20

Table 3.8 Measurement Result in DDR_RETENTION (Low-Power Mode) of LPDDR4X

Power Rail	Voltage [V]	Current [mA]	Power [mW]
VDD08_AWO	0.00	0.00	0.00
VDD08_OTHERS	0.00	0.00	0.00
VDD09_CA55	0.00	0.00	0.00
0.6V_DDR	0.65	0.03	0.02
1.1V_DDR	1.17	1.00	1.17
Total Power	—	—	1.19

REVISION HISTORY	RZ/G3E Power Consumption Measurement

Rev.	Date	Description	
		Page	Summary
1.00	June 27, 2025	—	First edition issued
1.10	Feb. 25, 2026	—	Added measurement results for the following three use cases: ・3D graphics rendering and multi-display output ・Multi-stream decoding and multi-display output ・DDR_RETENTION (low-power mode)

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
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   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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