RZ/G2LC
Thermal Management Guideline

R01AN6105EJ0100
Rev.1.00
Oct 07, 2021

Information

The calculation results of power consumption, Limit Ta and θja are shown after the next page as reference.

Please choose the use case which is similar to your application, and refer to these results as reference.

Target Device

RZ/G2LC

Table of Contents

1. Specification of Junction Temperature

Specification of Tj (junction temperature) is defined as follows.
Users have to use this device without violating the following specification.

- Operating temperature

  -40°C ≤ Tjmax(Max temperature of junction side) ≤ 125°C

The calculation method of Tjmax is shown on **Section 3, Calculation method of Tjmax**.
Please confirm Tjmax according to this calculation method.

2. Definition of each characteristic

- The temperature at the center of the package surface is defined as Tt-center.

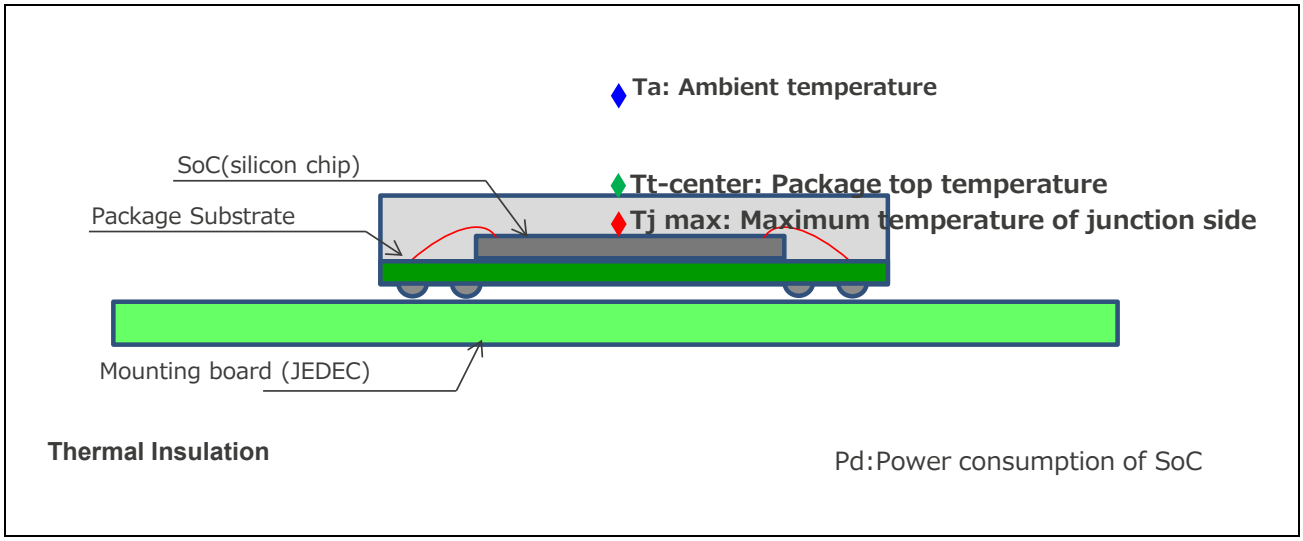


Figure 2.1 Definition of each characteristic

$$\theta ja(\text{Thermal resistance between Tj and Ta}) = \frac{Tjmax - Ta}{Pd}$$

$$\Psi jt(\text{at Package center}) = \frac{Tjmax - T_{t-center}}{Pd}$$

3. Calculation method of Tjmax

- After measuring Pd (Power consumption of Soc) and Tt-center in your environment, please calculate Tjmax using the next formula.
- Please confirm that "Tjmax" which you calculated is within the specification.

$$\mathrm{Tjmax}(℃) = \mathrm{Tt\text{-}center}(℃) + \Psi\mathrm{jt}(\text{at Package center})(℃/\mathrm{W})^{(*1)} \times \mathrm{Pd}(\mathrm{W})$$

Note 1. Refer to the table below for Ψjt(at Chip center).
Ψjt(at Chip center) is calculated value by thermal simulations.
Refer to **Section 5, Thermal simulation model** about the thermal simulation model.
Please remind that Ψjt is limited to the opentop case.

Table 3.1 Ψjt (at Package center) of 13mm sq

Package Outline	Heat Sink	Ψjt(at Package center) (°C/W)
13mm sq	No	1.32

4. Reference Information

4.1 Reference Information

- The calculation results of power consumption are shown after the next page as reference.
- Please choose the use case which is similar to your application, and refer to the power consumption as reference.
- Please confirm the limit Ta of your use case. The limit Ta was calculated from thermal simulation results.

4.2 Operation summary in each use case

The power consumptions in 4 use cases were calculated. You choose the use case which is similar to your application, and refer to the power consumption as reference.

- Estimation conditions of power consumption

  Tj = 125°C, Power supply (1.1V) = 1.1V, Power Supply (DDR4) = 1.2V, Power Supply (1.8V) = 1.8V,
  Power Supply (3.3V) = 3.3V, Process = FF process silicon, CPU: Cortex-A55@1.2GHz, DDR4-1600 16bit × 1ch

Table 4.1 Operation summary of each use case (1/2)

Use Case	Operation summary	Power consumption (w)
UseCase1	Use case assuming 1 screen display (2D graphics x 1) ● CortexA55 (2Core/CPU0: use rate 62%, CPU1: use rate 62%) ● GPU: use rate 65% ● System/Bus/Clock: use rate 50% ● MIPI-DSI: use rate 90% ● MIPI-CSI: use rate 25% ● USB2.0: use rate 0% ● Gbit-Ether: use rate 30% ● DRAM use rate 28%	2.57
UseCase2	Use case assuming 1 screen display (2D graphics x 1) ● CortexA55 (2Core/CPU0: use rate 62%, CPU1: use rate 62%) ● GPU: use rate 65% ● System/Bus/Clock: use rate 50% ● MIPI-DSI: use rate 90% ● MIPI-CSI: use rate 25% ● USB2.0: use rate 0% ● Gbit-Ether: use rate 30% ● DRAM use rate 43%	2.64
UseCase3	Use case assuming 1 screen display (3D graphics x 1) ● CortexA55 (2Core/CPU0: use rate 62%, CPU1: use rate 62%) ● GPU: use rate 70% ● System/Bus/Clock: use rate 55% ● MIPI-DSI: use rate 90% ● MIPI-CSI: use rate 25% ● USB2.0: use rate 0% ● Gbit-Ether: use rate 30% ● DRAM use rate 31%	2.62

Table 4.1 Operation summary of each use case (2/2)

Use Case	Operation summary	Power consumption (w)
UseCase4	Use case assuming 1 screen display (3D graphics x 1) • CortexA55 (2Core/CPU0: use rate 79%, CPU1: use rate 79%) • GPU: use rate 70% • System/Bus/Clock: use rate 75% • MIPI-DSI: use rate 90% • MIPI-CSI: use rate 25% • USB2.0: use rate 0% • Gbit-Ether: use rate 30% • DRAM use rate 66%	2.97

4.3 The power consumption in each use case

- Estimation conditions of power consumption

  Tj = 125°C, Power supply (1.1V) = 1.1V, Power Supply (DDR4) = 1.2V, Power Supply (1.8V) = 1.8V,
  Power Supply (3.3V) = 3.3V, Process = FF process silicon, CPU: Cortex-A55@1.2GHz, DDR4-1600 16bit × 1ch

Table 4.2 The power consumption in each use case

Unit: (W)

Use Case	1.1V	1.2V	1.8V	3.3V	total
UseCase1	1.81	0.06	0.20	0.50	2.57
UseCase2	1.84	0.09	0.20	0.50	2.64
UseCase3	1.86	0.06	0.20	0.50	2.62
UseCase4	2.13	0.13	0.20	0.50	2.97

4.4 Limit Ta in each use case (13mm sq)

We calculated Limit Ta*[1] from θja which is calculated by thermal simulation.
Limit Ta is shown in the following table. But please remind that the limit Ta and θja in each use case is reference value based on JEDEC environment, and the Ta and θja could be fluctuated by the customer use case.
The formula of Limit Ta is as follows.

Note 1. Limit Ta is the limit value of Ta to keep the Tjmax within the specified value.

$$\text{Formula: Limit Ta}(°C) = 125(°C) - \text{Pd} \times \theta\text{ja}$$

Table 4.3 The Limit Ta in each use case

Unit: (°C)

Use Case	w/o Heat Sink			w/ Heat Sink		
	Air Velocity 0m/sec	Air Velocity 1m/sec	Air Velocity 2m/sec	Air Velocity 0m/sec	Air Velocity 1m/sec	Air Velocity 2m/sec
UseCase1	74.9	83.4	85.0	80.5	85.0	85.0
UseCase2	73.5	82.2	84.6	79.3	85.0	85.0
UseCase3	73.9	82.6	84.9	79.7	85.0	85.0
UseCase4	67.1	76.9	79.6	73.6	85.0	85.0

θja is the following values.

Refer to **Section 5, Thermal simulation model** for the thermal simulation model.

Table 4.4 The θja in each use case

Unit: (°C)

Use Case	w/o Heat Sink			w/ Heat Sink		
	Air Velocity 0m/sec	Air Velocity 1m/sec	Air Velocity 2m/sec	Air Velocity 0m/sec	Air Velocity 1m/sec	Air Velocity 2m/sec
UseCase1	19.5	16.2	15.3	17.3	12.2	11.2
UseCase2	19.5	16.2	15.3	17.3	12.2	11.2
UseCase3	19.5	16.2	15.3	17.3	12.2	11.2
UseCase4	19.5	16.2	15.3	17.3	12.2	11.2

5. Thermal simulation model

5.1 Ref : SIMULATION model for thermal analysis (13mm sq)

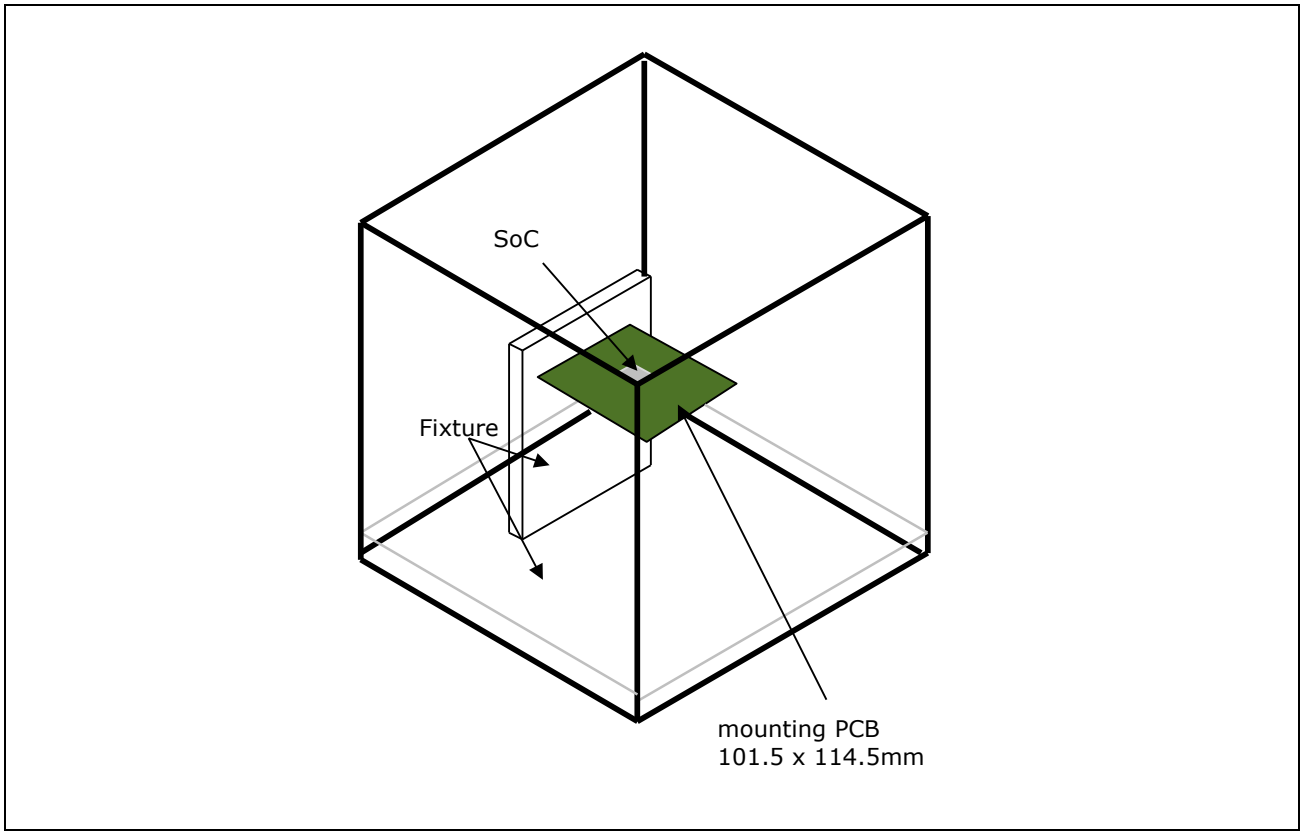
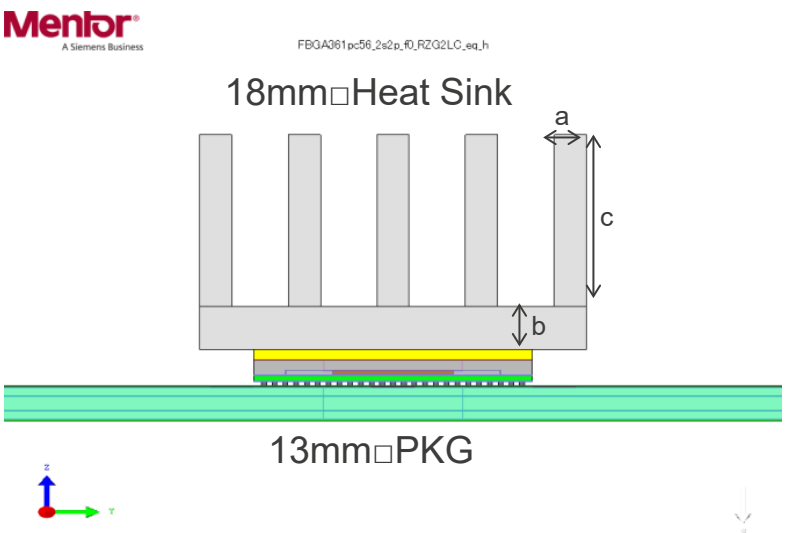


Figure 5.1 external environment based on JESD51-2A

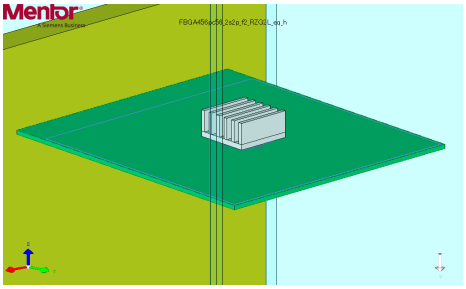
	SR	0.032	[mm]
L1	Cu 50%	0.07	[mm]
	FR4	0.375	[mm]
L2	Cu 95%	0.035	[mm]
	FR4	0.64	[mm]
L3	Cu 95%	0.035	[mm]
	FR4	0.375	[mm]
L4	Cu 50%	0.07	[mm]
	SR	0.032	[mm]
	Total	1.664	[mm]

Figure 5.2 mounting PCB layer information based on JESD51-9



a. Thickness of Fin : 1.50mm
b. Thickness of Pedestal : 2.00mm
c. Height of Fin : 8.00mm

Figure 5.3 Heat Sink information



Thermal conductivity of each materials

Heat Sink (Aluminum alloy ; A6071)	: 180W/(mK)
TIM between Device and Heat Sink	: 1.00W/(mK)

Figure 5.4 Thermal conductivity of each materials

5.2 Ref : Parameter (θjc, θjb)

Table 5.1 Prameter(θjc, θjb) of 13mm sq

Package Outline	Heat Sink	θjc (°C/W)	θjb (°C/W)
13mm sq	No	8.3	10.6

REVISION HISTORY	RZ/G2LC Thermal Management Guideline

Rev.	Date	Description	
		Page	Summary
1.00	Oct 07, 2021	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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Contact information

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