Design Guidelines

PCB Design Guidelines
For Core VDD and DDR3L DDR_VDDQ

Renesas Microprocessor
RZ Family / RZ/A Series

RTK0EF0137C01000BJ

Notice

1 Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2 Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights,or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3 No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4 You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export,manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.

5 You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

6 Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

7 No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE,HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.

8 When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

9 Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

10 Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11 Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

12 It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

13 This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

14 Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.1.00-19 July 2023)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1 Precaution against Electrostatic Discharge (ESD)
A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2 Processing at power-on
The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3 Input of signal during power-off state
Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4 Handling of unused pins
Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5 Clock signals
After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6 Voltage application waveform at input pin
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL(Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7 Prohibition of access to reserved addresses
Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8 Differences between products
Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values,operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a systemevaluation test for the given product.

The purpose of this guide

This guide helps PCB design engineers to verify their design and arrive to their design goal. To achieve the best SOC performance, Power Distribution Network (PDN) for core power supply is very important.
Therefore, we recommend the PDN impedance get lower than the target impedance of this SOC.
This guide describes a) PCB design restrictions, b) verification items and c) how to measure them.
It is indispensable to satisfy PCB restrictions described in this guide in order to enable core function in user's system. Renesas recommends the customer to confirm satisfying restrictions in this guide.
All information shown in this guide, including product specifications, represents the information at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp.
SOC means RZ/A3M (PBGA) in this document.

Table of Contents

1. Introduction

1.1 Overview

This application note provides guidelines for designing power supply line boards.

Target LSI:
RZ/A3M Group

[Note] In the rest of this application note, the term “group” will be omitted. The content in this application note is a reference example based on the USB standard, and does not guarantee the signal quality in the system. When incorporating it into an actual system, it is the responsibility of the customer to make a thorough examination and evaluation of the entire system and determine whether or not it can be applied.

Related application notes
Application notes related to this application note are listed below. See also.

- RZ/A Series Hardware Design Guide (R01AN4813JJ)

The chapters of this guide are organized as follows:

- **Section 1** describes operating conditions and power name list of core and DDR3L.
- **Section 2** PCB Design Guideline for Core VDD.
- **Section 3** PCB Design Guideline for DDR3L DDR_VDDQ1.
- **Section 4** PCB Design Guideline for DDR3L DDR_VDDQ2.

1.2 Power name

Power supply pins are listed in **Table 1.1**.

Table 1.1 Power supply

Pin Name	Description
VDD	Power supply for CPU core
DDR_VDDQ1	Power supply for internal DDR3L memory
DDR_VDDQ2	Power supply for built-in DDR3L memory control module
VSS	Ground pin (common with other power supplies)

1.3 Operating conditions

Operating conditions for each power supply are listed in **Table 1.2**.

Table 1.2 Power supply

Pin Name	Classification	Voltage range	Symbol
VDD	Digital power	1.05 ~ 1.15V	1.1V
DDR_VDDQ1	Digital power	1.283 ~ 1.450V	1.35V
DDR_VDDQ2	Digital power	1.283 ~ 1.450V	1.35V
VSS	Digital ground	0V	

2. PCB Design Guideline for Core VDD

2.1 Power supply configuration for Core VDD

Figure 2.1 shows a circuit diagram image of Core power supply and external parts.
Power supply impedance of your PCB must be lower than target impedance for Core power supply (VDD).

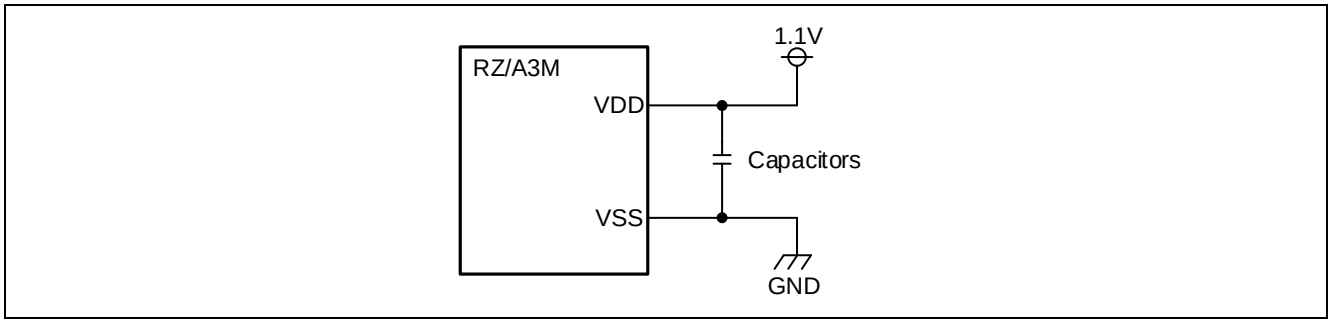

Figure 2.1 Circuit diagram of Core power supply (VDD) and external parts

2.2 An example of capacitor selections

Table 2.1 shows a concrete example of capacitor selections for RZ/A3M Reference board(RTK0EF0137C01000BJ).

Table 2.1 A concrete example of capacitor selections of RZ/A3M Reference board

Pin Name	Value	Pics.
	10uF	6
	4.7uF	7
	0.1uF	3

2.3 An example of board layer configuration

Table 2.2 shows a concrete example of board layer configuration for RZ/A3M Reference board(RTK0EF0137C01000BJ).

Table 2.2 A concrete example of board layer configuration of RZ/A3M Reference board

number of layers	2		
	Thickness **[um]**	**D**ielectric constant **(1GHz)**	**L**oss tangent **(1GHz)**
Resist	30	3.7	0.017
L1 copper foil	48	-	-
L1 – L2	1564	4.3	0.016
L2 copper foil	48	-	-
Resist	30	3.7	0.017

2.4 An example of Power/ground pattern

This section describes points to note when designing power supply and ground patterns.

Figures 2.2 and **Figures 2.3** show examples of power and ground connections.

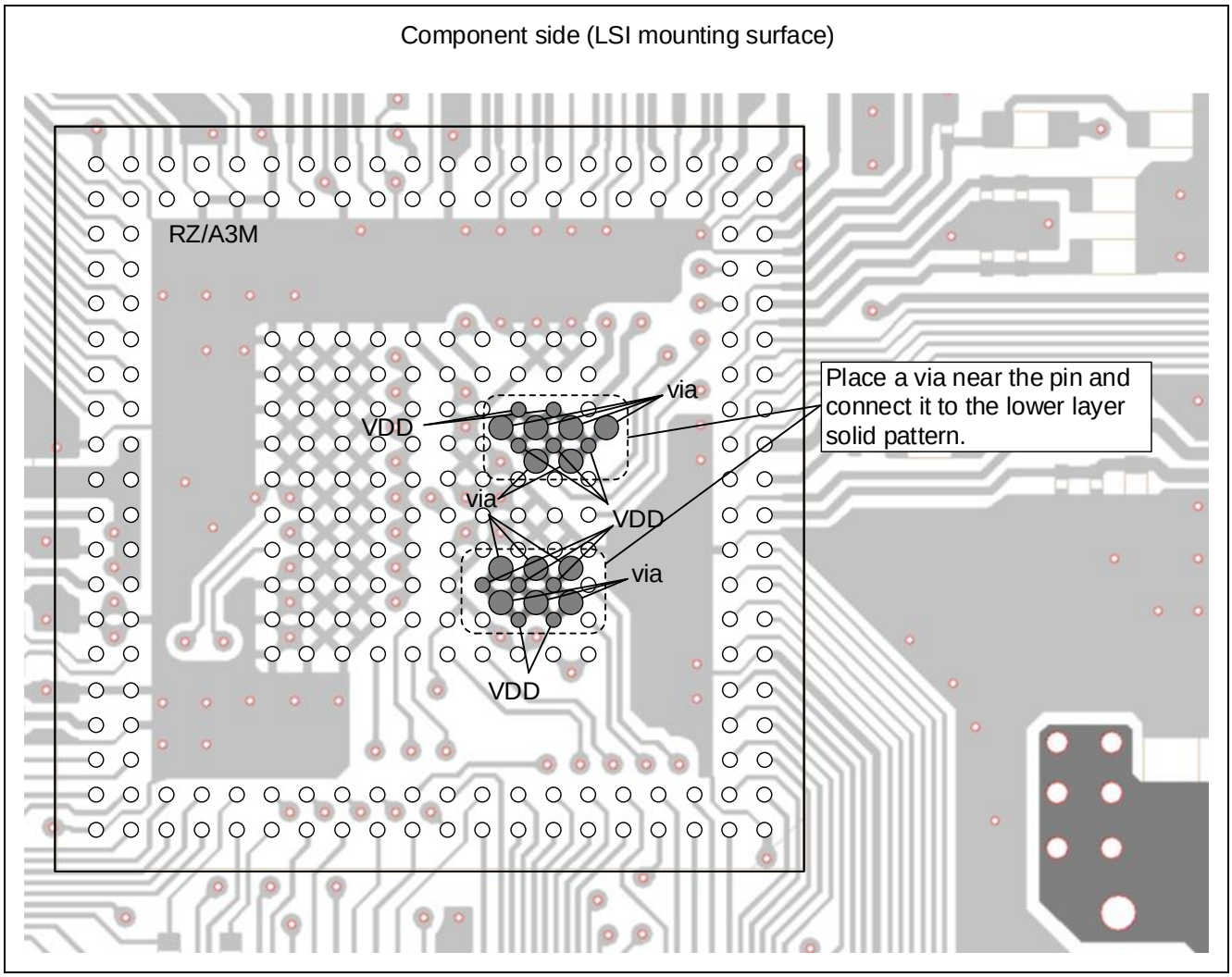

Figure 2.2 Patern image of Core power supply (VDD) and external parts (Component side)

Place the bypass capacitor close to the power supply pin. Also pay attention to the wiring resistance and wiring inductance of the power line.
Draw the solid pattern of the power supply as thick as possible.

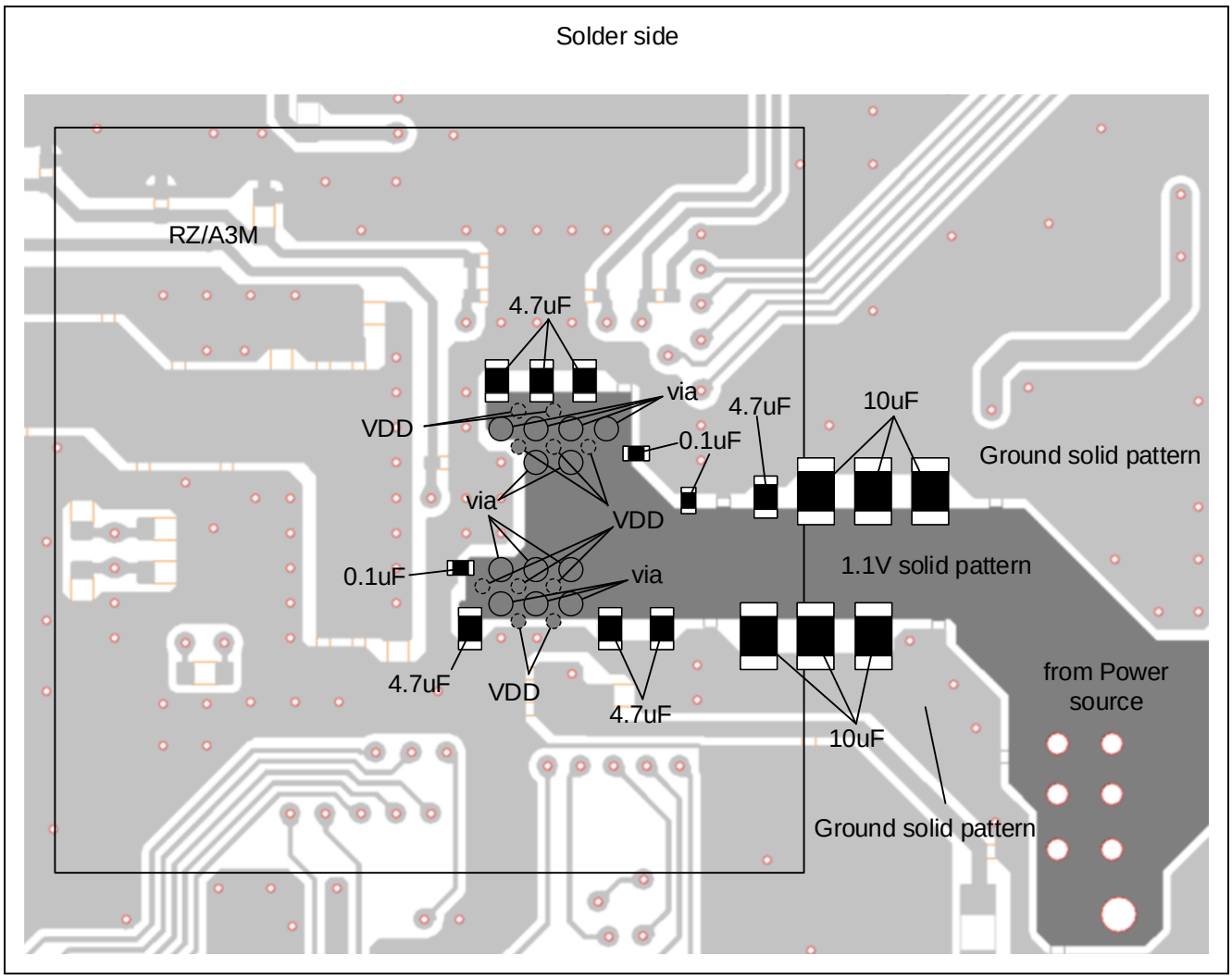

Figure 2.3 Patern image of Core power supply (VDD) and external parts (Solder side)

2.5 Simulation

2.5.1 Simulation conditions

See **Table 2.2** for board simulation conditions.
The target impedances Ztarget(f) are shown in **Table 2.3**. Frequency range for Ztarget(f) is defined higher than 1MHz.
Core PDN must be designed so that the voltage is kept in the range specified by SOC specification.

Table 2.3 Target impedance for SOC Core PDN

		Target impedance : Ztarget(f)		
Pin name	Frequency	Min	Max	Unit
VDD	1kHz ~ 1.1MHz	–	25	mΩ
	1.1MHz ~ 20MHz	–	60	mΩ
	20MHz ~ 1GHz	–	165	mΩ

2.5.2 Simulation result

As a result of the simulation, we have confirmed that the impedance at each frequency meets the target as shown in **Figure 2.4**.
As shown in **Figure 2.4**, design so that all impedances are smaller than the target impedance at all frequencies.

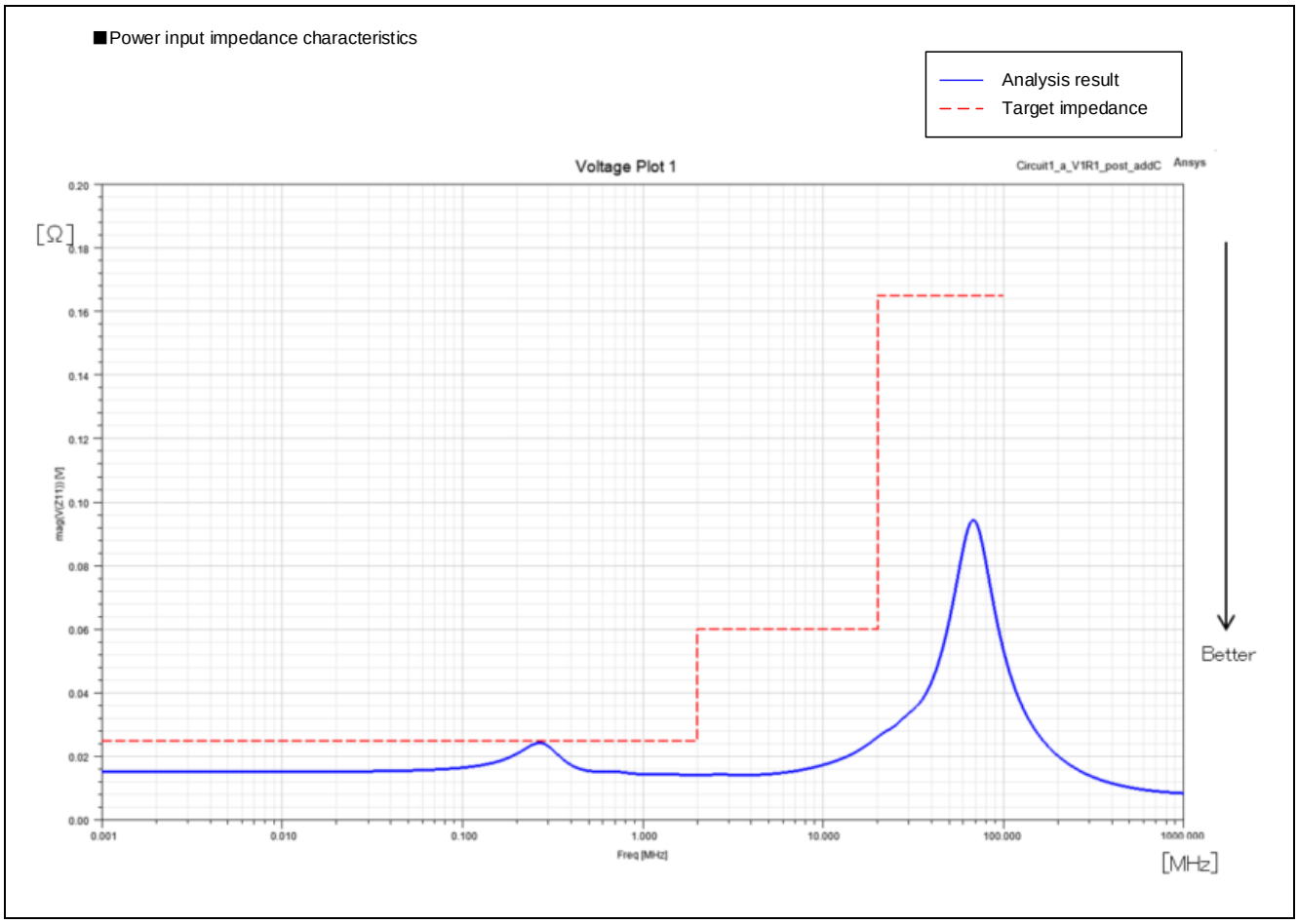

Figure 2.4 Target impedance of core power supply and impedance data

3. PCB Design Guideline for DDR3L DDR_VDDQ1

3.1 Power supply configuration for DDR3L DDR_VDDQ1

Figure 3.1 shows a circuit diagram image of DDR3L power supply and external parts.
Power supply impedance of your PCB must be lower than target impedance for DDR3L power supply (DDR_VDDQ1).

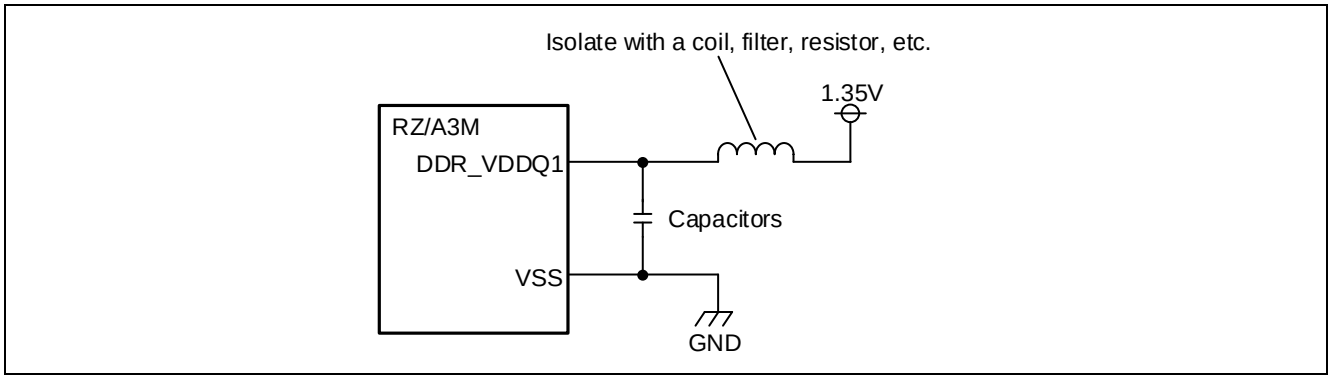

Figure 3.1 Circuit diagram of DDR3L power supply (DDR_VDDQ1) and external parts

3.2 An example of capacitor selections

Table 3.1 shows a concrete example of capacitor selections for RZ/A3M Reference board(RTK0EF0137C01000BJ).

Table 3.1 A concrete example of capacitor selections of RZ/A3M Reference board

Pin Name	Value	Pics.
	4.7uF	1
	1uF	2
	0.1uF	7
	100pF	4

3.3 An example of board layer configuration

Table 2.2 shows a concrete example of board layer configuration for RZ/A3M Reference board(RTK0EF0137C01000BJ).

3.4 An example of Power/ground pattern

This section describes points to note when designing power supply and ground patterns.

Figures 3.2 and **Figures 3.3** show examples of power and ground connections.

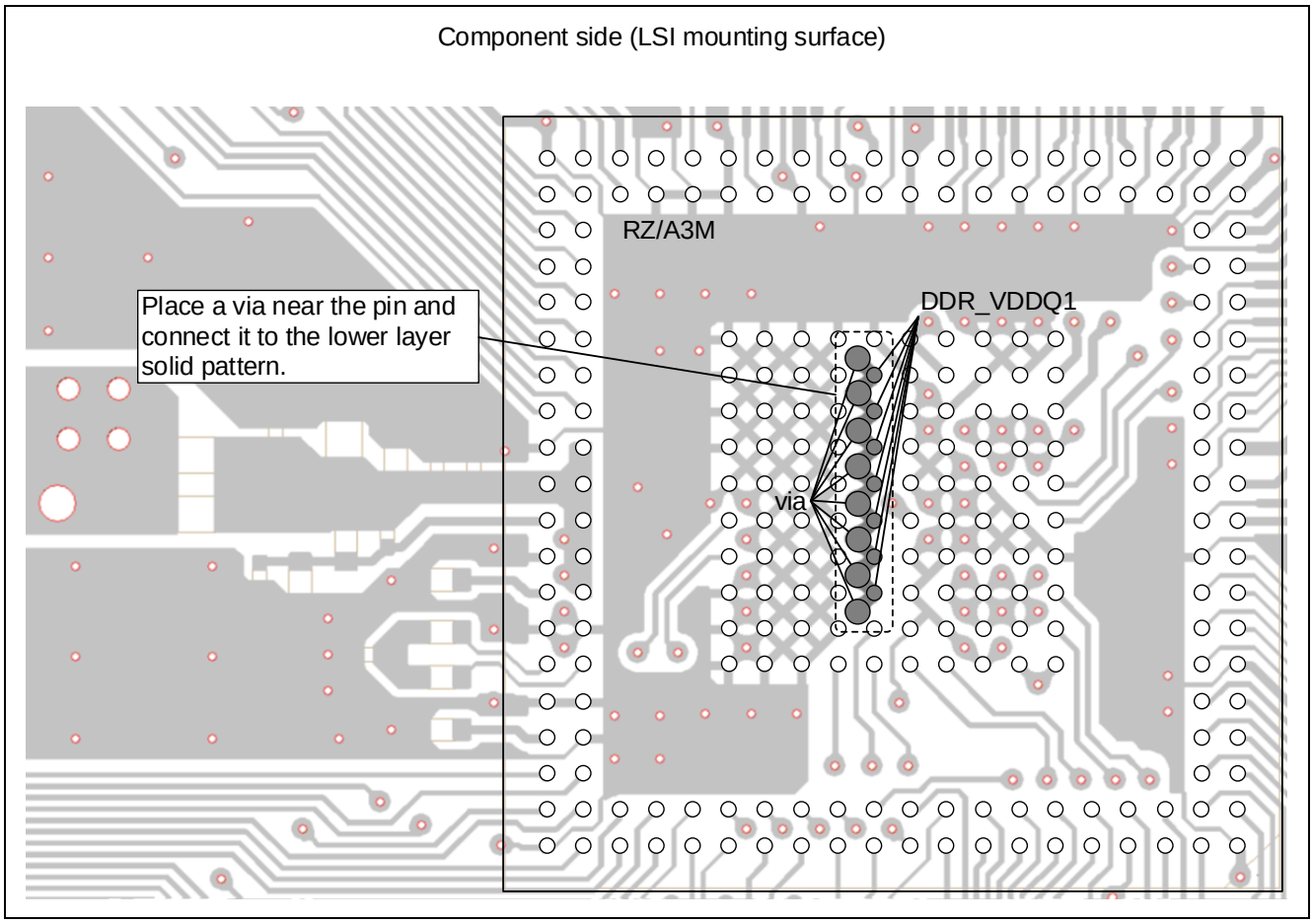

Figure 3.2 Patern image of DDR3L power supply (DDR_VDDQ1) and external parts (Component side)

Place the bypass capacitor close to the power supply pin. Also pay attention to the wiring resistance and wiring inductance of the power line.
Draw the solid pattern of the power supply as thick as possible.

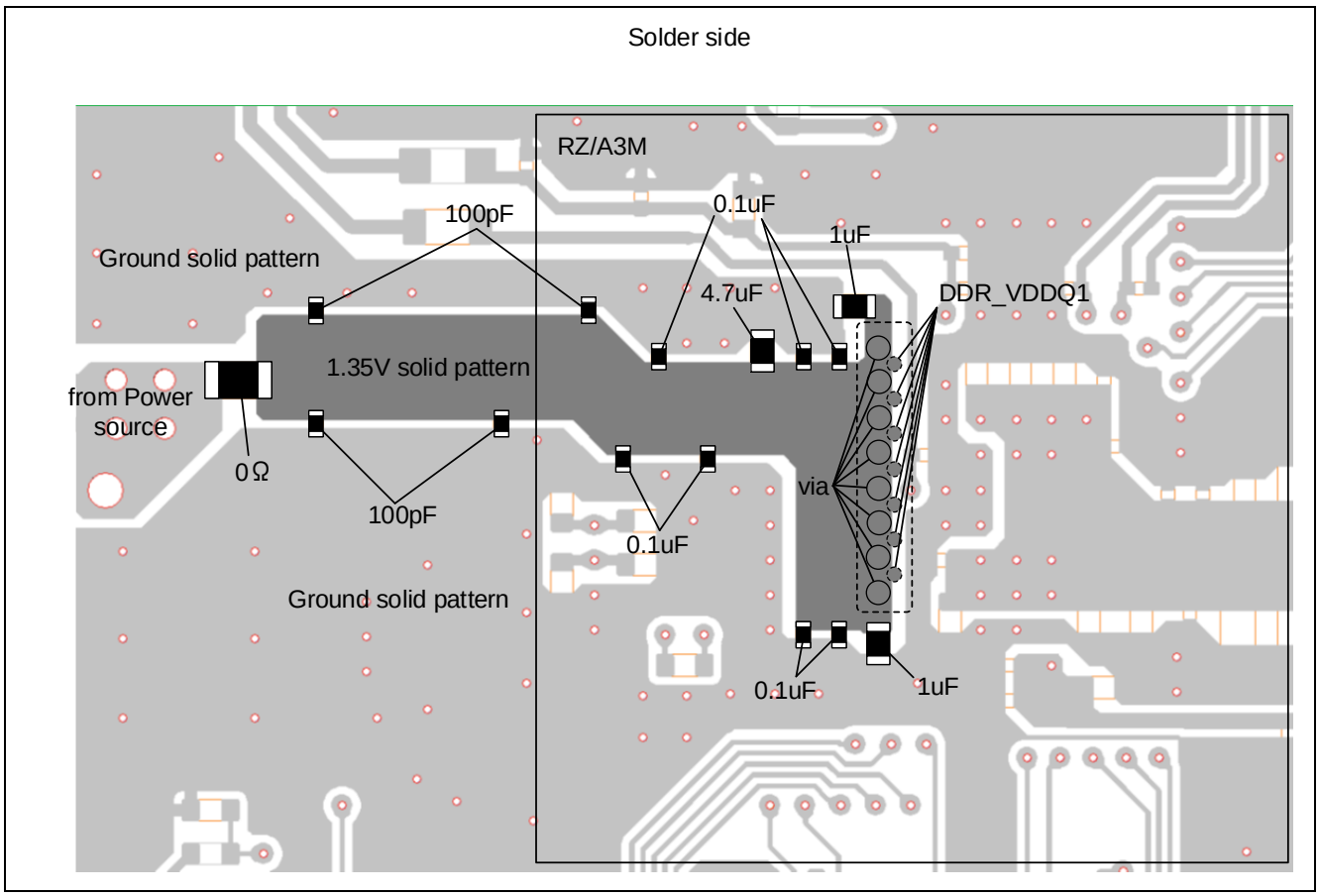

Figure 3.3 Patern image of DDR3L power supply (DDR_VDDQ1) and external parts (Solder side)

3.5 Simulation

3.5.1 Simulation conditions

See **Table 2.2** for board simulation conditions.
The target impedances Ztarget(f) are shown in **Table 3.2**. Frequency range for Ztarget(f) is defined higher than 1MHz.
Core PDN must be designed so that the voltage is kept in the range specified by SOC specification.

Table 3.2 Target impedance for SOC Core PDN

		Target impedance : Ztarget(f)		
Pin name	Frequency	Min	Max	Unit
DDR_VDDQ1	1kHz ~ 20MHz	–	80	mΩ
	20MHz ~ 1GHz	–	325	mΩ

3.5.2 Simulation result

As a result of the simulation, we have confirmed that the impedance at each frequency meets the target as shown in **Figure 3.4**.
As shown in **Figure 3.4**, design so that all impedances are smaller than the target impedance at all frequencies.

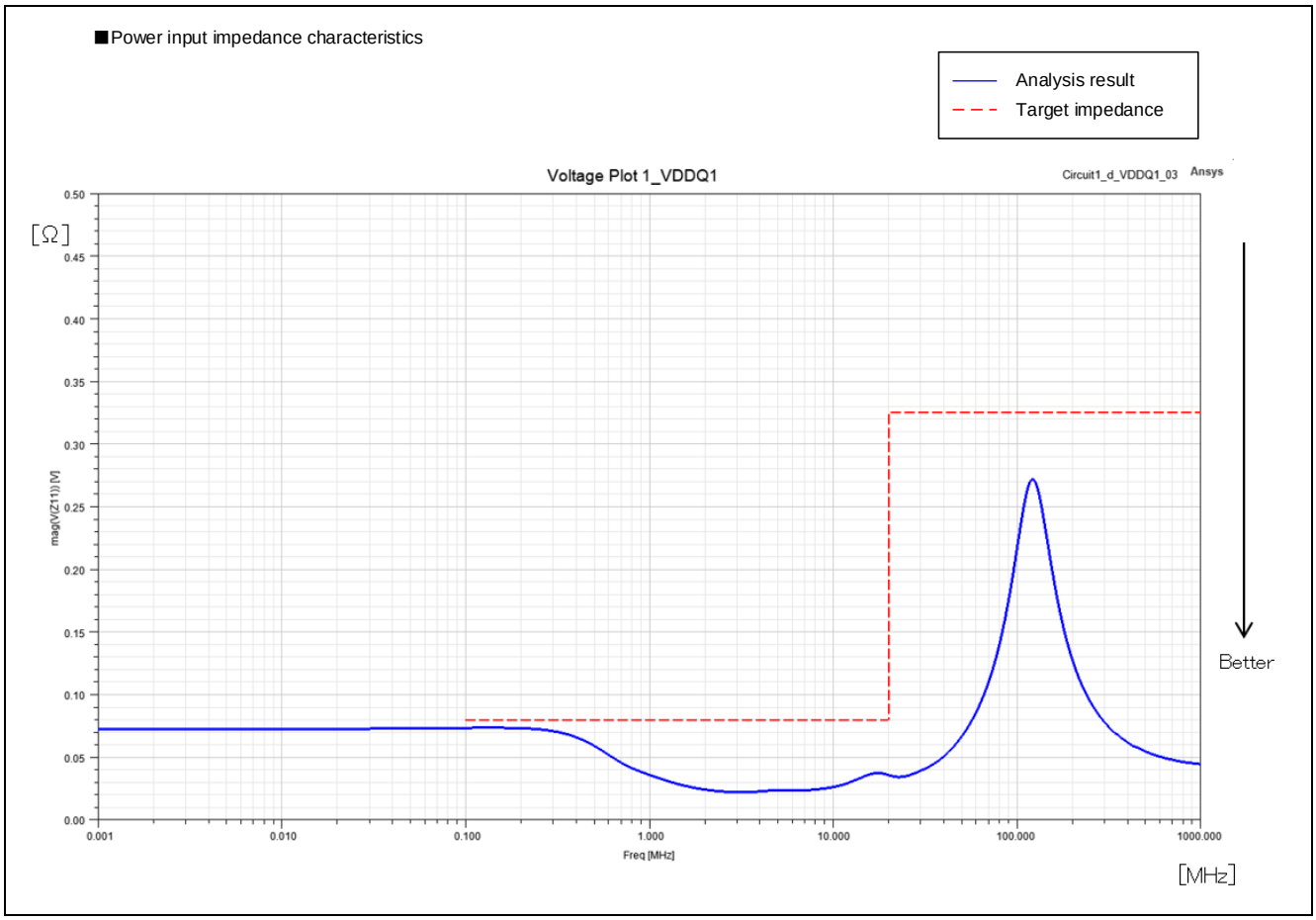

Figure 3.4 Target impedance of core power supply and impedance data

4. PCB Design Guideline for DDR3L DDR_VDDQ2

4.1 Power supply configuration for DDR3L DDR_VDDQ2

Figure 4.1 shows a circuit diagram image of DDR3L power supply and external parts.
Power supply impedance of your PCB must be lower than target impedance for DDR3L power supply (DDR_VDDQ2).

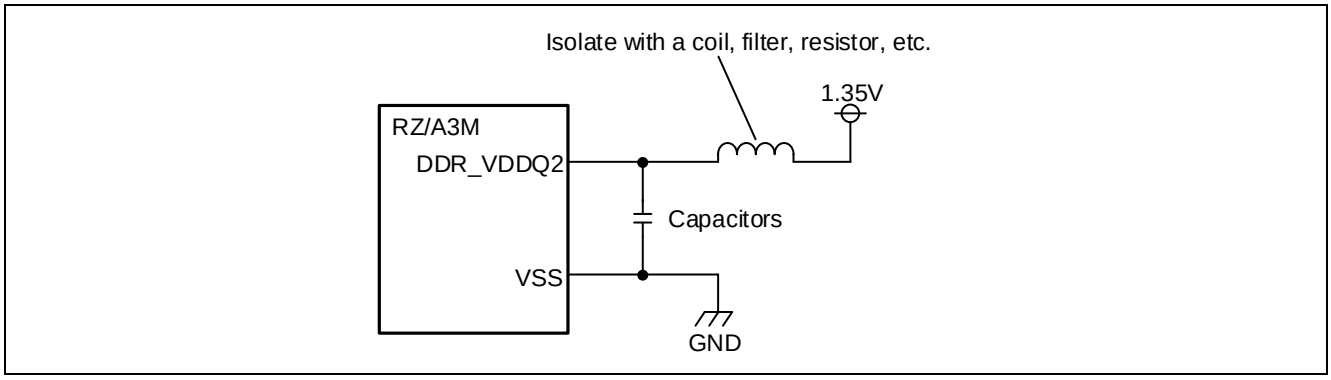

Figure 4.1 Circuit diagram of DDR3L power supply (DDR_VDDQ2) and external parts

4.2 An example of capacitor selections

Table 3.1 shows a concrete example of capacitor selections for RZ/A3M Reference board(RTK0EF0137C01000BJ).

Table 3.1 A concrete example of capacitor selections of RZ/A3M Reference board

Pin Name	Value	Pics.
	10uF	1
	4.7uF	5
	0.1uF	2

4.3 An example of board layer configuration

Table 2.2 shows a concrete example of board layer configuration for RZ/A3M Reference board(RTK0EF0137C01000BJ).

4.4 An example of Power/ground pattern

This section describes points to note when designing power supply and ground patterns.

Figures 4.2 and **Figures 4.3** show examples of power and ground connections.

Place the bypass capacitor close to the power supply pin. Also pay attention to the wiring resistance and wiring inductance of the power line.
Draw the solid pattern of the power supply as thick as possible.

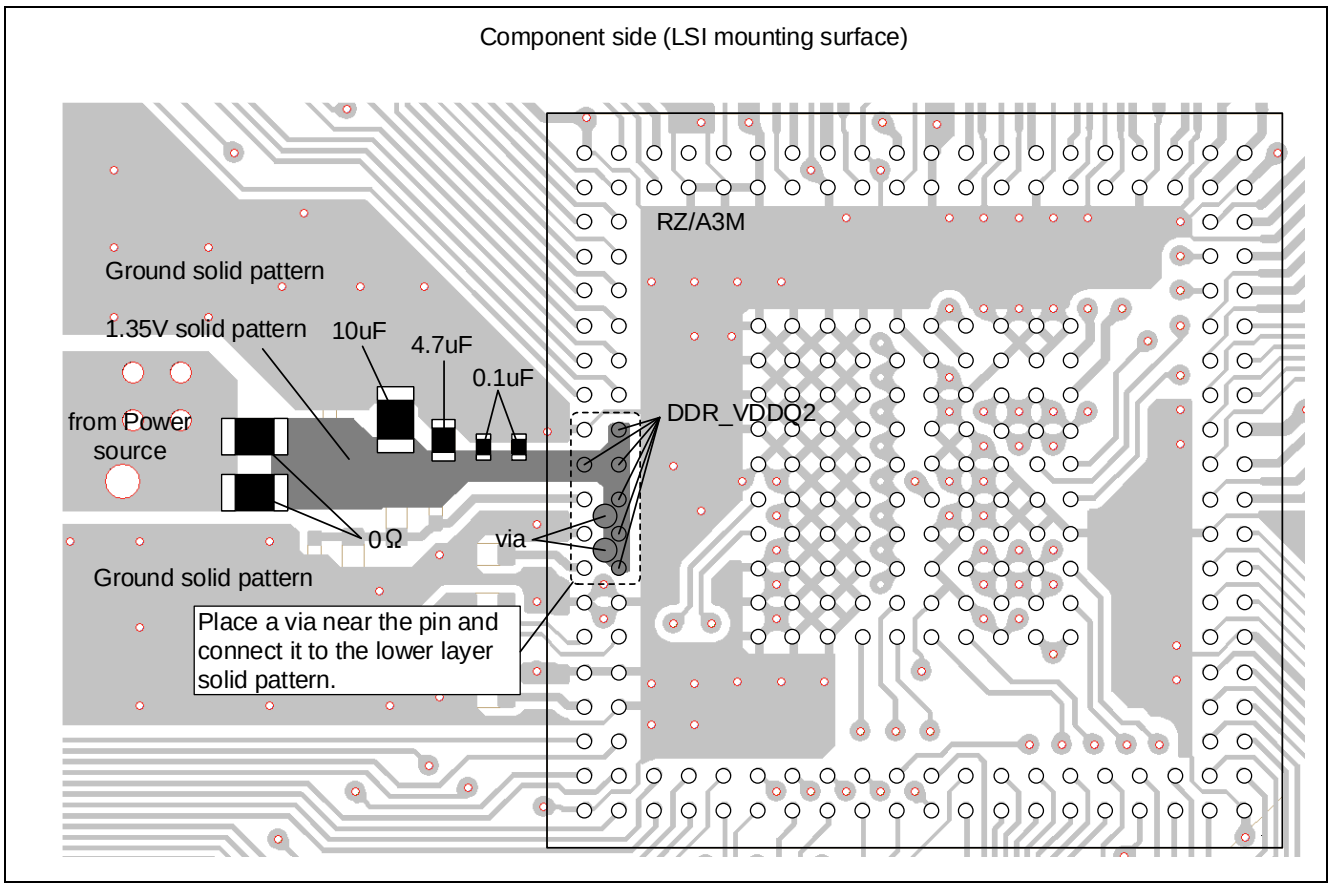

Figure 4.2 Patern image of DDR3L power supply (DDR_VDDQ2) and external parts (Component side)

Place the bypass capacitor close to the power supply pin. Also pay attention to the wiring resistance and wiring inductance of the power line.
Draw the solid pattern of the power supply as thick as possible.

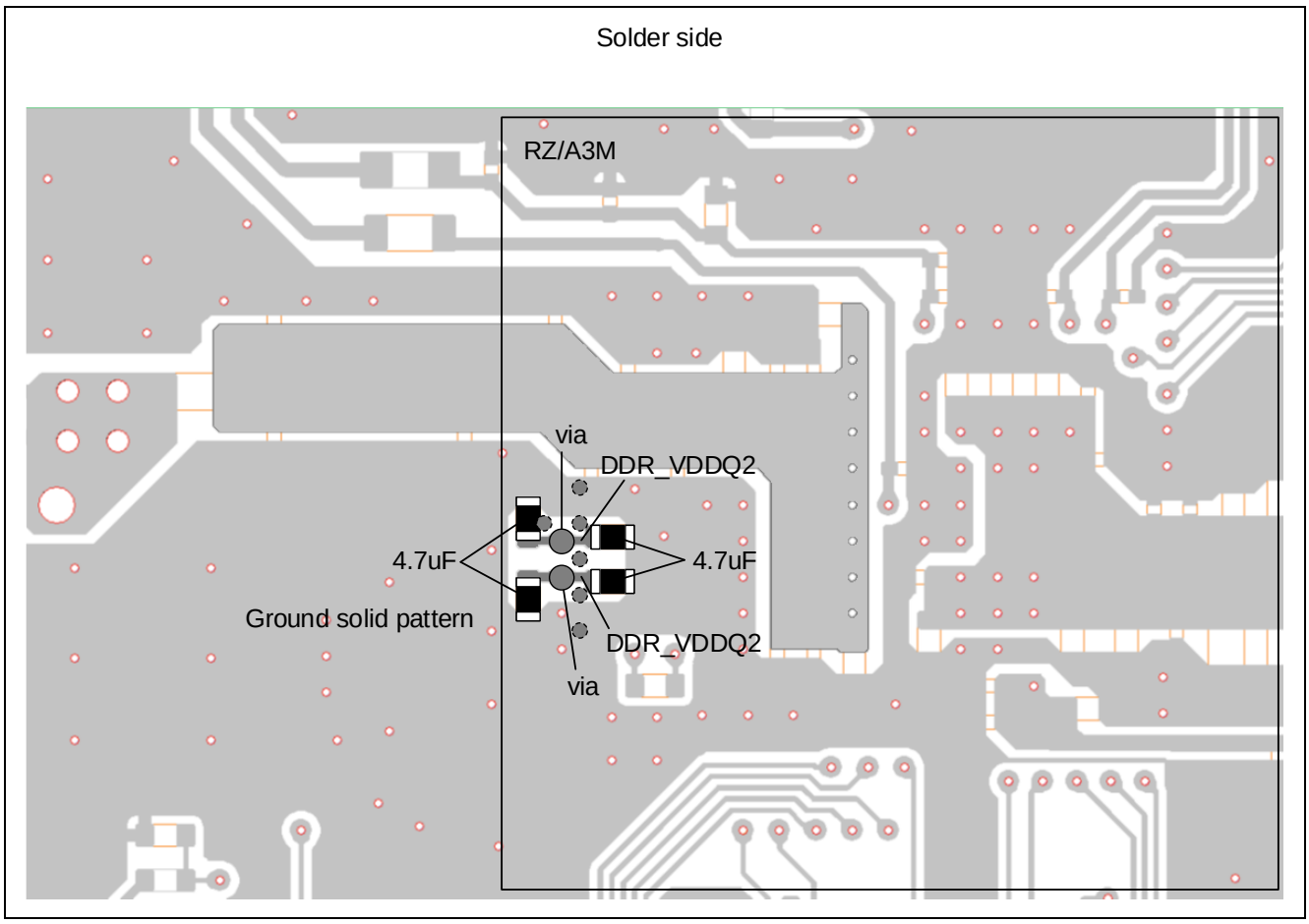

Figure 4.3 Patern image of DDR3L power supply (DDR_VDDQ2) and external parts (Solder side)

4.5 Simulation

4.5.1 Simulation conditions

See **Table 2.2** for board simulation conditions.
The target impedances Ztarget(f) are shown in **Table 4.2**. Frequency range for Ztarget(f) is defined higher than 1MHz.
Core PDN must be designed so that the voltage is kept in the range specified by SOC specification.

Table 4.2 Target impedance for SOC Core PDN

		Target impedance : Ztarget(f)		
Pin name	Frequency	Min	Max	Unit
DDR_VDDQ2	1kHz ~ 10MHz	–	70	mΩ
	10MHz ~ 20MHz	–	150	mΩ
	20MHz ~ 1GHz	–	450	mΩ

4.5.2 Simulation result

As a result of the simulation, we have confirmed that the impedance at each frequency meets the target as shown in **Figure 4.4**.
As shown in **Figure 4.4**, design so that all impedances are smaller than the target impedance at all frequencies.

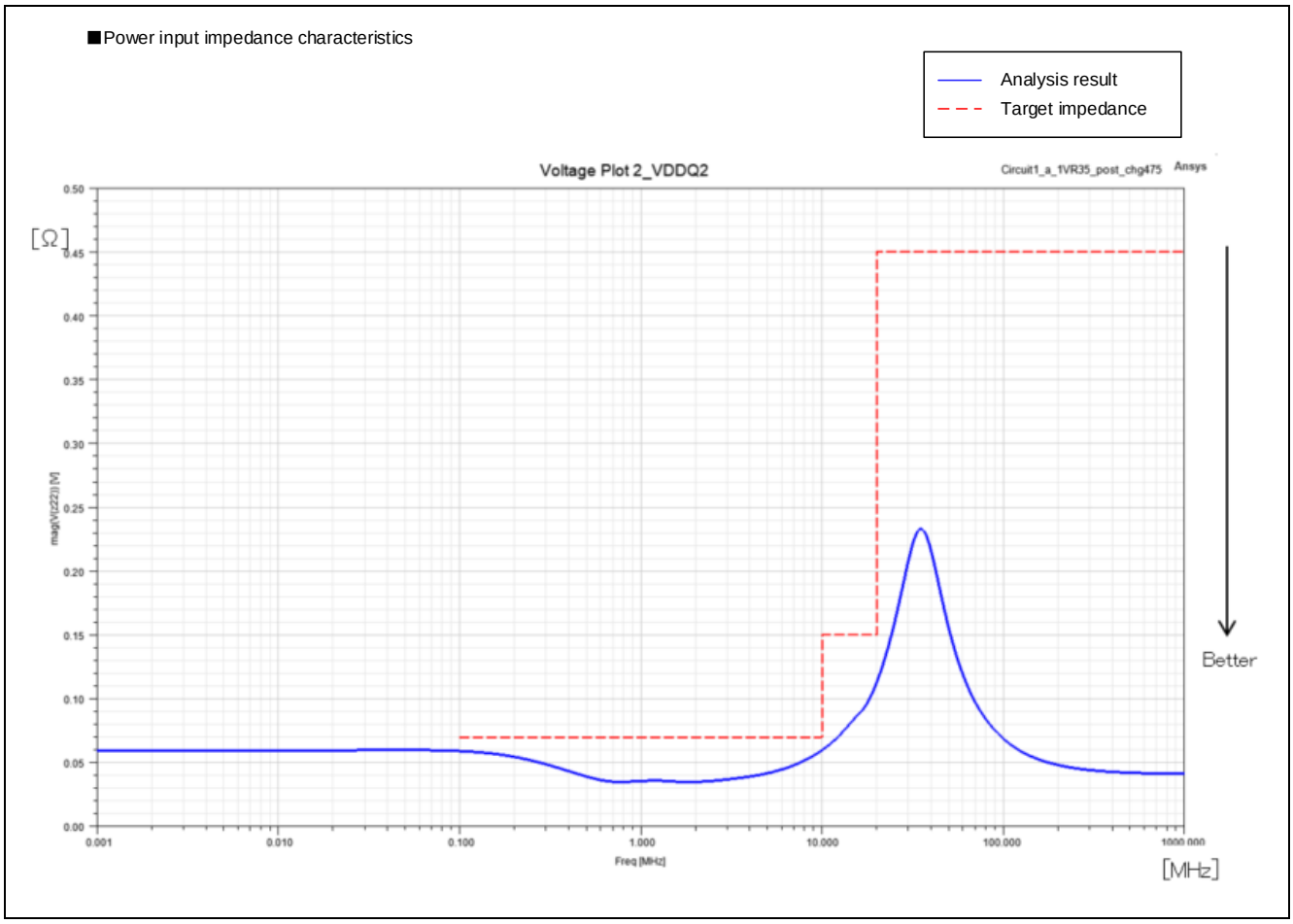

Figure 4.4 Target impedance of core power supply and impedance data

5. PCB Design Guideline for Ground plane

- Provide as wide a ground plane as possible.
- Perform appropriate grounding as necessary.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.07.03	–	First edition issued
1.01	2023.12.12	22	Item 5 Added PCB Design Guideline for Ground plane

RZ/A3M Group PCB Design Guidelines for Core VDD and DDR3L DDR_VDDQ

Publication Date: Rev.1.00 July 03 , 2023

Published by: Renesas Electronics Corporation