Design Guidelines

PCB Design Guidelines for MIPI-DSI and USB2.0

Renesas Microprocessor RZ Family / RZ/A Series

RTK0EF0137C01000BJ

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(Rev.1.00-19 July 2023)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1 Precaution against Electrostatic Discharge (ESD)
A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2 Processing at power-on
The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3 Input of signal during power-off state
Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4 Handling of unused pins
Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5 Clock signals
After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6 Voltage application waveform at input pin
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL(Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7 Prohibition of access to reserved addresses
Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8 Differences between products
Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values,operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a systemevaluation test for the given product.

The purpose of this guide

This guide helps PCB design engineers to verify their design and arrive to their design goal. To achieve the best SOC performance, Power Distribution Network (PDN) for core power supply is very important.
Therefore, we recommend the PDN impedance get lower than the target impedance of this SOC.
This guide describes a) PCB design restrictions, b) verification items and c) how to measure them.
It is indispensable to satisfy PCB restrictions described in this guide in order to enable core function in user's system. Renesas recommends the customer to confirm satisfying restrictions in this guide.
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SOC means RZ/A3M (PBGA) in this document.

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1. Guidelines for MIPI-DSI

1.1 Guidelines for signal lines topology(Tx)

MIPI-DSI interface is a MIPI DSI-2 host controller that supports MIPI DSI V1.3.1 and MIPI D-PHY V2.1.
Please refer to the MIPI D-PHY specification ver2.1 regarding the transmitter specifications.
Figure 1.1 shows a schematic diagram of MIPI-DSI connections, and **Table 1.1** shows an overview of MIPI-DSI module terminals.

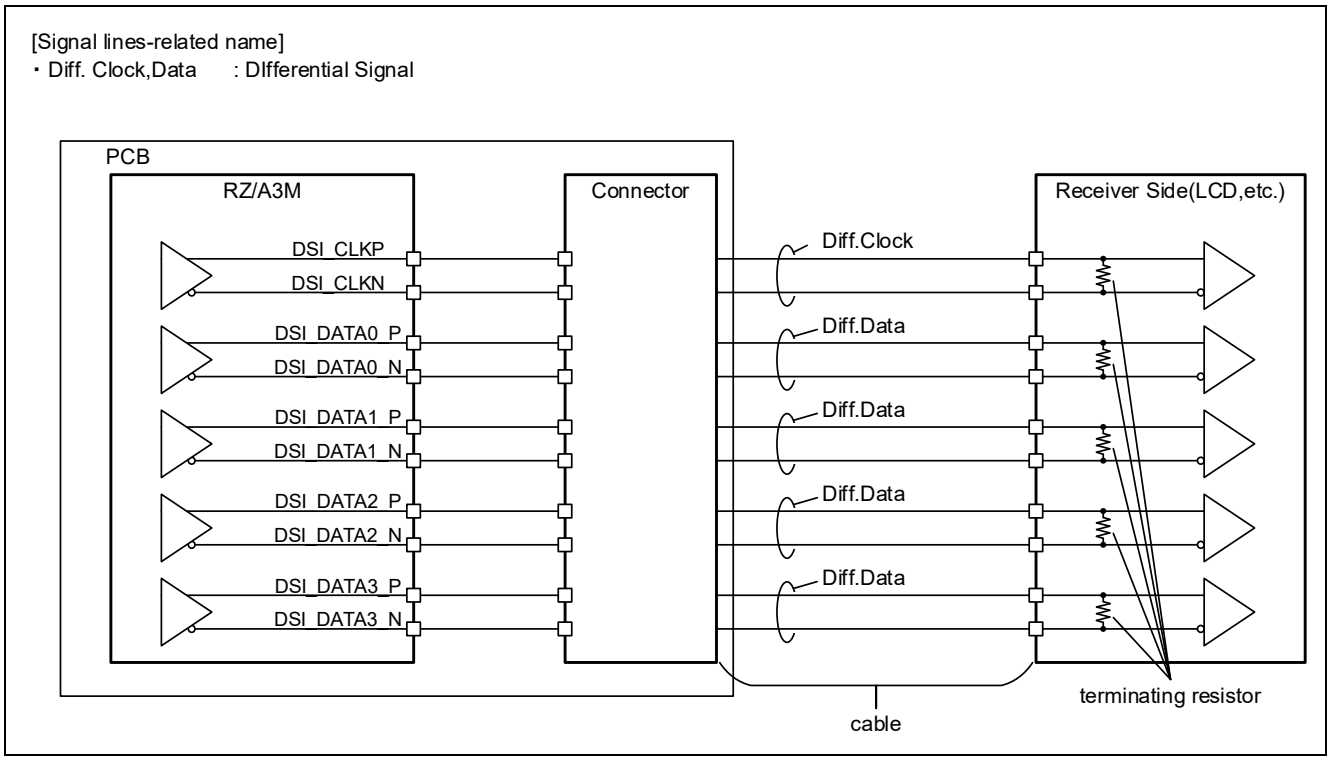

Figure 1.1 Signal lines topology of MIPI-DSI

Table1.1 MIPI-DSI module pin overview

Pin name	Input/Output	function
DSI_CLKP	Output	MIPI-DSI differential clock + output pin.
DSI_CLKN	Output	MIPI-DSI differential clock - output pin.
DSI_DATA0_P	Output	MIPI-DSI differential data (lane 0) output pin +.
DSI_DATA0_N	Output	MIPI-DSI differential data (lane 0) output pin -.
DSI_DATA1_P	Output	MIPI-DSI differential data (lane 1) output pin +.
DSI_DATA1_N	Output	MIPI-DSI differential data (lane 1) output pin -.
DSI_DATA2_P	Output	MIPI-DSI differential data (lane 2) output pin +.
DSI_DATA2_N	Output	MIPI-DSI differential data (lane 2) output pin -.
DSI_DATA3_P	Output	MIPI-DSI differential data (lane 3) output pin +.
DSI_DATA3_N	Output	MIPI-DSI differential data (lane 3) output pin -.
DSI_VDD18	Power	Digital terminal power supply for MIPI-DSI.

1.2 Operating conditions

Please see RZ/A3M User's Manual.

1.3 Power name

Power supply pins are listed in **Table 1.1**.

Table1.2 Powr supply

Classification	Pin name	Voltage range	Symbol
Digital power	DSI_VDD18	1.65V～1.95V	
Digital ground	VSS	0V	

2. MIPI-DSI transmission line

MIPI-DSI transmission line represents the wiring pattern that connects the RZ/A3M and the MIPI-DSI connector. Since the maximum communication speed is 1 Gbps/1 lane, it must be designed as a transmission line high-frequency circuit. Also, the transmission line requires impedance control.

The points to note when designing transmission lines are explained below.

- The characteristic impedance required for transmission lines is a differential impedance of 100Ω±20%.
- For impedance control, the pattern width and pattern spacing vary depending on the substrate thickness, material, and layer configuration. For details, please consult the board manufacturer.
- Wire transmission lines as short and as equal in length as possible. At this time, not only should the positive and negative signal lines of the differential pair be of equal length, but also the wiring lengths of each data differential pair and clock differential pair should be equal.
- When bending the transmission line, do not bend it at a sharp angle (right angle), but bend it gently by using 135° or an arc.
- Do not use vias for transmission lines as much as possible and route them on the surface layer.
- When using vias, use as few vias as possible and match the number of vias on each data differential pair and clock differential pair.
- Also, do not allow vias to create stubs. **Figure 2.1** shows an example of stub formation with vias.
- Place ground vias symmetrically on both sides of the transmission line. **Figure 2.2** shows an example of ground via placement.
- The bottom layer of the transmission line should be a solid ground, and should not be divided by slits or the like. **Figure 2.3** shows an example of a solid ground under the transmission line.
- Be sure to use EMI and ESD countermeasure parts that support each interface. Note that mounting EMI/ESD countermeasure parts may cause impedance mismatch in the transmission line and may distort the waveform.
- Adequate spacing is required between transmission lines and adjacent ground patterns and signal lines. **Table 2.1** shows recommended spacing values between transmission lines and adjacent patterns. **Figure 2.4** shows an example of the spacing between a transmission line and an adjacent pattern, and **Figure 2.5** shows an example of transmission line pattern design.

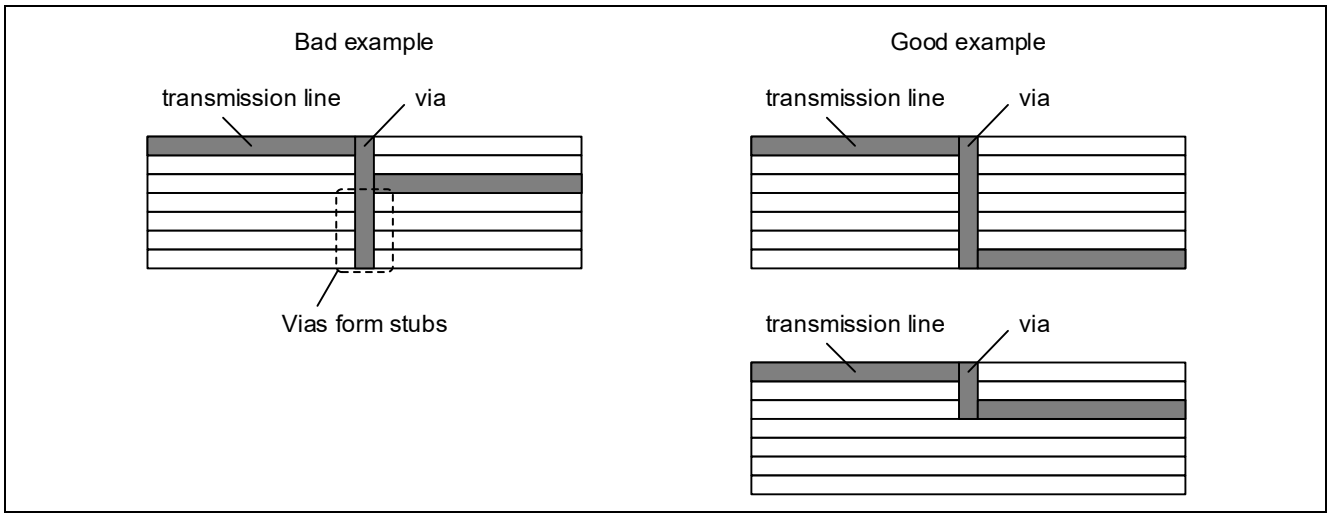

Figure 2.1 Example of stub formation with vias

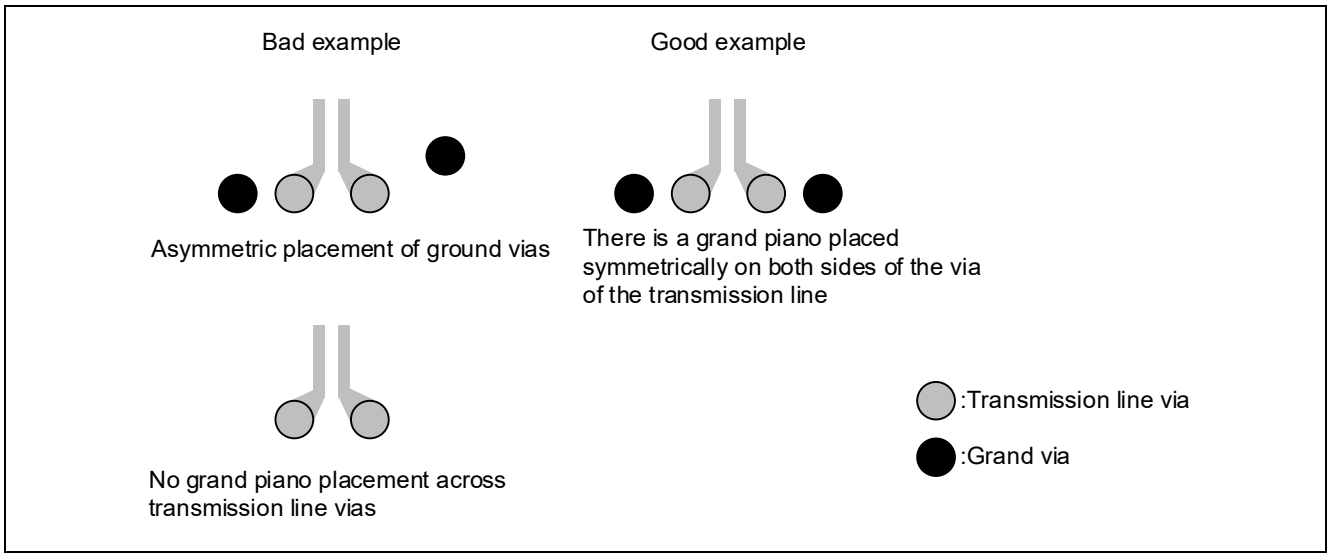

Figure 2.2 Ground via placement example

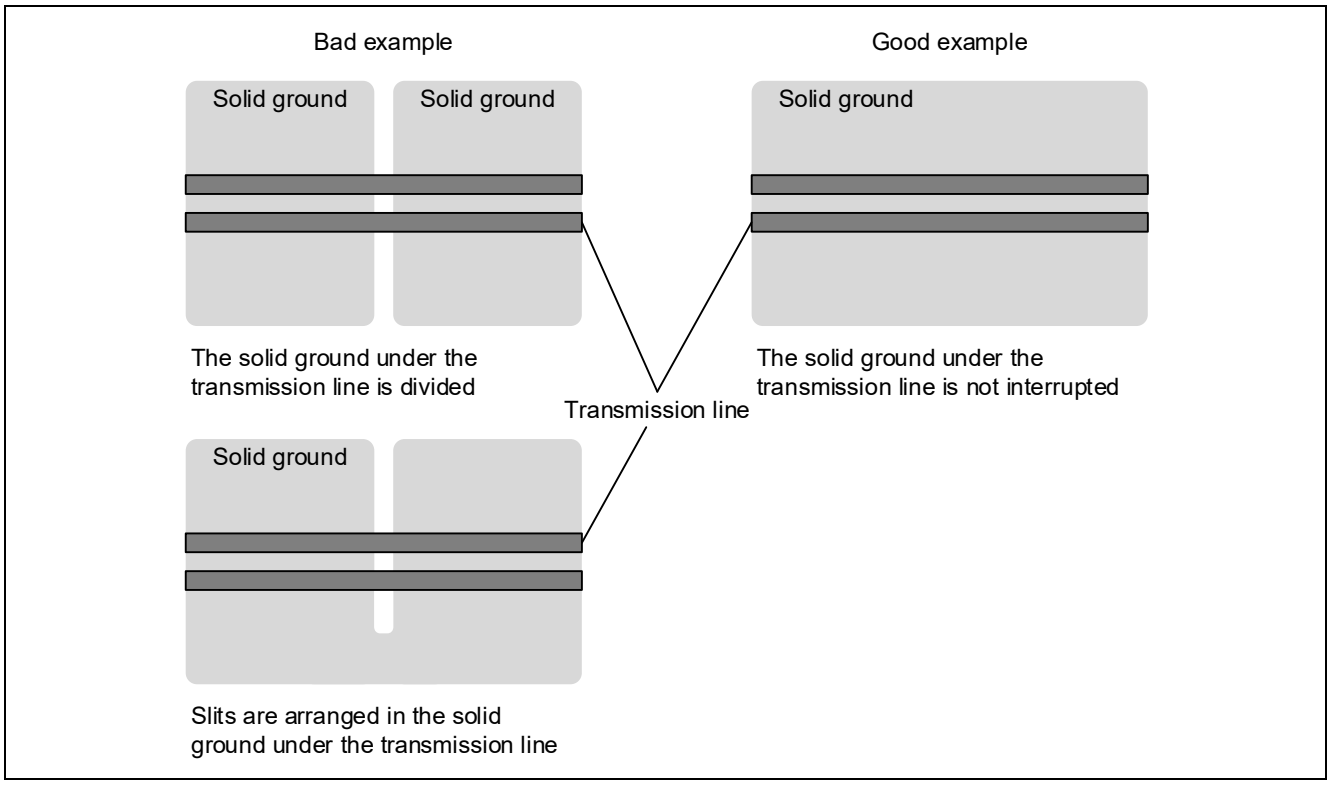

Figure 2.3 Example of solid ground on the lower layer of the transmission line

Table2.1 Recommended spacing values between transmission lines and adjacent traces

Item	Value
Spacing between differential pair and ground guard	S or more
Spacing between adjacent differential pairs	3S or more *1
Spacing between differential pairs and other adjacent signal lines	3S or more *2

Note: The distance between the positive signal line and the negative signal line is S.
*1. Value when there is no ground pattern between differential pairs.
*2. Value when there is no ground pattern between the differential pair and other signal lines.

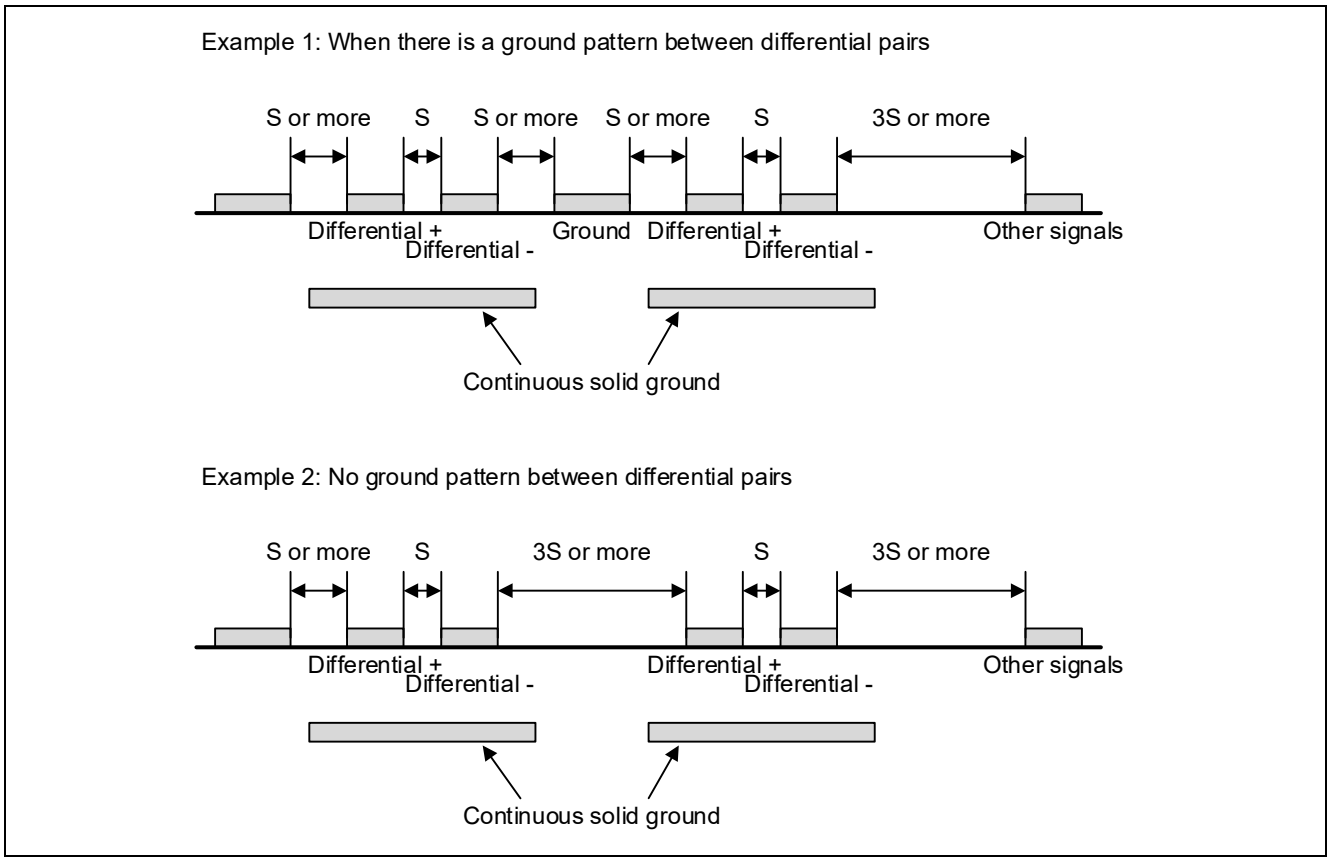

Figure 2.4 Examples of spacing between transmission lines and adjacent patterns

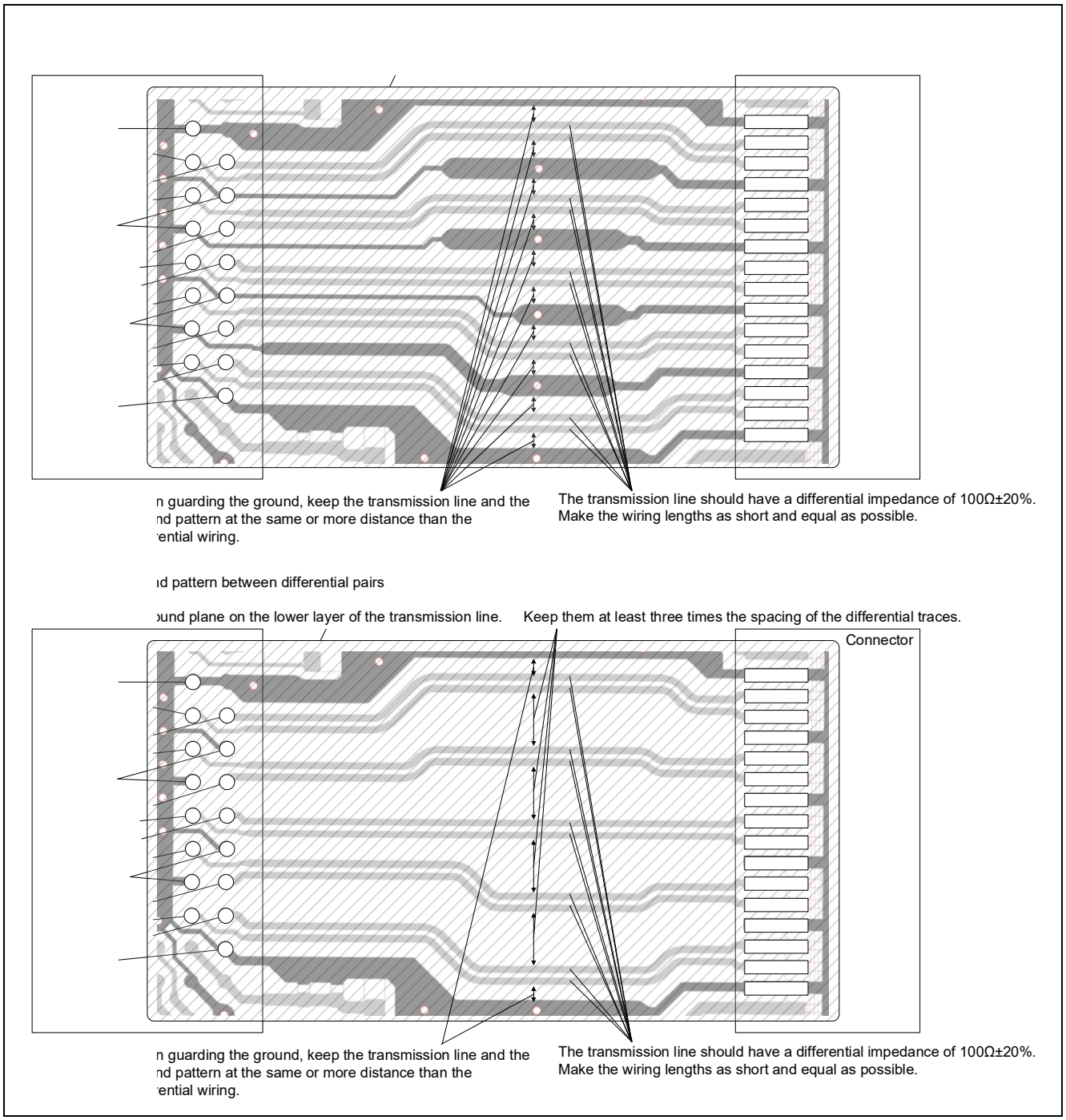

Figure 2.5 Transmission line pattern design example

3. Power/ground patter

The points to note when designing power supply and ground patterns are explained below.

Place the bypass capacitor close to the power supply pin. Also pay attention to the wiring resistance and wiring inductance of the power line. **Figure 3.1** shows the connection diagram and pattern example of the power supply pin, and **Table 3.1** shows the resistance, inductance, and capacitance of the bypass capacitor of the power supply line.
Figure 3.1 shows an example of power and ground connections.

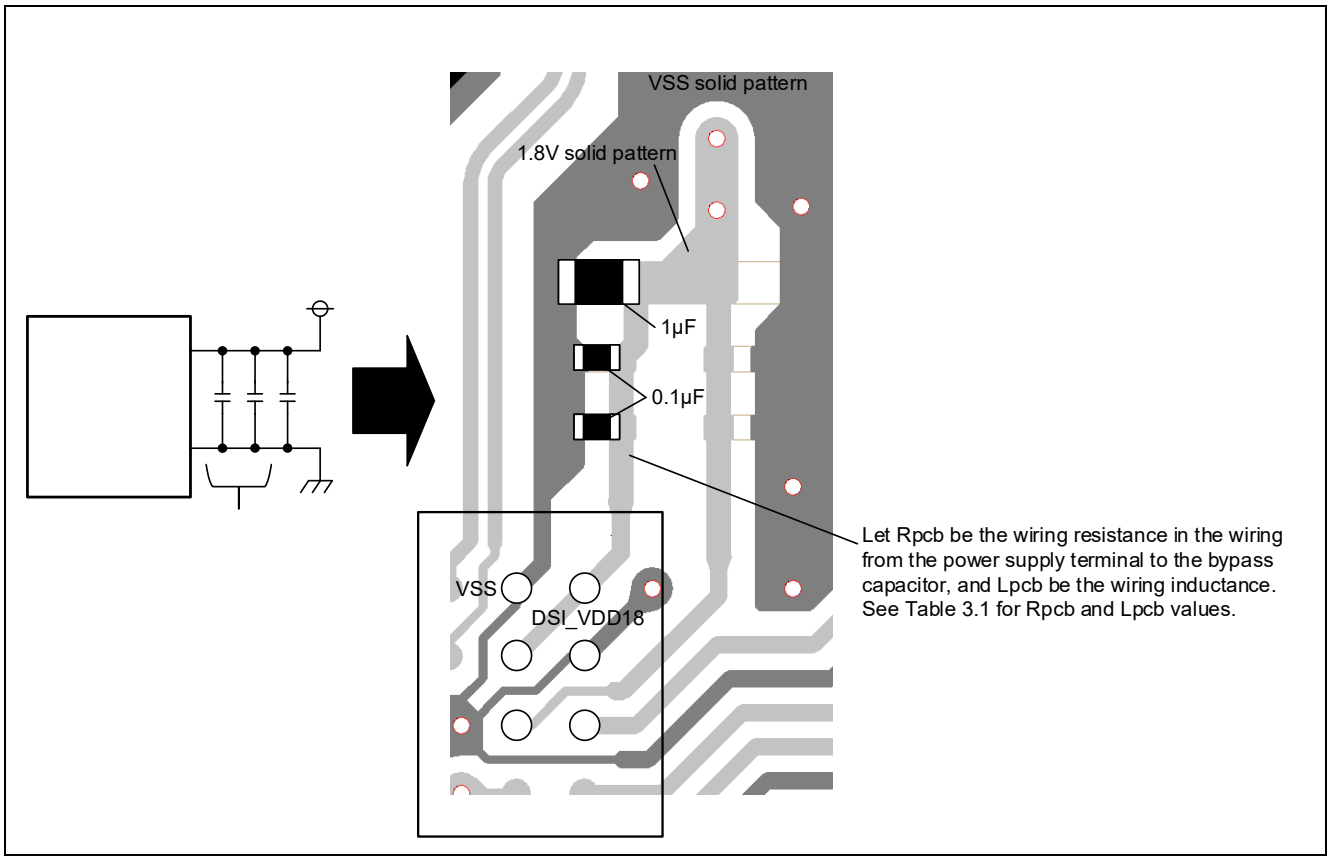

Figure 3.1 Power supply terminal connection diagram and pattern example

Table3.1 Power supply line resistance, inductance, bypass capacitor capacity

item	MIPI
Rpcb	30 mΩ or less
Lpcb*1	4.6 nH or less
Bypass capacitor	1.2uF (1uF + 0.1uF + 0.1uF)

Notes: *1. Set the value as small as possible.

Does not include bypass capacitor inductance.

The wiring inductance component varies depending on the board material and pattern width. For details, please consult the board manufacturer.

4. Checklist

Table4.1 Checklist 1 (schematic)

item number	Check items (circuit diagram)	☑	reference
1	When using MIPI, is an external terminating resistor attached?		Figure 1.1
2	Is the connection with the connector correct?		—
2-1	Are the polarities of the differential pairs reversed?		—
2-2	Are the channels/lanes correct?		—
3	Is the terminal processing correct?		—
3-1	Is the voltage of each power terminal correct? (Are there any unconnected power terminals?) DSI_VDD18 : 1.8V		Table 2.2
3-2	Is there a bypass capacitor of 0.1μF in each power supply pin?		Table 2.1
3-3	Is there a 1μF bypass capacitor before branching to the power supply terminal?		Table 2.1

Table4.2 Checklist 2 (pattern diagram)

item number	Check items (pattern diagram)	☑	reference
1	Is the transmission line correct?		—
1-1	Is the differential impedance 100Ω±20%?		2
1-2	Is it a pair wiring?		—
1-3	Are the positive and negative signal lines of the differential pair equal in length?		2
1-4	Are each data differential pair and clock differential pair the same length?		
1-5	Is the wiring as short as possible?		
1-6	Is the wire bent at 135° or in an arc?		
1-7	Are you routing without using vias?		
1-8	Do you have the same number of vias in each differential pair?		
1-9	Do vias form stubs?		Figure 2.1
1-10	Are ground vias placed symmetrically on both sides of the via?		Figure 2.2
1-11	Is the solid ground on the lower layer of the transmission line not interrupted?		Figure 2.3
1-12	Is there enough space between adjacent patterns?		Table 2.1 Figure 2.4 Figure 2.5
2	Is the power line correct?		—
2-1	Are the bypass capacitors located near the power supply pins?		3
2-2	Is the wiring resistance from the power supply terminal to the bypass capacitor 30mΩ or less?		Table 2.1
2-3	Is the wiring inductance from the power supply terminal (DSI_VDD18) to the bypass capacitor 4.6nH or less?		Table 2.1

5. Guidelines for USB 2.0

5.1 Guidelines for signal lines topology

This application note uses the USB2.0 host/function module pin names and the names and symbols listed in **Table 5.2**. **Table 5.1** shows the pin outline of the USB2.0 host/function module, and **Table 5.2** shows the classification of power supply and ground.

Table5.1 USB2.0 host/function module pin overview

Pin name	Input/Output	function
USB0_DP	Input/Output	D+ data of USB2.0 host/function module.
USB0_DM	Input/Output	D- data of USB2.0 host/function module.
USB0_VBUSIN	Input	USB cable connection monitor terminal. Step down the VBUS of the USB bus to 3.3V and connect. VBUS connection/disconnection can be detected.
USB0_VBUSEN	Output	Enable output for the VBUS power supply.
USB0_OVRCUR	Input	This is an overcurrent pin.
USB_RREF	Input	Connect to USB_VSS through a 1.8kΩ ±1% resistor.
USB_AVDD18	Power	Analog terminal power supply.
USB_VDD18	Power	Digital terminal power supply.
USB_VDD33	Power	Digital terminal power supply.
USB_VSS	Power	Ground for terminals.

Table5.2 Powr supply

Classification	Pin name	Voltage range	Symbol
Analog power	USB_AVDD18	1.62V～1.98V	
Digital power	USB_VDD18	1.65V～1.95V	
	USB_VDD33	3.0V～3.6V	
Digital ground	VSS	0V	
USB ground	USB_VSS	0V	

6. USB transmission line

USB transmission line refers to the wiring pattern that connects the USB connector and the USB transceiver.
USB2.0 has High-Speed, Full-Speed, and Low-Speed communication modes. Among these, High-Speed is a communication speed of 480 Mbps, so the USB transmission line must be designed as a high-frequency circuit. USB transmission lines require impedance control.
The points to note when designing the pattern wiring of the USB transmission line are described below.

- The characteristic impedance required for USB High-Speed transmission lines is a differential impedance of 90Ω±10%.
- For impedance control, the pattern width and pattern spacing vary depending on the substrate thickness, material, and layer configuration. For details, please consult the board manufacturer.
- Since the RZ/A3M USB module has built-in D+ and D- termination resistors (at High-speed operation) and output resistors (at Full-speed operation), no external resistors are required for the USB transmission line. Do not place
- The wiring pattern length of the USB transmission line from the RZ/A3M to the USB connector must be designed so as not to exceed the maximum delay time specified by the USB standard. Considering the waveform quality of High-Speed, shorter wiring is recommended. Table 2.1 shows the pattern design values for USB transmission lines on printed wiring boards made of common materials, considering the maximum delay time.

Table6.1 Wiring pattern design value of USB transmission line considering maximum delay time

	Maximum delay time (USB standard)	Wiring length*1	Difference in wiring length of D+ and D-
Host controller	3ns	300mm or less	2mm or less
Function controller	1ns	100mm or less	2mm or less

Notes: *1. This is an example when the wiring delay is 100ps/cm.

- The layer below the USB transmission lines should be a solid ground. Secure the solid ground 1mm or more outside the USB transmission line. The power supply for the solid ground is the USB ground.
- Do not place other signal lines near the USB transmission line. In particular, keep signals that change rapidly, such as clocks and data buses, away from the USB transmission line. Also, do not cross the USB transmission line with other signals.
- On the same layer (surface layer) as the USB transmission line, it is recommended to guard-ring the transmission line with the USB ground at a distance of 3 times or more the wiring interval of D+/D-.
- Wire the USB transmission lines on the same layer without vias. Also, do not branch the USB transmission line. (Except when using the Type-C receptacle.)
- When using a Type-C receptacle, short the A side D+ to the B side D+, and the A side D- to the B side D-. At this time, it is recommended that the wiring length to be short-circuited is 3.5 mm or less. If the length exceeds 3.5mm, please design the wiring as short as possible, evaluate it thoroughly by yourself, and judge whether the pattern is applicable.

- Make sure that the spacing of all USB transmission lines is constant.
- Keep USB transmission lines away from oscillators, power circuits, and other I/O connectors.
- Wire the USB transmission line as straight as possible. When bending the USB transmission line in terms of layout, bend gently by 135° or using an arc. Do not bend the USB transmission line at a sharp angle (right angle).

Figure 6.1 shows an example of USB transmission line pattern design for host controller, **Figure 6.2** shows an example of USB transmission line pattern design for function controller, and **Figure 6.3** shows an example of USB transmission line and ground guard ring spacing. **Figure 6.4** shows a connection example when using a Type-C receptacle.

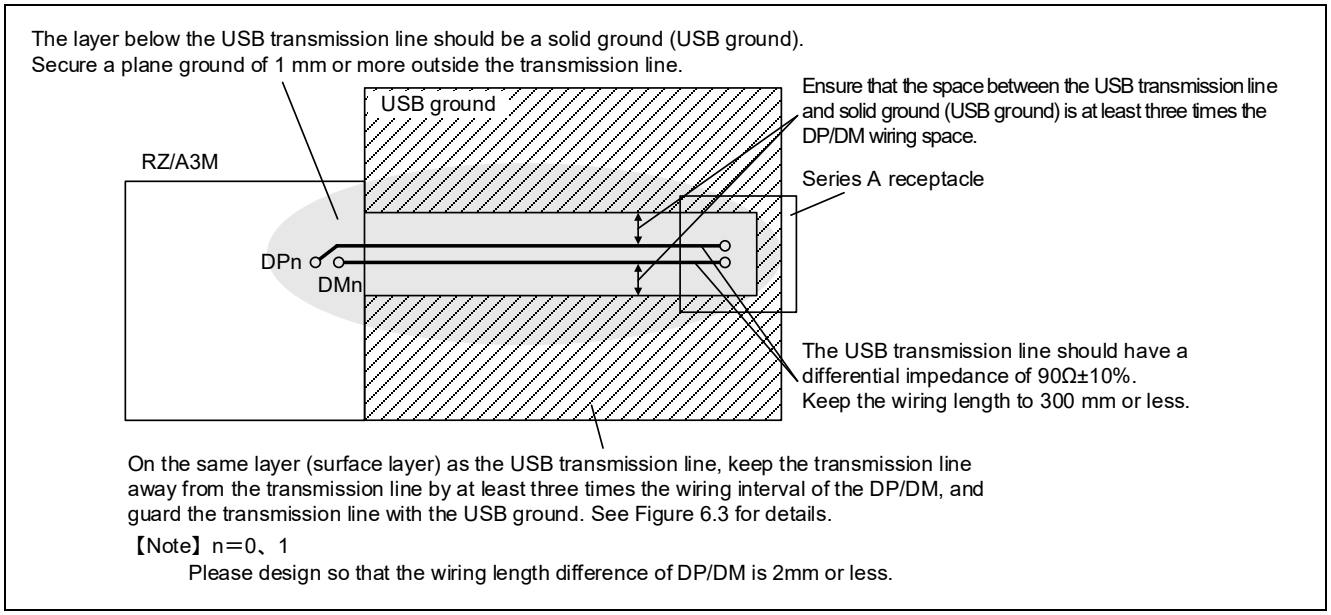

Figure 6.1 USB transmission line pattern design example for host controller

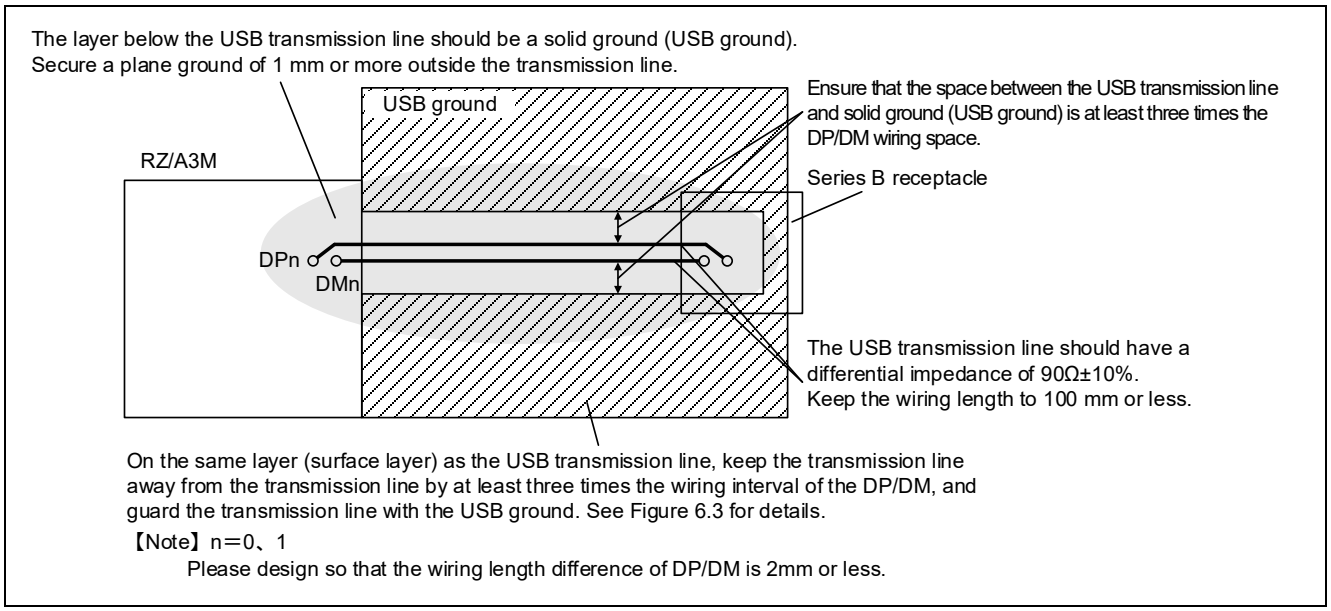

Figure 6.2 USB transmission line pattern design example for function controller

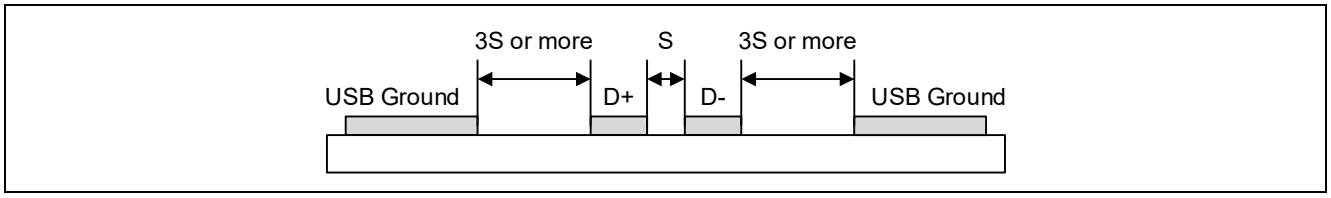

Figure 6.3 Example of USB transmission line and ground guard ring spacing

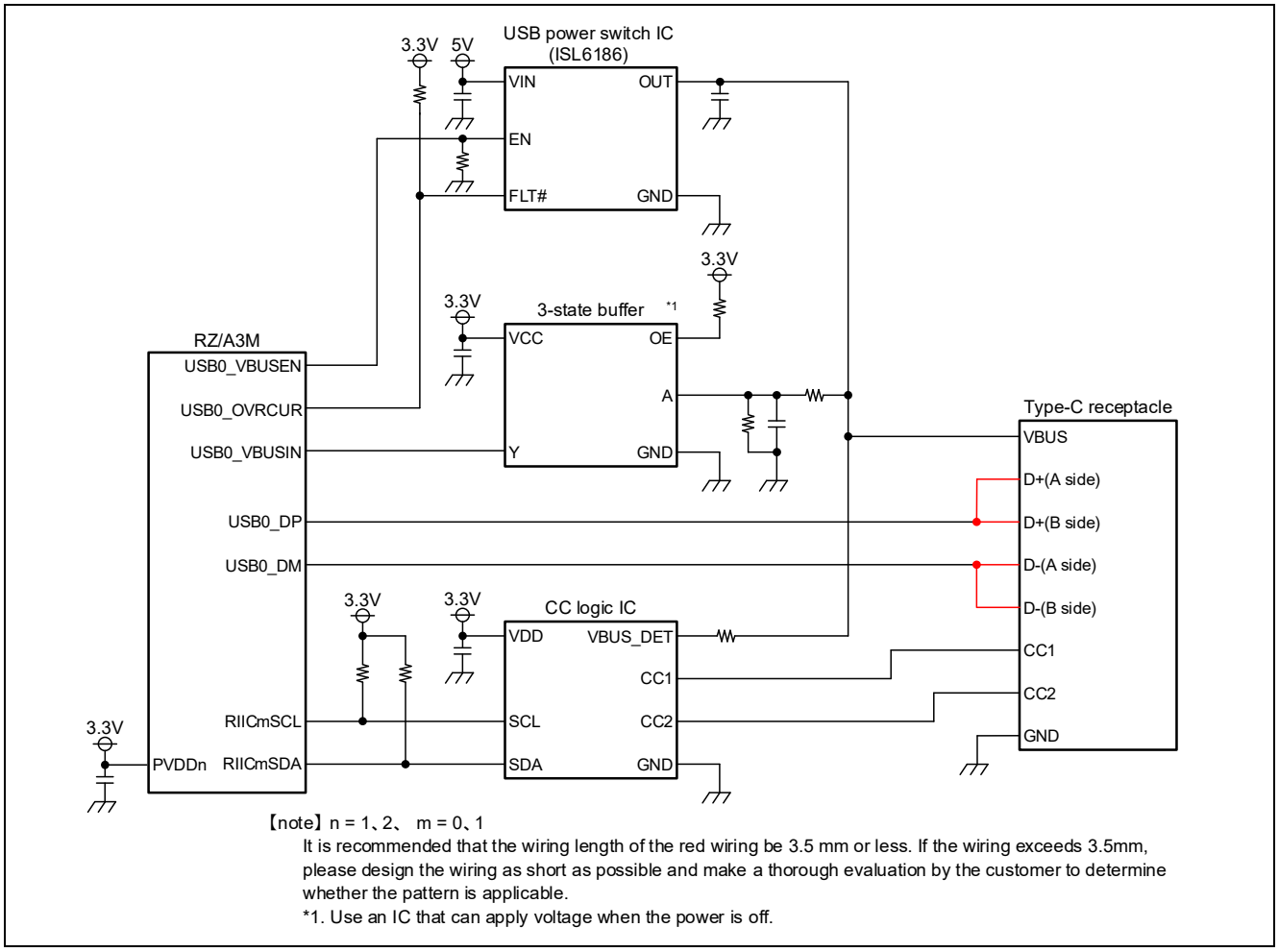

Figure 6.4 Connection example with Type-C receptacle

7. Power/ground pattern

The points to note when designing power supply and ground patterns are explained below

- Separate the analog 1.8V power supply (USB_VDD18, USB_AVDD18) from the digital power supply through an inductor or ferrite. In that case, please separate near RZ/A3M. The recommended inductor value is 3μH.
- Design the pattern so that the power supply and ground are on a layer with as wide a surface as possible.
- As for the capacitance value of the bypass capacitor, it is recommended to place a capacitance of 0.1μF for each pin for the 1.8V power supply (USB_VDD18, USB_AVDD18), and a capacitance of 47μF and 0.47uF for the digital 3.3V power supply (USB_VDD33) near the power supply pin. To do. Also place a 47μF capacitor between the digital 1.8V power supply and the USB ground.
- A ceramic capacitor with good high-frequency characteristics is recommended for the power supply capacitor.
- Electrolytic capacitors affect the jitter of the EYE pattern, so use them after thorough design and testing.

Figure 7.1 shows an example of power and ground connections.

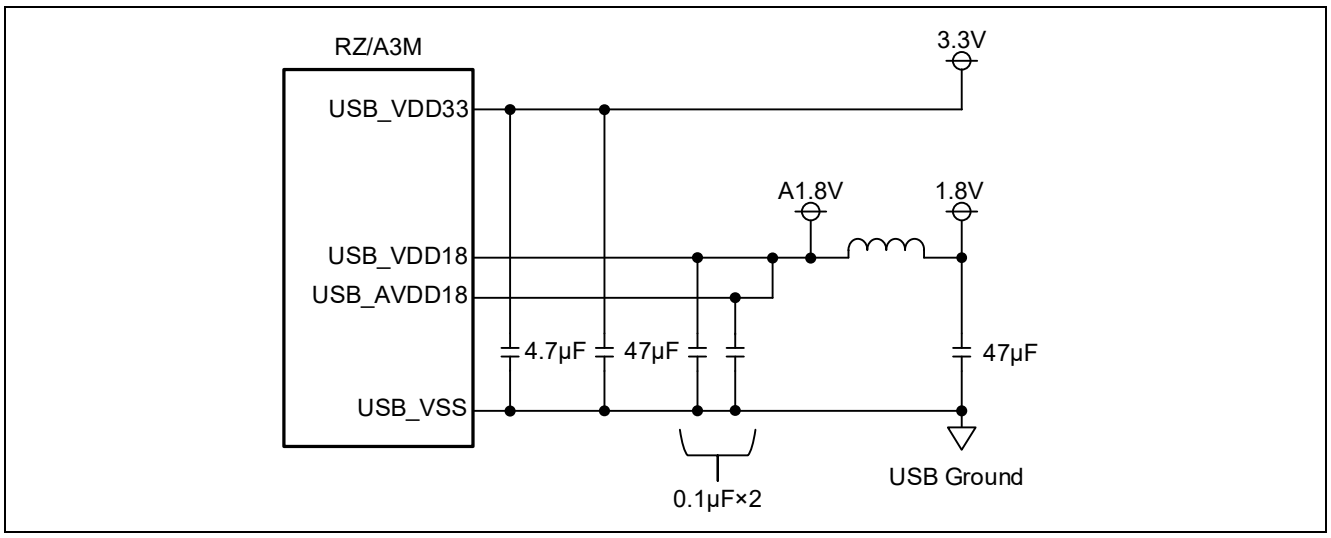

Figure 7.1 Example of power supply/ground connection

8. VBUS power circuit

The points to note when designing the VBUS power supply circuit are described below.

- When using the RZ/A3M as a host controller, please design so that the added capacitance of the VBUS line is 120μF or more.
- When using the RZ/A3M as a function controller, please design so that the additional capacitance of the VBUS line is 1.0μF to 10μF.
- When using the RZ/A3M as a function controller, if the USB host module is connected while the RZ/A3M is powered off, a voltage exceeding the absolute maximum ratings[*1] will be applied to the RZ/A3M's VBUSIN input pin. , the LSI may be permanently destroyed. To avoid this, protect RZ/A3M by referring to the protection circuit shown in **Figure 8.2**.
- Provide a filter circuit for the VBUS line, as overshoot may occur due to impedance mismatch when connecting the USB cable. As a filter circuit, attach a capacitor with a capacity of 1.0 μF to 10 μF and a resistor of 100 Ω to 1 kΩ. Also, determine the final constant after confirming that overshoot does not occur on the board. At that time, do not attach a resistor larger than 1kΩ.
- When used as a host controller, VBUS power must be supplied to function devices. For controlling the VBUS power supply, it is recommended to use a power switch IC with an overcurrent limit function for the USB power bus, such as the Renesas Electronics ISL6186 (hereafter referred to as the USB power switch IC).

  Consider the current limit value of the VBUS power line based on the power supply of the applicable system and the current value required by the communicating USB function device. Also, design the VBUS power supply control circuit by referring to the circuit example given in the data sheet of the USB power switch IC used.

Figure 8.1 shows an example of a VBUS power supply circuit when used as a host controller, and **Figure 8.2** shows an example of a VBUS power supply circuit when used as a function controller.

Notes: *1. The RZ/A3M's VBUSIN input pin is multiplexed to a general-purpose I/O port, and the absolute maximum rating of that pin is -0.3V to PVcc+0.3V.

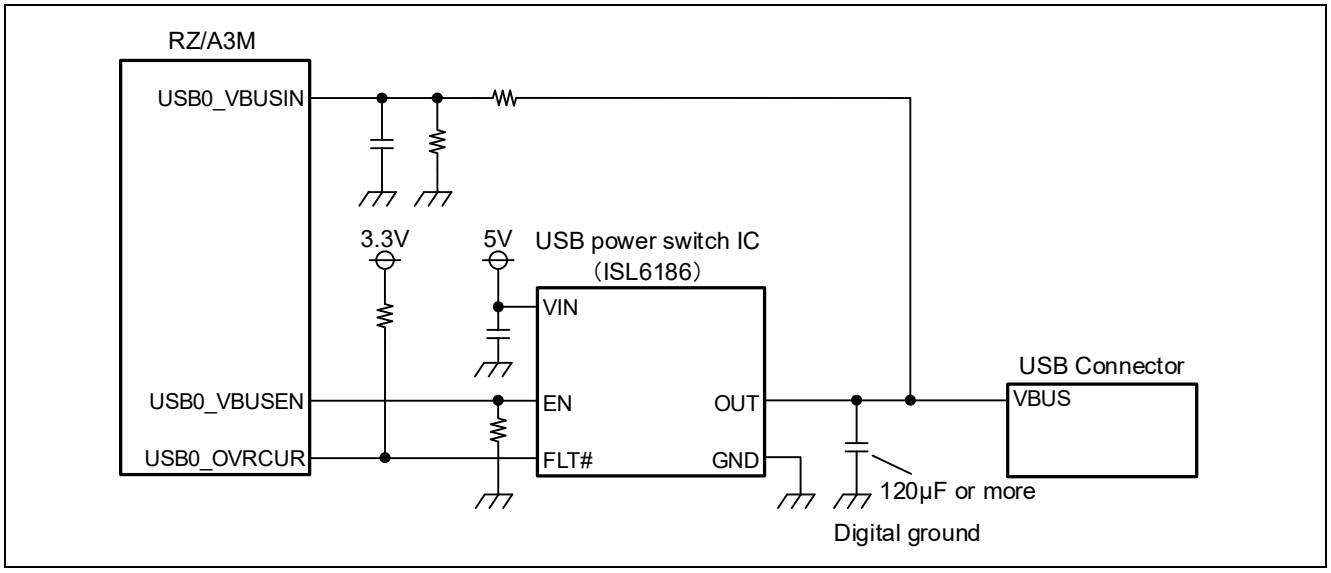

Figure 8.1 Host controller VBUS circuit example

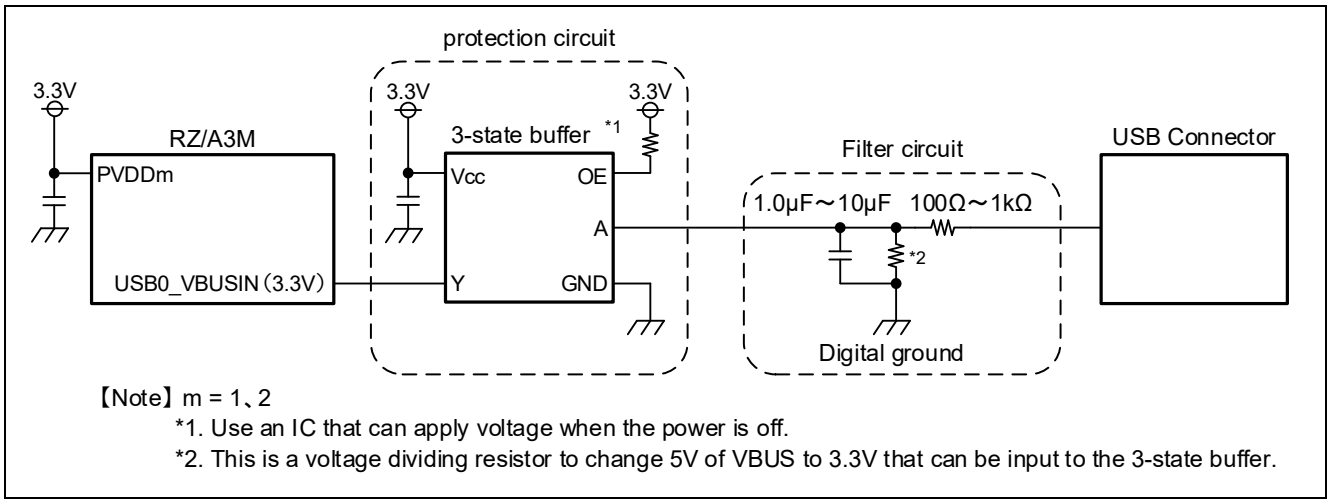

Figure 8.2 Function controller VBUS circuit example

9. RREF pin

The points to note when designing the RREF pin peripheral circuit are described below.

- Connect a 1.8kΩ±1% resistor (hereafter referred to as reference resistor) between the RREF pin and the USB ground.
- Place the reference resistor as close to RZ/A3M as possible, and design the RREF wiring so that it is 0.5Ω or less.
- To avoid crosstalk, avoid crossing or paralleling rapidly changing signals (D+, D-, clocks, address data control signals, etc.) near the reference resistor and its traces. It is recommended to guard ring the reference resistor and its pattern with the USB ground or analog power supply.
- The layer below the reference resistor and wiring should be the USB ground plane.

Figure 9.1 shows a connection diagram of the RREF pin, and **Figure 9.2** shows an example of pattern design around the RREF pin.

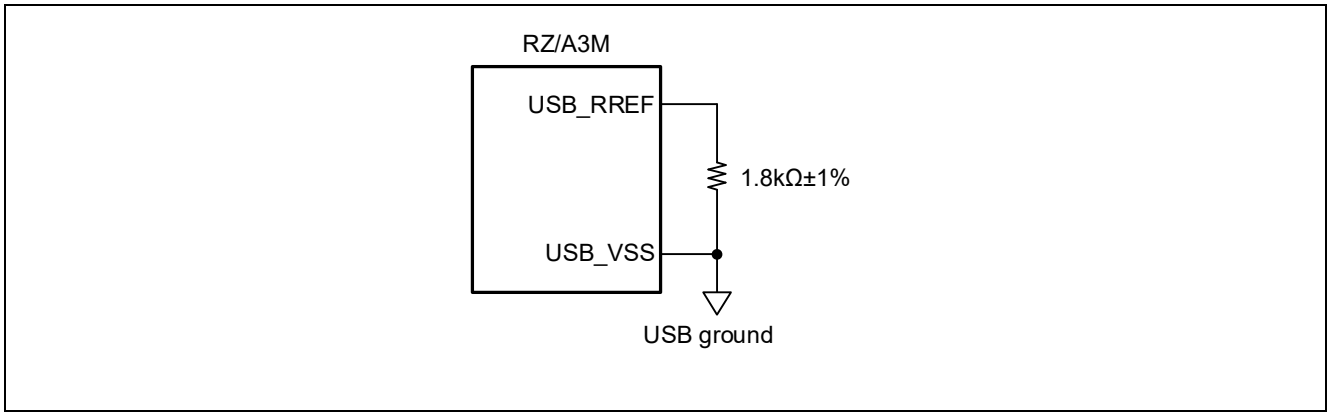

Figure 9.1 RREF pin connection diagram

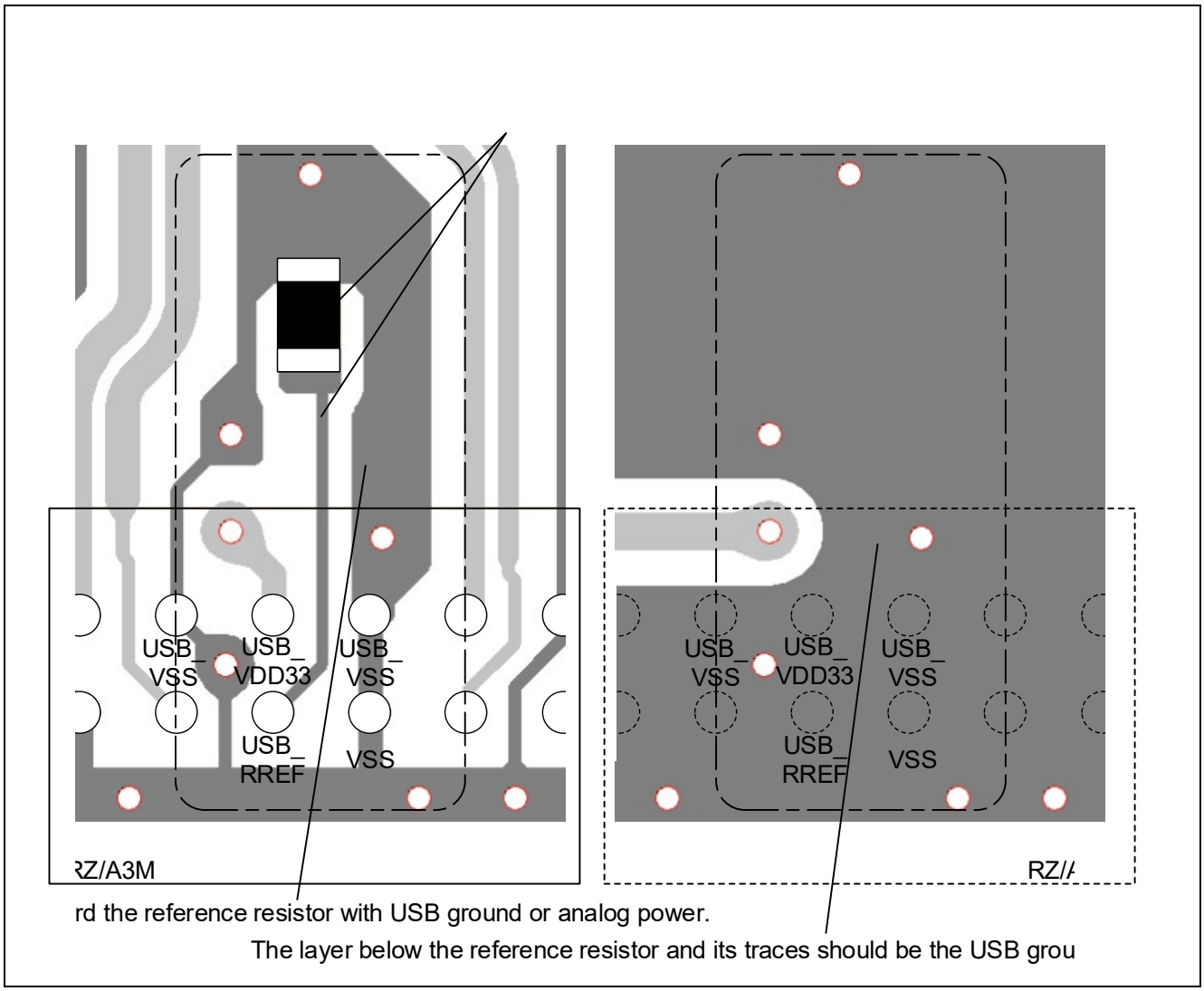

Figure 9.2 Example of pattern design around RREF pin

10. EMI/ESD countermeasures

The precautions for EMI and ESD countermeasures are explained below.

- When mounting EMI and ESD countermeasure parts such as coils and diodes on the USB transmission line, place them near the USB transmission line and keep the wiring as short as possible.
- Be sure to use USB2.0 High-Speed compatible parts for EMI and ESD countermeasures. Note that mounting EMI and ESD countermeasure parts may cause impedance mismatching in the USB transmission line and may distort the waveform.

Figure 10.1 shows a connection example when using EMI and ESD countermeasure parts.

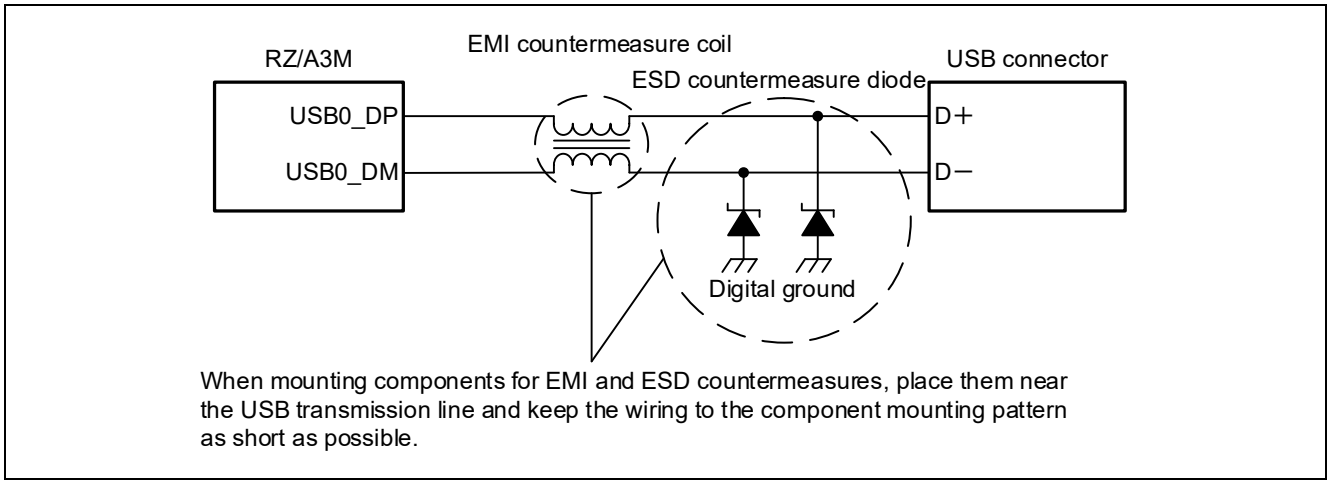

Figure 10.1 Connection example when using parts for EMI and ESD countermeasures

11. Checklist

Table11.1 Checklist 1 (schematic)

item number	Check items (circuit diagram)	☑	reference
1	Is there an external resistor placed on the transmission line?		6
2	Is the terminal processing correct?		—
2-1	Is the RREF pin connected to the USB ground via a 1.8kΩ±1% resistor?		Figure 9.1
2-2	Is there a 47μF capacitor between the digital power supply and the USB ground?		Figure 7.1
2-3	Is there a 10μF capacitor between the analog power supply and USB ground?		
2-4	Is there a bypass capacitor of 0.01μF in each USB power supply pin?		
2-5	Is the voltage of the power terminal correct? (Are there any unconnected power terminals?)		—
2-5-1	USBAPVcc1, USBAPVcc0: 3.3V analog power supply		Table 5.2
2-5-2	USBDPVcc1, USBDPVcc0: 3.3V Digital Power		
3	Are the analog and digital power supplies separated by an inductor or ferrite?		Figure 7.1
4	Is the VBUS circuit correct?		—
4-1	Is there a capacitor of 120μF or more in the VBUS line when using as a host?		Figure 6.1
4-2	Is there a capacitor of 1.0μF to 10μF in the VBUS line during function?		Figure 6.2
4-3	Is a protection circuit provided for the VBUSIN input pin during function?		
4-4	Is a filter circuit provided for the VBUS line during function?		—
4-4-1	Capacitance: 1.0μF to 10μF		Figure 6.2
4-4-2	Resistance: 100Ω to 1kΩ		

Table11.2 Checklist 2 (pattern diagram)

item number	Check items (pattern diagram)	☑	reference
1	Is the transmission line correct?		—
1-1	Is the differential impedance 90Ω±10%?		6
1-2	Is the wiring length 300mm or less at the time of host?		Table 6.1
1-3	Is the wiring length 100 mm or less at the time of function?		
1-4	Is the wiring length difference of D+/D- less than 2mm?		
1-5	Are you wiring on the same layer (except for Type-C)?		6
1-6	Is the wiring branched (excluding Type-C)?		
1-7	When using Type-C, is the wiring that shorts the A side and B side of D+ and D- 3.5 mm or less (recommended value)?		6 Figure 6.4
1-8	Are the wires laid out at regular intervals?		6
1-9	Are there any unnecessary bends in the wiring?		
1-10	Is the wire bent at 135° or in an arc?		
2	Is the clearance correct?		—
2-1	Is the USB solid ground on the lower layer of the transmission line 1 mm or more outside the transmission line?		6 Figure 6.1 Figure 6.2
2-2	Is the space between the USB ground and the transmission line at least 3 times the space between the D+/D- wiring?		6 Figure 6.1 Figure 6.2 Figure 6.3
3	Are the bypass capacitors located near the power supply pins?		7
4	Is the RREF pin peripheral circuit correct?		—
4-1	Are they connected without vias?		9 Figure 9.2
4-2	Is the reference resistor placed near RZ/A3M?		
4-3	Is the wiring resistance 0.5Ω or less?		
4-4	Is there a guard ring on the USB ground or analog power supply?		
4-5	Is the bottom layer a USB ground plane?		
5	Are EMI and ESD countermeasures correct?		—
5-1	Is the countermeasure component placed near the transmission line?		10 Figure 10.1
5-2	Is the wiring to the countermeasure component as short as possible?		

12. Reference Documents

- Hardware manual

  RZ/A3M Group User's Manual: Hardware (Rxxxxxxxxxx)
  (Get the latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2023.07.10	—	First edition issued

RZ/A3M Group PCB Design Guidelines for MIPI-DSI and USB2.0

Publication Date: Rev.1.00 July 10 , 2023

Published by: Renesas Electronics Corporation