

RX72M Group

EtherCAT CiA402 ETG.5003 Sample Program

Firmware Information Technology

Introduction

This application note describes a sample program for sub-device equipment applied to IO devices, motor control devices, and semiconductor manufacturing equipment in EtherCAT[®] communication, which is one of the industrial Ethernet communication protocols.

This sample program supports the following specifications.

- CANopen over EtherCAT (CoE)
- File access over EtherCAT (FoE)
- Distributed Clocks (DC)
- CiA402 Drive Profile
- Common Device Profile(ETG.5003.1)
- Firmware update functionality(ETG.5003.2)

Target Device

- RX72M Group

When using this product with your product, please thoroughly evaluate it according to your environment.

In addition, when applying this application note to other microcomputers, modify it according to the specifications of the other microcomputers and fully evaluate it.

About the old documents

This application note is the document which integrated the following old documents.

- RX72M Group Communication Board EtherCAT Startup Manual
(Document r01an4672ej0105-rx72m-ecat.pdf)
- RX72M Group CPU Card EtherCAT Startup Manual
(Document r01an6749ej0101-rx72m-cpucard-ecat.pdf)
- RX72M Group RSK Board EtherCAT Startup Manual
(Document r01an4689ej0105-rx72m-ecat-rsk.pdf)
- RX72M Group EtherCAT CiA402 Sample Program Firmware Information Technology
(Document r01an5393ej0110-rx72m-ecat-cia402.pdf)
- RX72M Group EtherCAT ETG.5003 Sample Program Firmware Information Technology
(Document r01an5538ej0120-rx72m-ecat-etg5003.pdf)

The old documents will no longer be updated, this application note will be updated.

Table of contents

Content

1. Overview	4
1.1 About this application note	4
1.2 Operating environment.....	4
1.3 FIT module configuration.....	4
1.4 About the Project.....	5
2. Obtaining the development environment.....	5
2.1 How to obtain e ² studio.....	5
2.2 How to obtain the compiler package	5
3. Building the project	6
3.1 Importing the EtherCAT Slave Stack Code to the sample program.....	6
3.2 Importing the project.....	8
3.3 How to install EtherCAT FIT module to e ² studio.....	9
4. Building and debugging the project.....	10
4.1 Generating code	10
4.2 Building the project.....	10
4.2.1 Building linear mode	10
4.2.2 Building dual mode.....	10
4.3 Preparation for debug.....	11
4.4 Debugging the project	12
4.4.1 Debugging on linear mode	12
4.4.2 Debugging on dual mode	13
5. Connection with TwinCAT 3.....	15
5.1 Preparation of the ESI file	15
5.2 Starting TwinCAT 3	15
5.3 Adding ether driver	15
5.4 Scanning the network.....	16
5.5 Writing of SII EEPROM	17
5.6 Rescan of the device.....	18
6. Operation check by TwinCAT 3	19
6.1 I/O operation check	19
6.2 CiA402 Drive Profile operation check.....	21
6.2.1 CiA402 State Transition	21
6.2.2 csp mode	23
6.2.3 csv mode	24
6.3 Firmware update operation check.....	25
6.3.1 Firmware writing	25
6.3.2 Firmware readout	30

7.	Configuration of project.....	33
7.1	Configuration of FIT module.....	33
7.2	Pin settings.....	34
7.3	build configuration.....	35
7.3.1	Linear mode build configuration.....	35
7.3.2	Build configuration of Dual mode.....	41
7.4	Debug configuration.....	47
7.4.1	Debug configuration of Linear mode.....	47
7.4.2	Debug configuration of Dual mode.....	48
8.	Sample program overview.....	50
8.1	File configuration.....	50
8.2	Modifications of Slave Stack Code.....	52
8.3	CiA402 Drive Profile overview.....	53
8.3.1	Operation mode.....	53
8.3.2	State Transition.....	54
8.3.3	State transition function.....	54
8.4	Firmware update overview.....	56
8.4.1	About bank numbers.....	56
8.4.2	Linear mode and dual mode comparison.....	57
8.4.3	Overview of linear mode operation.....	58
8.4.4	Overview of dual mode operation.....	60
8.4.5	Bank info.....	62
8.4.6	Download file.....	63
8.4.7	SII EEPROM.....	66
8.4.8	Firmware update program details.....	67
8.4.9	FoE program details.....	73
8.5	Object dictionary.....	76
9.	Appendix A. Semiconductor Device Profile [ETG.5003].....	83
9.1	Common Device Profile [ETG.5003.1].....	83
9.2	Semi Test Record [ETG.7000.2-Annex5003-0001].....	84
9.2.1	Device Reset Command (Standard reset).....	84
9.2.2	Dynamic PDO.....	85
9.2.3	Store Parameters.....	89
10.	Appendix B. How to support code flash memory capacity of 2MB.....	91
11.	Appendix C. How to use the SSC tool configuration file.....	93
12.	Reference documents.....	94

1. Overview

1.1 About this application note

This application note describes the sample program that supports process data communication in the CANopen over EtherCAT (CoE) protocol, the CiA402 drive profile, and the firmware update function (ETG.5003.2) using the File Access over EtherCAT (FoE) protocol.

About details on the support contents of the ETG.5003 Semiconductor Device Profile, which is a profile applied to semiconductor manufacturing equipment, refer to 9. Appendix A. Semiconductor Device Profile [ETG.5003].

This sample program works in combination with a board support package (hereinafter called “BSP”) and the FIT module such as EtherCAT.

The SSC is not included in this sample program. Obtain the SSC tool from the EtherCAT Technology Group (ETG Association) and use the SSC tool.

1.2 Operating environment

Table 1-1 shows the operating environment confirmed by this sample program.

Table 1-1 Operating Environments

Supported MCUs	RX72M Group R5F572MNxDBD The capacity of code flash memory: 4Mbyte
Evaluation board	RX72M Evaluation Board from TESSERA Technology (TS-RX72M-COM) (Hereinafter called “COM board”)
	RX72M CPU Card with RDC-IC (RTK0EMXDE0C00000BJ) (Hereinafter called “CPU card”)
	Renesas Starter Kit+ for RX72M (RTK5572MNxCxxxxxBJ) (Hereinafter called “RSK board”)
Integrated development environment (IDE)	e ² studio 2024-01 from Renesas Electronics Corporation
Cross-tool	C/C++ Compiler Package for RX Family V3.06.00
Emulator	E2 Lite
SSC tool	Slave Stack Code (SSC) tool Version 5.13 form EtherCAT Technology Group (ETG)
Software PLC	TwinCAT [®] 3 from Beckhoff Automation (Download from the Beckhoff website)

1.3 FIT module configuration

Table 1-2 shows the list of the FIT modules used in this sample program.

Table 1-2 FIT Module configuration

Type	Module name	FIT module name	Rev.
Board Support Package	Board Support Package (BSP)	r_bsp	7.42
Device Driver	Compare Match Timer (CMT)	r_cmt_rx	5.60
Device Driver	Serial Communication Interface (SCI)	r_sci_rx	4.90
Middleware	Byte Type Queue buffer (BYTEQ)	r_byteq	2.10
Device Driver	EtherCAT	r_ecat_rx	1.31
Device Driver	Flash	r_flash_rx	5.10

1.4 About the Project

Table 1-3 shows the lists of the project included in this sample program.

In the following chapters, we will explain by using the linear mode project of the CPU card (ecat_linear_demo_cpurx72m) as an example.

If you want to use a different project, replace the project name as appropriate.

Table 1-3 the lists of the project

MCU	Evaluation board	Dual bank function	Project name
RX72M	COM board	Linear mode	ecat_linear_demo_comrx72m
		Dual mode	ecat_dual_demo_comrx72m
	CPU card	Linear mode	ecat_linear_demo_cpurx72m
		Dual mode	ecat_dual_demo_cpurx72m
	RSK board	Linear mode	ecat_linear_demo_rskrx72m
		Dual mode	ecat_dual_demo_rskrx72m

2. Obtaining the development environment

2.1 How to obtain e² studio

Access the following URL and download the e² studio.

<https://www.renesas.com/us/en/products/software-tools/tools/ide/e2studio.html#downloads>

This application note assumes that you will be using 2024-01 or a later version of the e² studio. If you are using a version earlier than 2024-01, some functions of the e² studio may not be available.

When downloading the e² studio, obtain the latest version on the website.

2.2 How to obtain the compiler package

Access the following URL and download the RX family C/C++ Compiler Package.

<https://www.renesas.com/us/en/software-tool/cc-compiler-package-rx-family>

This application note assumes that you will be using V3.06.00 or a later version. If you are using a version earlier than V3.06.00, some functions of the CC-RX may not be available.

When downloading the CC-RX, obtain the latest version on the website.

3. Building the project

3.1 Importing the EtherCAT Slave Stack Code to the sample program

This sample project does not include the EtherCAT Slave Stack Code.

However, the project requires the EtherCAT Slave Stack Code and to generate and use this you must obtain the EtherCAT Slave Stack Code (SSC) tool.

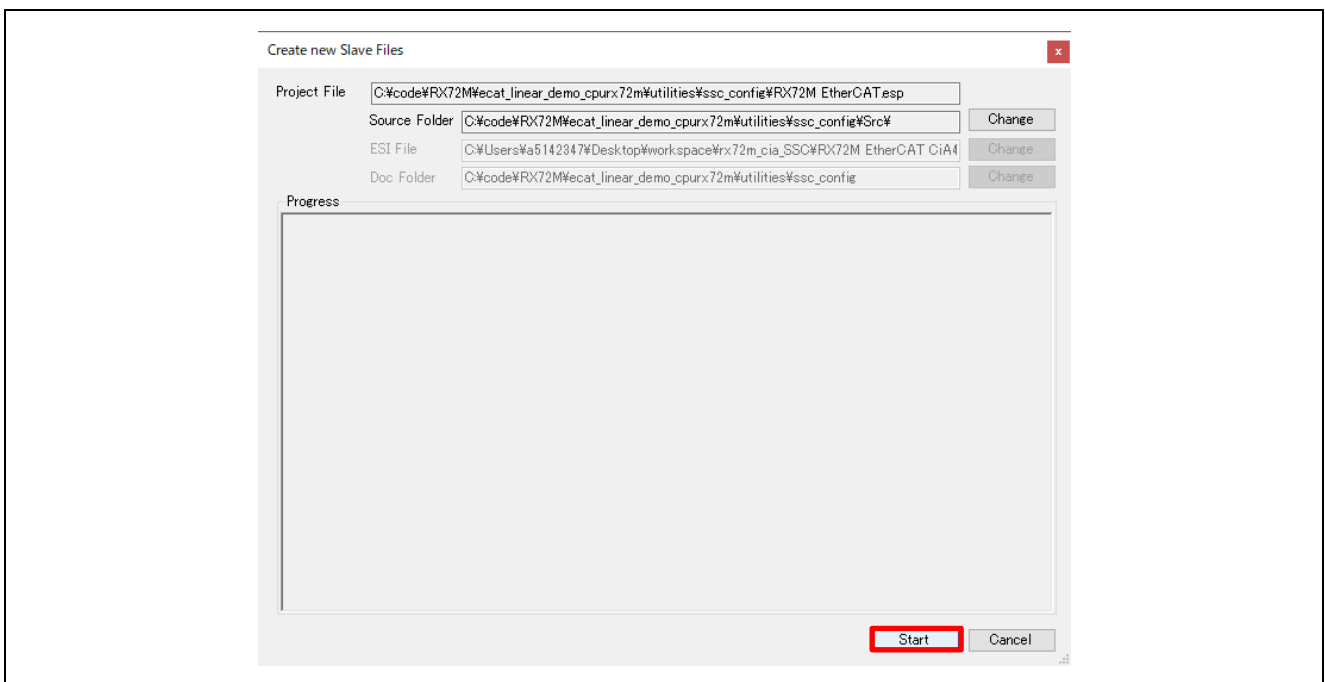
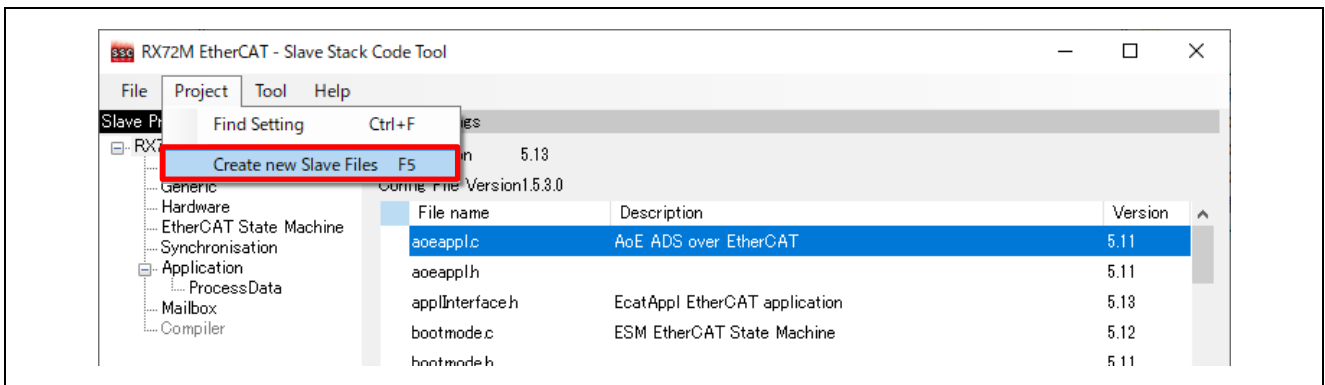
The EtherCAT Technology Group (ETG) provides the SSC package.

The sample program is provided in the from "ecat_linear_demo_cpurx72m.zip", extract it to any folder in advance.

- (1) Double-click on the SSC project file of the sample program to activate the SSC tool.

ecat_linear_demo_cpurx72m\utilities\ssc_config\RX72M EtherCAT.esp

- (2) Click on [Project] → [Create New Slave Files], and then click on [Current new Slave Files] → [Start].



(3) When the source code has been generated normally, "New files created successfully" will be displayed. Click on [OK].

(4) If you have not installed the patch file, GNU Patch Ver2.5.9 or later is required. If it has been installed, skip this step.

Download the patch file (Ver2.5.9) from the following Web page and store "patch.exe" in a folder that has a path executable from the command prompt.

<http://gnuwin32.sourceforge.net/packages/patch.htm>

(5) Double-click on the apply_patch.bat file.

The patch file contains the RX-specific modifications to the SSC source files.

ecat_linear_demo_cpurx72m\utilities\rx72m\patch\apply_patch.bat

After the patch has been applied, the modified source file will be stored in the following folder.

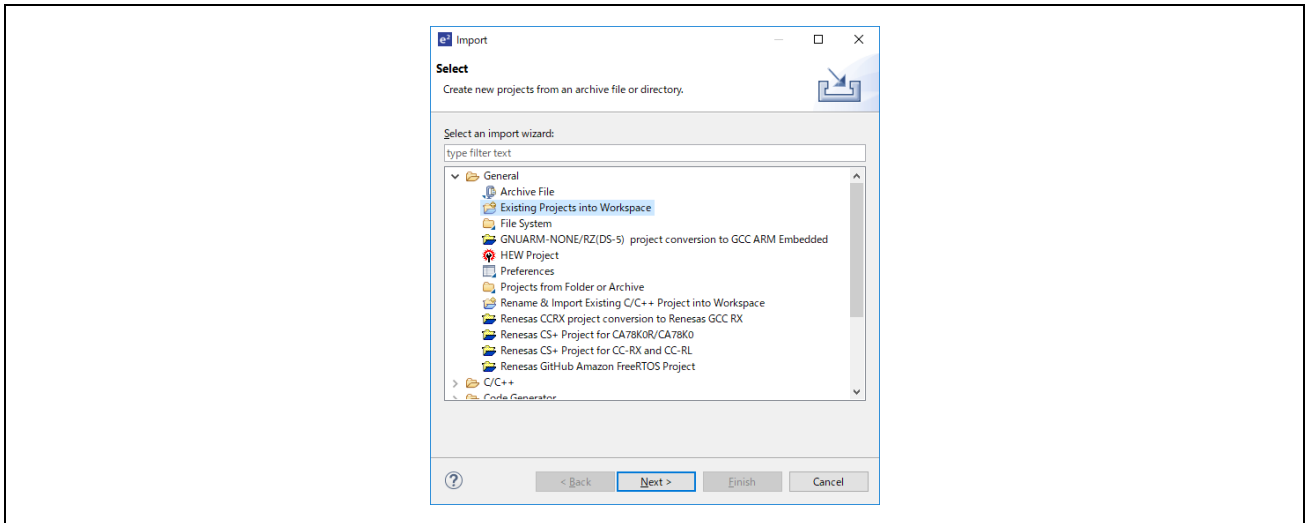
ecat_linear_demo_cpurx72m\project\src\application\ecat



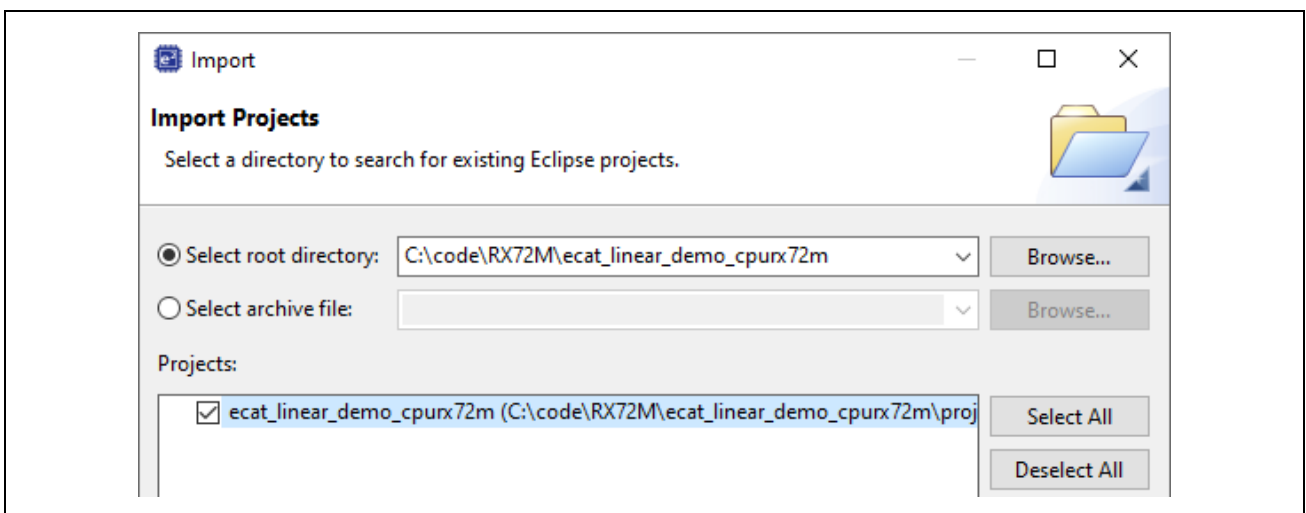
```
C:\WINDOWS\system32\cmd.exe
--- Move SSC Src folder ---
1 dir(s) moved.
--- Patching process start ---
patching file Src/bootmode.c
patching file Src/bootmode.h
patching file Src/cia402appl.c
patching file Src/cia402appl.h
patching file Src/coeappl.c
patching file Src/coeappl.h
patching file Src/ecatappl.c
patching file Src/ecatcoe.h
patching file Src/ecatslv.c
patching file Src/mailbox.h
patching file Src/objdef.c
patching file Src/sdoserv.h
--- Patching process end ---
--- Move patched Src folder ---
Press any key to continue . . . _
```

3.2 Importing the project

- (1) Click on [File] → [Import].
- (2) In the [Select an import wizard] dialog box, select [General] → [Existing Project to Workspace] and click on [Next].



- (3) Select the [Select root directory] checkbox in the [Import Project] dialog box and click on [Browse].
- (4) Select "ecat_linear_demo_cpurx72m" and click [Open].



- (5) Check [ecat_linear_demo_cpurx72m] in [Project] and click [Next] to import the linear mode project of the CPU card.

3.3 How to install EtherCAT FIT module to e² studio

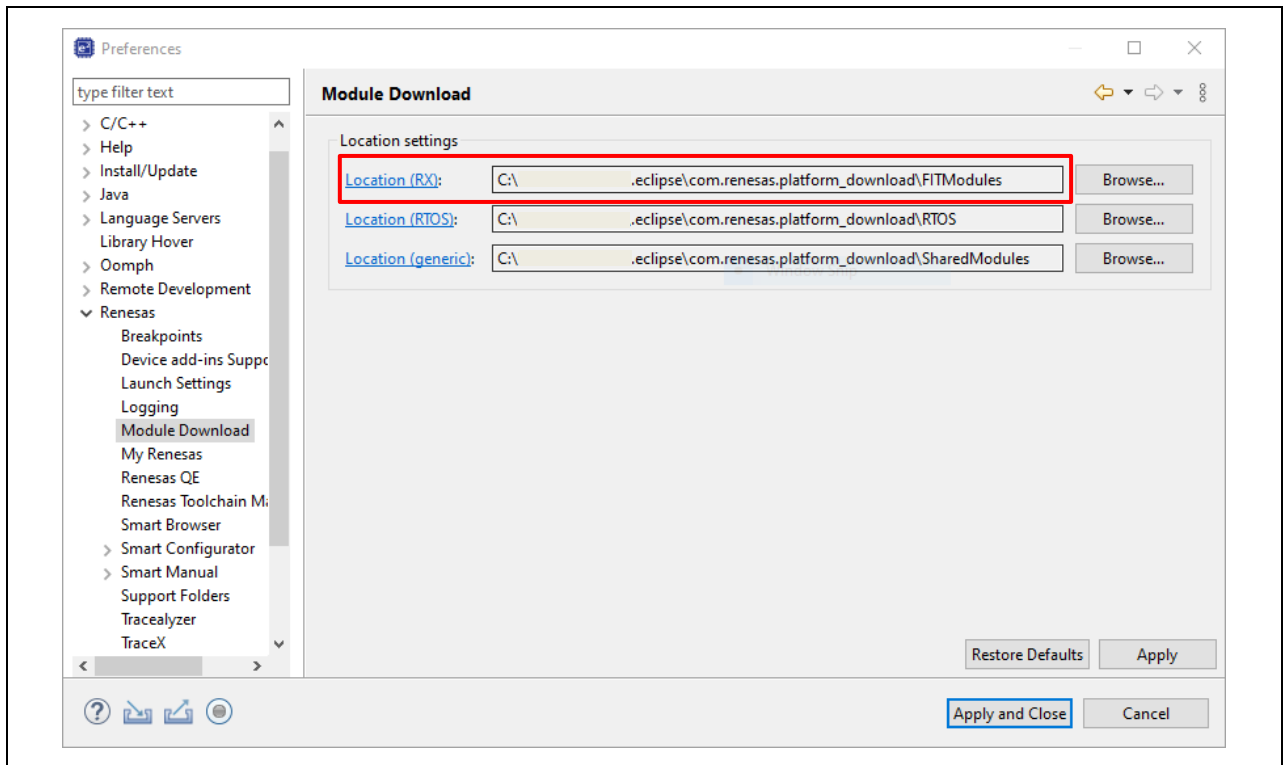
To be able to use the EtherCAT FIT module in the Smart Configurator, you need to add it to e² studio. Shows how to add it manually.

- Copy the EtherCAT FIT module to the folder where the FIT module is saved in e² studio.

In e² studio, check the location of the FIT module.

1. "Window" → "Preferences" → Open setting window.
2. Select "Renesas" → "Module Download".

The path shown as Location (RX): is the destination folder of the FIT module.



The EtherCAT FIT module is stored in the FITModules folder of the sample program.

- ※ Copy the file in the r01an7288xx0100-rx72m-ecat\FITModules folder to the folder where the FIT module is saved.

r_ecat_rx_vN.NN.xml

r_ecat_rx_vN.NN.zip

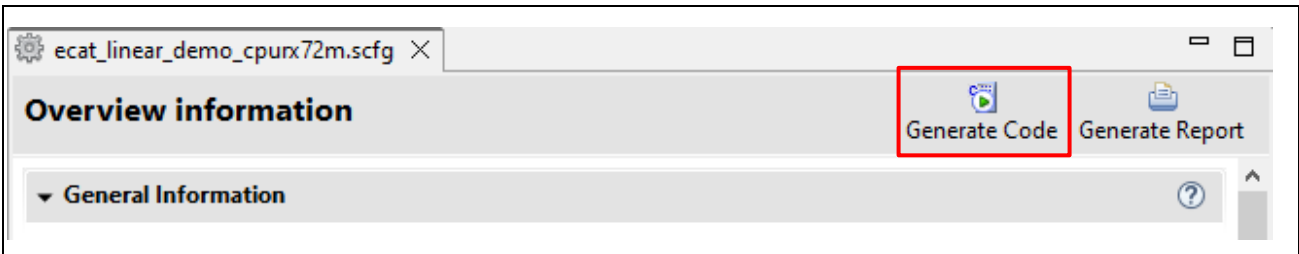
r_ecat_rx_vN.NN_extend.mdf

Note that N.NN is a numerical value that represents the version.

4. Building and debugging the project

4.1 Generating code

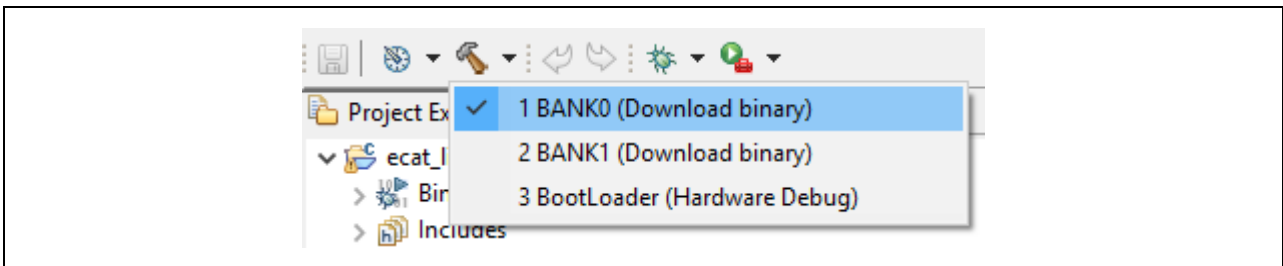
- (1) Open the smart configuration file “ecat_linear_demo_cpux72m.scfg” and press [Generate Code] to run the code generation.
- (2) The generated code is stored under the ecat_linear_demo_cpux72m\src\smc_gen folder.



4.2 Building the project

4.2.1 Building linear mode

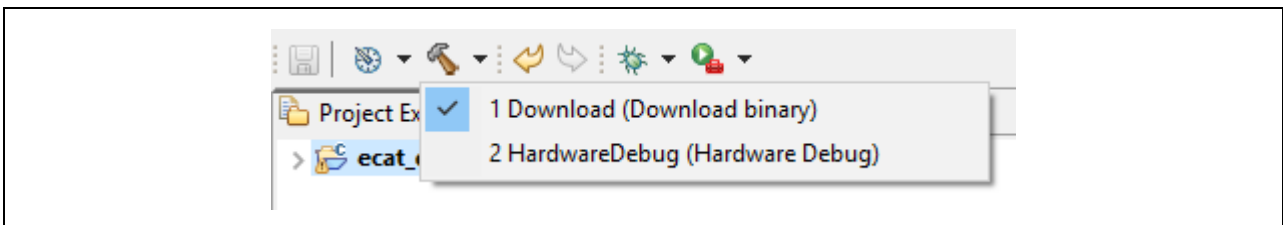
- (1) Click the arrow next to the [Build] button (hammer icon) in the toolbar and select [BANK0] from the drop-down menu.



- (2) Similarly, select [BANK1] and [BootLoader] and build.

4.2.2 Building dual mode

- (1) Click the arrow next to the [Build] button (hammer icon) in the toolbar and select [HardwareDebug] from the drop-down menu.



- (2) Similarly, select [Download] and build.

4.3 Preparation for debug

Table 4-1 shows the settings of the evaluation boards for running this sample program.

Table 4-1 Evaluation Board Settings

Setting Item	MCU	Evaluation board	Setting contents
LAN Cable	RX72M	COM board	Connected to the "ECAT IN" side
		CPU card	Connected to the "CN8" side
		RSK board	Connected to the "ECAT IN" side
Debugger	RX72M	COM board	Connecting the E2 Lite to the JTAG Connector
		CPU card	Connect the USB cable to the USB connector
		RSK board	Connecting the E2 Lite to the JTAG Connector

- (1) Connect the LAN cable as described in Table 4-1.
- (2) Connect the debugger and PC as described in Table 4-1.
- (3) The "Found new hardware" wizard appears. Follow the procedure described below to install the driver. In case of Windows™ 7/8/8.1, administrator privileges are required.

Windows™ 7/8/8.1: A notice appears on the Windows taskbar when the installation is finished.

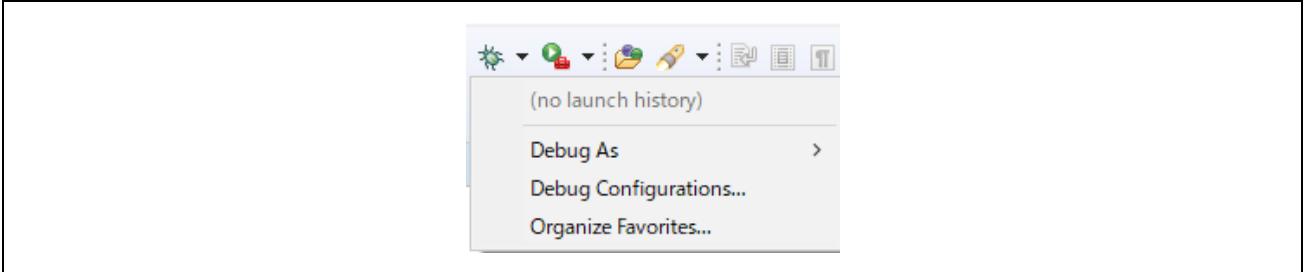
Windows™ 10: A button for device configuration appears on the Windows taskbar and installation is automatic.

- (4) Supply power to the evaluation board.

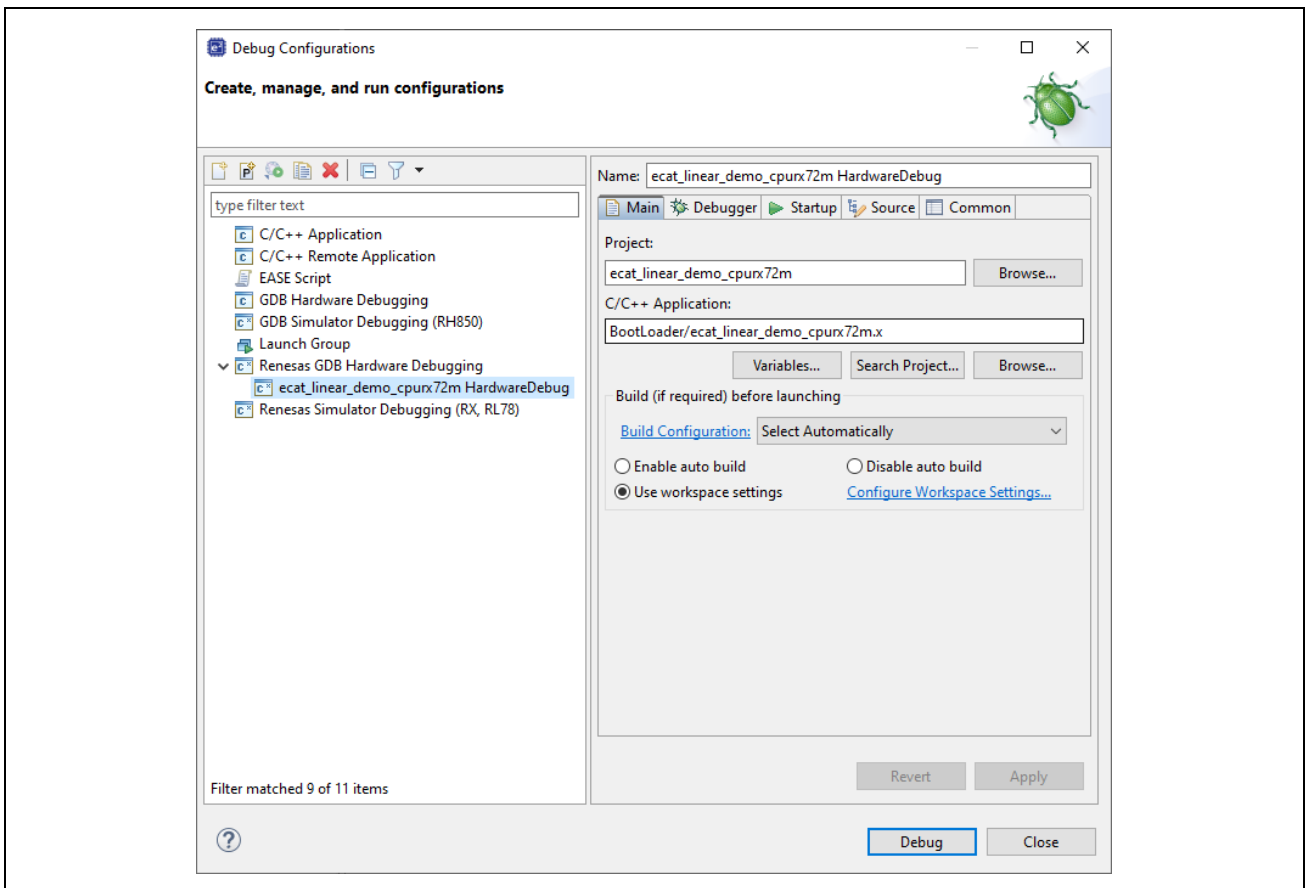
4.4 Debugging the project

4.4.1 Debugging on linear mode

- (1) Click on the arrow next to the [Debug] button (Bug icon), select [Debug configurations...], then it will start debugging.



- (2) Click on "ecat_linear_demo_cpux72m HardwareDebug" to download the program into the target and press debug button to start.



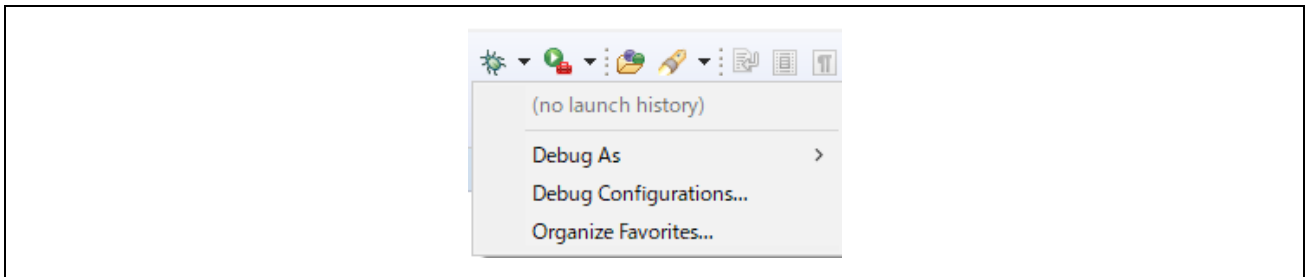
- (3) The firewall warning 'e2-server-gdb.exe' may be shown. Check [Private Network such as home and office network] checkbox and click on < Allow Access >.

- (4) The User Account Control (UAC) dialog is shown. Enter your administration password and click [YES].

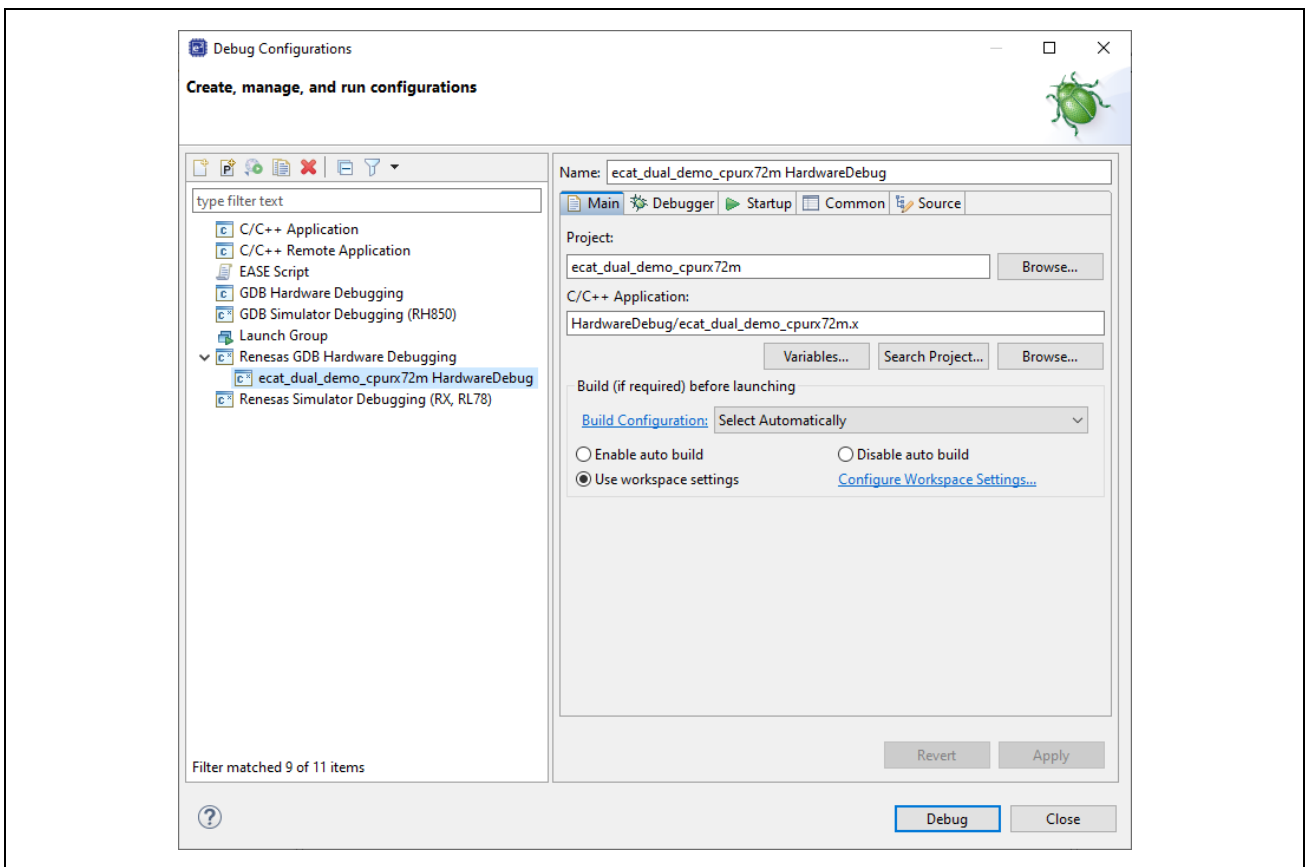
- (5) If there is recommended dialog to change the perspective display in the confirmation dialog for switching perspective. Check “Always use this setting” checkbox and click on [Yes].
- (6) After download the code, click on < Resume > button and executes the code until the first line of main () function. Click on < Resume > button again to run the target with the rest of the code.

4.4.2 Debugging on dual mode

- (1) Click on the arrow next to the [Debug] button (Bug icon), select [Debug configurations], then it will start debugging.



- (2) Click on “ecat_dual_demo_cpux72m HardwareDebug” to download the program into the target and press debug button to start.



- (3) The firewall warning 'e2-server-gdb.exe' may be shown. Check [Private Network such as home and office network] checkbox and click on < Allow Access >.
- (4) The User Account Control (UAC) dialog is shown. Enter your administration password and click [YES].
- (5) If there is recommended dialog to change the perspective display in the confirmation dialog for switching perspective. Check “Always use this setting” checkbox and click on [Yes].
- (6) After download the code, click on < Resume > button and executes the code until the first line of main () function. Click on < Resume > button again to run the target with the rest of the code.

5. Connection with TwinCAT 3

5.1 Preparation of the ESI file

Before starting TwinCAT please copy the ESI file included in the sample program to the prescribed location of TwinCAT (\\TwinCAT3.x\Config\IO\EtherCAT).

ecat_linear_demo_comrx72m\utilities\esi\RX72M EtherCAT.xml

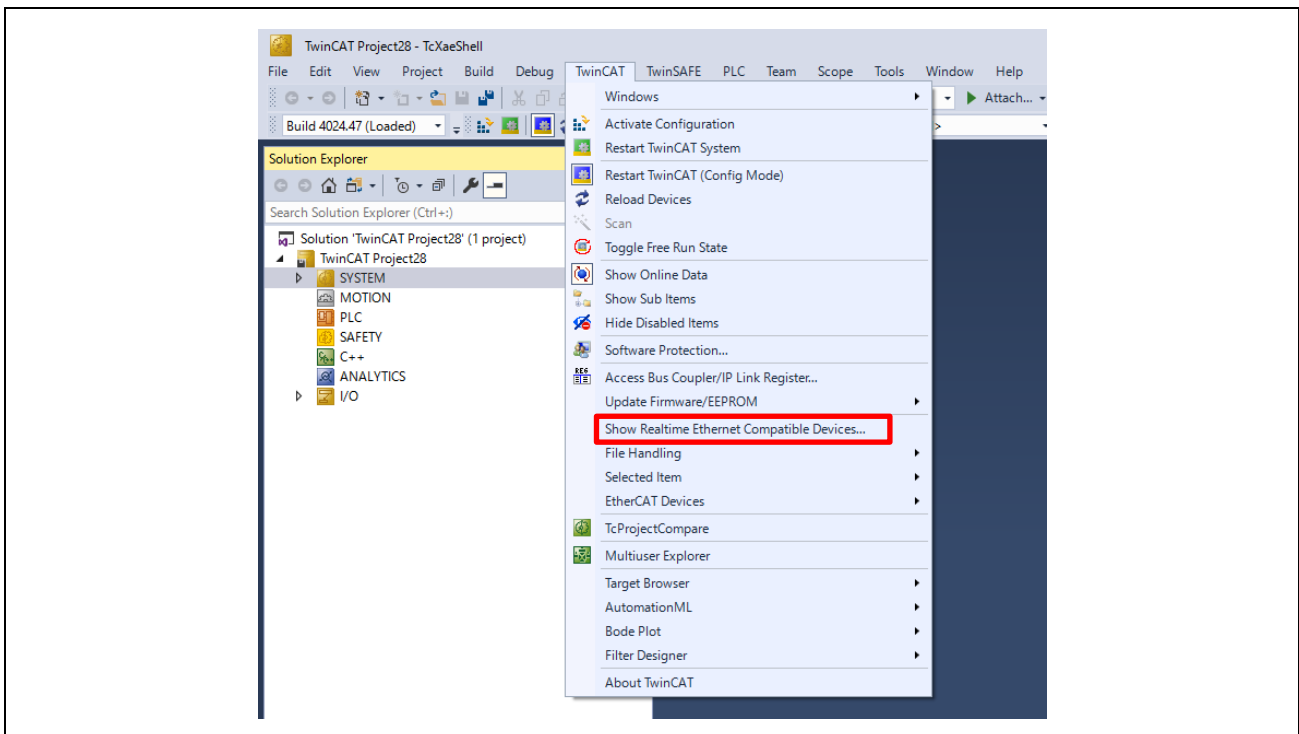
5.2 Starting TwinCAT 3

- (1) From the start menu, select [Beckhoff] → [TwinCAT 3] → [TwinCAT XAE (VS 20 xx)].
- (2) After starting the program, create a new project of type TwinCAT XAE Project as [File] → [New] → [Project].

5.3 Adding ether driver

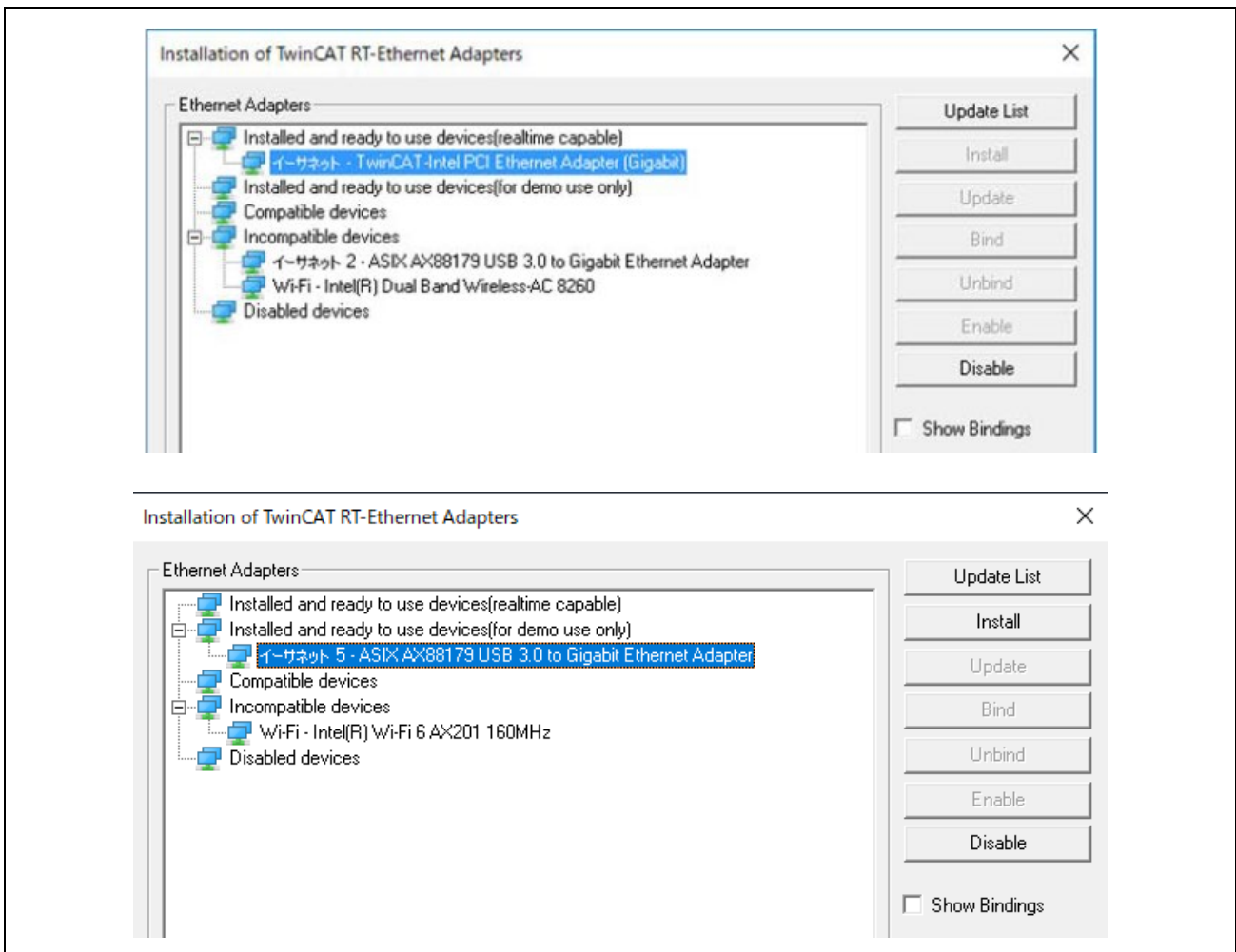
*If you have already processed this section, you do not need to process this section.

- (1) From the top menu bar, select [TwinCAT] → Select the [Show Realtime Ethernet Compatible Devices...]



- (2) After selecting the Ethernet adapter connected to the PC, press [Install] to install it.

Make sure that the installed driver is added to [Installed and ready to use devices (realtime capable)] or [Installed and ready to use devices (for demo use only)].



5.4 Scanning the network

- (1) In the System Manager tree, right-click [I / O] → [Devices] and select [Scan].
- (2) Click [OK] on the [HINT: Not all types of devices can be found automatically] dialog
- (3) In the [new I / O devices found] dialog box, select the check box of the Ethernet adapter to be scanned and click [OK].
- (4) Clicking [Yes] in the [Scan for Boxes] dialog starts scanning and the devices in the EtherCAT segment are automatically recognized.
- (5) "Active Free Run" dialog is displayed and click [Yes].

In the system manager tree, if Box is added as "Device1" → "Box1" under "I/O" → "Devices", it is normal.

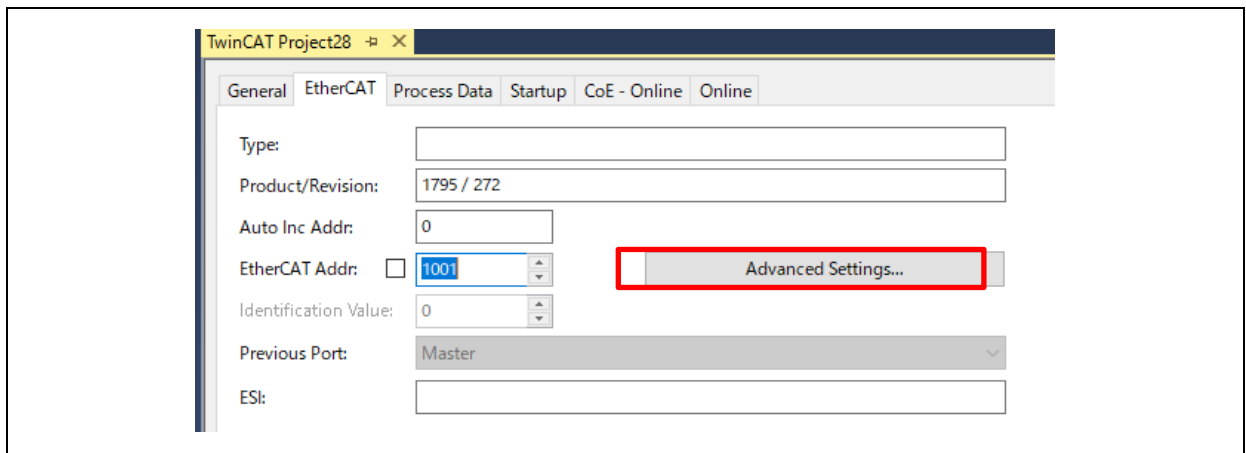
5.5 Writing of SII EEPROM

* Because the EEPROM is blank at the time of shipment of the communication board, be sure to perform writing.

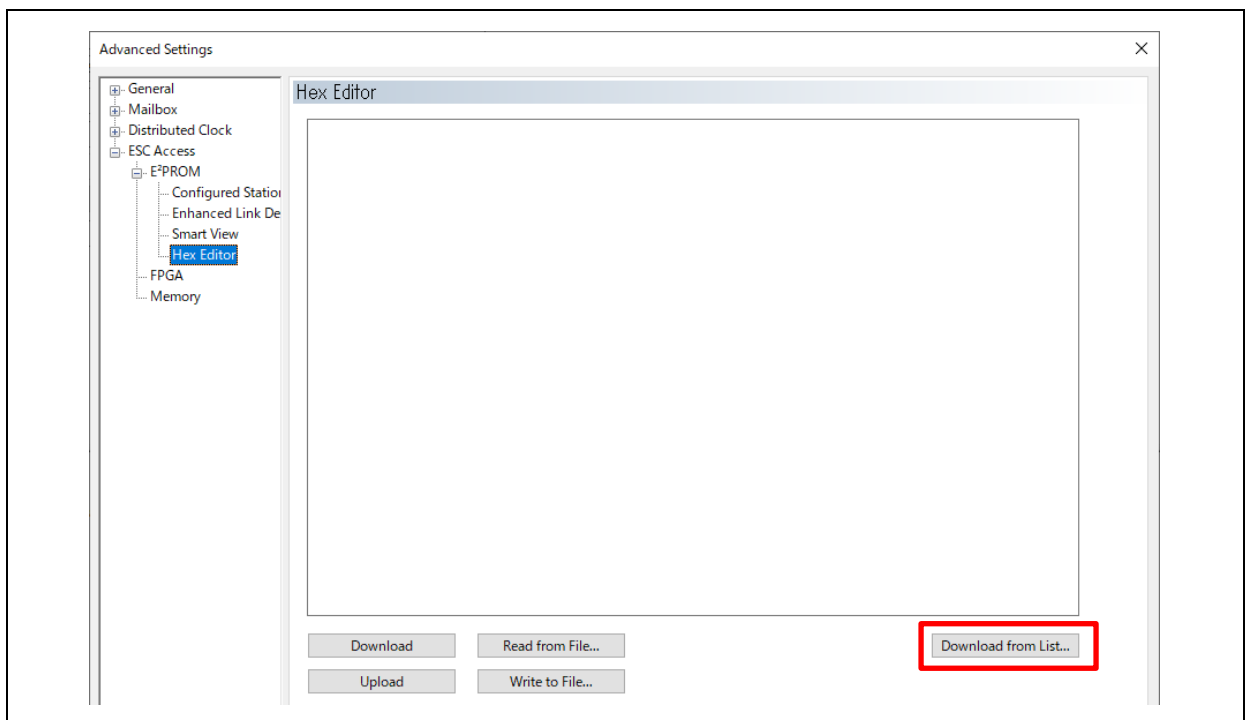
* If the EEPROM has been written, the processing in this section is unnecessary.

If the EEPROM is blank, it is displayed as "Box 1 (FFFFFFFF RFFFFFFFF)" in the system manager tree.

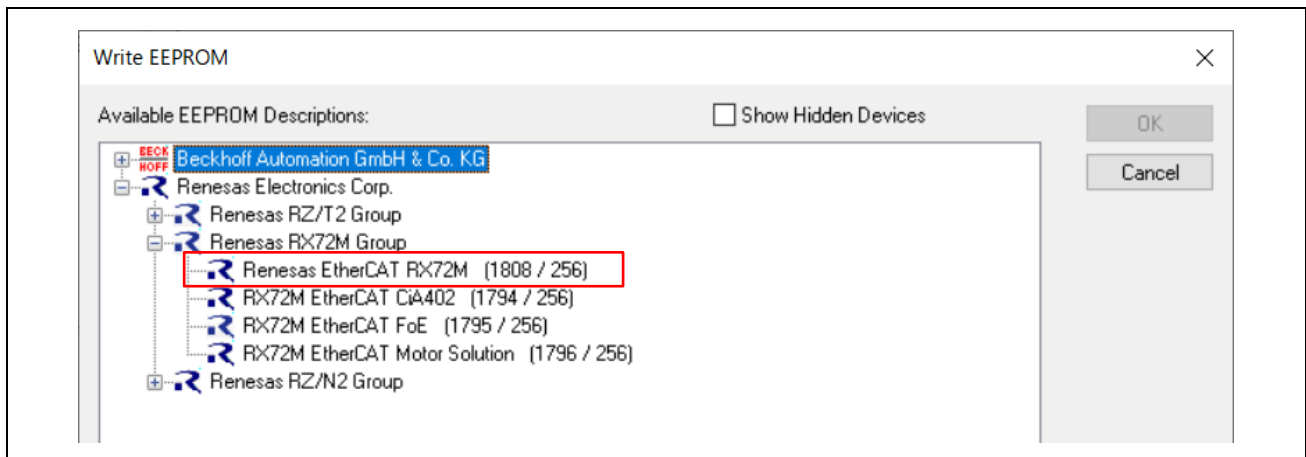
- (1) Double-click [Box 1] in the System Manager tree, the panel will be displayed on the right side.
- (2) Select the [EtherCAT] tab and click the [Advanced Settings] button.



- (3) Select [ESC Access] -> [EEPROM] -> [Hex Editor] in the left tree of the [Advanced Settings] dialog.
- (4) In the [Hex Editor] dialog, select [Download from list...].



- (5) In the [Write EEPROM] dialog box, select [Renesas Electronics Corp.] → [Renesas RX72M Group] → [Renesas EtherCAT RX72M] and click [OK]. The EEPROM is written.

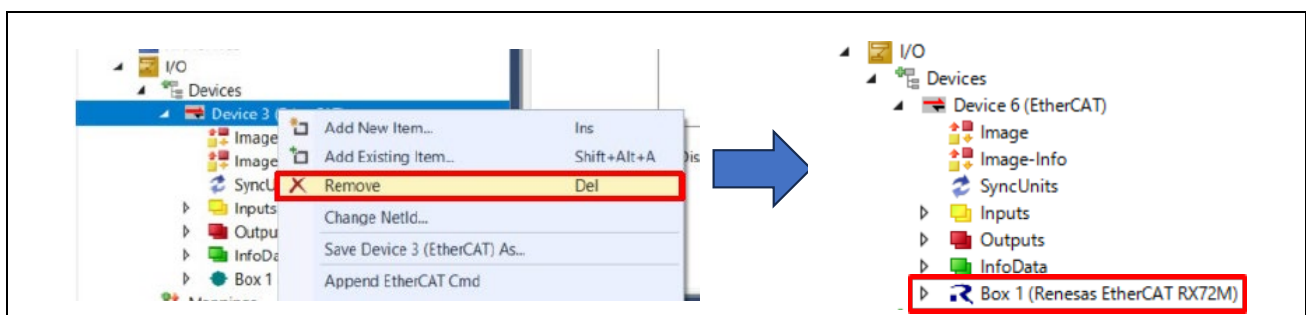


- (6) After writing, restart the communication board (turn the power supply on again or reset), so that the rewritten data is reflected in the operation of the microcomputer.

5.6 Rescan of the device

- (1) Delete [Device x] under [devices] in [I/O].
- (2) In the System Manager tree again, right-click [I/O] → [Devices] and select [Scan].
- (3) In the [HINT: Not all types of devices can be found automatically] dialog, click [OK].
- (4) In the [new I/O devices found] dialog, select the check boxes of the Ethernet adapters you want to scan, and then click [OK].
- (5) In the [Scan for Boxes] dialog, click [Yes].
- (6) In the [EtherCAT drive(s) added] dialog, select [NC - Configuration] and click [OK].
- (7) In the [Active Free Run] dialog, click [Yes].

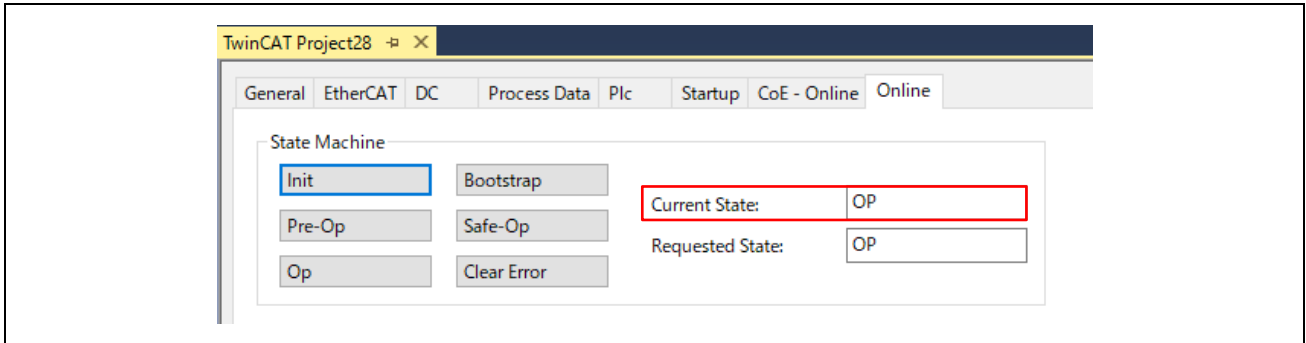
If "Box1" in the System Manager tree is "Box1 (Renesas EtherCAT RX72M)", it is normal.



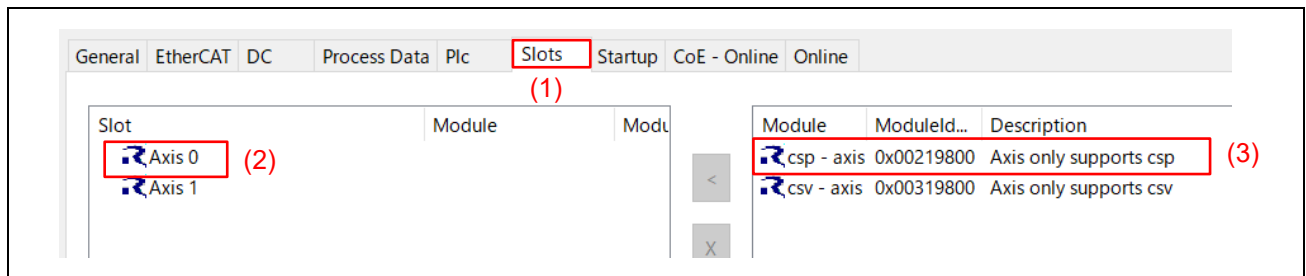
6. Operation check by TwinCAT 3

6.1 I/O operation check

- (1) Double-click "Box 1" in the System Manager tree, the panel will be displayed on the right side.
- (2) Select the "Online" tab and make sure "Current Status" is "OP".



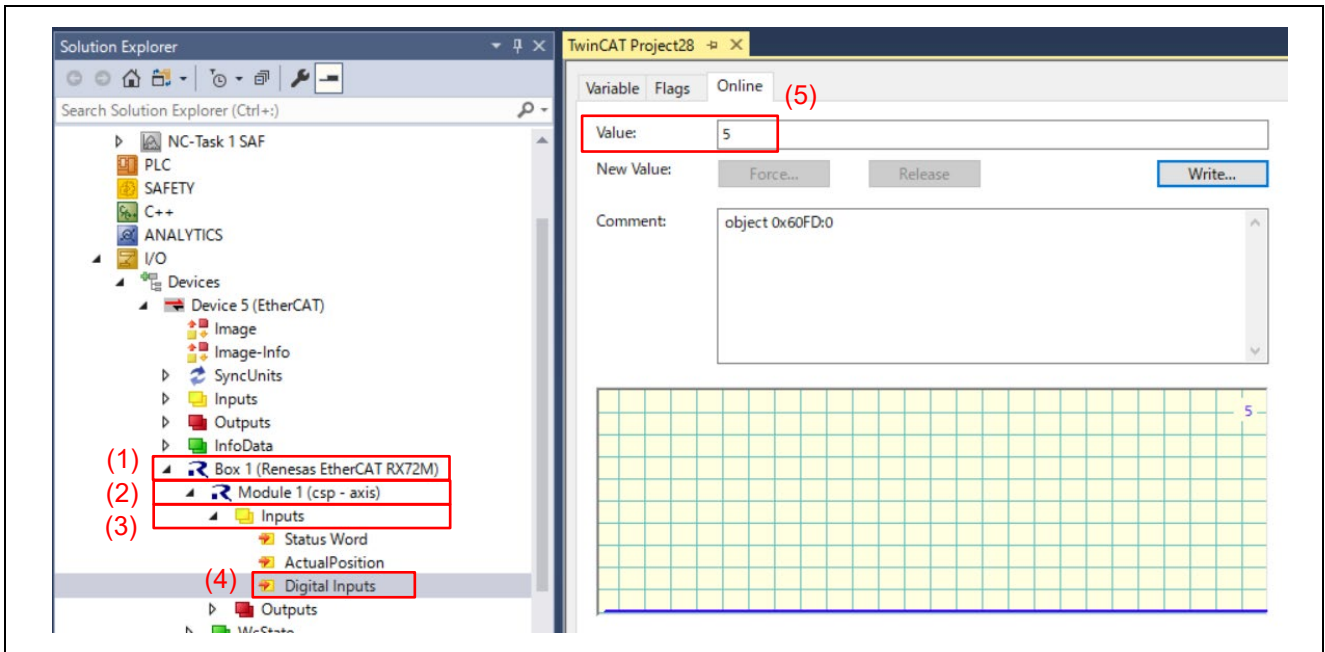
- (3) If the "Current Status" is "ERR PREOP", select the "Slots" tab to see the current slot.
 If "Axis 0" in "Slot" in the left frame is not Module "csp-axis", select "csp-axis" in the right frame and add it to "Axis 0".
 When you have added a new module to "Slot", restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.



- (4) Expand the + next to "Box 1" in the System Manager tree.
- (5) Select "Module 1 (csp - axis)" → "Inputs" → "Digital Inputs" and select the "Online" tab in the right-side panel to display "Value".
 The value of "Digital Inputs" is determined by the DIP SW or jumper pins (JP) on the evaluation board.
Table 6-1 shows the DIP SW or JP used as the value of "Digital Inputs" in this sample program.

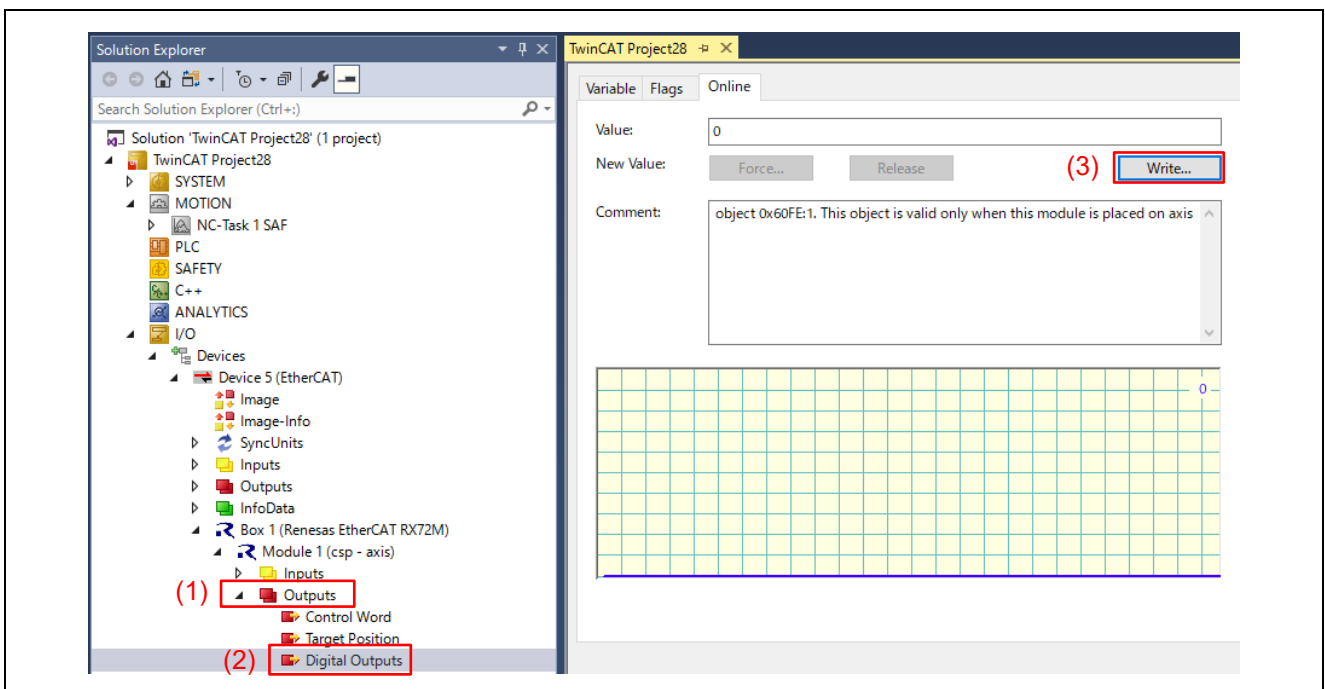
Table 6-1 DIP SW or jumper pins (JP) used as values for "Digital Inputs"

Evaluation Board	Used DIPSW or JP	Upper and lower limits of numbers
COM board	DIP SW 5	0 ~ 255
CPU card	JP 5	0 ~ 7
RSK board	DIP SW 5	0 ~ 255



(6) Select "Outputs" → "Digital Outputs" in the system manager tree and "Value" is displayed when you select the "Online" tab on the right panel.
 Make sure that "0" is displayed.

(7) Click [Write] and enter an arbitrary numerical value in the "Set Value Dialog" dialog.



(8) Click "OK" and confirm that the value "Value" is the entered value.

Depending on the value you enter, the LED on the evaluation board will light up.
 (LED lights up when bit = 1)

Table 6-2 shows the correspondence between the "Digital Outputs" defined in this sample program and the LEDs on each evaluation board.

Table 6-2 The correspondence between the “Digital Outputs” and the LEDs on Each Evaluation Board

Evaluation Board	Value of "Digital Outputs"	LEDs that light up
COM board	Bit 0 is 1	LED 1
	Bit 1 is 1	LED 2
	Bit 2 is 1	LED 3
	Bit 3 is 1	LED 4
CPU card	Bit 0 is 1	LED 6
	Bit 1 is 1	LED 7
RSK board	Bit 0 is 1	LED 1
	Bit 1 is 1	LED 2
	Bit 2 is 1	LED 3
	Bit 3 is 1	LED 4

6.2 CiA402 Drive Profile operation check

6.2.1 CiA402 State Transition

In order to check the operation of the csp mode and csv mode, it is necessary to transition to the “Operation Enabled” state for both modes.

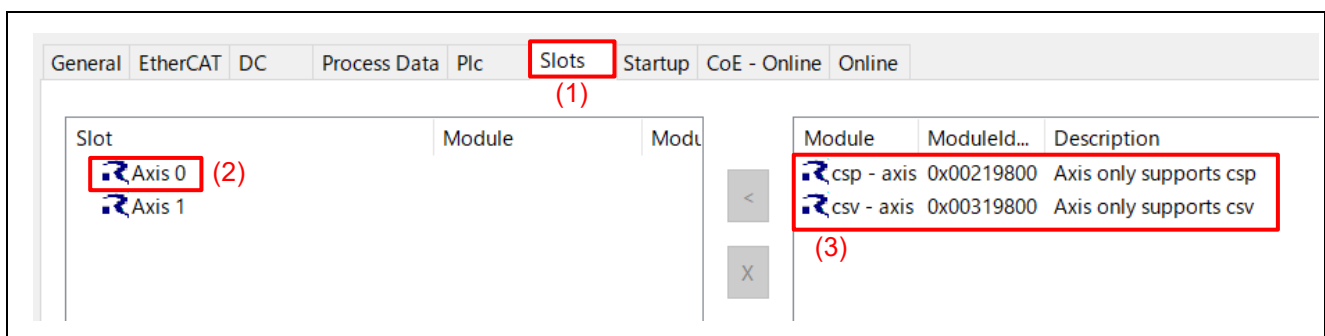
The state transition is triggered by setting the value in the "Control Word" object, and the status is checked by the value of the "Status Word" object.

(1) Double-click "Box 1" in the System Manager tree to display a panel on the right side.

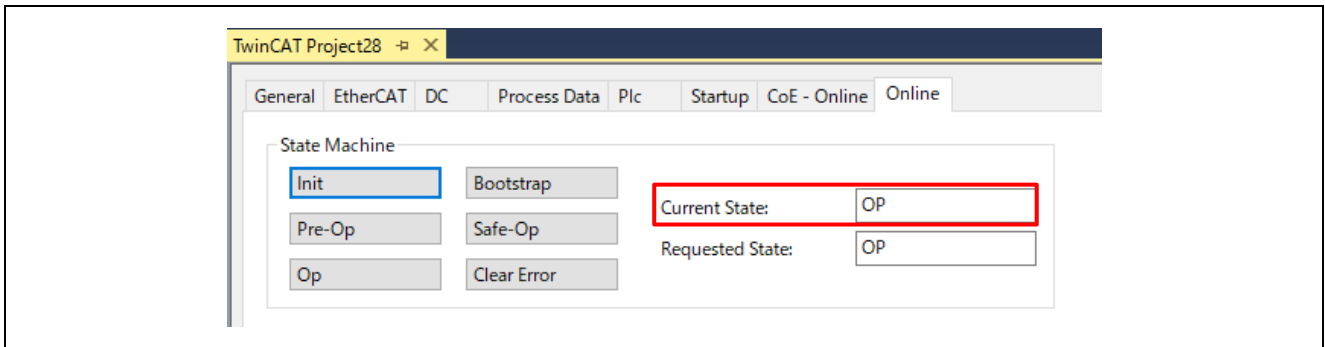
(2) Select the "Slots" tab to confirm the current slots.

Select and add the module you want to transition to the "Operation Enabled" state to "Axis 0" or "Axis 1" in the "Slot" in the left frame.

If you add or change a module to "Slot", restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.



- (3) Select the "Online" tab, make sure that the "Current Status" is set to "OP".



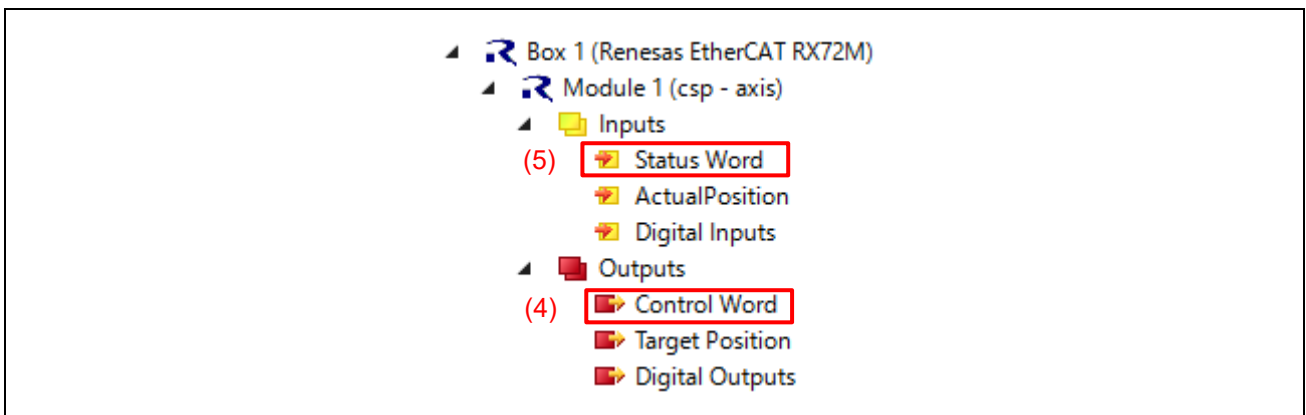
- (4) In the System Manager tree, select "Outputs" → "Control Word" and select the "Online" tab in the right panel to display "Value".

Click [Write] and set the value to [7] → [15].

- (5) In the System Manager tree, select "Inputs" → "Status Word", and then select the "Online" tab in the right panel to display "Value".

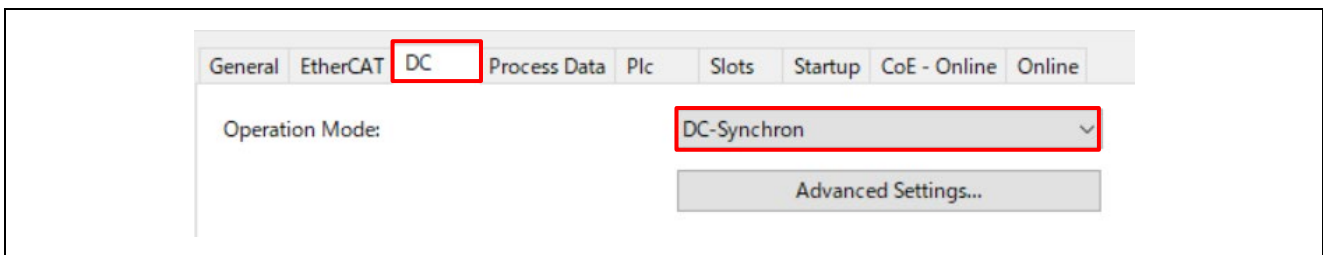
If it is [4663], it has transitioned to "Operation Enabled" and please proceed to the next step.

If it is [4616], it has transitioned to "Fault" for some reason. Set "Control Word" to [128] and then return to (1).

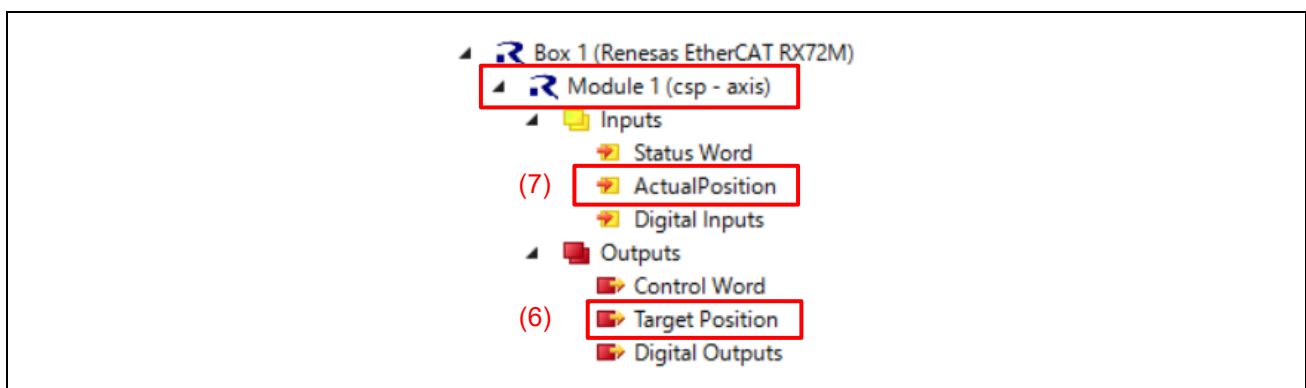


6.2.2 csp mode

- (1) Double-click "Box 1" in the System Manager tree to display a panel on the right side.
- (2) Select the "Slots" tab and make sure that there is "csp-axis" in "Axis 0" in the "Slot" in the left pane. Otherwise, select "csp-axis" in "Axis 0" of "Slot" in the left frame and add or change it.
When you have added a new module to "Slot", restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.
- (3) Select the "Online" tab, make sure that the "Current Status" is set to "OP".
- (4) Select the "DC" tab and make sure that the Operation Mode is "DC-Synchron".

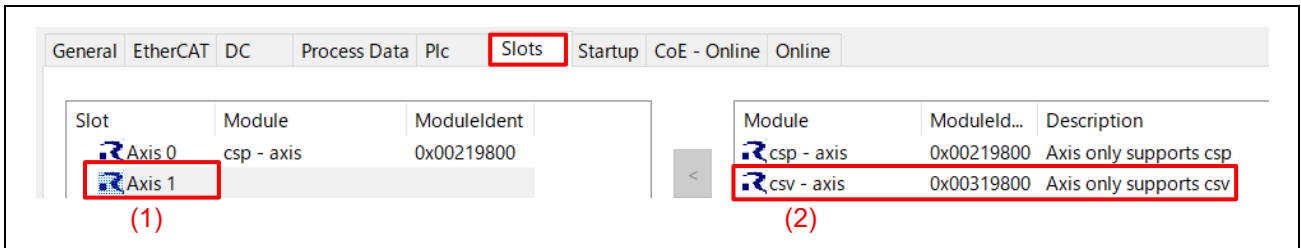


- (5) Follow the procedure in 6.2.1 and transition to "Operation Enabled".
- (6) In the System Manager tree, select "Outputs" → "Target Position" and select the "Online" tab in the right panel to display "Value".
Click [Write] and set the value to the desired value.
As an example, here we set [100000].
- (7) In the System Manager tree, select "Inputs" → "Actual Position" and select the "Online" tab in the right panel to display "Value".
Make sure that it is incremented to [100000] set in "Target Position".

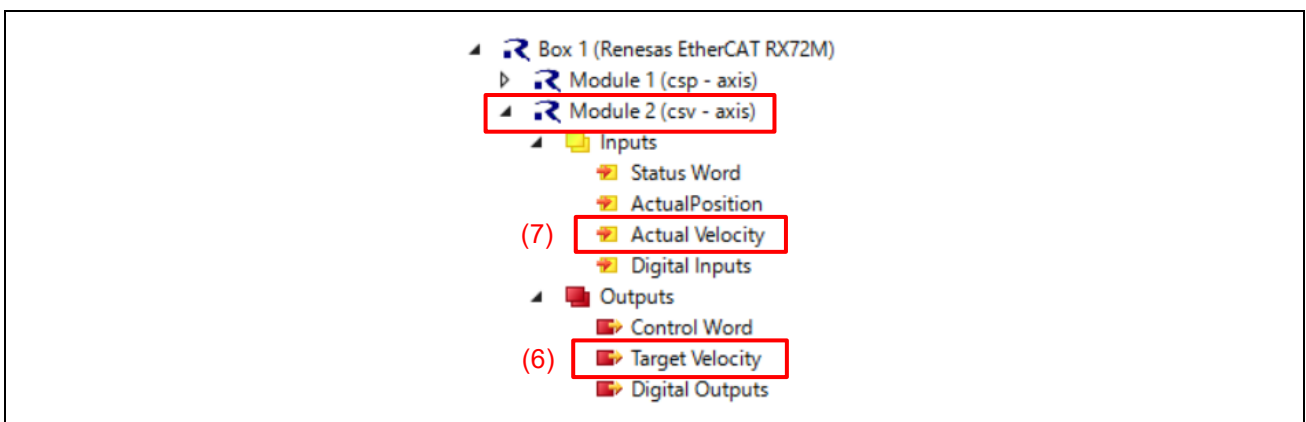


6.2.3 csv mode

- (1) Double-click "Box 1" in the System Manager tree to display a panel on the right side.
- (2) Select the "Slots" tab and make sure that there is "csv-axis" in "Axis 1" in the "Slot" in the left pane. Otherwise, select "csv-axis" in "Axis 1" of "Slot" in the left frame and add or change it.
When you have added a new module to "Slot", restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.



- (3) Select the "Online" tab, make sure that the "Current Status" is set to "OP".
- (4) Select the "DC" tab and make sure that the Operation Mode is "DC-Synchron".
- (5) Follow the procedure in 6.2.1 and transition to "Operation Enabled".
- (6) In the System Manager tree, select "Outputs" → "Target Velocity" and select the "Online" tab in the right panel to display "Value".
Click [Write] and set the value to the desired value.
As an example, here we set [100000].
- (7) In the System Manager tree, select "Inputs" → "Actual Velocity" and select the "Online" tab in the right panel to display "Value".
Make sure that it is incremented to [100000] set in "Target Velocity".

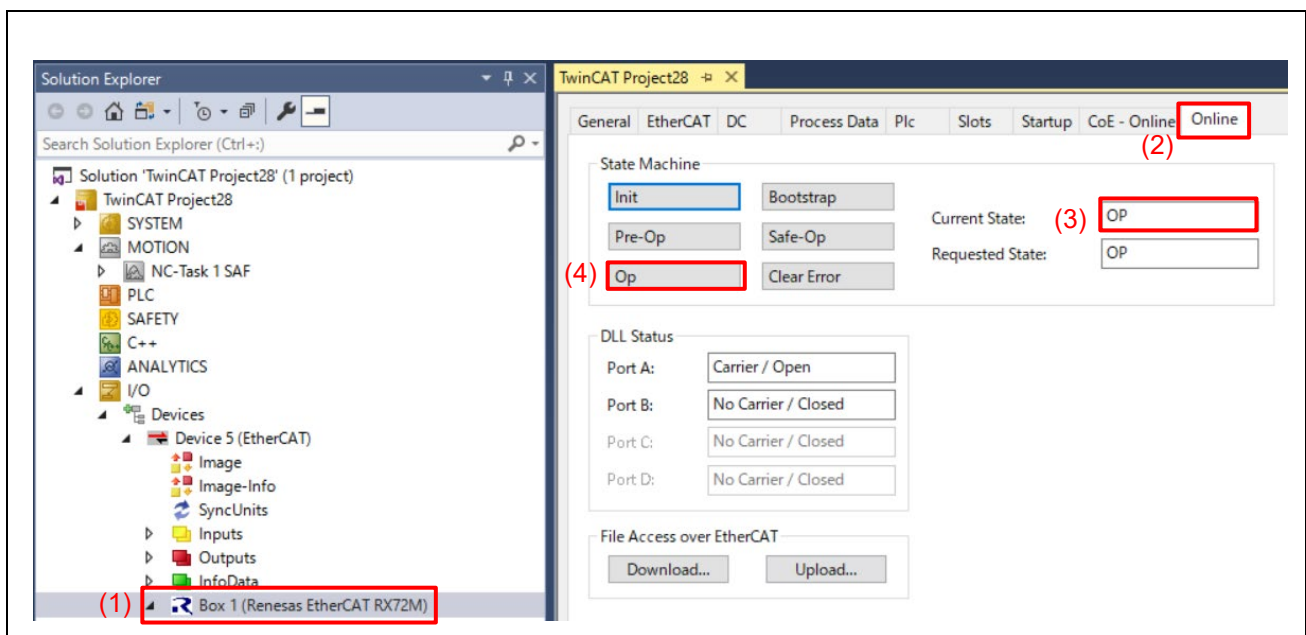


6.3 Firmware update operation check

6.3.1 Firmware writing

This chapter describes the procedure to write the new revision firmware to BANK1 while the program is running on BANK0.

- (1) Select "Box 1 (Renesas EtherCAT RX72M)" in "Solution Explorer"
- (2) Click the "Online" tab
- (3) Make sure the Current State is "OP".
- (4) If it is not "OP", press the "Op" button to transition to "OP"



※If "Current Status" is "ERR PREOP", select the "Slots" tab to check the current slots.

If there is no Module "csp-axis" in "Axis 0" in "Slot" in the left frame, select "csp-axis" in the right frame and add it to "Axis 0".

If you have added a new module to "Slot", restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.

- (5) Click the "CoE – Online".
- (6) Confirm "Show Offline Data" is not checked. If it is checked, please clear it.
- (7) Press the "Update List" button to update the CoE list.
- (8) Check the value of Index 1018:03 Revision. In the example, 0x00000100(256), which means Rev 1.00, is displayed.
- (9) Check the value of Index 5000 Firmware Writable Bank. In the example, the writable bank is BANK1, so 0x01(1) is displayed.

The screenshot shows the 'CoE - Online' window with the following elements highlighted:

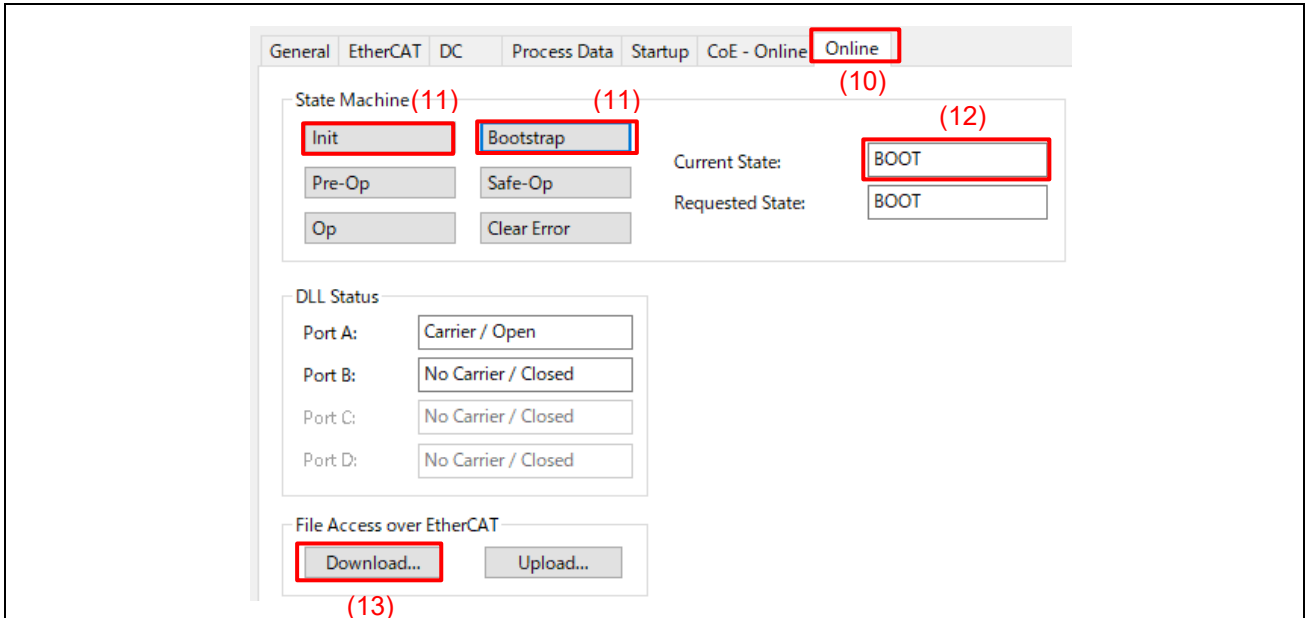
- (5) The 'CoE - Online' tab is selected.
- (6) The 'Show Offline Data' checkbox is unchecked.
- (7) The 'Update List' button is highlighted.
- (8) The row for Index 1018:03 'Revision Number' is highlighted, showing a value of 0x00000100 (256).
- (9) The row for Index 5000 'Firmware Writable Bank' is highlighted, showing a value of 0x01 (1).

Index	Name	Flags	Value
1010:0	Store parameters	RO	> 1 <
1011:0	Restore default parameters	RO	> 1 <
1018:0	Identity Object	RO	> 4 <
1018:01	Vendor ID	RO	0x00000766 (1894)
1018:02	Product Code	RO	0x00000710 (1808)
1018:03	Revision Number	RO	0x00000100 (256)
1018:04	Serial Number	RO	0x00000000 (0)
10F0:0	Backup parameter handling	RO	> 2 <
10F1:0	Error Settings	RO	> 2 <
1C32:0	SM output parameter	RO	> 32 <
1C33:0	SM input parameter	RO	> 32 <
5000	Firmware Writable Bank	RO	0x01 (1)
603F	Error Code	RO P	0x0000 (0)
6040	Control Word	RW P	0x000F (15)

(10) Click on the "Online" tab

(11) Press "Init" button -> "Bootstrap" button in sequence.

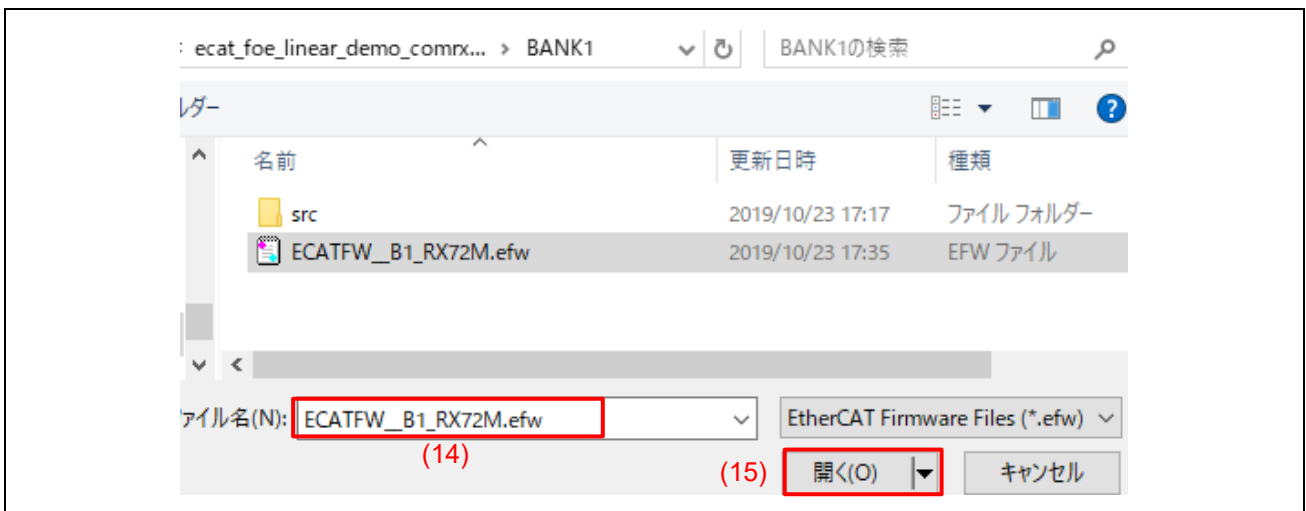
(12) Confirm that the Current State changes to "BOOT"



(13) Click the "Download" button of File Access over EtherCAT to open the window for selecting the download file.

(14) Select "ECAT__B1_RX72M.efw" which is the download file for BANK1

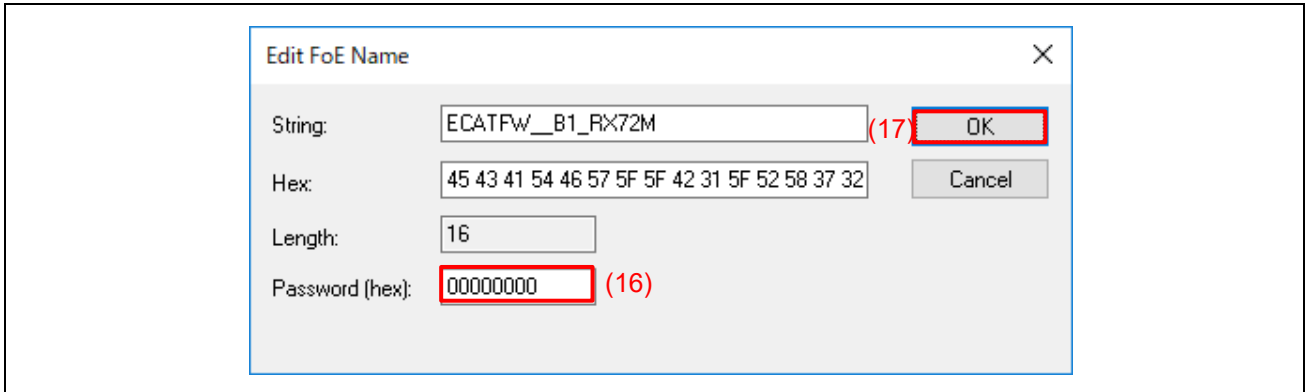
(15) Pressing the "Open".



The file name editing window will open.

(16) Password remains of "00000000"

(17) Press "OK"



The download status is displayed along with the message "Downloading" on the bottom left of TwinCAT System Manager screen.

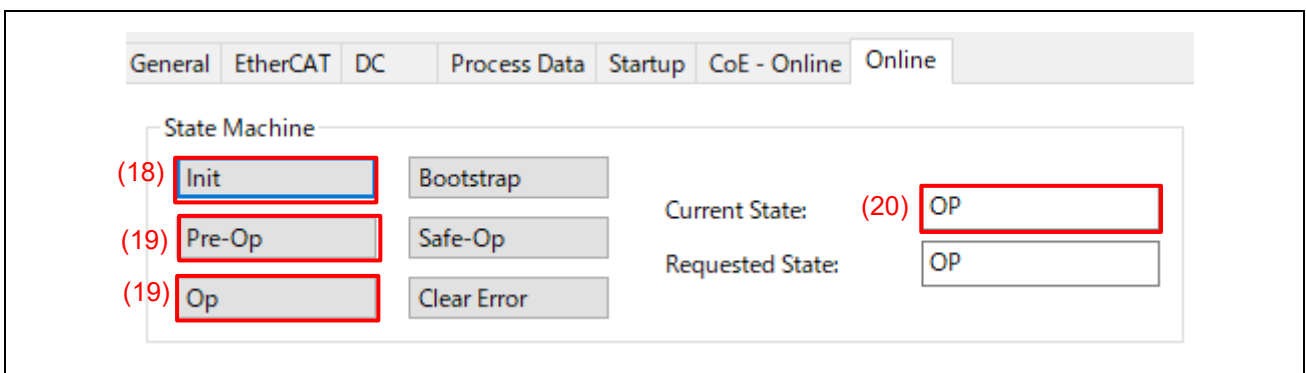
If no error message is displayed and the above window disappears and the status is "Ready", the firmware update was successful.

In the "Online" tab

(18) Press the "Init" button to restart with the updated firmware.

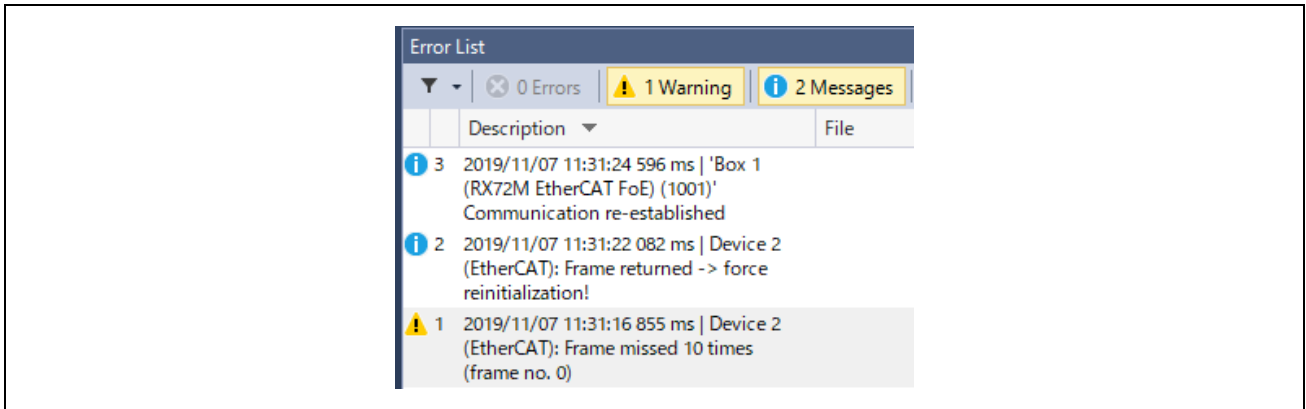
(19) Press "Preop" button -> "Op" button.

(20) Current State transitions to "OP" and can see the updated firmware action.



In case of linear mode, can verify that EtherCAT does not leak links during reboots.

In case of dual mode, the software is reset when the system is restarted, so the link will be broken and the Warning message shown below will be displayed, but this is not a problem.

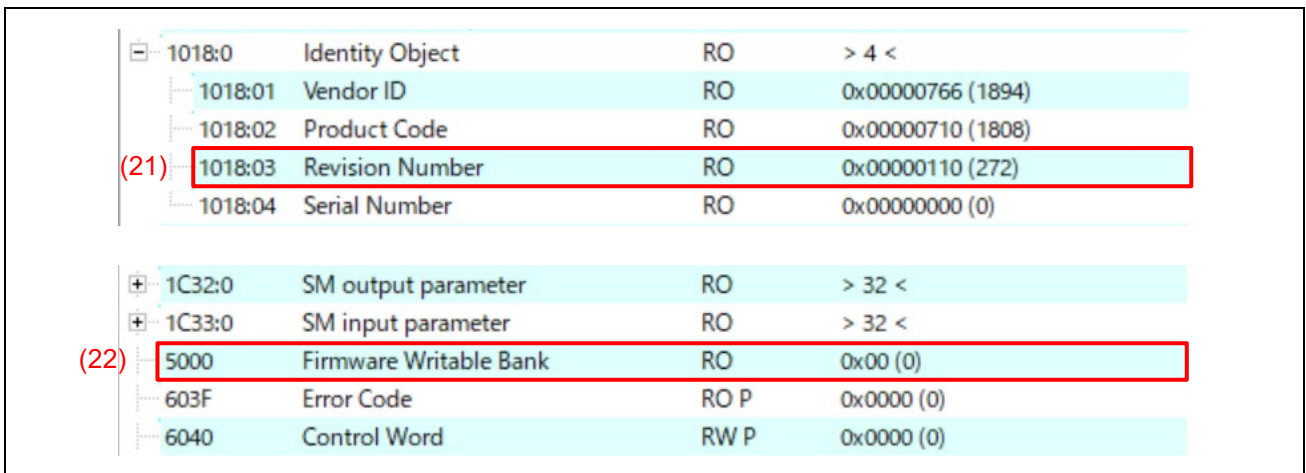


Click the “CoE – Online” tab again and click the “Update List” button to update the CoE list.

(21) Check the value of Index 1018:03 Revision. You can see that it changed to Rev 1.10 of BANK 1 revision 0x00000110(272).

(22) Check the value of Index 5000 Firmware Writable Bank. The writable bank has changed from BANK1 to BANK0, so 0x00(0) is displayed.

In case of dual mode it will remain at 0x01(1).



6.3.2 Firmware readout

It is possible to read the binary data of the firmware stored in the BANK area where the program is executed.

The binary data is saved in the EtherCAT master as an upload file.

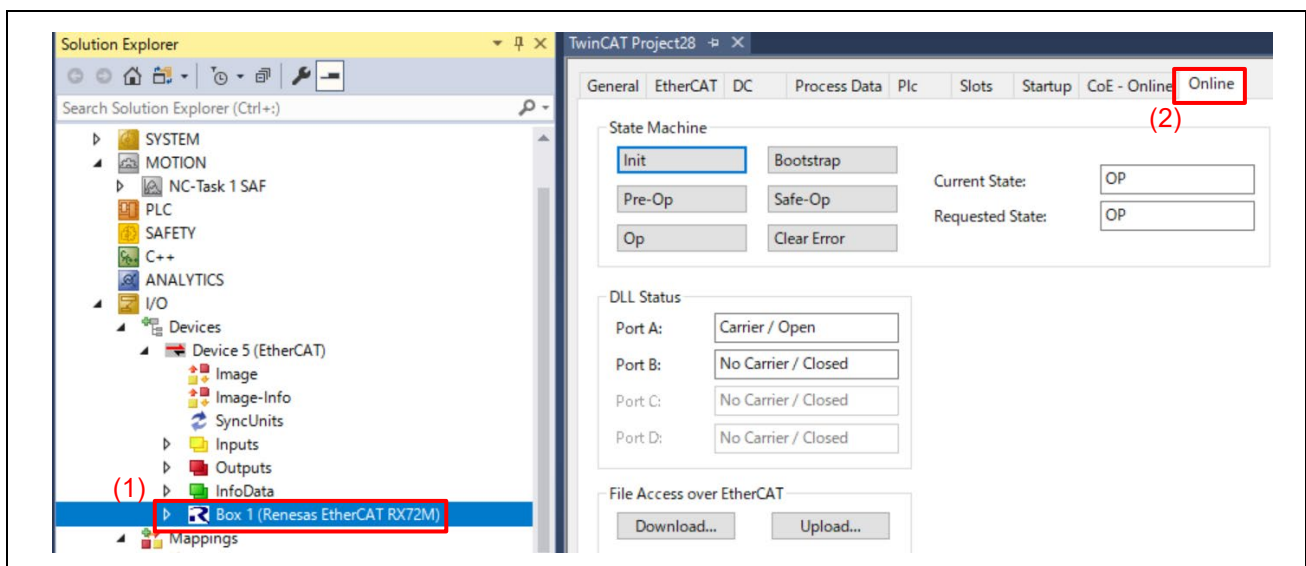
The format of the upload file is shown in Table 6-3.

Table 6-3 Format of the upload file

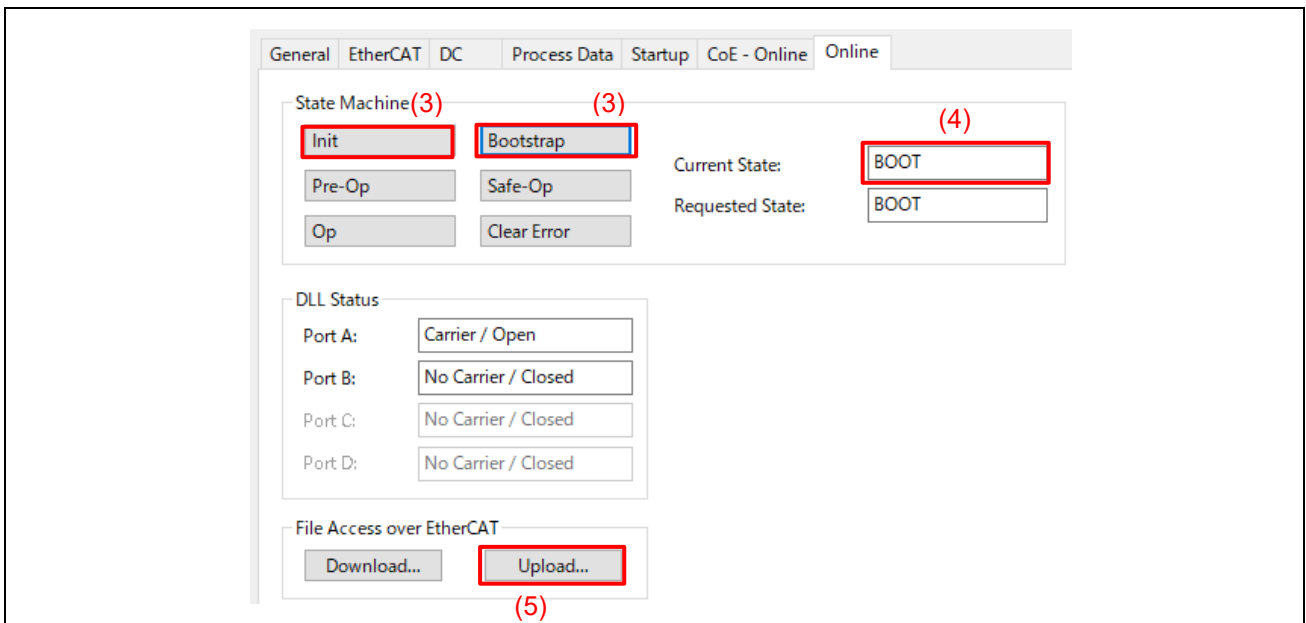
Item	Contents	
File name prefix	"ECATFW_"	
File extension	bin	
File Formats	Binary format * Note that this is different from the Motorola S format of the download file.	
File size	Linear mode	4MB Product : 2016KB 2MB Product : 992KB
	Dual mode	4MB Product : 2048KB 2MB Product : 1024KB
Read target BANK	Linear mode	BANK1 when Firmware Writable Bank = 0 BANK0 when Firmware Writable Bank = 1
	Dual mode	Always BANK0

This section describes the procedure for reading the binary data of the firmware.

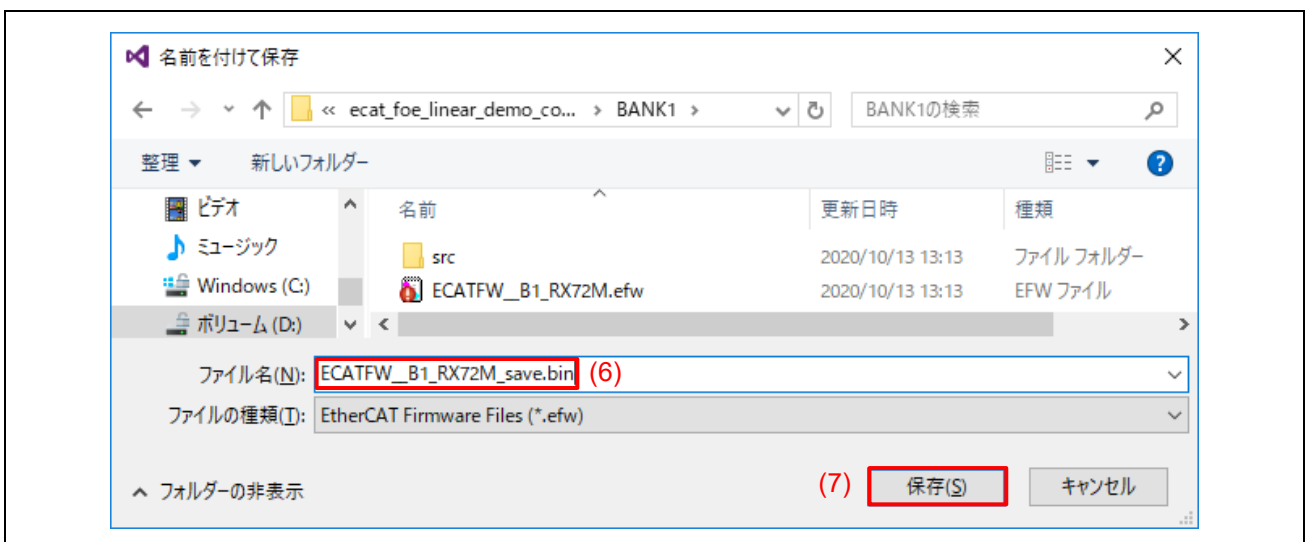
- (1) After selecting "Box 1 (Renesas EtherCAT RX72M)" in "Solution Explorer"
- (2) Click the "Online" tab.



- (3) Press the "Init" button-> "Bootstrap" button in order,
- (4) Make sure that the Current State transitions to "BOOT".



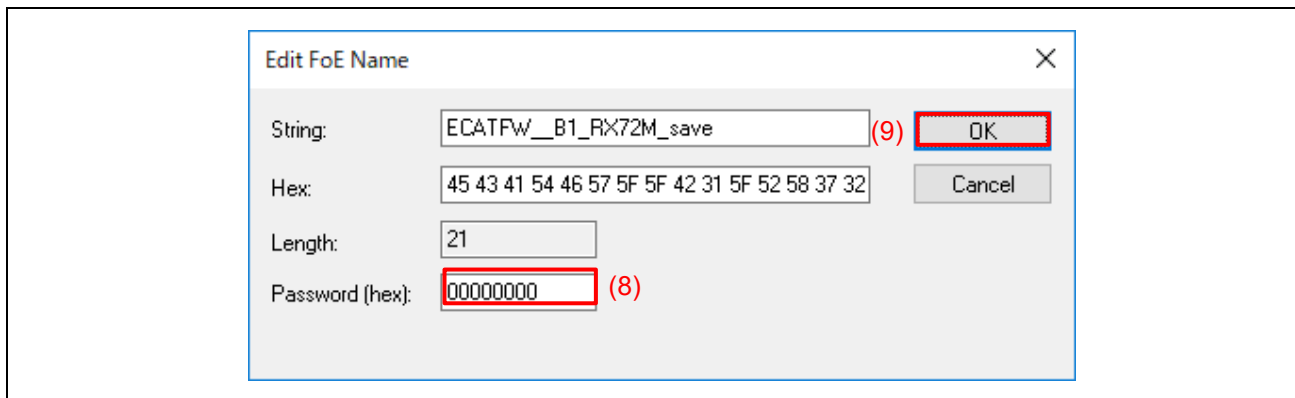
- (5) Click the "Upload" button of File Access over EtherCAT to open the save file window.
- (6) Enter "ECATFW_B1_RX72M_save.bin" as the upload file name.
- (7) Press "Save".



The file name editing window will open.

(8) Password remains "00000000"

(9) Press "OK".



The upload status is displayed with the message "Uploading" at the bottom left of the screen of TwinCAT System Manager.

If no error message is displayed and the upper window disappears and becomes "Ready", the upload is successful.

7. Configuration of project

This chapter describes the configuration for constructing this sample program.

Refer to this page when making a new project.

7.1 Configuration of FIT module

In this project, the configuration of the FIT module are changed from the default to construct this sample program.

You can open the Smart Configuration file and check or change the configuration of the FIT module on the components tab.

Table 7-1 shows the changes of the FIT module configuration.

Table 7-1 The list of the FIT module configuration changes

FIT module	Reason for change	Configuration	Settings
r_bsp	Increasing the heap size	Heap size	0x8000
	Using the user charget function	Enable user stdio charget function	Use user charget() function
	Using the user charput function	Enable user stdio charput function	Use user charput() function
r_sci_rx	Enabling SCI CH6	Include software suport for channel 6	Include
	Enabling Transmit end interrupt	Transmit end interrupt	Enable

The configuration of the EtherCAT FIT module is different for each evaluation board.

Table 7-2 shows the configuration of the EtherCAT FIT module.

Table 7-2 the list of the EtherCAT FIT module configuration changes

Evaludation board	Reason for change	Configuration	Settings
COM borad CPU card	Setting the waitng time for reset completion of PHY-LSI	The waitng time for reset completion of PHY-LSI (us)	500
	Setting used PHY-LSI	Use supported PHY-LSI	The KSZ8081MNX is used.
RSK board	Setting the waitng time for reset completion of PHY-LSI	The waitng time for reset completion of PHY-LSI (us)	1000
	Setting used PHY-LSI	Use supported PHY-LSI	The KSZ8041NL is used.

The configuration of the Flash FIT module is different for each bank mode.

Table 7-3 shows the configuration of the Flash FIT module.

Table 7-3 the list of the Flash FIT module configuration changes

Bank mode	Reason for change	Configuration	Settings
Linear mode	Enabling code flash programming.	Enable code flash programming	Include code to program ROM area
	Programming code flash on the RAM area.	Enable code flash self-programming	Programming code flash while executing on RAM. (Default)
Dual mode	Enabling code flash programming.	Enable code flash programming	Include code to program ROM area
	Programming code flash on another bank.	Enable code flash self-programming	Programming code flash while executing from another segment in ROM.

The configuration of bank mode is different for each bank mode.

Table 7-4 shows the configuration of the bank mode.

Table 7-4 the list of the bank mode configuration changes

Macro name	Bank mode	settings
BSP_CFG_CODE_FLASH_BANK	Linear mode	1 (Default)
	Dual mode	0

Bank mode settings cannot be checked or changed on the Components tab.

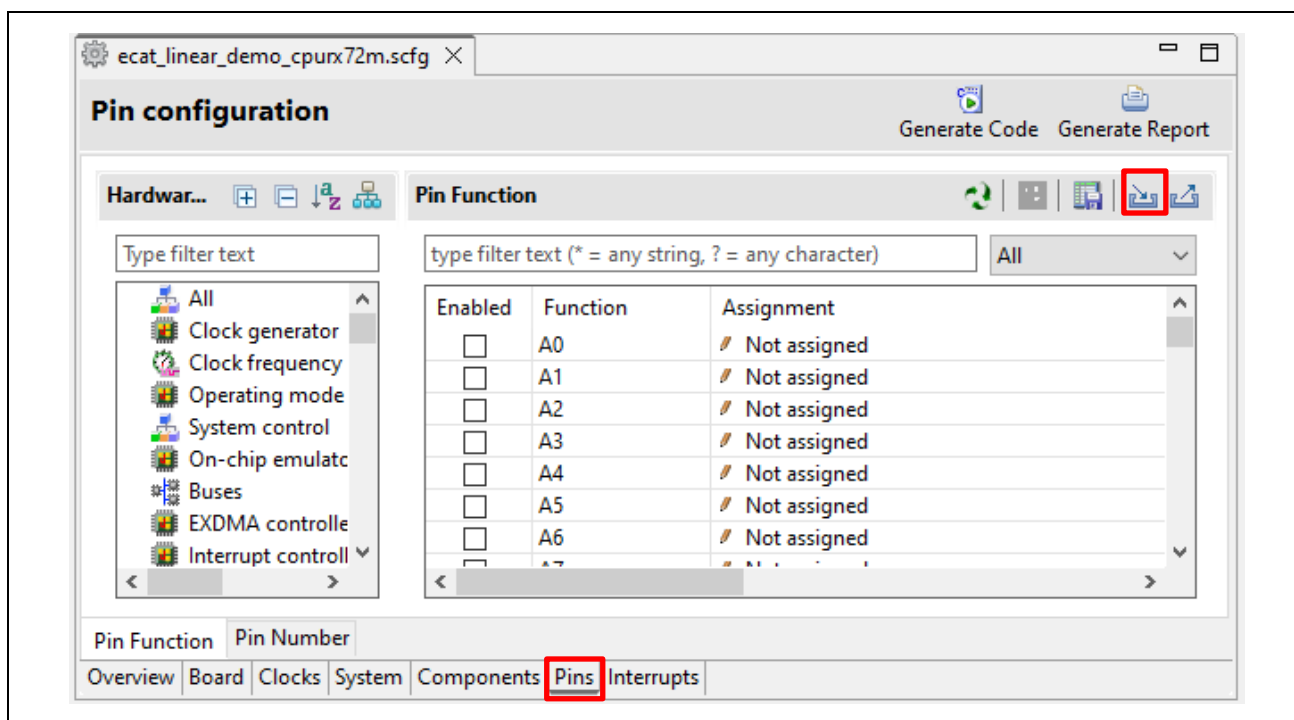
You can check and change it in the generated file “src\smc_gen\r_config\r_bsp_config.h” after code generation.

7.2 Pin settings

You can import the terminal settings to run the sample program.

On the [Pins] tab of Smart Configurator, click the [Import Terminal Function Arrangement] button and select “ecat_linear_demo_cpurx72m_board.xml”.

The xml file is included in the sample program.



Select the pins used by the FIT module in the [Resources] of the [Components] tab of the Smart Configurator.

The items listed in Table 7-5 must be enabled.

Table 7-5 The list of the enabled pins

Component	Resources to enable	Pins to enable
r_ecat_rx	ESC ESC_MII0 ESC_MII1	All pins
r_sci_rx	SCI6	RXD6/SMISO6/SSCL6 pin TXD6/SMOSI6/SSDA6 pin

7.3 build configuration

7.3.1 Linear mode build configuration

Describes the changes of each build configuration for a project used in linear mode.

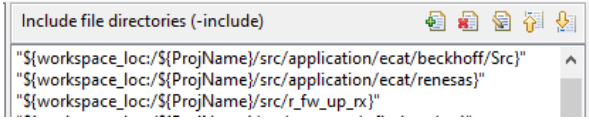
Table 7-6 Linear mode build configuration

Composition name.	Description
<p>BootLoader</p>	<p>Build the boot loader program.</p> <p>Files other than the functionality required by the boot loader are excluded from the build.</p> <p>Right-click the corresponding file or folder and exclusion of build is possible by selecting [Resource Configuration] → [Exclude from Build].</p> <p><Settings></p> <ul style="list-style-type: none"> ▼ src <ul style="list-style-type: none"> ▼ demo <ul style="list-style-type: none"> > bt_main.c > siorw.c ✗ main.c ▼ r_fw_up_rx <ul style="list-style-type: none"> > r_fw_up_bank.c > r_fw_up_buf.h > r_fw_up_rx_if.h > r_fw_up_rx_private.h ✗ r_fw_up_buf.c ✗ r_fw_up_rx.c ▼ smc_gen <ul style="list-style-type: none"> > general > r_bsp > r_byteq > r_config > r_flash_rx > r_pincfg > r_sci_rx > r_cmt_rx > r_ecat_rx > application
<p>BANK0</p>	<p>Build the EtherCAT slave program that you want to download to BANK0.</p> <p>Build artifacts are Motorola S-formatted files.</p> <p>Excludes only demo/bt_main.c from build.</p> <p><Settings></p> <ul style="list-style-type: none"> ▼ src <ul style="list-style-type: none"> ▼ demo <ul style="list-style-type: none"> > main.c > siorw.c ✗ bt_main.c
<p>BANK1</p>	<p>Build the EtherCAT slave program that you want to download to BANK1.</p> <p>Bank0 and bank1 have the same settings except that the code flash mapping and the download file name that is the build artifacts is different.</p>

7.3.1.1 BootLoader

You can check the settings in [Project] → [Properties] → [C/C++ Build] → [Settings].

Table 7-7 BootLoader – tools Settings tab

Item	Changing Contents	Description																										
Compiler - Source	Add Include path to [Include · File · Directory]	<p>In each FIT module, please add the required include path for the setting.</p> <p>The code-generated folders are automatically configured only if you use the FIT Configurator to include each FIT module.</p> <p>About program files that you do not want to generate, you must manually add the include path.</p> <p>In this project, the following three items have been added.</p> 																										
Compiler - Optimization	Change optimization Level 0 : No performing optimization	The optimization level is set to 0 due to prevent the const table referenced by bootloader from being built by optimization.																										
Linker - Section	<p>Change the starting position of the PResetPRG placed in the ROM area to 0xFFFF8000.</p> <p><Setting></p> <table border="1" data-bbox="359 1108 758 1579"> <tbody> <tr><td>0xFFFF8000</td><td>PResetPRG</td></tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>C\$*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM</td></tr> <tr><td>0xFFFFF80</td><td>EXCEPTVECT</td></tr> <tr><td>0xFFFFF8C</td><td>RESETVECT</td></tr> </tbody> </table>	0xFFFF8000	PResetPRG		C_1		C_2		C		C_8		C\$*		D*		W*		L		P		PFRAM	0xFFFFF80	EXCEPTVECT	0xFFFFF8C	RESETVECT	<p>The mapping of boot loader is from 0xFFFF8000 to 0xFFFFFFFF. Size is 32KB.</p> <p>The exception vector table of 128 bytes including reset vector is placed at the end of the line.</p>
0xFFFF8000	PResetPRG																											
	C_1																											
	C_2																											
	C																											
	C_8																											
	C\$*																											
	D*																											
	W*																											
	L																											
	P																											
	PFRAM																											
0xFFFFF80	EXCEPTVECT																											
0xFFFFF8C	RESETVECT																											

7.3.1.2 BANK0

You can check the settings in Project → Properties → C/C++ Build → Settings.

Table 7-8 BANK0 – Setting Tool Tab

Item	Changing Contents	Description																								
Compiler - Source	Add Include path to [Include · File · Directory]	The settings are the same as those of BootLoader.																								
Compiler - Source	Add the definition of processor macro <Setting> Macro definition FLASH_APPL_BANK=0 _DISABLE_REVNO_CHECK REVISION_NUMBER=0x00000100	If set “FLASH_APPL_BANK=0”, the code for BANK0 will be built. If define “_DISABLE_REVNO_CHECK” even the firmware and EEPROM revision No are different, the error will not occur. Define “REVISION_NUMBER” as 1.00																								
Compiler – Optimization	Change optimization level Level 1: Implement a part of the optimization	The optimization level is set to 1 due to prevent some of the code generated by SSC from being built by optimization.																								
Linker – Section	Add RPFRAM section into RAM area < Setting > <table border="1"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr><td>0x00000004</td><td>SU</td></tr> <tr><td></td><td>SI</td></tr> <tr><td></td><td>B_1</td></tr> <tr><td></td><td>R_1</td></tr> <tr><td></td><td>B_2</td></tr> <tr><td></td><td>R_2</td></tr> <tr><td></td><td>B</td></tr> <tr><td></td><td>R</td></tr> <tr><td></td><td>B_8</td></tr> <tr><td></td><td>R_8</td></tr> <tr><td></td><td>RPFRAM</td></tr> </tbody> </table>	Address	Section Name	0x00000004	SU		SI		B_1		R_1		B_2		R_2		B		R		B_8		R_8		RPFRAM	The rewrite code of the code flash memory is added to the RAM area.
Address	Section Name																									
0x00000004	SU																									
	SI																									
	B_1																									
	R_1																									
	B_2																									
	R_2																									
	B																									
	R																									
	B_8																									
	R_8																									
	RPFRAM																									
	Change the starting position of the PResetPRG placed in the ROM area to 0xFFE00000. Added PFRAM section. < Setting > <table border="1"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr><td>0xFFE00000</td><td>PRResetPRG</td></tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>C\$*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM</td></tr> </tbody> </table>	Address	Section Name	0xFFE00000	PRResetPRG		C_1		C_2		C		C_8		C\$*		D*		W*		L		P		PFRAM	The mapping of BANK0 is from 0xFFE00000 to 0xFFFF7FFF. Size is 2016KB. Add code to the ROM area to rewrite the code flash memory.
Address	Section Name																									
0xFFE00000	PRResetPRG																									
	C_1																									
	C_2																									
	C																									
	C_8																									
	C\$*																									
	D*																									
	W*																									
	L																									
	P																									
	PFRAM																									

	<p>Add IDENTIFY section in ROM, set The start position to 0xFFFF7F70.</p> <p>< Setting ></p> <table border="1"> <tr> <td>0xFFFF7F70</td> <td>IDENTIFY</td> </tr> <tr> <td>0xFFFF7F80</td> <td>EXCEPTVECT</td> </tr> <tr> <td>0xFFFF7FFC</td> <td>RESETVECT</td> </tr> </table>	0xFFFF7F70	IDENTIFY	0xFFFF7F80	EXCEPTVECT	0xFFFF7FFC	RESETVECT	<p>The 16 bytes of table data including in firmware version is placed in the IDENTIFY section.</p> <p>The IDENTIFY section and the exception vector table (128 bytes) including reset vector is placed at the end of BANK0.</p>
0xFFFF7F70	IDENTIFY							
0xFFFF7F80	EXCEPTVECT							
0xFFFF7FFC	RESETVECT							
<p>Linker</p> <p>– Section</p> <p>– Symbol file</p>	<p>Add the section to map from ROM to RAM</p> <p>< Setting ></p> <pre>ROM to RAM mapped section D=R D_1=R_1 D_2=R_2 D_8=R_8 PFRAM=RPFRAM</pre>	<p>The sample program performs the code flash memory rewrite in RAM. Therefore, add the setting “PFRAM=RPFRAM” that maps form ROM to RAM.</p>						
<p>Converter</p> <p>– Output</p>	<p>Change the setting to output Motorola S format file.</p> <p>< Setting ></p> <p><input type="checkbox"/> Intel HEX format file (-form=hexadecimal)</p> <p><input checked="" type="checkbox"/> Motorola S format file (-form=stype)</p> <p><input type="checkbox"/> Binary file (-form=binary)</p>	<p>The download file is a Motorola S format file.</p>						

Table 7-9 BANK0 – the other tab

Tab Item	Changing Contents	Description
Build result	<p>Change the output file to ECATFW__B0_RX72.mot</p> <p>< Setting ></p> <p>Artifact Type: <input type="text"/></p> <p>Artifact name: <input type="text" value="ECATFW__B0_RX72M"/></p> <p>Artifact extension: <input type="text" value="mot"/></p> <p>Output prefix: <input type="text"/></p>	<p>The prefix of the download file name is “ECATFW__B0”.</p>
Build · Step	<p>Create a copy of output file as ECATFW__B0_RX72.efw after completed building.</p> <p>< Setting ></p> <p>Post-build steps</p> <p>Command(s):</p> <pre>cmd /c copy /Y ECATFW__B0_RX72M.mot ECATFW__B0_RX72M.efw</pre>	<p>The reason is that the extension of file can be downloaded by TwinCAT is “efw”.</p>

7.3.1.3 BANK1

You can check the settings in [Project] → [Properties] → [C/C++ Build] → [Settings].

Table 7-10 BANK1 – Setting Tool tab

Item	Changing Contents	Description																								
Compiler - Source	Add Include path to [Include · File · Directory]	The settings are the same as those of BootLoader.																								
Compiler - Source	Add the definition of processor macro <Setting> Macro definition <hr/> <u>FLASH_APPL_BANK=1</u> <u>_DISABLE_REVNO_CHECK</u> <u>REVISION_NUMBER=0x00000110</u>	If set "FLASH_APPL_BANK=1", the code for BANK1 will be built. If define "_DISABLE_REVNO_CHECK" even the firmware and EEPROM revision No are different, the error will not occur. Define "REVISION_NUMBER" as 1.10																								
Compiler - Optimization	Change optimization level Level 1: Implement a part of the optimization	The optimization level is set to 1 due to prevent some of the code generated by SSC from being built by optimization.																								
Linker - Section	Add RPFRAM section into RAM area < Setting > <table border="1"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr><td>0x00000004</td><td>SU</td></tr> <tr><td></td><td>SI</td></tr> <tr><td></td><td>B_1</td></tr> <tr><td></td><td>R_1</td></tr> <tr><td></td><td>B_2</td></tr> <tr><td></td><td>R_2</td></tr> <tr><td></td><td>B</td></tr> <tr><td></td><td>R</td></tr> <tr><td></td><td>B_8</td></tr> <tr><td></td><td>R_8</td></tr> <tr><td></td><td>RPFRAM</td></tr> </tbody> </table>	Address	Section Name	0x00000004	SU		SI		B_1		R_1		B_2		R_2		B		R		B_8		R_8		RPFRAM	The rewrite code of the code flash memory is added to the RAM area.
Address	Section Name																									
0x00000004	SU																									
	SI																									
	B_1																									
	R_1																									
	B_2																									
	R_2																									
	B																									
	R																									
	B_8																									
	R_8																									
	RPFRAM																									
	Change the starting position of the PResetPRG placed in the ROM area to 0xFFC00000. Added PFRAM section. < Setting > <table border="1"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr><td>0xFFC00000</td><td>PRresetPRG</td></tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>C\$*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM</td></tr> </tbody> </table>	Address	Section Name	0xFFC00000	PRresetPRG		C_1		C_2		C		C_8		C\$*		D*		W*		L		P		PFRAM	The mapping of BANK1 is from 0xFFC00000 to 0xFFDF7FFF. Size is 2016KB. Add code to the ROM area to rewrite the code flash memory.
Address	Section Name																									
0xFFC00000	PRresetPRG																									
	C_1																									
	C_2																									
	C																									
	C_8																									
	C\$*																									
	D*																									
	W*																									
	L																									
	P																									
	PFRAM																									

	<p>Add IDENTIFY section in ROM, set The start position to 0xFFDF7F70.</p> <p>< Setting ></p> <table border="1"> <tr> <td>0xFFDF7F70</td> <td>IDENTIFY</td> </tr> <tr> <td>0xFFDF7F80</td> <td>EXCEPTVECT</td> </tr> <tr> <td>0xFFDF7FFC</td> <td>RESETVECT</td> </tr> </table>	0xFFDF7F70	IDENTIFY	0xFFDF7F80	EXCEPTVECT	0xFFDF7FFC	RESETVECT	<p>The 16 bytes of table data including in firmware version is placed in the IDENTIFY section.</p> <p>The IDENTIFY section and the exception vector table (128 bytes) including reset vector is placed at the end of BANK1.</p>
0xFFDF7F70	IDENTIFY							
0xFFDF7F80	EXCEPTVECT							
0xFFDF7FFC	RESETVECT							
<p>Linker</p> <p>– Section</p> <p>– Symbol file</p>	<p>Add the section to map from ROM to RAM</p> <p>< Setting ></p> <pre> ROM to RAM mapped section ----- D=R D_1=R_1 D_2=R_2 D_8=R_8 PFRAM=RPFRAM </pre>	<p>The sample program performs the code flash memory rewrite in RAM. Therefore, add the setting “PFRAM=RPFRAM” that maps form ROM to RAM.</p>						
<p>Converter</p> <p>– Output</p>	<p>Change the setting to output Motorola S format file.</p> <p>< Setting ></p> <p><input type="checkbox"/> Intel HEX format file (-form=hexadecimal)</p> <p><input checked="" type="checkbox"/> Motorola S format file (-form=stype)</p> <p><input type="checkbox"/> Binary file (-form=binary)</p>	<p>The download file is a Motorola S format file.</p>						

Table 7-11 BANK1 - the other tab

Tab Item	Changing Contents	Description
Build result	<p>Change the output file to ECATFW__B1_RX72.mot.</p> <p>< Setting ></p> <p>Artifact Type: <input type="text"/></p> <p>Artifact name: <input type="text" value="ECATFW__B1_RX72M"/></p> <p>Artifact extension: <input type="text" value="mot"/></p> <p>Output prefix: <input type="text"/></p>	<p>The prefix of the download file name is “ECATFW__B1”.</p>
Build · Step	<p>Create a copy of output file as ECATFW__B1_RX72.efw after completed building.</p> <p>< Setting ></p> <pre> Post-build steps Command(s): cmd /c copy /Y ECATFW__B0_RX72M.mot ECATFW__B0_RX72M.efw </pre>	<p>The reason is that the extension of file can be downloaded by TwinCAT is “efw”.</p>

7.3.2 Build configuration of Dual mode

This chapter describes the build configuration of project on using dual mode.

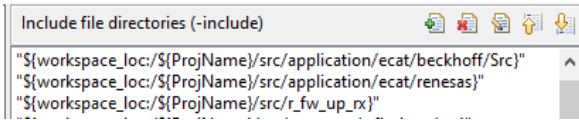
Table 7-12 Build configuration of dual mode

Configuration name	Description
Hardware Debug	Generate a load module with debug information of EtherCAT slave program. There are no files to exclude from the build.
Download	Build download EtherCAT slave program. Result of building is Motorola S format file. There are no files to exclude from the build.

7.3.2.1 HardwareDebug

You can check the settings in [Project] → [Properties] → [C/C++ Build] → [Settings].

Table 7-13 HardwareDebug – Setting Tool tab

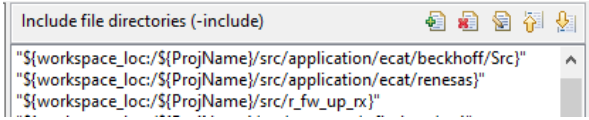
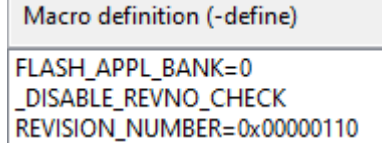
Item	Changing Contents	Description																								
Compiler - Source	Add Include path to [Include · File · Directory]	In each FIT module, please add the required include path for the setting. The code-generated folders are automatically configured only if you use the FIT Configurator to include each FIT module. About program files that you do not want to generate, you must manually add the include path. In this project, the following three items have been added. 																								
Compiler - Source	Add the definition of processor macro. <Setting> <table border="1" data-bbox="363 965 727 1122"> <tr> <td>Macro definition</td> </tr> <tr> <td>FLASH_APPL_BANK=0</td> </tr> <tr> <td>_DISABLE_REVNO_CHECK</td> </tr> <tr> <td>REVISION_NUMBER=0x00000100</td> </tr> </table>	Macro definition	FLASH_APPL_BANK=0	_DISABLE_REVNO_CHECK	REVISION_NUMBER=0x00000100	If set “FLASH_APPL_BANK=0”, the code for BANK0 will be built. If define “_DISABLE_REVNO_CHECK” even the firmware and EEPROM revision No are different, the error will not occur. Define “REVISION_NUMBER” as 1.00																				
Macro definition																										
FLASH_APPL_BANK=0																										
_DISABLE_REVNO_CHECK																										
REVISION_NUMBER=0x00000100																										
Compiler – Optimization	Change optimization level. Level 1: Implement a part of the optimization	The optimization level is set to 1 due to prevent some of the code generated by SSC from being built by optimization.																								
Linker – Section	Add RPFRAM2 section into RAM area. < Setting > <table border="1" data-bbox="363 1368 831 1823"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr> <td>0x00000004</td> <td>SU</td> </tr> <tr> <td></td> <td>SI</td> </tr> <tr> <td></td> <td>B_1</td> </tr> <tr> <td></td> <td>R_1</td> </tr> <tr> <td></td> <td>B_2</td> </tr> <tr> <td></td> <td>R_2</td> </tr> <tr> <td></td> <td>B</td> </tr> <tr> <td></td> <td>R</td> </tr> <tr> <td></td> <td>B_8</td> </tr> <tr> <td></td> <td>R_8</td> </tr> <tr> <td></td> <td>RPFRAM2</td> </tr> </tbody> </table>	Address	Section Name	0x00000004	SU		SI		B_1		R_1		B_2		R_2		B		R		B_8		R_8		RPFRAM2	Add code to switch bank in RAM area.
Address	Section Name																									
0x00000004	SU																									
	SI																									
	B_1																									
	R_1																									
	B_2																									
	R_2																									
	B																									
	R																									
	B_8																									
	R_8																									
	RPFRAM2																									

	<p>Changed the starting position of PResetPRG to 0xFFE08000 in the ROM area.</p> <p>Added PFRAM2 section.</p> <p>< Setting ></p> <table border="1" data-bbox="363 360 798 734"> <tr><td>0xFFE08000</td><td>PResetPRG</td></tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>C\$*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM2</td></tr> </table>	0xFFE08000	PResetPRG		C_1		C_2		C		C_8		C\$*		D*		W*		L		P		PFRAM2	<p>The mapping for BANK0 is from 0xFFE00000 to 0xFFFFFFFF, but the starting position of PResetPRG is set to 0xFFE08000.</p> <p>The size of BANK0 is 2048 KB.</p> <p>The code for rewriting the code flash memory is added to the ROM area.</p> <p>The 0xFFE00000~0xFFE08000 area of this sample program is reserved for Store Parameters. For more information about Store Parameters, see Section 9.2.3.</p>
0xFFE08000	PResetPRG																							
	C_1																							
	C_2																							
	C																							
	C_8																							
	C\$*																							
	D*																							
	W*																							
	L																							
	P																							
	PFRAM2																							
	<p>Add IDENTIFY section in ROM, set the start position at 0xFFFFFFFF70.</p> <p>< Setting ></p> <table border="1" data-bbox="363 875 783 994"> <tr><td>0xFFFFFFFF70</td><td>IDENTIFY</td></tr> <tr><td>0xFFFFFFFF80</td><td>EXCEPTVECT</td></tr> <tr><td>0xFFFFFFFFFC</td><td>RESETVECT</td></tr> </table>	0xFFFFFFFF70	IDENTIFY	0xFFFFFFFF80	EXCEPTVECT	0xFFFFFFFFFC	RESETVECT	<p>The 16 bytes of table data including in firmware version is placed in the IDENTIFY section.</p> <p>The IDENTIFY section and the exception vector table (128 bytes) including reset vector is placed at the end of BANK0.</p>																
0xFFFFFFFF70	IDENTIFY																							
0xFFFFFFFF80	EXCEPTVECT																							
0xFFFFFFFFFC	RESETVECT																							
<p>Linker</p> <ul style="list-style-type: none"> - Section - Symbol file 	<p>Add the section to map from ROM to RAM</p> <p>< Setting ></p> <p><u>ROM to RAM mapped section</u></p> <pre>D=R D_1=R_1 D_2=R_2 D_8=R_8 PFRAM2=RPFRAM2</pre>	<p>The code to switch bank is executed in RAM.</p> <p>Therefore, add the setting that maps from ROM to RAM.</p>																						

7.3.2.2 Download

You can check the settings in [Project] → [Properties] → [C/C++ Build] → [Settings].

Table 7-14 Download – Setting Tool tab

Item	Changing Contents	Description																								
Compiler - Source	Add Include path to [Include · File · Directory]	In each FIT module, please add the required include path for the setting. The code-generated folders are automatically configured only if you use the FIT Configurator to include each FIT module. About program files that you do not want to generate, you must manually add the include path. In this project, the following three items have been added. 																								
Compiler - Source	Add the definition of processor macro < Setting > 	If set “FLASH_APPL_BANK=0”, the code for BANK0 will be built. If define “_DISABLE_REVNO_CHECK” even the firmware and EEPROM revision No are different, the error will not occur. Define “REVISION_NUMBER” as 1.10																								
Compiler – Optimization	Change optimization level Level 1: Implement a part of the optimization.	The optimization level is set to 1 due to prevent some of the code generated by SSC from being built by optimization.																								
Linker – Section	Add RPPFRAM2 section into RAM area < Setting > <table border="1" data-bbox="359 1377 805 1814"> <thead> <tr> <th>Address</th> <th>Section Name</th> </tr> </thead> <tbody> <tr> <td>0x00000004</td> <td>SU</td> </tr> <tr> <td></td> <td>SI</td> </tr> <tr> <td></td> <td>B_1</td> </tr> <tr> <td></td> <td>R_1</td> </tr> <tr> <td></td> <td>B_2</td> </tr> <tr> <td></td> <td>R_2</td> </tr> <tr> <td></td> <td>B</td> </tr> <tr> <td></td> <td>R</td> </tr> <tr> <td></td> <td>B_8</td> </tr> <tr> <td></td> <td>R_8</td> </tr> <tr> <td></td> <td>RPPFRAM2</td> </tr> </tbody> </table>	Address	Section Name	0x00000004	SU		SI		B_1		R_1		B_2		R_2		B		R		B_8		R_8		RPPFRAM2	Add the rewrite code of code flash memory in RAM area.
Address	Section Name																									
0x00000004	SU																									
	SI																									
	B_1																									
	R_1																									
	B_2																									
	R_2																									
	B																									
	R																									
	B_8																									
	R_8																									
	RPPFRAM2																									

	<p>Changed the starting position of PResetPRG to 0xFFE08000 in the ROM area.</p> <p>Added PFRAM2 section.</p> <p>< Setting ></p> <table border="1" data-bbox="363 376 799 748"> <tr><td>0xFFE08000</td><td>PRResetPRG</td></tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>C\$*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM2</td></tr> </table>	0xFFE08000	PRResetPRG		C_1		C_2		C		C_8		C\$*		D*		W*		L		P		PFRAM2	<p>The mapping for BANK0 is from 0xFFE00000 to 0xFFFFFFFF, but the starting position of PResetPRG is set to 0xFFE08000.</p> <p>The size of BANK0 is 2048 KB.</p> <p>Code for rewriting the code flash memory is added to the ROM area.</p> <p>The 0xFFE00000~0xFFE08000 area of this sample program is reserved for Store Parameters. For more information about Store Parameters, see Section 9.2.3.</p>
0xFFE08000	PRResetPRG																							
	C_1																							
	C_2																							
	C																							
	C_8																							
	C\$*																							
	D*																							
	W*																							
	L																							
	P																							
	PFRAM2																							
	<p>Add IDENTIFY section in ROM, set the start position at 0xFFFFFFFF70.</p> <p>< Setting ></p> <table border="1" data-bbox="363 909 746 1014"> <tr><td>0xFFFFFFFF70</td><td>IDENTIFY</td></tr> <tr><td>0xFFFFFFFF80</td><td>EXCEPTVECT</td></tr> <tr><td>0xFFFFFFFFFC</td><td>RESETVECT</td></tr> </table>	0xFFFFFFFF70	IDENTIFY	0xFFFFFFFF80	EXCEPTVECT	0xFFFFFFFFFC	RESETVECT	<p>The 16 bytes of table data including in firmware version is placed in the IDENTIFY section.</p> <p>The IDENTIFY section and the exception vector table (128 bytes) including reset vector is placed at the end of BANK0.</p>																
0xFFFFFFFF70	IDENTIFY																							
0xFFFFFFFF80	EXCEPTVECT																							
0xFFFFFFFFFC	RESETVECT																							
<p>Linker</p> <p>– Section</p> <p>– Symbol file</p>	<p>Add the section to map from ROM to RAM</p> <p>< Setting ></p> <p><u>ROM to RAM mapped section</u></p> <p>D=R D_1=R_1 D_2=R_2 D_8=R_8 PFRAM2=RPFRAM2</p>	<p>The code to switch bank is executed in RAM.</p> <p>Therefore, add the setting to map form ROM to RAM.</p>																						
<p>Converter</p> <p>– Output</p>	<p>Change the output setting for Motorola S format file.</p> <p>< Setting ></p> <p><input type="checkbox"/> Intel HEX format file (-form=hexadecimal)</p> <p><input checked="" type="checkbox"/> Motorola S format file (-form=stype)</p> <p><input type="checkbox"/> Binary file (-form=binary)</p>	<p>The download file is a Motorola S format file.</p>																						

Table 7-15 Download - the other tab

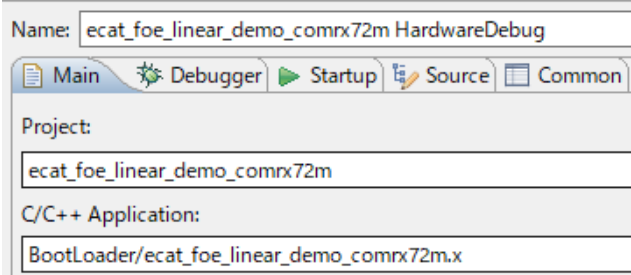
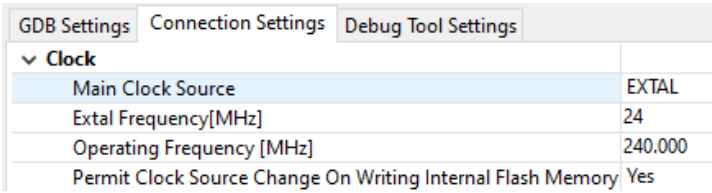

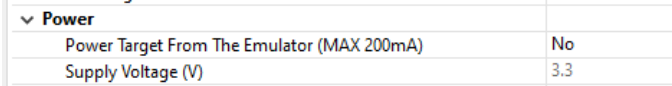
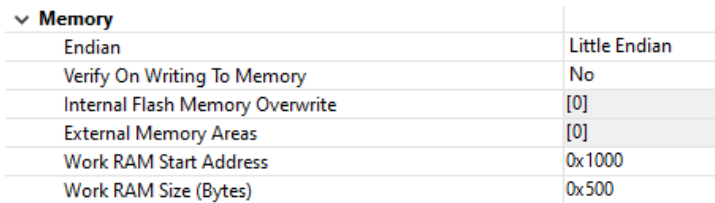
Tab Item	Changing Contents	Description
Build result	Change the output file to ECATFW__B1_RX72.mot. < Setting > Artifact Type: <input type="text"/> Artifact name: <input type="text" value="ECATFW__B1_RX72M"/> Artifact extension: <input type="text" value="mot"/> Output prefix: <input type="text"/>	The prefix of the download file name is "ECATFW__B1".
Build Steps	Create a copy of output file as ECATFW__B1_RX72.efw after completed building. < Setting > Post-build steps Command(s): <input type="text" value="cmd /c copy /Y ECATFW__B1_RX72M.mot ECATFW__B1_RX72M.efw"/>	The reason is that the extension of file can be downloaded by TwinCAT is "efw".

7.4 Debug configuration

7.4.1 Debug configuration of Linear mode

You can check the settings in [Run] → [the debug configuration] → [ecat_foe_linear_demo_comrx72m].

Table 7-16 Debug configuration of linear mode

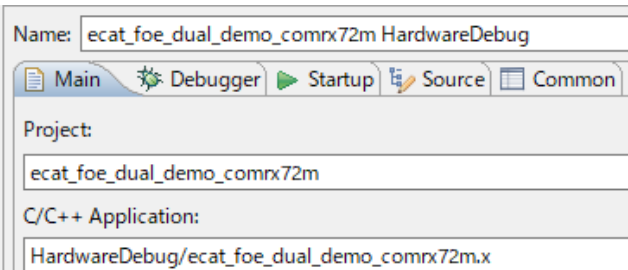
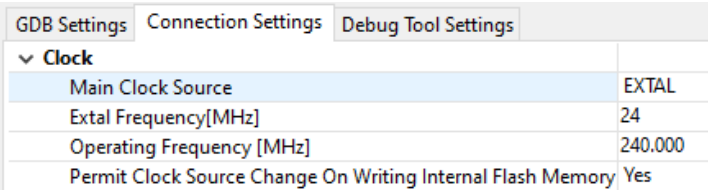

Tab Item	Changing Contents	Description
main	Change C/C++ application to boot loader. < Setting > 	
Debugger – Connection Settings – Clock	Set the main clock source to EXTAL, the EXTAL frequency to 24 MHz, and the operating frequency to 240 MHz < Setting > 	
Debugger – Connection Settings – Connection with Target Board	Set the connection type to "JTAG". In case of using a CPU card, set it to "FINE". < configuration example > 	
Debugger – Connection Settings – Power	Change the setting to not supply power from the emulator. < configuration example > 	
Debugger – Setting Tool Debug	In all blocks change the overwrite of the internal flash memory. < Setting > 	Click on the button at the right of “ Overwrite internal flash memory ”, click on [Deselect all] → [OK], than all blocks will be deleted and overwritten, and [0] will be displayed.

<p>Startup</p>	<p>Set the image to write to code flash along with boot loader.</p> <p>< Setting > Debug BANK0 and boot loader</p> <div style="border: 1px solid gray; padding: 5px;"> <p>Load image and symbols</p> <table border="1"> <thead> <tr> <th>Filename</th> <th>Load type</th> <th>Offset (hex)</th> <th>On connect</th> </tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Program Binary [ecat_f...</td> <td>Image and Symbols</td> <td></td> <td>Yes</td> </tr> <tr> <td><input checked="" type="checkbox"/> ECATFW_B0_RX72M.x ...</td> <td>Image and Symbols</td> <td>0</td> <td>Yes</td> </tr> <tr> <td><input type="checkbox"/> ECATFW_B1_RX72M.x ...</td> <td>Image and Symbols</td> <td>0</td> <td>Yes</td> </tr> </tbody> </table> </div> <p>< Setting > Debug BANK1 and boot loader</p> <div style="border: 1px solid gray; padding: 5px;"> <p>Load image and symbols</p> <table border="1"> <thead> <tr> <th>Filename</th> <th>Load type</th> <th>Offset (hex)</th> <th>On connect</th> </tr> </thead> <tbody> <tr> <td><input checked="" type="checkbox"/> Program Binary [ecat_f...</td> <td>Image and Symbols</td> <td></td> <td>Yes</td> </tr> <tr> <td><input type="checkbox"/> ECATFW_B0_RX72M.x ...</td> <td>Image and Symbols</td> <td>0</td> <td>Yes</td> </tr> <tr> <td><input checked="" type="checkbox"/> ECATFW_B1_RX72M.x ...</td> <td>Image and Symbols</td> <td>0</td> <td>Yes</td> </tr> </tbody> </table> </div>	Filename	Load type	Offset (hex)	On connect	<input checked="" type="checkbox"/> Program Binary [ecat_f...	Image and Symbols		Yes	<input checked="" type="checkbox"/> ECATFW_B0_RX72M.x ...	Image and Symbols	0	Yes	<input type="checkbox"/> ECATFW_B1_RX72M.x ...	Image and Symbols	0	Yes	Filename	Load type	Offset (hex)	On connect	<input checked="" type="checkbox"/> Program Binary [ecat_f...	Image and Symbols		Yes	<input type="checkbox"/> ECATFW_B0_RX72M.x ...	Image and Symbols	0	Yes	<input checked="" type="checkbox"/> ECATFW_B1_RX72M.x ...	Image and Symbols	0	Yes	<p>Set the setting to load the images and symbols of the bank you want to debug.</p> <p>Specify the download module from [Add] → [search project].</p>
Filename	Load type	Offset (hex)	On connect																															
<input checked="" type="checkbox"/> Program Binary [ecat_f...	Image and Symbols		Yes																															
<input checked="" type="checkbox"/> ECATFW_B0_RX72M.x ...	Image and Symbols	0	Yes																															
<input type="checkbox"/> ECATFW_B1_RX72M.x ...	Image and Symbols	0	Yes																															
Filename	Load type	Offset (hex)	On connect																															
<input checked="" type="checkbox"/> Program Binary [ecat_f...	Image and Symbols		Yes																															
<input type="checkbox"/> ECATFW_B0_RX72M.x ...	Image and Symbols	0	Yes																															
<input checked="" type="checkbox"/> ECATFW_B1_RX72M.x ...	Image and Symbols	0	Yes																															

7.4.2 Debug configuration of Dual mode

You can check the settings in [Run] → [the debug configuration] → [ecat_foe_linear_demo_comrx72m].

Table 7-17 Debug configuration of Dual mode

Tab Item	Changing Contents	Description
<p>main</p>	<p>Set C/C++ application.</p> <p>< Setting ></p> 	
<p>Debugger – Connection Settings – Clock</p>	<p>Set the main clock source to EXTAL, the EXTAL frequency to 24 MHz, and the operating frequency to 240 MHz.</p> <p>< Setting ></p> 	
<p>Debugger – Connection Settings – Connection with Target Board</p>	<p>Set the connection type to "JTAG".</p> <p><u>In case of using a CPU card, set it to "FINE".</u></p> <p>< configuration example ></p> 	

<p>Debugger – Connection Settings – Power</p>	<p>Change the setting to not supply power from the emulator. < configuration example ></p> <table border="1" data-bbox="384 264 1054 353"> <tr> <td colspan="2">▼ Power</td> </tr> <tr> <td>Power Target From The Emulator (MAX 200mA)</td> <td>No</td> </tr> <tr> <td>Supply Voltage (V)</td> <td>3.3</td> </tr> </table>	▼ Power		Power Target From The Emulator (MAX 200mA)	No	Supply Voltage (V)	3.3									
▼ Power																
Power Target From The Emulator (MAX 200mA)	No															
Supply Voltage (V)	3.3															
<p>Debugger – Connection Settings – Communication Mode</p>	<p>[CPU operation mode] – [Change startup bank] is set to "No" to start the user program of BANK0.</p>	<p>When the debugger is starting, the BANKSWP[2:0] bits are set to "111b".</p>														
<p>Debugger – Debug Tool Setting</p>	<p>In all blocks change the overwrite of the internal flash memory. < Setting ></p> <table border="1" data-bbox="384 696 1098 898"> <tr> <td colspan="2">▼ Memory</td> </tr> <tr> <td>Endian</td> <td>Little Endian</td> </tr> <tr> <td>Verify On Writing To Memory</td> <td>No</td> </tr> <tr> <td>Internal Flash Memory Overwrite</td> <td>[0]</td> </tr> <tr> <td>External Memory Areas</td> <td>[0]</td> </tr> <tr> <td>Work RAM Start Address</td> <td>0x1000</td> </tr> <tr> <td>Work RAM Size (Bytes)</td> <td>0x500</td> </tr> </table>	▼ Memory		Endian	Little Endian	Verify On Writing To Memory	No	Internal Flash Memory Overwrite	[0]	External Memory Areas	[0]	Work RAM Start Address	0x1000	Work RAM Size (Bytes)	0x500	<p>Click on the button at the right of " Overwrite internal flash memory ", click on [Deselect all] → [OK], than all blocks will be deleted and overwritten, and [0] will be displayed.</p>
▼ Memory																
Endian	Little Endian															
Verify On Writing To Memory	No															
Internal Flash Memory Overwrite	[0]															
External Memory Areas	[0]															
Work RAM Start Address	0x1000															
Work RAM Size (Bytes)	0x500															

8. Sample program overview

8.1 File configuration

Table 8-1 shows the file structure under the "ecat_linear_demo_cpurx72m" folder.

Table 8-1 The file structure of this sample program

Folder	Sub folder	File	Content
project	-	.cproject	CPROJECT file
		.project	PROJECT file
		ecat_linear_demo_cpurx72m HardwareDebug.launch	Configuration file for debugging
		ecat_linear_demo_cpurx72m.scfg	Smart Configuration file
		ecat_linear_demo_cpurx72m_board.xml	Pin setting save file
utilities	esi	Renesas EtherCAT RX72M.xml	ESI file
	patch	apply_patch.bat	Batch file to apply the patch
		RX72M.patch	Patch file for this sample program
	ssc_config	RX72M EtherCAT.esp	SSC Tool project file
		RX72M_EtherCAT_config.xml	SSC Tool configuration file

The "project" folder also contains the "src" folder that contains program files.

Table 8-2 shows the folder structure under the "src" folder and the details of each file.

Table 8-2 The folder structure under the "src" folder

Folder	Content	
application\ecat\beckhoff	Folder where programs generated by SSC and modified by patch are stored	
application\ecat\renesas	Folder where the programs SSC doesn't generate for EtherCAT are stored	
	File	Content
	cia402sample.c	CiA402 transition function definition file
	cia402sample.h	CiA402 transition function declaration file
	foesample.c	Function definition file for FoE protocol
	foesample.h	File declaring function for FoE protocol and defining object 0x5000
	iosample.c	Function definition file for checking I/O operation
	iosample.h	Function declaration file for checking I/O operation
	semisample.c	Function definition file for Store Parameters
	semisample.h	File declaring function for Store Parameters and defining CDP-related object

Folder	Content	
demo	Folder where programs including main and boot loader function are stored	
	File	Content
	bt_main.c	Boot loader program (Using only linear mode)
	main.c	Main function of this sample program
	siorw.c	SCI related source programs
r_fw_up_rx	Folder where programs for firmware update are stored	
	File	Content
	r_fw_up_rx.c	Firmware update source file
	r_fw_up_rx_if.h	Firmware update interface file
	r_fw_up_rx_private.h	Firmware update header file
	r_fw_up_buf.c	Source file handling buffer for firmware date
	r_fw_up_buf.h	Header file handling buffer for firmware date
	r_fw_up_bank.c	Source file handling information about bank.
smc_gen	Folder where programs about FIT module are stored	

Refer to Application Note ET9300 (EtherCAT Slave Stack Code) for the details of program files that are stored in application\ecat\beckhoff folder.

Refer to the documents of each FIT module for the details of the files about FIT module that are stored in smc_gen folder.

8.2 Modifications of Slave Stack Code

This sample programs modify programs generated by SSC for EtherCAT communication by using patch.

Table 8-3 shows the overview of modifications

Table 8-3 the overview of modifications of source code generated by SSC

File	Overview of modifications
bootmode.c	Constant array placed in the IDENTIFY section was added. The definition of the function for boot loader was added.
bootmode.h	The declaration of the function for boot loader was added.
cia402appl.c	The entry part of object dictionary of CiA402_Init function was modified. CiA402 state transition function was added in CiA402 application function. CiA402_LocalError and CiA402_DummyMotionControl function definition was deleted. Process data I/O function was modified for adjusting to PDO entry. I/O and CiA402 application function were added in APPL_Application function.
cia402appl.h	Object dictionary definition was modified.
coeappl.c	Object dictionary definition was modified.
coeappl.h	Conditional compilation was added.
ecatappl.c	MainInit function and Mainloop function were modified.
ecatcoe.h	The alignment of the structures was changed to 1.
ecatstv.c	AL event was modified for preventing sync0 and sync1 event from occurring. The update function of firmware version of SII and the reboot function after firmware update were added.
mailbox.h	The alignment of the structures was changed to 1.
objdef.c	Conditional compilation was added.
sdoserv.h	The alignment of the structures was changed to 1.

For the details of modifications, refer to RX72M.patch file.

8.3 CiA402 Drive Profile overview

The CiA402 drive profile is a device profile for driving motors and motion control and mainly defines functional operations for servo drives, sine-wave inverters and stepping motor controllers.

In this profile, the multiple operation modes and corresponding parameters are defined as an object dictionary.

Also, Finite State Automaton (FSA) to define the internal and external behavior in every state is included.

When changing the state, the result after transition is reflected in the status word object that shows the current state by specifying the state through the control word object.

The control word and various command values (such as speed) are assigned to RxPDO, and the status word and various real values (such as position) are assigned to TxPDO.

Please see the contents of the CiA402 standard for more details.

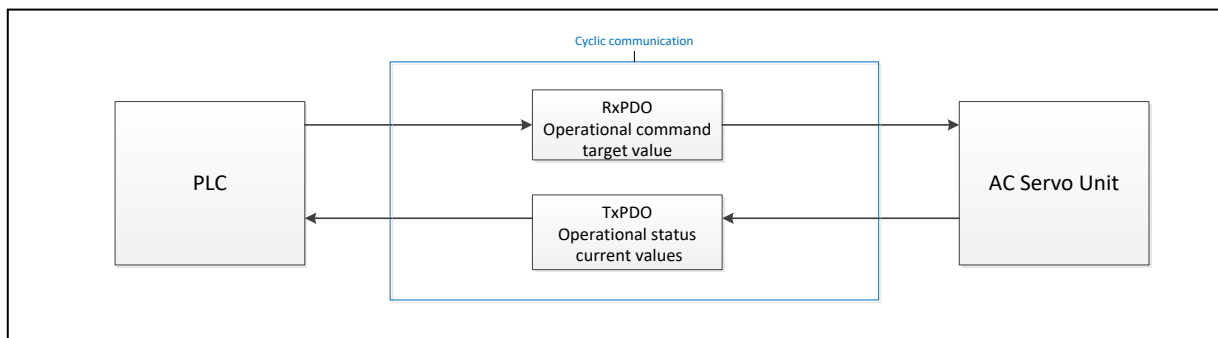


Figure 8-1 CiA402 Communication Flow

8.3.1 Operation mode

In the application note, Table 8-4 shows the operation modes supported by this application note in the operation modes defined in the CiA402 standard.

Table 8-4 the list of the operation modes supported

Operation Mode	Support
Profile position mode	×
Velocity mode(frequency converter)	×
Profile velocity mode	×
Profile torque mode	×
Homing mode	×
Interpolated position mode	×
Cyclic synchronous position mode	○
Cyclic synchronous velocity mode	○
Cyclic synchronous torque mode	×
Cyclic synchronous torque mode with commutation angle	×
Manufacturer specific mode	×

8.3.2 State Transition

In this application note, the following is supported as FSA defined in the CiA402 standard.

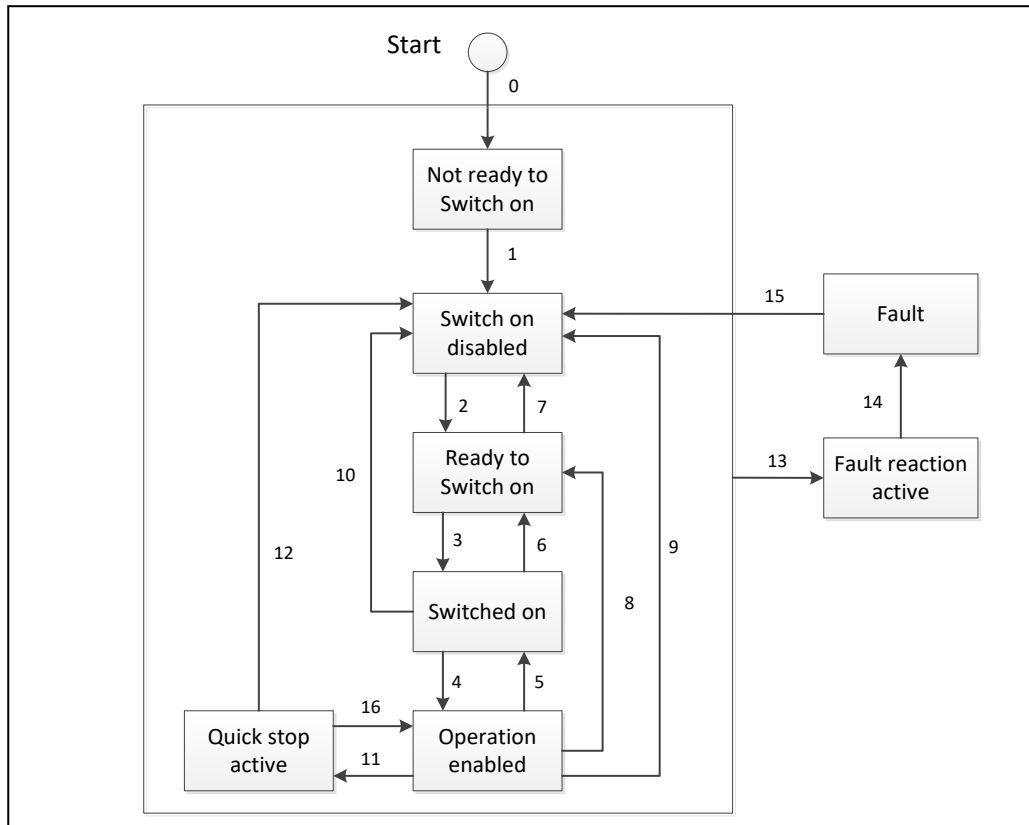


Figure 8-2 CiA402 State Transition Diagram

8.3.3 State transition function

Table 8-5 shows the list of CiA402 state transition function.

CiA402_StateTransition function and CiA402_LocalError function correspond each state transition number of CiA402 FSA shown in figure 8-1, when the state transition occurs the corresponded function will be called.

In case of using this sample program for motor control, etc., describe the process executed when the state transition occurs in each transition function.

Table 8-5 the list of CiA402 protocol - stack I/F function

Function name	Overview
CiA402_StateTransition1	The function called when the state transition 1 occurs.
CiA402_StateTransition2	The function called when the state transition 2 occurs.
CiA402_StateTransition3	The function called when the state transition 3 occurs.
CiA402_StateTransition4	The function called when the state transition 4 occurs.
CiA402_StateTransition5	The function called when the state transition 5 occurs.
CiA402_StateTransition6	The function called when the state transition 6 occurs.
CiA402_StateTransition7	The function called when the state transition 7 occurs.
CiA402_StateTransition8	The function called when the state transition 8 occurs.
CiA402_StateTransition9	The function called when the state transition 9 occurs.
CiA402_StateTransition10	The function called when the state transition 10 occurs.
CiA402_StateTransition11	The function called when the state transition 11 occurs.
CiA402_StateTransition12	The function called when the state transition 12 occurs.
CiA402_LocalError	The function called when the state transition 13 occurs.
CiA402_StateTransition14	The function called when the state transition 14 occurs.
CiA402_StateTransition15	The function called when the state transition 15 occurs.
CiA402_StateTransition16	The function called when the state transition 16 occurs.
APPL_MOTOR_MotionControl_Main	The function called when the state is "Operation enabled". Describe the process per the operation mode.

About the details of the functions shown in table 8-5, refer to [cia402sample.c](#).

8.4 Firmware update overview

8.4.1 About bank numbers

Sample program is stored in code flash memory and can be updated while the program is running.

Sample program supports two banks, one for executing the user program and one for writing the update program.

In this application note, the bank or BANK number is fixed because it is shared between the linear mode and dual mode.

In dual mode, the start-up bank switching bit(BANKSEL. Note that the numbers are not swapped by the value of BANKSWP[2:0]).

From the one close to the reset vector(FFFF FFFCH-FFFF FFFFH), it is (0 to 1)

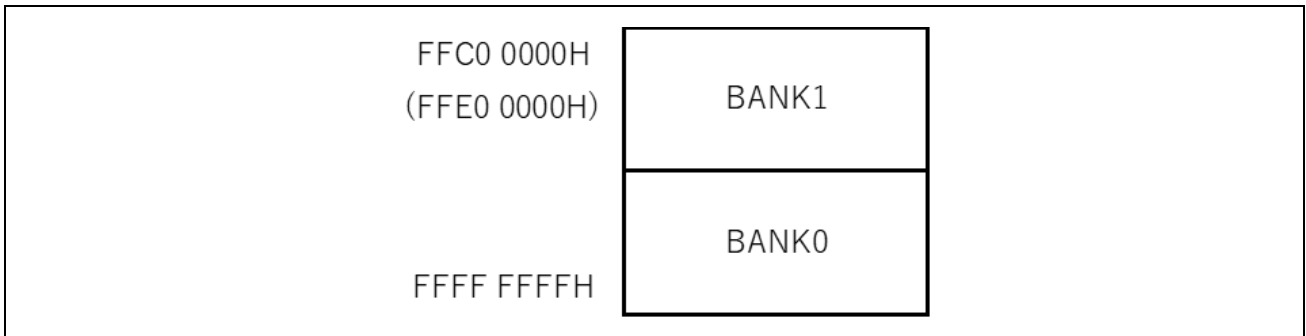


Figure 8-3 Bank number

8.4.2 Linear mode and dual mode comparison

This application note supports both linear mode and dual mode, but there are differences and limitations of functions depending on the mode.

The following is a summary, use it as a reference when choosing a mode.

Table 8-6 Comparing the features of the sample program

Item	Linear mode	Dual mode
Switching user program at startup	Switching which depend on Bootloader program	Switching which depend on dual bank function of hardware
Code flash block configuration	The configurations are different for two banks of 8Kbyte and 32Kbyte	The configuration of two banks is same
Trusted Memory Target area	Blocks 8, 9	Blocks 8, 9 and blocks 78, 79
User program size can be used in one blank	Excluding capacity for 32KB that allocated to boot loader from 1/2 of the installed code flash memory capacity	Entire of 1/2 of the installed code flash memory capacity
Reboot when EtherCAT link is broken ^{**}	without broken link	With broken link (for using software reset)
Operation of update firmware	For two banks case, user need to determine which one is available for writing. Then download the appropriate file	User can download the download file without being aware of the banks

^{**}When reboot is occurred, it is possible to reconnect even though EtherCAT link is broken

8.4.3 Overview of linear mode operation

Linear mode uses code flash in three areas.

Table 8-7 Linear mode code flash area segment

Defined	Features
BANK1	Area to store user program : BANK1 Can be rewritten while running a user program on BANK0
BANK0	Area to store user program : BANK0 Can be rewritten while running a user program on BANK1
Boot Loader	Run the user program by selecting and branching the new BANK user program by comparing Rev No. stored in BANK0 and BANK1 at startup. Not included in user-programmed rewrites

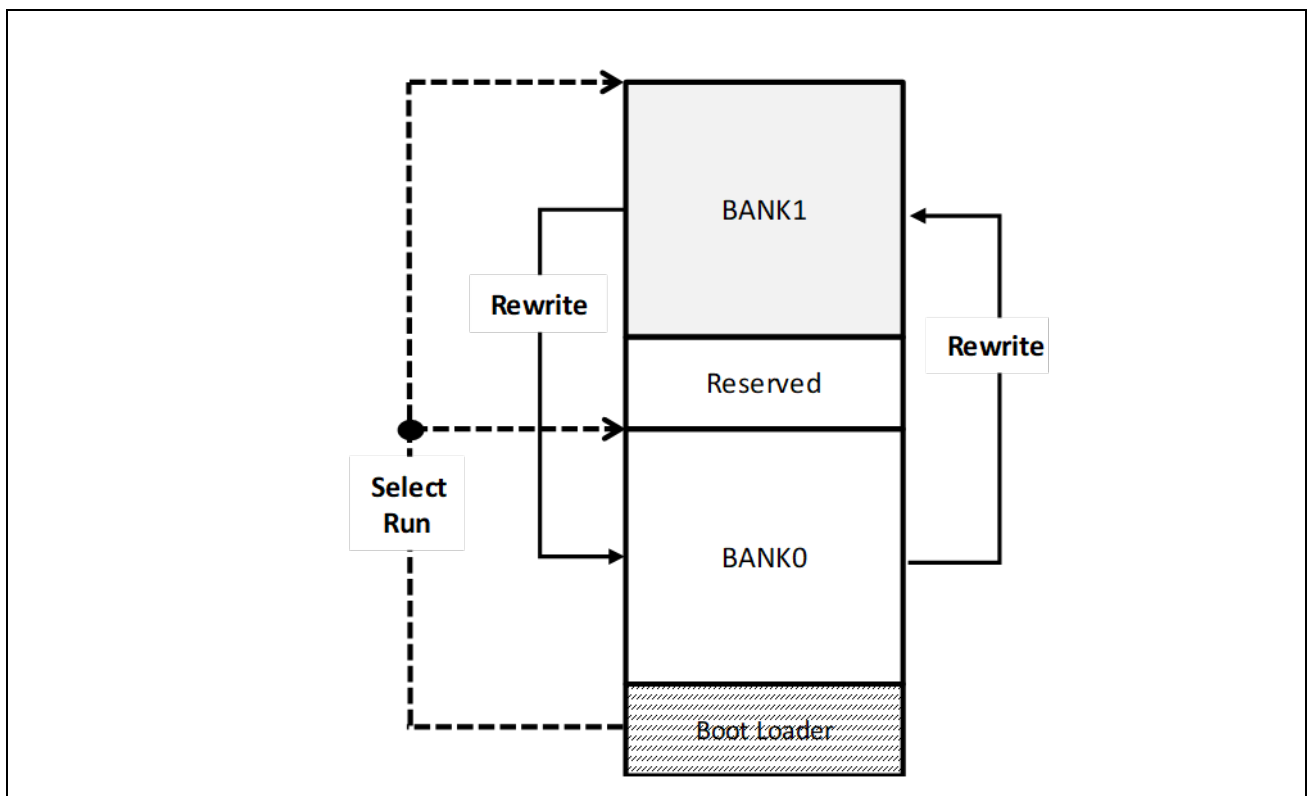


Figure 8-4 Linear mode code flash use image

The relationship between the address and capacity of each region and the block No belonging to each region is shown in the table below.

Table 8-8 Address range and capacity of each area and block No (in case of linear 4MB product)

Defined	First address	Last address	Capacity	Block No.
BANK1	FFC0_0000H	FFDF_7FFFH	2016KB	133~71 (32KB)
Reserved	FFDF_8000H	FFDF_FFFFH	32KB	70 (32KB)
BANK0	FFE0_0000H	FFFF_7FFFH	2016KB	69~8(32KB) 7~4(8KB)
Boot Loader	FFFF_8000H	FFFF_FFFFH	32KB	3~0(8KB)

Table 8-9 Address range and capacity of each area and block No (in case of linear 2MB product)

Defined	First address	Last address	Capacity	Block No.
BANK1	FFE0_0000H	FFEF_7FFFH	992KB	69~39(32KB)
Reserved	FFEF_8000H	FFEF_FFFFH	32KB	38(32KB)
BANK0	FFF0_0000H	FFFF_7FFFH	992KB	37~8 (32KB) 7~4(8KB)
Boot Loader	FFFF_8000H	FFFF_FFFFH	32KB	3~0(8KB)

Here is a memory block diagram.

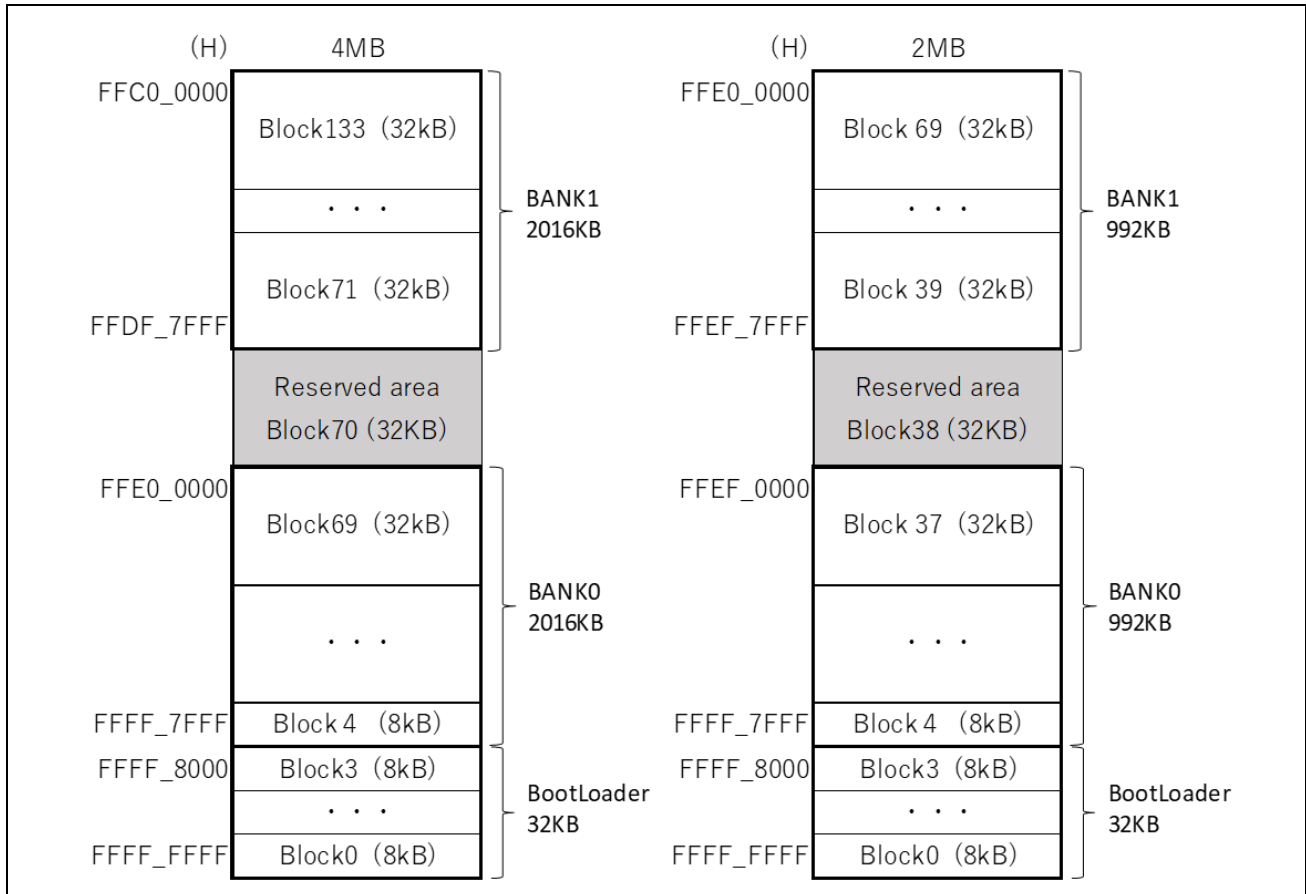


Figure 8-5 Block Assignments in Linear Mode

8.4.4 Overview of dual mode operation

This section describes the dual mode operation by using the sequence of rewriting a user program from Rev 1.0 to Rev 1.1 and restarting it as an example.

- (1) After booting, the Rev1.0 user program stored in the second 2 MB of the code flash area starts. At this time, the value of the startup bank switching bits (BANKSEL.BANKSWP[2:0]) is 111b.
- (2) While the Rev1.0 user program is running, erase the first 2MB and rewrite to the Rev1.1 user program.
- (3) After flipping the startup bank switching bit (BANKSEL.BANKSWP[2:0]=000b), execute a software reset and restart.
- (4) Rev1.1 is replaced by 2MB in the latter half and Rev1.0 is replaced by 2MB in the first half by the startup bank selection function. Rev1.1 user program starts.

Updates from Rev1.1 to Rev1.2 are a similar sequence.

Therefore, dual mode firmware update has the following features.

- Rewriting the code flash is always for the first half 2MB (1MB)
- Banks will be swapped after rebooting, so rewrite with the code that runs in the second half 2MB (1MB)

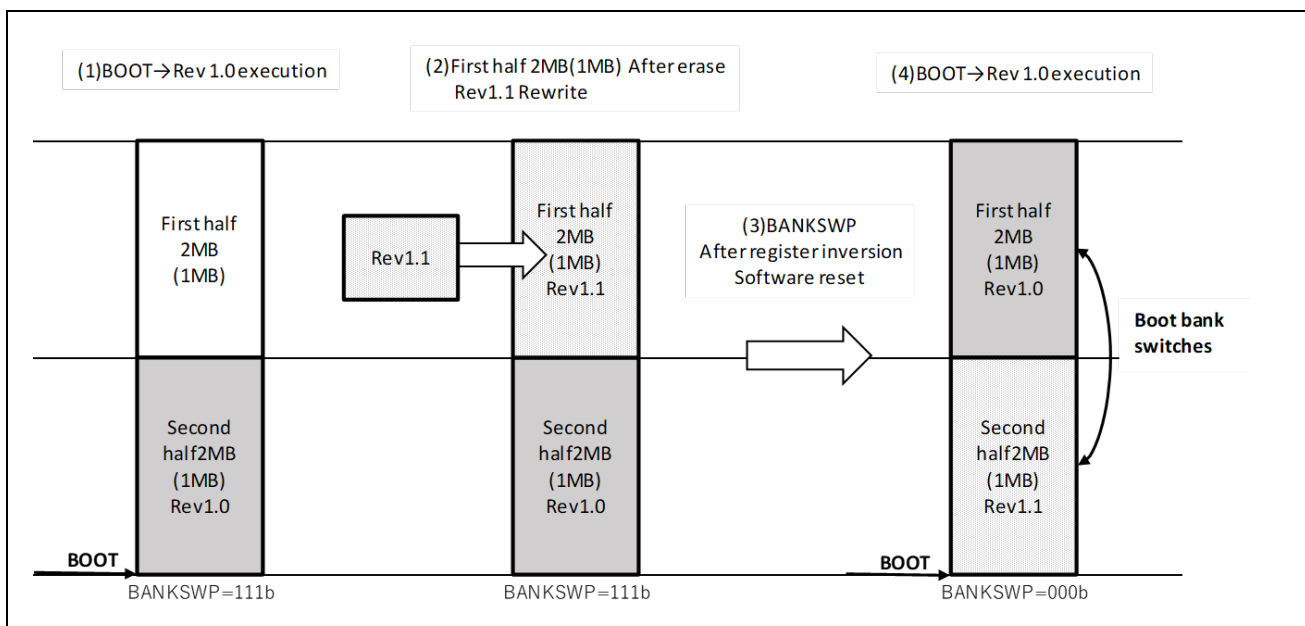


Figure 8-6 Dual-mode sequence of operations

As described in "8.4.1 About bank Numbers", in this application note, the first half 2MB (1MB) is BANK1 and the second half 2MB (1MB) is BANK0.

The table below shows the relationship between the address and capacity of each area and the block numbers belonging to each area.

Table 8-10 Address range and capacity for each area and block No (In case of 4MB product)

Defined	First address	Last address	Capacity	Block No.
BANK1	FFC0_0000H	FFDF_FFFFH	2048KB	139~78 (32KB) 77~70(8KB)
BANK0	FFE0_0000H	FFFF_FFFFH	2048KB	69~8(32KB) 7~0(8KB)

Table 8-11 Address range and capacity for each area and block No (In case of 2MB product)

Defined	First address	Last address	Capacity	Block No.
BANK1	FFD0_0000H	FFDF_FFFFH	1024KB	107~78(32KB) 77~70(8KB)
BANK0	FFF0_0000H	FFFF_FFFFH	1024KB	37~8 (32KB) 7~0(8KB)

8.4.5 Bank info

(1) Bank Erasure

Erase before writing the user program to the bank.

In the linear mode, erase the bank on the opposite side to the bank currently executing the program.

(BANK0→BANK1、BANK1→BANK0)

In dual mode, the eraser will always be BANK1.

(2) Writable Bank Objects

"Firmware Writable Bank" has been added as an object that indicates a writable bank so that the EtherCAT master can confirm which bank the firmware can be written.

If BANK1 is rewritable, the object value is "1", and if BANK0 is rewritable, the object value is "0".

Table 8-11 shows the details of the object.

Table 8-11 Writable Bank Objects

OBJECT Name	INDEX	Category	Access	Data Type	PDO Mapping
Firmware Writable Bank	0x5000	Optional	RO	UINT8	No

(3) Selecting reboots and boot banks

After writing the new firmware to the bank, reboot and execute the new firmware.

Table 8-12 shows the reboot method and boot bank selection method.

Table 8-12 Rebooting and Selecting Banks

Item	Linear mode	Dual mode
Reboot method	Branch from the user program to the boot loader	Perform a software reset in the user program.
Start-up bank selection method	The boot loader compares the Rev No. stored in BANK0 and BANK1 and selects the newer BANK user program.	Start-up bank switch bit Selected by the value of (BANKSEL.BANKSWP[2:0]). The bank is switched at the next reset by inverting the value of the startup bank switch bit before rebooting.

8.4.6 Download file

(1) Download file format

The sample program outputs download files that can be transferred by TwinCAT as build artifacts.

Table 8-13 shows the format of the download file.

Table 8-13 Download file format

Item	Description
File name prefix	Bank 0 : "ECATFW__B0" Banks 1 : "ECATFW__B1"
File extension	efw
File Formats	Motorola S format

(2) Relationship between download files and banks

The download file is for each bank only and cannot be used for other banks or modes. Shows the relationship between the download file and the bank.

The dual mode download file is for BANK1 but note that the address range is BANK0. This is because it is executed as BANK0 by changing the startup bank after rewriting.

Table 8-14 Relationship between download files and banks

Bank mode	Linear mode		Dual mode
Download file	ECATFW__B1_xxx.efw	ECATFW__B0_xxx.efw	ECATFW__B1_xxx.efw
Banks to be rewritten	BANK1	BANK0	BANK1
Address range 4MB product	FFC0_0000H~ FFDF_7FFFH	FFE0_0000H~ FFFF_7FFFH	FFE0_0000H~ FFFF_FFFFH
Address range 2MB product	FFE0_0000H~ FFEF_7FFFH	FFF0_0000H~ FFFF_7FFFH	FFF0_0000H~ FFFF_FFFFH
Firmware Writable Bank values to check before downloading	1	0	1
Bank running program at download	BANK0	BANK1	BANK0

(3) Check items when downloading files

Since the firmware is rewritten with the data of the download file, using an invalid file may cause the malfunction.

For this reason, some check items are provided.

Table 8-15 shows the check item and the contents of the check, etc.

Table 8-15 Check items for download files

Item	Check contents	Check timing
File name prefix	String In case of BANK0 : "ECATFW__B0" In case of BANK1 : "ECATFW__B1"	Check that the prefix is correct at the start of the download
File password	8 digits Default value : 00000000	Check to see if the password matches at the start of the download
Address range	Motorola S Record Format Address Field	Check if the address is within the address range of the bank to be rewritten during the download
Checksum	Checksum field in Motorola S record format	Check if the checksum calculated from the received record matches during the download

(4) Download file writing in linear mode

In linear mode, write the download file to the bank on the side opposite to the one running the program.

The download file for BANK0 cannot be written while the BANK0 user program is running. Similarly, the download file for BANK1 cannot be written while the BANK1 user program is running.

Therefore, the user needs to find out which bank is to be written in advance and prepare an appropriate download file.

The writable bank can be confirmed from the EtherCAT master as the value of the object "Firmware Writable Bank".

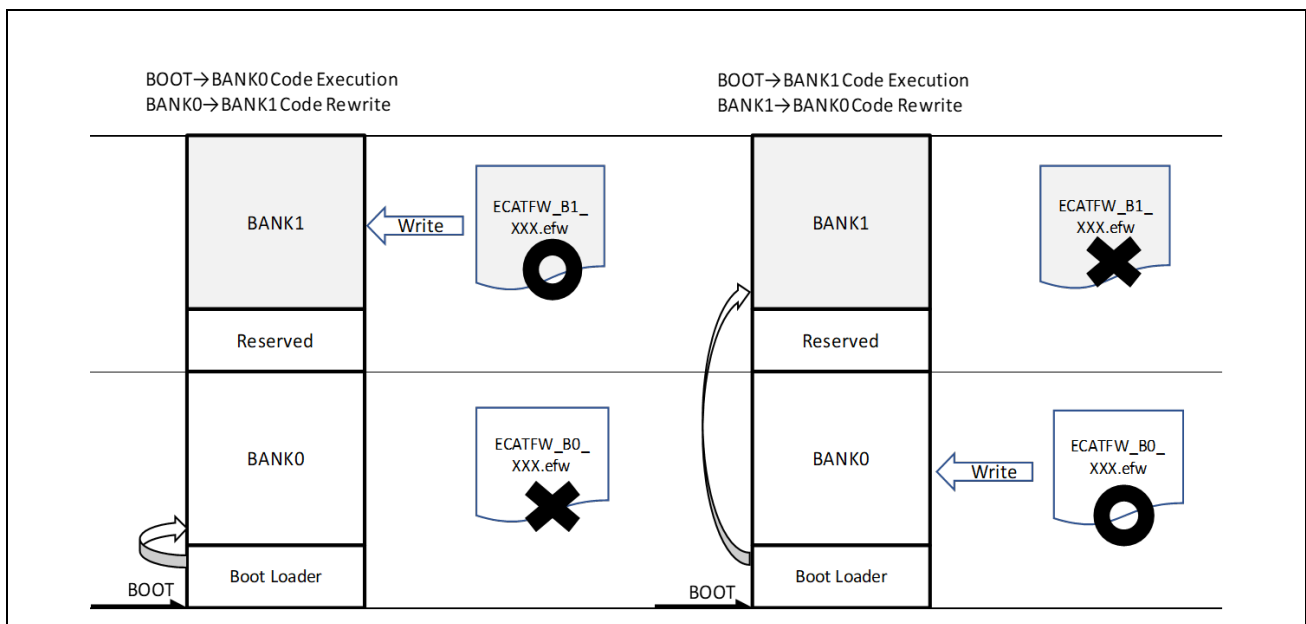


Figure 8-7 Relationship between Banks and Download Files in Linear Mode

(5) Download files in dual mode

In dual mode, the startup bank is swapped after rebooting, so the specifications are as follows.

- Always set the write target bank to BANK1
- Download file uses the one mapped to BANK0

The address included in the Motorola S record format, which is the file format of the download file, indicates BANK0, so when writing to BANK1, write the address as -2MB or -1MB.

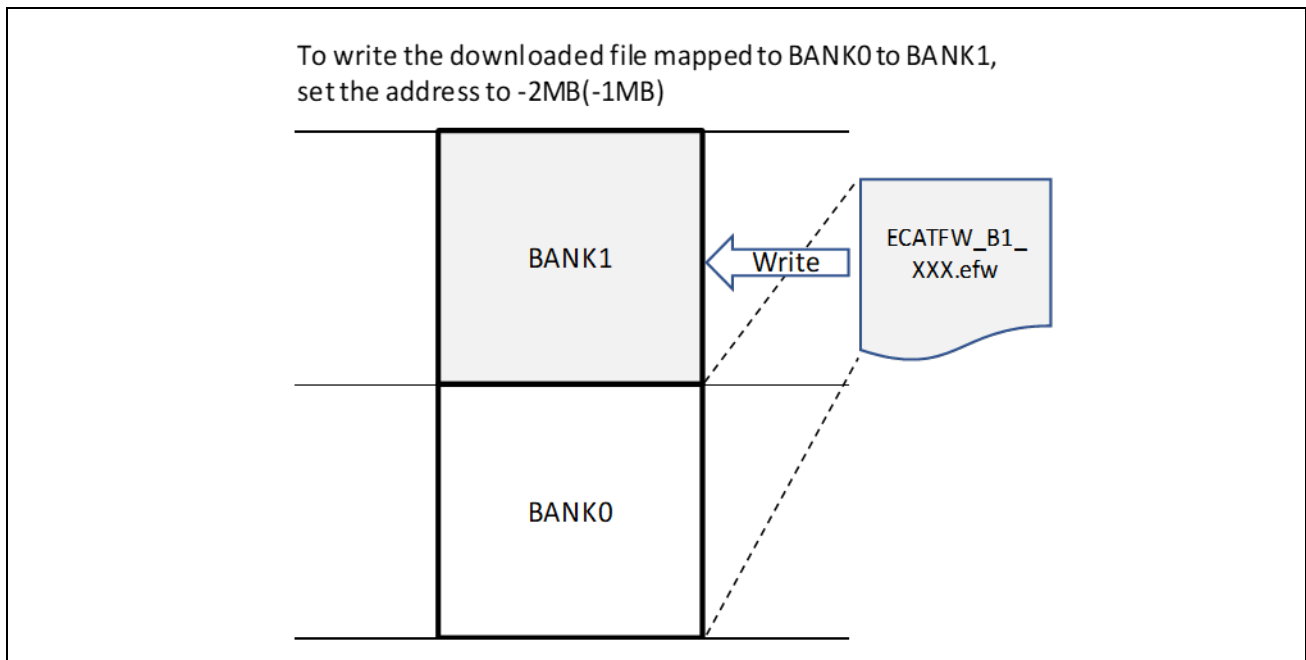


Figure 8-8 Writing Download Files in Dual Mode

8.4.7 SII EEPROM

(1) SII EEPROM UPDATE

The sample program includes a function to update Revision of SII EEPROM when the firmware is updated. The contents of the Identify object (Index: 1018) are stored in addresses 16 to 31 bytes of the SII EEPROM. Table 8-16 Shows the structure of the Identify object.

Table 8-16 Configuring the Identity Object

Defined	Contents	Index	Offset address(Byte)
Vendor ID	Vendor ID Defined as "VENDOR_ID" in ecat_def.h	1018:01	0-3
Product code	Product Codes Defined as "PRODUCT_CODE" in ecat_def.h	1018:02	4-7
Revision	Firmware Revision No. Defined as ecat_def.h or the preprocessor macro "REVESION_NUMBER".	1018:03	8-11
Serial number	Serial No. It is defined as "SERAIL_NUMBER" in ecat_def.h.	1018:04	12-15

The contents of the Identify object are assigned to the fixed address of the code flash as an IDENTIFY section.

Table 8-17 shows the base address of the IDENTIFY section.

Table 8-17 Base address of the IDENTIFY section

Mode	Bank	Base address (H)
Linear mode	BANK0	FFFF_7F80
	BANK1	FFDF_7F80
Dual mode	BANK1	FFFF_7F80

Update the revision of the SII EEPROM to the value of the firmware revision written to the flash after updating the firmware.

(2) Firmware revision check

At the time of INIT->PREOP transition, check whether the revision of firmware being executed and the revision of SII EEPROM match.

If they do not match, an error code will be returned to the EtherCAT master.

AL stratus code (0x0006) AL Status (ERROR INIT)

The issue of error code can be disabled by defining the preprocessor macro "_DISABLE_REVNO_CHECK".

8.4.8 Firmware update program details

8.4.8.1 File structure

Table 8-18 Files to be used in the firmware update program

File name	Overview
r_fw_up_rx.c	Firmware Update Source Files
r_fw_up_rx_if.h	Firmware Update Interface File
r_fw_up_rx_private.h	Firmware Update Header File
r_fw_up_buf.c	Buffering source files for firmware data
r_fw_up_buf.h	Buffer data header file for firmware data
r_fw_up_bank.c	Source file of processing that handles information about banks

Table 8-19 Standard include files used in the firmware update program

File name	Overview
stdbool.h	Defines a macro for logical type and logical value
stdint.h	Declare an integer type with a specified width to define a macro
stdlib.h	This library performs standard processing with C programs such as storage area management
string.h	It is a library that compares and copies character strings

8.4.8.2 List of constants

Table 8-20 Constants to be used in the firmware update program(r_fw_up_rx_if.h)

Constant name	Setting value	Contents
FW_UP_BANK0	(0)	Defines BANK0
FW_UP_BANK1	(1)	Defines BANK1
FW_UP_CFG_PART_MEMORY_SIZE	BSP_CFG_MCU_PART_MEMORY_SIZE	Refer to the value defined in BSP FIT module and define the memory size of CPU
FW_UP_DUAL_BANK_MODE	FLASH_IN_DUAL_BANK_MODE	Refer to the value defined in the flash FIT module to indicate whether it is dual mode. When in dual mode (1)

Table 8-21 Constants to be used in the firmware update program(r_fw_up_rx_private.h)

Constant name	Setting value	Contents
FW_UP_BINARY_BUF_SIZE	(256u)	Buffer size of data for writing to code flash memory
FW_UP_BINARY_BUF_NUM	(2u)	Number of buffers for writing data to code flash memory
FW_UP_BUF_NUM	(60u)	Number of arrays that store the contents of the analyzed Motorola S record format data
FW_UP_BLANK_VALUE	(0xFFFFFFFFu)	Read value when the code flash memory is blank

Table 8-22 Constants to be used in the firmware update program(r_fw_up_buf.h)

Constant name	Setting value	Contents
MOT_S_CHECK_SUM_FIELD	(0x02)	Number of characters in checksum field of Motorola S record format
ADDRESS_LENGTH_S1	(0x04)	Motorola S Record Format Address Field Characters (S1 Type)
ADDRESS_LENGTH_S2	(0x06)	Number of characters in the address field of the Motorola S record format (S2 type)
ADDRESS_LENGTH_S3	(0x08)	Number of characters in the address field of the Motorola S record format (S3 type)
BUF_LOCK	(1)	The specified Motorola S record format buffer is locked.
BUF_UNLOCK	(0)	The specified Motorola S record format buffer is free.

8.4.8.3 Type definition list

```
typedef enum e_fw_up_return_t
{
    FW_UP_SUCCESS,
    FW_UP_ERR_OPENED,
    FW_UP_ERR_NOT_OPEN,
    FW_UP_ERR_NULL_PTR,
    FW_UP_ERR_INVALID_RECORD,
    FW_UP_ERR_BUF_FULL,
    FW_UP_ERR_BUF_EMPTY,
    FW_UP_ERR_INITIALIZE,
    FW_UP_ERR_ERASE,
    FW_UP_ERR_WRITE,
    FW_UP_ERR_INTERNAL,
} fw_up_return_t;

typedef struct st_fw_up_fl_data_t
{
    uint32_t src_addr;
    uint32_t dst_addr;
    uint32_t len;
    uint16_t count;
} fw_up_fl_data_t;

typedef struct st_fw_up_bank_t
{
    uint32_t low_addr;
    uint32_t high_addr;
    uint32_t start_block;
    uint32_t revno;
    uint32_t blockno;
} fw_up_bank_t;

typedef struct st_fw_up_bankinfo_t
{
    uint16_t active;
    uint16_t writable;
} fw_up_bankinfo_t;
```

Figure 8-9 Type definitions used in the firmware update program(r_fw_up_rx_if.h)

```
typedef enum fw_up_mot_s_cnt_t
{
    STATE_MOT_S_RECORD_MARK = 0,
    STATE_MOT_S_RECORD_TYPE,
    STATE_MOT_S_LENGTH_1,
    STATE_MOT_S_LENGTH_2,
    STATE_MOT_S_ADDRESS,
    STATE_MOT_S_DATA,
    STATE_MOT_S_CHKSUM_1,
    STATE_MOT_S_CHKSUM_2
} fw_up_mot_s_cnt_t;

typedef struct MotSBufS
{
    uint8_t addr_length;
    uint8_t data_length;
    uint8_t *paddress;
    uint8_t *pdata;
    uint8_t type;
    uint8_t act;
    struct MotSBufS *pNext;
} fw_up_mot_s_buf_t;

typedef struct WriteDataS
{
    uint32_t addr;
    uint32_t len;
    uint8_t data[FW_UP_BINARY_BUF_SIZE];
    struct WriteDataS *pNext;
    struct WriteDataS *pprev;
} fw_up_write_data_t;
```

Figure 8-10 Type definitions used in the firmware update program(r_fw_up_buf.h)

8.4.8.4 Variable list

Table 8-23 Static type variables used in the firmware update program(r_fw_up_rx.c)

Type	Variable name	Contents	Use function
static bool	is_opead	Firmware update initial setting completion flag	fw_up_open fw_up_close write_firmware fw_up_put_data fw_up_get_data

Table 8-24 Static type variables used in the firmware update program(r_fw_up_buf.c)

Type	Variable name	Contents	Use function
static fw_up_mot_s_buf_t	*papp_put_mot_s_buf	Pointer to the Motorola S record data buffer currently used in Motorola S format analysis processing	fw_up_buf_init fw_up_put_mot_s
static fw_up_mot_s_buf_t	*papp_get_mot_s_buf	Pointer to the Motorola S record data buffer currently used in the code flash memory write data creation process	fw_up_buf_init fw_up_get_binary
static fw_up_mot_s_buf_t	mot_s_buf[FW_UP_BUF_NUM]	Buffer to store the contents of Motorola S record format data	fw_up_buf_init fw_up_memory_init
static fw_up_write_data_t	*papp_write_buf	Pointer to the currently used code flash memory write data buffer	fw_up_buf_init fw_up_get_binary
static fw_up_write_data_t	write_buf[FW_UP_BINARY_BUF_NUM]	Buffer that stores data for writing code flash memory	fw_up_buf_init
static fw_up_mot_s_cnt_t	mot_s_data_state	Motorola S record format data analysis status	fw_up_buf_init fw_up_put_mot_s
static uint32_t	write_current_address	Current code flash memory write destination address	fw_up_buf_init fw_up_get_binary
static bool	detect_terminal_flag	End record detection flag	fw_up_buf_init fw_up_put_mot_s fw_up_get_binary

Table 8-25 Variables for bank information used in the firmware update program(r_fw_up_bank.c)

Type	Variable name	Contents	Use function
fw_up_bank_t	Bank[2]	For BANK0 and BANK1, the upper and lower limits of address, starting block address, firmware revision, and total number of blocks are shown	main(Boot loader) fw_up_bank_initial fw_up_check_addr_value fw_up_bank_revno_update BL_Data BL_Reboot
fw_up_bank_t	BankInfo	The bank executing the program and the writable bank are shown	main(User program) erase_another_bank analyze_and_write_data BL_Data

8.4.8.5 Function list

Table 8-26 Functions used in the firmware update program

Function name	Overview	Listed files
fw_up_open_flash	Flash FIT module initialization	r_fw_up_rx.c
fw_up_open	Firmware update initialization	r_fw_up_rx.c
fw_up_close	Firmware update end process	r_fw_up_rx.c
erase_another_bank	Bank code flash memory erase	r_fw_up_rx.c
analyze_and_write_data	Received data analysis and code flash memory write processing	r_fw_up_rx.c
bank_toggle	Switch startup bank	r_fw_up_rx.c
fw_up_soft_reset	Software reset execution	r_fw_up_rx.c
write_firmware	Code flash memory writing	r_fw_up_rx.c
fw_up_put_data	Received data analysis	r_fw_up_rx.c
fw_up_get_data	Acquisition of code flash memory write data	r_fw_up_rx.c
fw_up_buf_init	Initialization of buffer used for firmware update	r_fw_up_buf.c
fw_up_memory_init	Initialize pointer to buffer	r_fw_up_buf.c
fw_up_put_mot_s	Motorola S record format data analysis	r_fw_up_buf.c
fw_up_get_binary	Acquisition of code flash memory write data	r_fw_up_buf.c
fw_up_ascii_to_hexbyte	Conversion from ASCII format data to binary format data	r_fw_up_buf.c
fw_up_bank_initial	Initial setting of bank information	r_fw_up_bank.c
fw_up_check_addr_value	Check if specified address is within bank range	r_fw_up_bank.c
fw_up_bank_revno_update	Update bank info revision to current value	r_fw_up_bank.c

8.4.9 FoE program details

8.4.9.1 File structure

Table 8-27 Files used by the FoE program

File Name	Overview
foesample.c	Source file of application layer processing including FoE service
foesample.h	Header file of application layer processing including FoE service
bootmode.c	Source files for firmware update and dual mode reboot process
bootmode.h	Header file for firmware update and dual mode reboot process

Table 8-28 Standard include files used in FoE programs

File Name	Overview
stdio.h	Define functions and macros related to input/output.
stdint.h	Defines a macro by declaring an integer type with the specified width.

8.4.9.2 List of constants

Table 8-29 Constants used in FoE programs(foesample.h)

Constant name	Setting value	Contents
SII_EEP_IDENTIFY_OFFSET	0x08	Start word address of Identify stored in SII EEPROM
SII_EEP_VENDORID	0x00	Offset word address of vendor ID stored in SII EEPROM
SII_EEP_PRODUCTCODE	0x02	Offset word address of product code stored in SII EEPROM
SII_EEP_REVESIONNO	0x04	Offset word address of revision stored in SII EEPROM
SII_EEP_SERIALNO	0x04	Offset word address of serial number stored in SII EEPROM

Table 8-30 Constants used in FoE programs(bootmode.c)

Constant name	Setting value	Contents
BL_DATA_STATUS_IDLE	(0)	Indicates that the file data reception processing status is IDLE
BL_DATA_STATUS_ERASE_START	(1)	Indicates that the file data reception processing status is the code flash erase start status.
BL_DATA_STATUS_ERASE	(2)	Indicates that the file data reception processing status is the code flash erase completion status.
BL_DATA_STATUS_WRITE	(3)	File data reception processing status indicates that code flash is being written

8.4.9.3 Type definition list

```
typedef union
{
    UINT32    dword[4];
    UINT16    word[8];
    UINT8     byte[16];
}EEPBUFFER;
```

Figure 8-11 Type definitions used in FoE programs(foesample.h)

8.4.9.4 Variable list

Table 8-31 Static variables used in FoE programs(bootmode.c)

Type	Variable name	Contents	Use function
static UINT8	DataStatus	File data reception processing status	BL_StartDownload BL_Data
static BOOL	bReboot	Reboot flag. Set to 1 when doing a reboot	BL_SetRebootFlag BL_CheckRebootFlag

Table 8-32 Cosnt variables used in FoE programs(bootmode.c)

Type	Variable name	Contents	Use function
const UINT32	tbl_identify[4]	(VENDOR_ID), (PRODUCT_CODE), (REVISION_NUMBER), (SERIAL_NUMBER)	AL_ControlInd

Table 8-33 Cosnt variables used in FoE programs(foesample.c)

Type	Variable name	Contents	Use function
const UINT16	aFileDownloadHeader [5]	Download file prefix string Bank 0: "ECATFW__B0" Bank 1: "ECATFW__B1"	FoE_Write FoE_Read
const UINT32	aFilePassword	Download file password 8 digits Initial value: 0x00000000	FoE_Write FoE_Read

8.4.9.5 Function list

Table 8-34 Functions used in FoE programs

Function Name	Overview	Listed files
BL_Start	Processing executed at INIT→BOOT transition	bootmode.c
BL_Stop	Processing executed at BOOT→INIT transition	bootmode.c
BL_StartDownload	File download start processing	bootmode.c
BL_Data	File data reception processing Erase and write code flash	bootmode.c
BL_SetRebootFlag	Reboot flag set	bootmode.c
BL_CheckRebootFlag	Reboot flag check	bootmode.c
BL_Reboot	Dual-mode reboot process	bootmode.c
FoE_Read	FoE read request reception process	foesample.c
FoE_ReadData	FoE file data reception processing	foesample.c
FoE_WriteData	FoE light request reception processing	foesample.c
FoE_Write	FoE file data transmission processing	foesample.c
HW_Reboot	Linear mode reboot process	foesample.c

8.5 Object dictionary

Table 8-35 shows the object dictionary defined in this sample program.

Table 8-35 Object dictionary

Index	ObjectCode	SI	DataType	Access	Object Name
0x1nnn Communication Area					
0x1000	VAR	-	UDINT	RO	Device Name
0x1001	VAR	-	USINT	RO	Error Register
0x1008	VAR	-	STRING(32)	RO	Manufacture Device Name
0x1009	VAR	-	STRING(3)	RO	Manufacturer Hardware Version
0x100A	VAR	-	STRING(3)	RO	Manufacturer Software Version
0x100B	VAR	-	STRING(3)	RO	Manufacturer Bootloader Version
0x1010	ARRAY	0	USINT	RO	Store parameters
		1	UDINT	RW	SubIndex 00x
0x1011	ARRAY	0	USINT	RO	Restore default parameters
		1	UDINT	RW	SubIndex 00x
0x1018	RECORD	0	USINT	RO	Identity Object
		1	UDINT	RO	Vendor ID
		2	UDINT	RO	Product Code
		3	UDINT	RO	Revision Number
		4	UDINT	RO	Serial Number
0x10F0	RECORD	0	USINT	RO	Backup parameter handling
		1	UDINT	RO	Checksum
		2	BOOL	RW	Backup Parameter Changed
0x10F1	RECORD	0	USINT	RO	Error Settings
		1	UDINT	RO	Local Error Reaction
		2	UINT	RW	Sync Error Counter Limit
0x10F8	VAR	-	ULINT	RO	Timestamp Object
0x1600	RECORD	0	USINT	RO	csp/csv RxPDO Mapping
		1-5	UDINT	RO	SubIndex 00x
0x1601	RECORD	0	USINT	RO	csp RxPDO Mapping
		1-3	UDINT	RO	SubIndex 00x
0x1602	RECORD	0	USINT	RO	csv RxPDO Mapping
		1-3	UDINT	RO	SubIndex 00x
0x17FF	RECORD	0	USINT	RW	Device User RxPDO-Map
		1	UDINT	RW	SubIndex 00x
0x1A00	RECORD	0	USINT	RO	csp/csv TxPDO Mapping
		1-5	UDINT	RO	SubIndex 00x

Index	ObjectCode	SI	Data Type	Access	Object Name
0x1A01	RECORD	0	USINT	RO	csp TxPDO Mapping
		1-3	UDINT	RO	SubIndex 00x
0x1A02	RECORD	0	USINT	RO	csv TxPDO Mapping
		1-4	UDINT	RO	SubIndex 00x
0x1BFF	RECORD	0	USINT	RW	Device User TxPDO-Map
		1	UDINT	RW	SubIndex 00x
0x1C00	ARRAY	0	USINT	RO	Sync Manager Communication Type
		1-4	USINT	RO	SubIndex 00x
0x1C12	ARRAY	0	USINT	RO *	RxPDO Assign
		1-2	UINT	RO *	SubIndex 00x
0x1C13	ARRAY	0	USINT	RO *	TxPDO Assign
		1-2	UINT	RO *	SubIndex 00x
0x1C32	RECORD	0	USINT	RO	SM output parameter
		1	UINT	RO *	Synchronization Type
		2	UDINT	RO	Cycle Time
		4	UINT	RO	Synchronization Types supported
		5	UDINT	RO	Minimum Cycle Time
		6	UDINT	RO	Calc and Copy Time
		8	UINT	RW	Get Cycle Time
		9	UDINT	RO	Delay Time
		10	UDINT	RW	Sync0 Cycle Time
		11	UINT	RO	SM-Event Missed
		12	UINT	RO	Cycle Time Too Small
		13	UINT	RO	Shift Time Too Short Counter
		32	BOOL	RO	Sync Error
0x1C33	RECORD	0	USINT	RO	SM input parameter
		1	UINT	RO *	Synchronization Type
		2	UDINT	RO	Cycle Time
		4	UINT	RO	Synchronization Types supported
		5	UDINT	RO	Minimum Cycle Time
		6	UDINT	RO	Calc and Copy Time
		8	UINT	RW	Get Cycle Time
		9	UDINT	RO	Delay Time
		10	UDINT	RW	Sync0 Cycle Time
		11	UINT	RO	SM-Event Missed
		12	UINT	RO	Cycle Time Too Small
		13	UINT	RO	Shift Time Too Short Counter
		32	BOOL	RO	Sync Error

Index	ObjectCode	SI	Data Type	Access	Object Name
0x5nnn Manufacturer Area					
0x5000	VAR	-	USINT	RO	Firmware Writable Bank
0x6nnn CiA402 Drive Profile Area					
0x603F	VAR	-	UINT	RO	Error Code
0x6040	VAR	-	UINT	RW	Control Word
0x6041	VAR	-	UINT	RO	Status Word
0x605A	VAR	-	INT	RW	Quick stop option code
0x605B	VAR	-	INT	RW	Shutdown option code
0x605C	VAR	-	INT	RW	Disable operation option code
0x605D	VAR	-	INT	RW	Halt option code
0x605E	VAR	-	INT	RW	Fault reaction option code
0x6060	VAR	-	SINT	RW	Modes of Operation
0x6061	VAR	-	SINT	RO	Modes of operation display
0x6062	VAR	-	DINT	RO	Position demand value
0x6063	VAR	-	DINT	RO	Position actual internal value
0x6064	VAR	-	DINT	RO	Position actual value
0x6065	VAR	-	UDINT	RW	Following error window
0x6066	VAR	-	UINT	RW	Following error time out
0x6067	VAR	-	UDINT	RW	Position window
0x606C	VAR	-	DINT	RO	Velocity actual value
0x6072	VAR	-	UINT	RW	Max Torque
0x6077	VAR	-	INT	RO	Torque actual value
0x607A	VAR	-	DINT	RW	Target position
0x607B	RECORD	0	USINT	RO	Position range limit
		1	DINT	RW	Min position range limit
		2	DINT	RW	Max position range limit
0x607C	VAR	-	DINT	RW	Home Offset
0x607D	RECORD	0	USINT	RO	Software position limit
		1	DINT	RW	Min position limit
		2	DINT	RW	Max position limit
0x6091	RECORD	0	USINT	RO	Gear ratio
		1	UDINT	RW	Motor revolutions
		2	UDINT	RW	Shaft revolutions
0x6099	RECORD	0	USINT	RO	Homing speeds
		1	UDINT	RW	Speed during search for switch
		2	UDINT	RW	Speed during search for zero

Index	ObjectCode	SI	Data Type	Access	Object Name
0x60B0	VAR	-	DINT	RW	Position offset
0x60B1	VAR	-	DINT	RW	Velocity offset
0x60B2	VAR	-	INT	RW	Torque offset
0x60B8	VAR	-	UINT	RW	Touch probe function
0x60B9	VAR	-	UINT	RO	Touch probe status
0x60BA	VAR	-	DINT	RO	Touch probe position 1 positive value
0x60BB	VAR	-	DINT	RO	Touch probe position 1 negative value
0x60C2	RECORD	0	USINT	RO	Interpolation time period
		1	USINT	RW	Interpolation time period value
		2	SINT	RW	Interpolation time index
0x60D0	RECORD	0	USINT	RO	Touch probe source
		1	INT	RW	Touch probe 1 source
0x60E0	VAR	-	UINT	RW	Positive torque limit value
0x60E1	VAR	-	UINT	RW	Negative torque limit value
0x60F4	VAR	-	DINT	RO	Following error actual value
0x60FD	VAR	-	UDINT	RO	Digital inputs
0x60FE	RECORD	0	USINT	RO	Digital outputs
		1	UDINT	RW	Physical outputs
		2	UDINT	RW	Bit mask
0x60FF	VAR	-	DINT	RW	Target velocity
0x6402	VAR	-	UINT	RW	Motor Type
0x6502	VAR	-	UDINT	RO	Supported drive modes
0xFnnn Common Device Profile Area					
0xF000	RECORD	0	USINT	RO	Semiconductor Device Profile
		1	UINT	RO	Index Distance
		2	UINT	RO	Maximum Number of Modules
0xF010	ARRAY	0	USINT	RO	Module Profile List
		1	UDINT	RO	SubIndex 00x
0xF020	ARRAY	0	USINT	RO	Configured Address List
		1	UDINT	RO	SubIndex 00x
0xF030	ARRAY	0	USINT	RO	Configured Module Ident List
		1	UDINT	RO	SubIndex 00x
0xF050	ARRAY	0	USINT	RO	Detected Module Ident List
		1	UDINT	RO	SubIndex 00x
0xF380	VAR	-	USINT	RO	Active Exception Status
0xF381	ARRAY	0	USINT	RO	Active Device Warming Details
		1	UDINT	RO	SubIndex 00x

Index	ObjectCode	SI	Data Type	Access	Object Name
0xF382	ARRAY	0	USINT	RO	Active Manufacture Warning Details
		1	UDINT	RO	SubIndex 00x
0xF383	ARRAY	0	USINT	RO	Active Device Error Details
		1	UDINT	RO	SubIndex 00x
0xF384	ARRAY	0	USINT	RO	Active Manufacture Error Details
		1	UDINT	RO	SubIndex 00x
0xF385	RECORD	0	USINT	RO	Active Global Device Warning Details
		1	UDINT	RO	SubIndex 001
0xF386	RECORD	0	USINT	RO	Active Global Manufacture Warning Details
		1	UDINT	RO	SubIndex 001
0xF387	RECORD	0	USINT	RO	Active Global Device Error Details
		1	UDINT	RO	SubIndex 001
0xF388	RECORD	0	USINT	RO	Active Global Manufacture Error Details
		1	UDINT	RO	SubIndex 001
0xF390	VAR	-	USINT	RO	Latched Exception Status
0xF391	ARRAY	0	USINT	RO	Latched Device Warning Details
		1	UDINT	RO	SubIndex 00x
0xF392	ARRAY	0	USINT	RO	Latched Manufacture Warning Details
		1	UDINT	RO	SubIndex 00x
0xF393	ARRAY	0	USINT	RO	Latched Device Error Details
		1	UDINT	RO	SubIndex 00x
0xF394	ARRAY	0	USINT	RO	Latched Manufacture Error Details
		1	UDINT	RO	SubIndex 00x
0xF395	RECORD	0	USINT	RO	Latched Global Device Warning Details
		1	UDINT	RO	SubIndex 001
0xF396	RECORD	0	USINT	RO	Latched Global Manufacture Warning Details
		1	UDINT	RO	SubIndex 001
0xF397	RECORD	0	USINT	RO	Latched Global Device Error Details
		1	UDINT	RO	SubIndex 001
0xF398	RECORD	0	USINT	RO	Latched Global Manufacture Error Details
		1	UDINT	RO	SubIndex 001
0xF3A1	ARRAY	0	USINT	RO	Device Warning Mask
		1	UDINT	RW	SubIndex 00x
0xF3A2	ARRAY	0	USINT	RO	Manufacture Warning Mask
		1	UDINT	RW	SubIndex 00x
0xF3A3	ARRAY	0	USINT	RO	Device Error Mask
		1	UDINT	RW	SubIndex 00x

Index	ObjectCode	SI	Data Type	Access	Object Name
0xF3A4	ARRAY	0	USINT	RO	Manufacture Error Mask
		1	UDINT	RW	SubIndex 00x
0xF3A5	RECORD	0	USINT	RO	Global Device Warming Mask
		1	UDINT	RW	SubIndex 001
0xF3A6	RECORD	0	USINT	RO	Global Manufacture Warming Mask
		1	UDINT	RW	SubIndex 001
0xF3A7	RECORD	0	USINT	RO	Global Device Error Mask
		1	UDINT	RW	SubIndex 001
0xF3A8	RECORD	0	USINT	RO	Global Manufacture Error Mask
		1	UDINT	RW	SubIndex 001
0xF6F0	ARRAY	0	USINT	RO	Input Latch Local Timestamp
		1	UDINT	RO	SubIndex 00x
0xF6F1	ARRAY	0	USINT	RO	Input Latch ESC Timestamp (32-bit)
		1	UDINT	RO	SubIndex 00x
0xF6F2	ARRAY	0	USINT	RO	Input Latch ESC Timestamp (64-bit)
		1	ULINT	RO	SubIndex 00x
0xF9F0	VAR	-	STRING(8)	RO	Manufacturer Serial Number
0xF9F1	ARRAY	0	USINT	RO	CDP Function Generation Number
		1	UDINT	RO	SubIndex 00x
0xF9F2	ARRAY	0	USINT	RO	SDP Function Generation Number
		1	UDINT	RO	SubIndex 00x
0xF9F3	VAR	-	STRING(7)	RO	Vendor Name
0xF9F4	ARRAY	0	USINT	RO	Semiconductor SDP Device Name
		1	STRING(8)	RO	SubIndex 00x
0xF9F5	ARRAY	0	USINT	RO	Output Identifier
		1	USINT	RW	SubIndex 00x
0xF9F6	VAR	-	UDINT	RO	Time since power on
0xF9F7	VAR	-	UDINT	RO	Total time powered
0xF9F8	VAR	-	UDINT	RO	Firmware Update Functional Generation Number
0xF9F9	ARRAY	0	USINT	RO	Module Manufacturer Hardware Version
		1	STRING (8)	RO	SubIndex 00x
0xF9FA	ARRAY	0	USINT	RO	Module Manufacturer Software Version
		1	STRING (8)	RO	SubIndex 00x
0xF9FB	ARRAY	0	USINT	RO	Module Manufacturer Serial Number
		1	STRING (8)	RO	SubIndex 00x

Index	ObjectCode	SI	Data Type	Access	Object Name
0xFBF0	RECORD	0	USINT	RO	Device Reset Command
		1	ARRAY [0..5] OF BYTE	RW	Command
		2	USINT	RO	Status
		3	ARRAY [0..1] OF BYTE	RO	Response
0xFBF1	RECORD	0	USINT	RO	Exception Reset Command
		1	ARRAY [0..4] OF BYTE	RW	Command
		2	USINT	RO	Status
		3	ARRAY [0..1] OF BYTE	RO	Response
0xFBF2	RECORD	0	USINT	RO	Store Parameters Command
		1	ARRAY [0..3] OF BYTE	RW	Command
		2	USINT	RO	Status
		3	ARRAY [0..1] OF BYTE	RO	Response
0xFBF3	RECORD	0	USINT	RO	Calculate Checksum Command
		1	ARRAY [0..3] OF BYTE	RW	Command
		2	USINT	RO	Status
		3	ARRAY [0..7] OF BYTE	RO	Response
0xFBF4	RECORD	0	USINT	RO	Load Parameters Command
		1	ARRAY [0..3] OF BYTE	RW	Command
		2	USINT	RO	Status
		3	ARRAY [0..1] OF BYTE	RO	Response

* This is RW only if its status is PreOP.

※ In case This sample program is used for customer's products, refer to ETG specification documents and, separately consider and implement the settings and necessary processing for each object.

9. Appendix A. Semiconductor Device Profile [ETG.5003]

9.1 Common Device Profile [ETG.5003.1]

In case of handling semiconductor devices with EtherCAT, it is necessary to support the device profile specified in the ETG5003 specifications.

The structure of ETG.5003 is as follows.

1. Common Device Profile (CDP) [ETG.5003.1]
2. Firmware update functionality [ETG.5003.2]
3. Specific Device Profile (SDP) [ETG.5003.2xxx]

Common Device Profile (CDP) specifies requirements that apply to all devices described in Specific Device Profile (SDP)

This sample program provides the object dictionary definition equivalent to CDP [ETG.5003.1 Ver1.1.0] Appendix A. Table 9-1 shows the details of CDP supported by this sample program.

Table 9-1 The details of CDP supported by this sample program.

Items	Details
File defining object about CDP	Header file "semisample.h" ESI file "Renesas EtherCAT RX72M.xml"
Object index about CDP	0x10B0, x17FFF, 0x1BFF, and all after 0xF000
If you want to disable object definition about CDP	Change the macro "CDP_SAMPLE" that is defined in semisample.h to 0, delete Information about CDP in ESI file.

This sample program provides only the framework of object dictionary definition. Separately consider and implement the settings and necessary processing.

For Common Device Profile Ver1.1.0, please refer to the following ETG.5003.1 standard.

If you have any questions regarding CDP, please contact the ETG Association.

ETG5003.1 standard

ETG5003-1 S (R) V1.1.0

EtherCAT Semiconductor Device Profile

Part1 Common Device Profile

9.2 Semi Test Record [ETG.7000.2-Annex5003-0001]

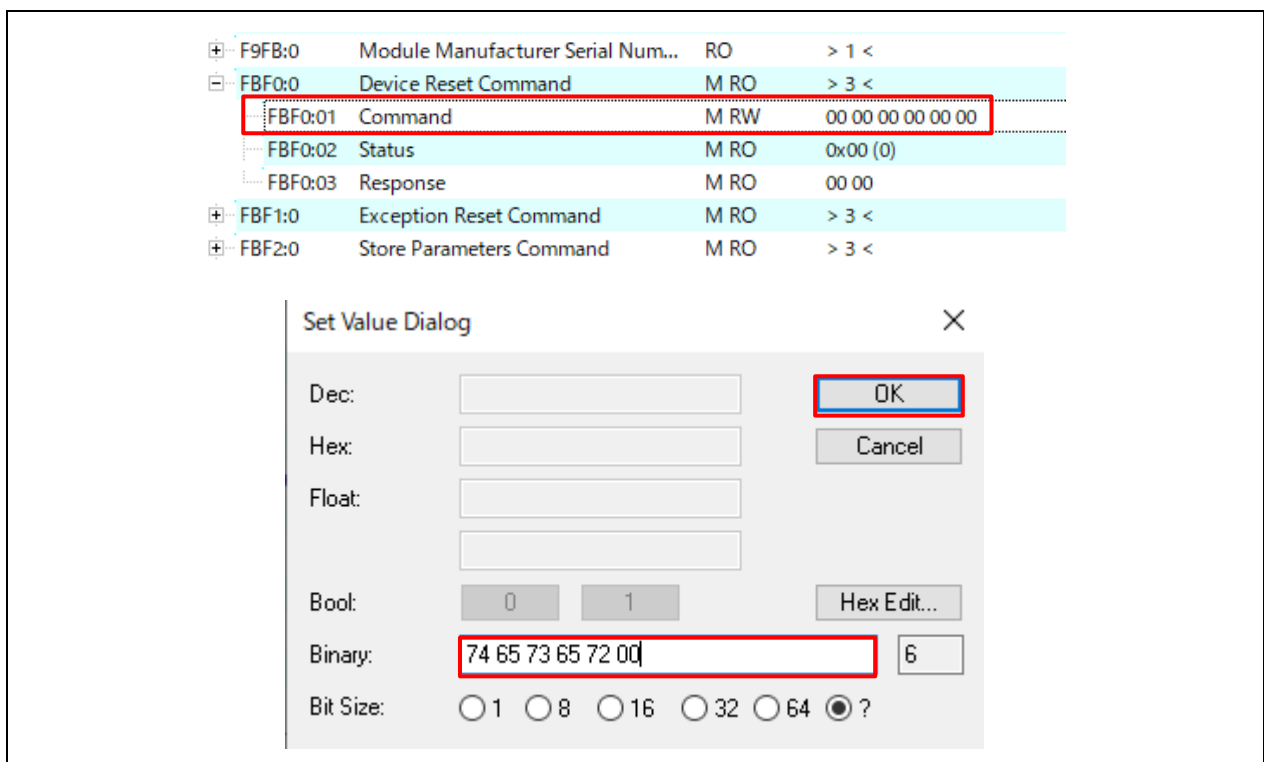
In this sample program, the program is implemented assuming that it corresponds to the following test items of Semi Test Record ETG.7000.2-Annex5003-0001.

1. Device Reset Command (Standard reset)
2. Dynamic PDO
3. Store Parameters

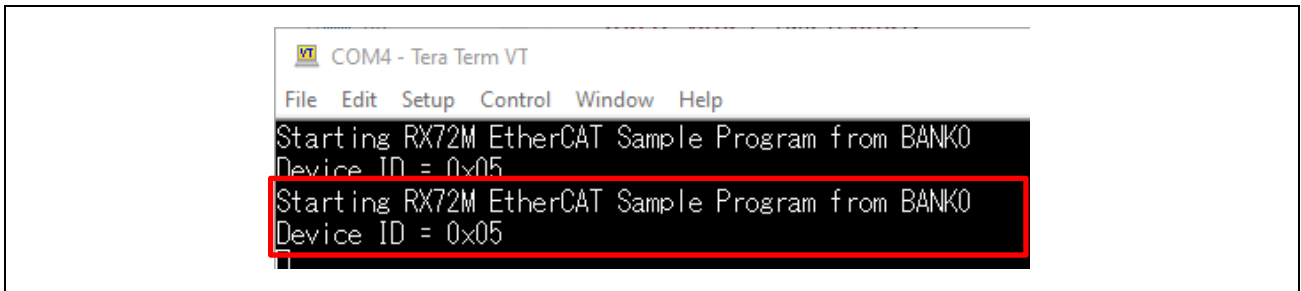
9.2.1 Device Reset Command (Standard reset)

When a specific value is entered in subindex 1 of the object 0xFBFB0, the evaluation board restarts.

- How to check
 - (1) Connect the serial port of the evaluation board to the serial port of the PC and start terminal software such as Tera Term on the PC. In the serial settings of the terminal, set 115200 bps, 8-bit data, no parity, 1 stop bit, no flow control.
 - (2) Perform From 5. "Connecting to TwinCAT" to 5.6 "Rescan of the device" , Connect the evaluation board to TwinCAT.
 - (3) Select the "Online" tab and make sure that the "Current Status" is set to "OP".
 - (4) Select the "CoE - Online" tab, double-click on Index FBF0:01 "Command" and write "74 65 73 65 72 00" in "binary".



- (5) If the "Starting RX72M EtherCAT Sample Program from BANKx" output by serial communication is displayed in terminal software such as Tera Term, the evaluation board has been successfully restarted.



9.2.2 Dynamic PDO

In this sample program, the settings related to PDO in the ESI file are shown in Table 9-2.

Table 9-2 PDO Settings for this Sample Program

PDO Items	setting
PdoAssign	true
PdoConfig	true

In addition, the PDO assignment/mapping object settings are shown in Table 9-3.

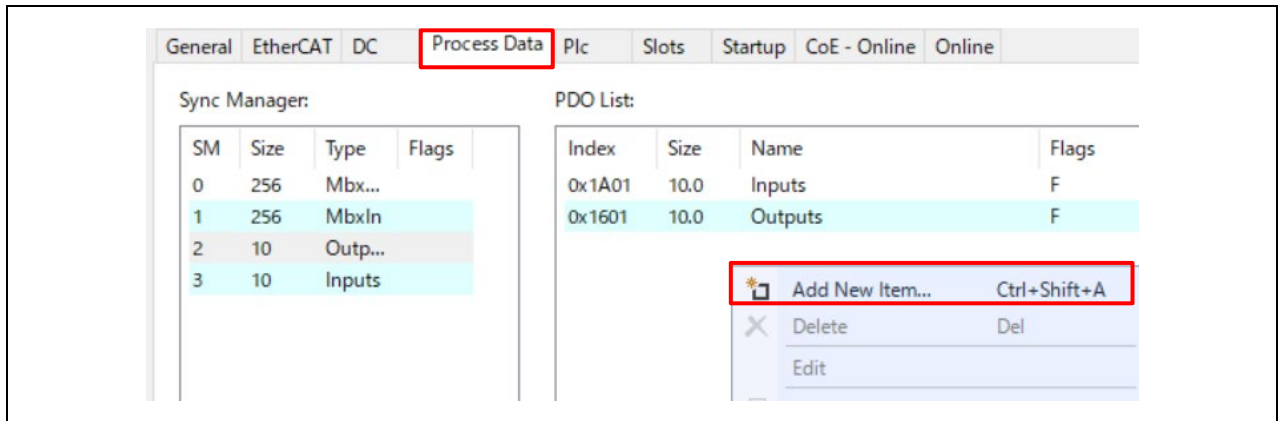
Table 9-3 PDO Assignment Mapping Object Settings

Object Name	Index	Access
RxPDO assign	0x1C12	RW only in the PreOP state
TxPDO assign	0x1C13	RW only in the PreOP state
Device User RxPDO-Map	0x17FF	RW only in the PreOP state
Device User TxPDO-Map	0x1BFF	RW only in the PreOP state

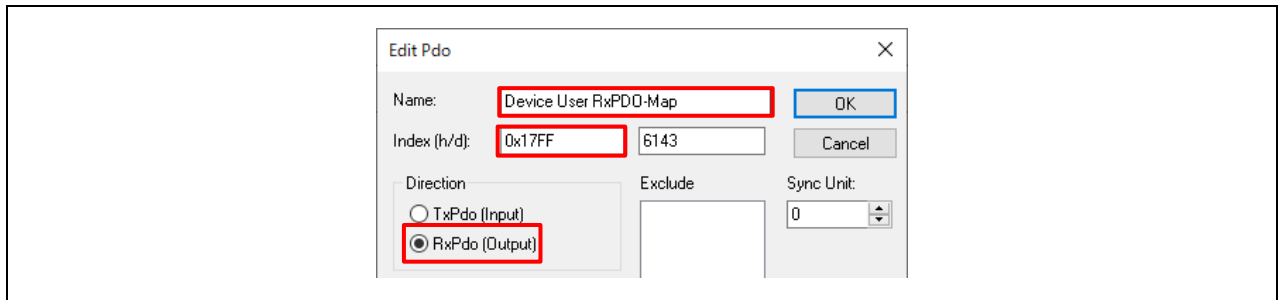
Therefore, objects 0x17FF "Device User RxPDO-Map" and 0x1BFF "Device User TxPDO-Map" that are not assigned by default can be assigned and mapped on the EtherCAT setting tool.

- How to set up
 - (1) Perform From 5. "Connecting to TwinCAT" to 5.6 "Rescan of the device" , Connect the evaluation board to TwinCAT.
 - (2) Select the "Slots" tab, confirm the current slot.
 Select "csp-axis" in "Axis 0" of "Slot" of the left window, add it or change to it.
 Also, "Axis 1" must be empty.
 When you have added a module to "Slot" or changed it, restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.
 - (3) Select the "Online" tab and make sure that the "Current Status" is set to "OP".

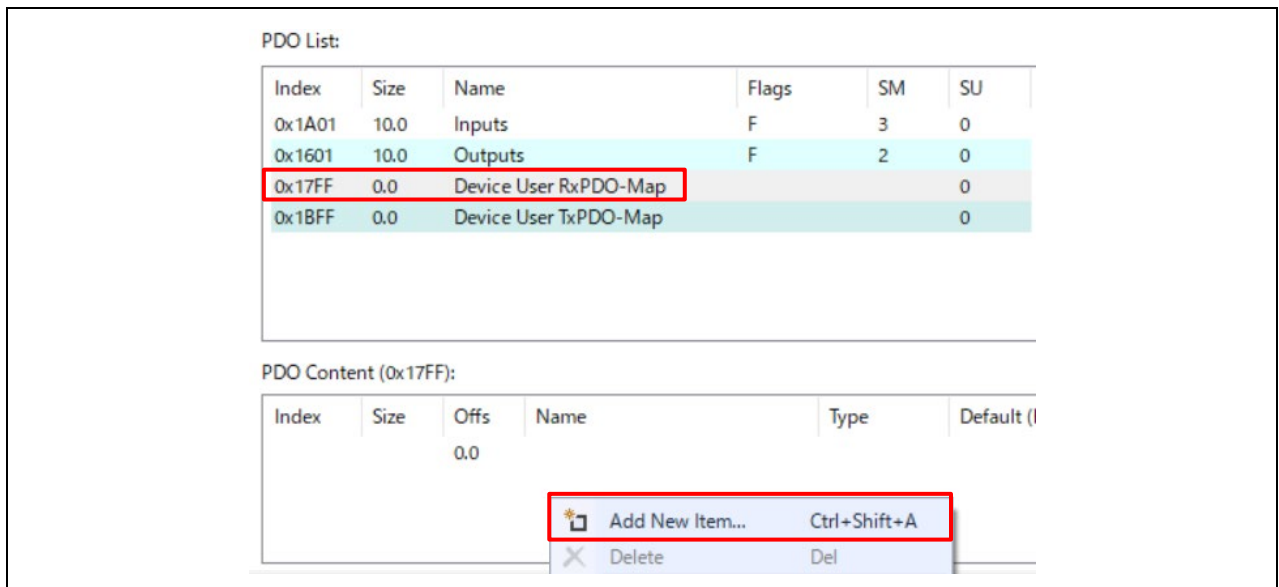
- (4) Select the "Process Data" tab and right-click in the "PDO List" area, select "Add New Item...".



- (5) In the "Edit Pdo" window, set the name to "Device User RxPDO-Map", the Index to "0x17FF", the Direction to "RxPdo" and press "OK".

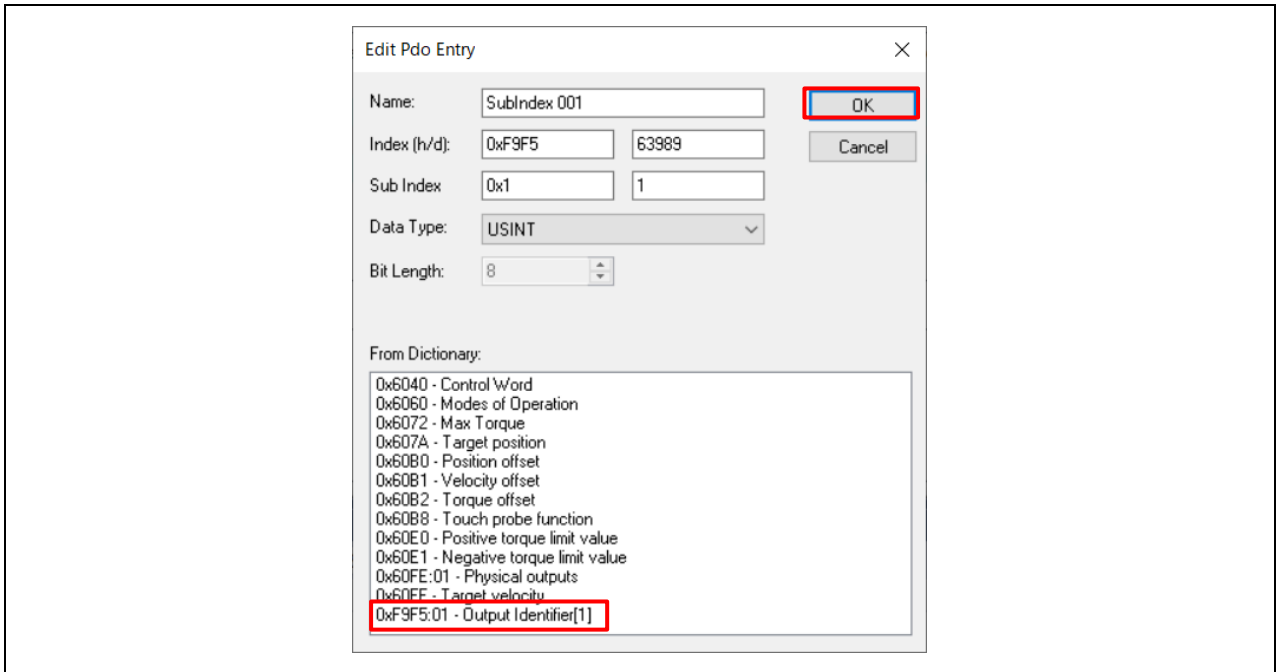


- (6) Right-click in the "PDO List" area again, select "Add New Item...", in the "Edit Pdo" window set the name to "Device User TxPDO-Map", the Index to "0x1BFF", the Direction to "TxPdo" and press "OK". "Device User RxPDO-Map" and "Device User TxPDO-Map" have now been added to the "PDO List".
- (7) Click "Device User RxPDO-Map" in the "PDO List" and right-click in the "PDO Content (0x17FF):" area, select "Add New Item...".



- (8) In the "Edit Pdo Entry" window, click "0xF9F5:01 – Output Identifier[1]" from "From Dictionary" and press OK.

The Index 0xF9F5 is now mapped to the Index 0x17FF.

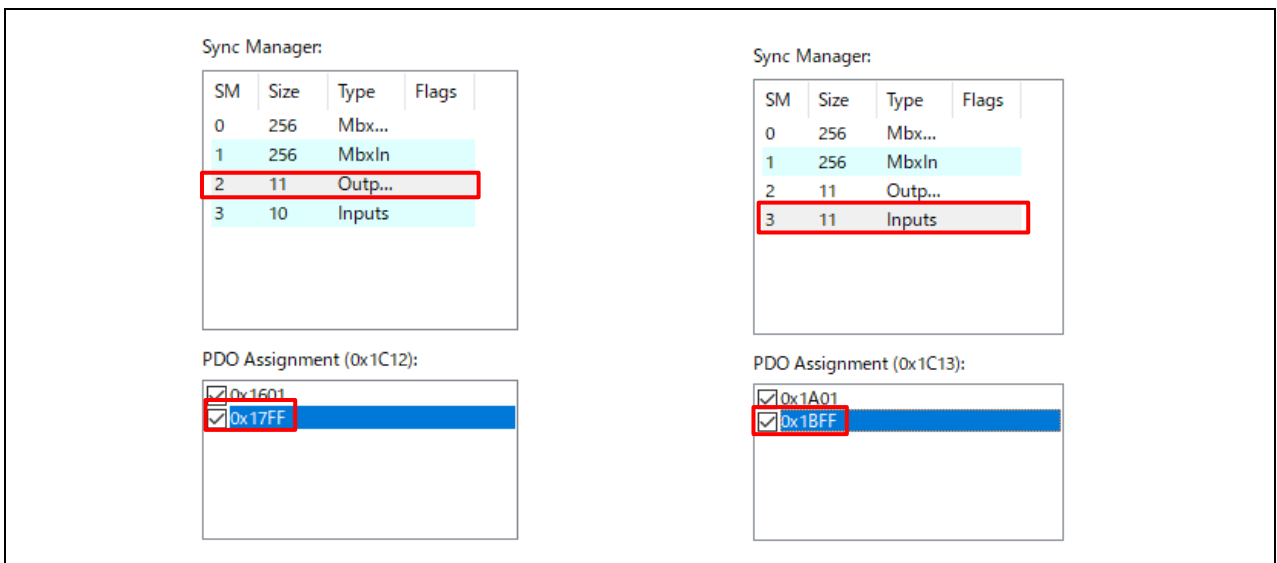


- (9) Similarly, click on "Device User TxPDO-Map" in the "PDO List", right-click on the "PDO Content (0x1BFF):" area, select "Add New Item...".

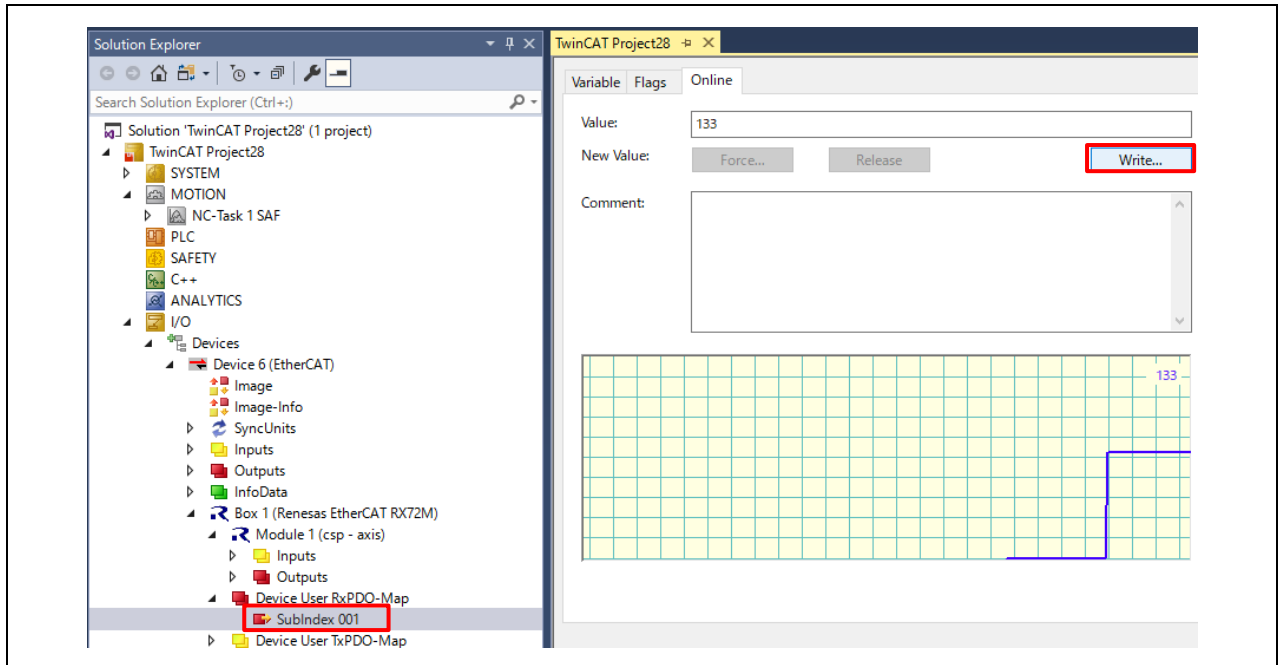
In the "Edit Pdo Entry" window, select "From Dictionary" to "0xF9F5:01 - Output Identifier[1]" and press OK. The Index 0xF9F5 is now mapped to the Index 0x1BFF.

- (10) In the "Sync Manager" area, click on the row with the "SM" column of 2 and check the 0x17FF in the "PDO Assignment (0x1C12)" area.

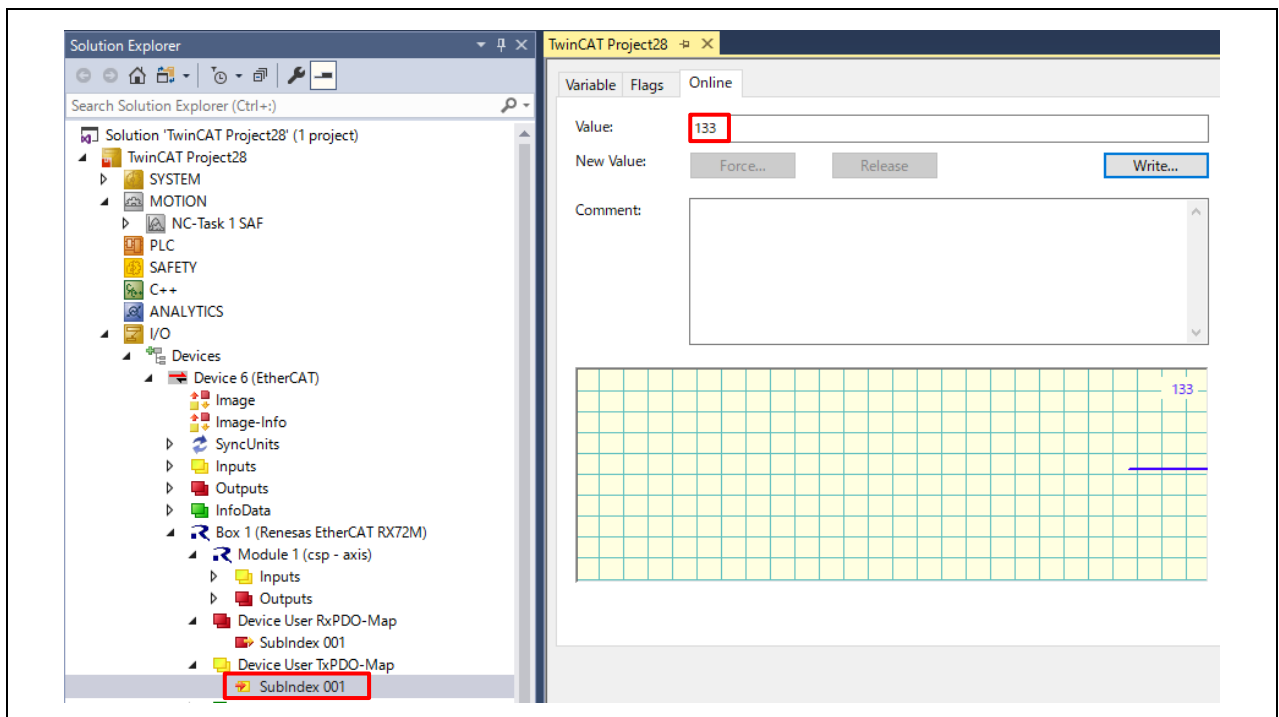
- (11) Similarly, in the "Sync Manager" area, click on the row with the "SM" column of 3 and check the 0x1BFF in the "PDO Assignment (0x1C13)" area. You have now assigned an additional 0x17FF to the Index 0x1C12 and an additional 0x1BFF to the 0x1C13.



- (12) Restart TwinCAT by pressing [TwinCAT] → [Restart TwinCAT (Config Mode)] in the upper menu bar.
- (13) Expand [Device User RxPDO-Map] in [Box 1] and click [SubIndex 001].
- (14) Write an arbitrary value of 1~255 in Value.



- (15) Expand Device User TxPDO-Map and click SubIndex 001.
- (16) If the value of Value is the same as the value written in (13), it is normal.



9.2.3 Store Parameters

In this sample program, when the object value with the backup flag is changed by SDO communication, its value will be stored in the non-volatile memory of the evaluation board.

Table 9-4 shows the objects with the backup flag in this sample program.

Table 9-4 Objects with Backup Flags

Index	Name
0x10F0	Backup parameter handling
0xF3A1	Device Warming Mask
0xF3A2	Manufacture Warming Mask
0xF3A3	Device Error Mask
0xF3A4	Manufacture Error Mask
0xF3A5	Global Device Warming Mask
0xF3A6	Global Manufacture Warming Mask
0xF3A7	Global Device Error Mask
0xF3A8	Global Manufacture Error Mask

Table 9-5 shows the code flash memory area used in this sample program as a non-volatile memory area in which the values of objects with the Backup flag are stored.

Table 9-5 Non-volatile Memory Areas for Backup Objects

Bank mode	First address	Last address	Capacity	Block No.
Linear (4MB)	FFDF_8000H	FFDF_FFFFH	32KB	70 (32KB)
Linear (2MB)	FFEF_8000H	FFEF_FFFFH	32KB	38 (32KB)
Dual (4MB)	FFC0_0000H	FFC0_8000H	32KB	139 (32KB)
Dual (2MB)	FFD0_0000H	FFD0_8000H	32KB	107 (32KB)

Table 9-6 shows the constants used by programs that store in non-volatile memory.

Table 9-6 Constants used in programs storing non-volatile memory (semisample.h)

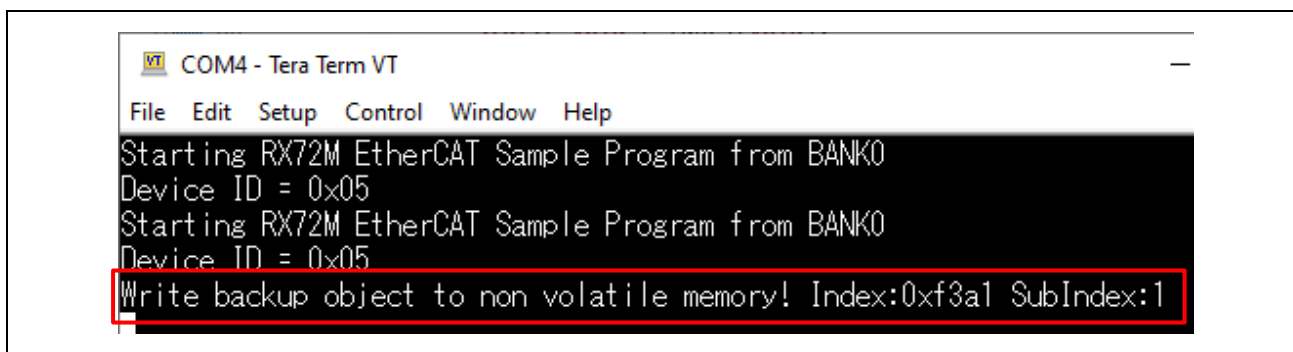
Constant Name	Setting Values	Details
BACKUP_MEMORY_START_ADDRESS	Table 9-4 First Addresses	The beginning address of the non-volatile memory area for the Backup objects.
BACKUP_BYTESIZE	FLASH_CF_MIN_PGM_SIZE	Amount of non-volatile memory area for Backup objects.
Default_Data_Is_Not_Initialized	(0xFFFF)	The non-volatile memory area for the Backup object has not been initialized.
Default_Data_Is_Initialized	(0x5555)	The non-volatile memory area for the Backup object has been initialized.
NonVolatileWordOffset_0x10F0	(0x0001)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A1	(0x0008)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.

NonVolatileWordOffset_0xF3A2	(0x000c)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A3	(0x0010)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A4	(0x0014)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A5	(0x0018)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A6	(0x001c)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A7	(0x0020)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.
NonVolatileWordOffset_0xF3A8	(0x0024)	Number of offset words from BACKUP_MEMORY_START_ADDRESS.

This sample program uses the functions defined in 6.2.4.1 "Backup Parameter Support" of Application Note ET9300 (EtherCAT Slave Stack Code).

For more information, see Application Note ET9300 (EtherCAT Slave Stack Code) and semisample.c.

- How to check
 - (1) Connect the serial port of the evaluation board to the serial port of the PC and start terminal software such as Tera Term on the PC. In the serial settings of the terminal, set 115200 bps, 8-bit data, no parity, 1 stop bit, no flow control.
 - (2) Connect the evaluation board to TwinCAT by completing 5.6 "Rescan the device" in 5. "Connecting to TwinCAT".
 - (3) Select the "Online" tab and make sure that "Current Status" is set to "OP".
 - (4) Write the value to the Backup object. Here, we write "0xAAAAAAAA" at Index 0xF3A1:01.
 - (5) If the writing is successful, "Write backup object to non volatile memory! Index:0xf3a1 SubIndex:1" will be displayed in terminal software such as Tera Term.



- (6) Run the 9.2.1 'Device Reset Command' to reboot the evaluation board.
- (7) It is normal if the Index 0xF3A1:01 written in (4) is "0xAAAAAAAA".

Objects with the backup flag are stored in non-volatile memory and are read at startup.

10. Appendix B. How to support code flash memory capacity of 2MB

The project included in this application note is a product with a code flash memory capacity of 4MB.

To support products with 2MB code flash memory, it is necessary to change the configuration file of BSP and some of the section settings of build configuration.

The changes in the BSP configuration file are as follows:

【 src/smc_gen/r_config/r_bsp_config.h 】

Change the value of BSP_CFG_MCU_PART_MEMORY_SIZE to 0xD

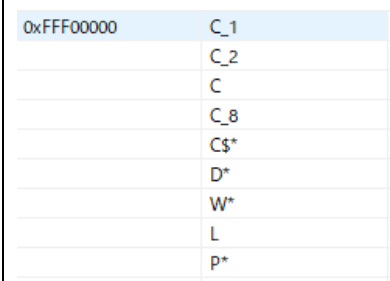
```
#define BSP_CFG_MCU_PART_MEMORY_SIZE    (0xD)
```

Changes to the build configuration section settings are as follows:

To change the settings, go to Project → Properties → C/C++ Build → Settings.

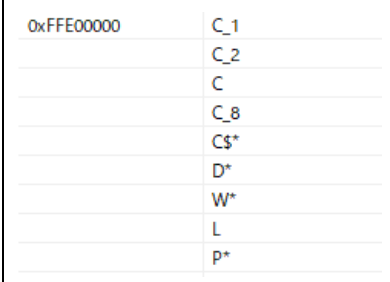
- Linear mode BANK0

Table 10-1 BANK0 Changes - Tools Settings tab

Item	Changes	Description
Linker-section	Change the ROM start position to 0xFFFF0000 <Settings> 	BANK0 mapping is from 0xFFFF0000 to 0xFFFF7FFF. The size is 992KB.

- Linear mode BANK1

Table 10-2 BANK1 Changes - Tools Settings tab

Item	Changes	Description
Linker-section	Change the ROM start position to 0xFFE00000 <Settings> 	BANK1 mapping is from 0xFFE00000 to 0xFFEF7FFF. The size is 992KB.

	<p>Add an IDENTIFY section to the ROM area and set the start position to 0xFFEF7F70.</p> <p><Settings></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">0xFFEF7F70</td> <td>IDENTIFY</td> </tr> <tr> <td>0xFFEF7F80</td> <td>EXCEPTVECT</td> </tr> <tr> <td>0xFFEF7FFC</td> <td>RESETVECT</td> </tr> </table>	0xFFEF7F70	IDENTIFY	0xFFEF7F80	EXCEPTVECT	0xFFEF7FFC	RESETVECT	
0xFFEF7F70	IDENTIFY							
0xFFEF7F80	EXCEPTVECT							
0xFFEF7FFC	RESETVECT							

- Dual mode HardwareDebug

Table 10-3 HardwareDebug changes-Tool settings tab

Item	Changes	Description																						
Linker-section	<p>Changed the starting position of the PResetPRG placed in the ROM area to 0xFFFF08000.</p> <p><Settings></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">0xFFFF08000</td> <td>PResetPRG</td> </tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>CS*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM2</td></tr> </table>	0xFFFF08000	PResetPRG		C_1		C_2		C		C_8		CS*		D*		W*		L		P		PFRAM2	<p>The mapping for BANK0 is 0xFFFF00000 to 0xFFFFFFFF but sets the starting position of PResetPRG to 0xFFFF08000.</p> <p>The size of BANK0 is 1024 KB.</p>
0xFFFF08000	PResetPRG																							
	C_1																							
	C_2																							
	C																							
	C_8																							
	CS*																							
	D*																							
	W*																							
	L																							
	P																							
	PFRAM2																							

- Dual mode Download

Table 10-4 Download changes-Tool settings tab

Item	Changes	Description																						
Linker-section	<p>Changed the starting position of the PResetPRG placed in the ROM area to 0xFFFF08000.</p> <p><Settings></p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">0xFFFF08000</td> <td>PResetPRG</td> </tr> <tr><td></td><td>C_1</td></tr> <tr><td></td><td>C_2</td></tr> <tr><td></td><td>C</td></tr> <tr><td></td><td>C_8</td></tr> <tr><td></td><td>CS*</td></tr> <tr><td></td><td>D*</td></tr> <tr><td></td><td>W*</td></tr> <tr><td></td><td>L</td></tr> <tr><td></td><td>P</td></tr> <tr><td></td><td>PFRAM2</td></tr> </table>	0xFFFF08000	PResetPRG		C_1		C_2		C		C_8		CS*		D*		W*		L		P		PFRAM2	<p>The mapping for BANK0 is 0xFFFF00000 to 0xFFFFFFFF but sets the starting position of PResetPRG to 0xFFFF08000.</p> <p>The size of BANK0 is 1024 KB.</p>
0xFFFF08000	PResetPRG																							
	C_1																							
	C_2																							
	C																							
	C_8																							
	CS*																							
	D*																							
	W*																							
	L																							
	P																							
	PFRAM2																							

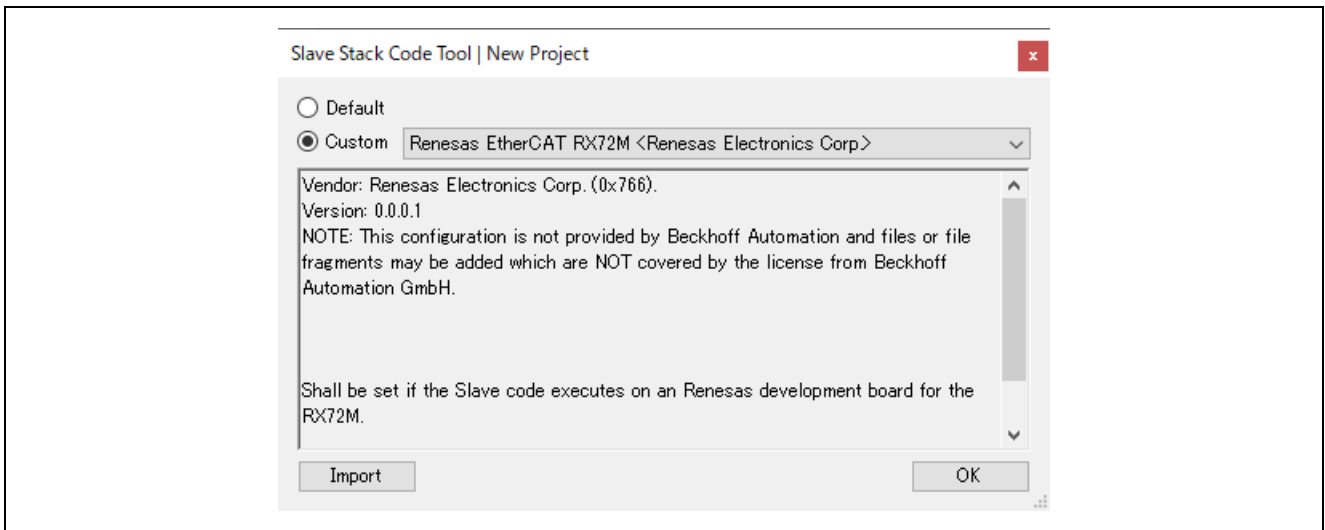
11. Appendix C. How to use the SSC tool configuration file

This section describes how to create the SSC project file by using the SSC tool configuration file.

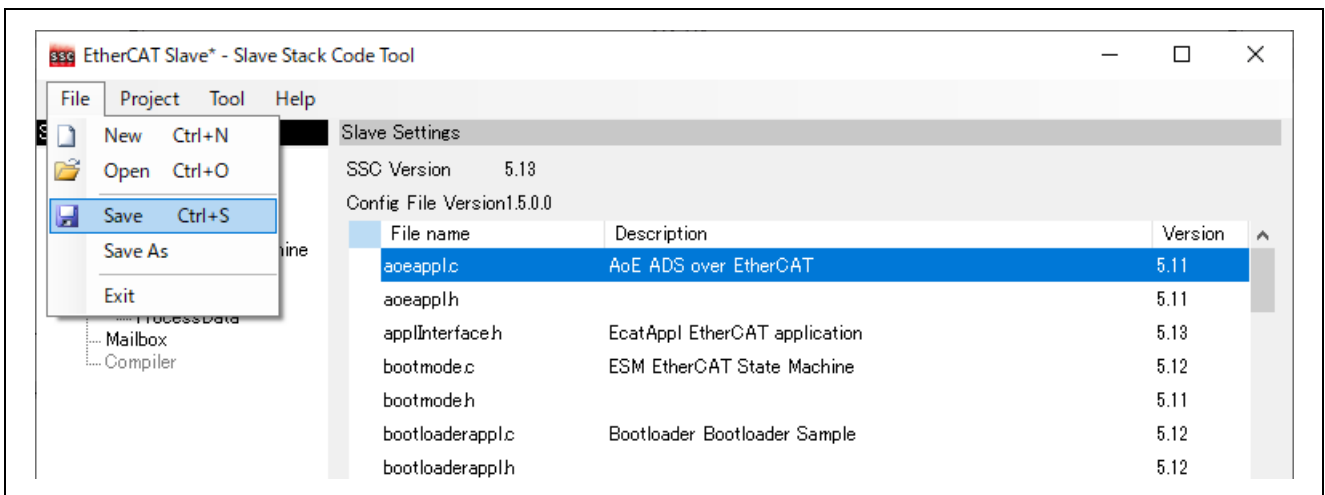
- (1) Start the SSC tool by clicking [EtherCAT Slave Stack Code] → [SSC Tool] in Windows start menu.
- (2) Click [import] in the [New Project] dialog, select the below SSC tool configuration file in this sample program, and click [OK].

ecat_linear_demo_cpurx72m\utilities\ssc_config\RX72M_EtherCAT_config.xml

- (3) Check the [Custom] checkbox, select “Renesas EtherCAT RX72M <Renesas Electronics Corp>” in the list, and click [OK].



- (4) Click [File]→[Save], Save the SSC project file as any project file name. (The default is “Renesas EtherCAT RX72M.esp”.)



12. Reference documents

User's Manual: Hardware

RX72M Group User's Manual Hardware Edition (Document r01uh0804jj0120-rx72m.pdf)

RX72M CPU Card with RDC-IC User's Manual (Document r12uz0098jj0110-motor.pdf)

RX72M Renesas Starter Kit+ for RX72M User's Manual

(Document REN_r20ut4391eg0100-rsk+rx72m-usermanual_MAT_20190731.pdf)

(Please obtain the latest version from the Renesas Electronics website.)

TS-RX72M-COM User's Manual

(Please obtain the latest version from the [TESSERA TECHNOLOGY website](#).)

EtherCAT Slave Stack Code Reference material :

Application Note ET9300 (EtherCAT Slave Stack Code)

EtherCAT Specification :

ETG.1000.1 EtherCAT Specification – Part1 Overview

ETG.1000.2 EtherCAT Specification – Part2 Physical Layer service and protocol specification

ETG.1000.3 EtherCAT Specification – Part3 Data Link Layer service definition

ETG.1000.4 EtherCAT Specification – Part4 Data Link Layer protocol specification

ETG.1000.3 EtherCAT Specification – Part5 Application Layer service definition

ETG.1000.6 EtherCAT Specification – Part6 Application Layer protocol specification

ETG.1020 EtherCAT Protocol Enhancements

ETG.2000 EtherCAT Slave Information Specification

ETG.5003.1 EtherCAT Semiconductor Device Profile Part1 Common Device Profile

ETG.5003.2 EtherCAT Semiconductor Device Profile Part2 Firmware Update

ETG.6010 EtherCAT Implementation Directive for CiA402 Drive Profile

ETG.7000.Annex5003-0001 EtherCAT Semi Test Record

CiA402 Specification :

IEC 61800-7-201 Edition 1.0

Adjustable speed electrical power drive systems Part 7-201: Generic interface and use of profiles for power drive systems Profile type 1 specification

IEC 61800-7-301 Edition 1.0

Adjustable speed electrical power drive systems Part 7-301: Generic interface and use of profiles for power drive systems Mapping of profile type 1 to network technologies

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 31, 2024	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

- Arm[®] and Cortex[®] are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.
- Ethernet is a registered trademark of Fuji Xerox Co., Ltd.
- IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.
- TRON is an acronym for "The Real-time Operation system Nucleus".
- ITRON is an acronym for "Industrial TRON".
- μ ITRON is an acronym for "Micro Industrial TRON".
- TRON, ITRON, and μ ITRON do not refer to any specific product or products.
- EtherCAT[®] and TwinCAT[®] are registered trademarks and patented technologies, licensed by Beckhoff Automation GmbH, Germany.
- Additionally all product names and service names in this document are trademarks or registered trademarks which belong to the respective owners.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.