RX65N Group, RX651Group

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Differences Between Products with 1 Mbyte or Less of Code Flash Memory and Products with 1.5 Mbytes or More of Code Flash Memory

Introduction

This application note is the reference document to show differences in peripheral modules, I/O registers, and pin functions between products with 1 Mbytes or less of the code flash memory (RX65N (CF ≤ 1 Mbyte)) and products with 1.5 Mbytes or more of the code flash memory (RX65N (CF ≥ 1.5 Mbytes)) in the RX65N Group. This document also provides the important information that needs to be taken into account when replacing the MCU.

Unless explicitly stated, this application note describes differences between RX65N products with 144/145 pins and 1 Mbyte or less of the code flash memory, and RX65N products with 177/176 pins and 1.5 Mbytes or more of the code flash memory. Refer to the User's Manual: Hardware for differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

- **RX65N Group**

Contents

1. Comparison of Build-In Functions Between RX65N (CF <= 1 Mbyte) and RX65N (CF >= 1.5 Mbytes)

Table 1.1 lists the Comparison of Build-In Functions Between RX65N (CF ≤ 1 Mbyte) and RX65N (CF ≥ 1.5 Mbytes).

Refer to 2. Comparison of Specifications Overview and the User's Manual: Hardware listed in 5. Reference Documents for details of each function.

Table 1.1 Comparison of Build-In Functions Between RX65N (CF ≤ 1 Mbyte) and RX65N (CF ≥ 1.5 Mbytes)

Function	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
CPU	✓	
Operating modes	✓	
Reset	✓	
Option-Setting Memory	✦	
Voltage Detection Circuit (LVDA)	✓	
Clock Generation Circuit	✦	
Clock Frequency Accuracy Measurement Circuit (CAC)	✓	
Low Power Consumption	✦	
Battery Backup Function	✓	
Register Write Protection Function	✓	
Exception Handling	✓	
Interrupt Controller (ICUB)	✦	
Buses	✦	
Memory-Protection Unit (MPU)	✓	
DMA Controller (DMACAa)	✓	
EXDMA Controller (EXDMACa)	✓	
Data Transfer Controller (DTCb)	✓	
Event Link Controller (ELC)	✓	
I/O Ports	✦	
Multi-Function Pin Controller (MPC)	✦	
Multi-Function Timer Pulse Unit 3 (MTU3a)	✓	
Port Output Enable 3 (POE3a)	✓	
16-Bit Timer Pulse Unit (TPUa)	✓	
Programmable Pulse Generator (PPG)	✓	
8-Bit Timer (TMR)	✓	
Compare Match Timer (CMT)	✓	
Compare Match Timer W (CMTW)	✓	
Realtime Clock (RTCd)	✓	
Watchdog Timer (WDTA)	✓	
Independent Watchdog Timer (IWDTa)	✓	
Ethernet Controller (ETHERC)	✓	
DMA Controller for the Ethernet Controller (EDMACa)	✓	
USB 2.0 FS Host/Function Module (USBb)	✓	
Serial Communications Interface (SCIg, SCIi, SCIh)	✓	
I²C-bus Interface (RIICa)	✦	
CAN Module (CAN)	✓	
Serial Peripheral Interface (RSPIc)	✓	
Quad Serial Peripheral Interface (QSPI)	✓	

Function	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
CRC Calculator (CRCA)	✓	
SD Host Interface (SDHI)	✓	
SD Slave Interface (SDSI)	✓	
MultiMediaCard Interface (MMCIF)	✓	
Parallel Data Capture Unit (PDC)	✓	
Graphic LCD Controller (GLCDC)	×	✓
2D Drawing Engine (DRW2D)	×	✓
Boundary Scan	✦	
AESa	✓	× (1)
RNG	✓	× (1)
Trusted Secure IP (TSIP)	×	✓
12-Bit A/D Converter (S12ADFa)	✓	
12-Bit D/A Converter (R12DA)	✓	
Temperature Sensor (TEMPS)	✓	
Data Operation Circuit (DOC)	✓	
RAM	✦	
Standby RAM	✓	
Flash Memory	✦	

✓: Available, ×: Not available, ✦: There are differences in the function between RX65N (CF ≤ 1 Mbyte) and RX65N (CF ≥ 1.5 Mbytes)

Note 1: The AES and RNG are built into the Trusted Secure IP in RX65N (CF ≥ 1.5 Mbytes).

2. Comparison of Specifications Overview

2.1 Option-Setting Memory

Table 2.1 lists the Comparison of Registers for the Option-Setting Memory.

Table 2.1 Comparison of Registers for the Option-Setting Memory

Register	Bit Symbol	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
MDE	BANKMD[2:0]	— (1)	Bank Mode Select
TMEF	TMEFDB[2:0]	— (2)	Dual-Bank TM Enable
BANKSEL	—	—	Bank Select Register

Notes: 1. Dual mode cannot be set for RX65N (CF ≤ 1 Mbyte). When programming, set these bits to linear mode (111b).
2. These bits are reserved bits for RX65N (CF ≤ 1 Mbyte). When reading these bits, the value written by the user are returned. The write value should be 111b.

2.2 Clock Generation Circuit

Table 2.2 lists the Comparison of Specifications for the Clock Generation Circuit.

Table 2.2 Comparison of Specifications for the Clock Generation Circuit

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, and AES. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral module. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, GLCDC, and DRW2D. • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12AD. • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM. • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Operating frequency	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 60 MHz (max) • PCLKD: 60 MHz (max) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory) • BCLK: 120 MHz (max) • BCLK pin output: 60 MHz (max) • SDCLK pin output: 60 MHz (max) • UCLK: 48 MHz (max) • CACCLK: Same as the clock from respective oscillators. • CANMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max)	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 60 MHz (max) • PCLKD: 60 MHz (max) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) 60 MHz (max) (for reading from the data flash memory) • BCLK: 120 MHz (max) • BCLK pin output: 60 MHz (max) • SDCLK pin output: 60 MHz (max) • UCLK: 48 MHz (max) • CACCLK: Same as the clock from respective oscillators. • CANMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pin: EXTAL, XTAL • Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
High-speed on-chip oscillator (HOCO)	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	• Oscillation frequency: 240 kHz	• Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	• Oscillation frequency: 120 kHz	• Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	• Input clock frequency: 10 MHz (max)	• Input clock frequency: 10 MHz (max)
Control of output on the BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable
Control of output on the SDCLK pin	• SDCLK clock output or high output is selectable	• SDCLK clock output or high output is selectable
Event linking (output)	• Detection of stopping of the main clock oscillator	• Detection of stopping of the main clock oscillator
Event linking (input)	• Switching of the clock source to the low-speed on-chip oscillator	• Switching of the clock source to the low-speed on-chip oscillator

2.3 Low Power Consumption

Table 2.3 lists Comparison of Registers for the Low Power Consumption.

Table 2.3 Comparison of Registers for the Low Power Consumption

Register	Bit Symbol	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
MSTPCRB	MSTPB20	— (1)	I^2C Bus Interface 1 Module Stop
MSTPCRC	MSTPC29	— (1)	Graphic-LCD controller Module Stop
	MSTPC28	— (1)	2D drawing engine Module Stop
	MSTPC2	— (2)	Expansion RAM Module Stop
MSTPCRD	MSTPD27	— (1)	Trusted Secure IP Module Stop

Notes: 1. This bit is reserved bit in RX65N (CF ≤ 1 Mbyte). The bit is read as 1 and the write value should be 1.
2. This bit is reserved bit in RX65N (CF ≤ 1 Mbyte). The bit is read as 0 and the write value should be 0.

2.4 Interrupt Controller

Table 2.4 lists the Comparison of Specifications for the Interrupt Controller and Table 2.5 lists the Comparison of Registers for the Interrupt Controller.

Table 2.4 Comparison of Specifications for the Interrupt Controller

Item		ICUB in RX65N (CF ≤ 1 Mbyte)	ICUB in RX65N (CF ≥ 1.5 Mbytes)
Interrupts	Peripheral interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. • Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) • Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) • Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source. • Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) • Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) • Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupt	Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.	Interrupt by the input signal to the IRQi pin (i = 0 to 15) • Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter can be used to remove noise.

Item		ICUB in RX65N (CF ≤ 1 Mbyte)	ICUB in RX65N (CF ≥ 1.5 Mbytes)
Interrupts	Software interrupt	• Interrupt request can be generated by writing to a register. • Two interrupt sources	• Interrupt request can be generated by writing to a register. • Two interrupt sources
	Interrupt priority	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.	Interrupt by the input signal to the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	This interrupt occurs when the main clock oscillator stop is detected.	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	This interrupt occurs when a parity check error is detected in the RAM.	This interrupt occurs when a parity check error is detected in the RAM (including the expanded RAM).

Item		ICUB in RX65N (CF ≤ 1 Mbyte)	ICUB in RX65N (CF ≥ 1.5 Mbytes)
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).	Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).	Exit software standby mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).	Exit deep software standby mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.5 Comparison of Registers for the Interrupt Controller

Register	Bit Symbol	ICUB in RX65N (CF ≤ 1 Mbyte)	ICUB in RX65N (CF ≥ 1.5 Mbytes)
PIBRk	—	Software Configurable Interrupt B Request Register k (k = 0h to Ah)	Software Configurable Interrupt B Request Register k (k = 0h to Bh)

2.5 Buses

Table 2.6 lists the Comparison of Bus Specifications, Table 2.7 lists the Comparison of Addresses Assigned for Each Bus, Table 2.8 lists the Comparison of Bus Master Priorities, Table 2.9 lists the Comparison of Peripheral Modules Connected to Internal Peripheral Buses, Table 2.10 lists the Comparison of External Bus Specifications, Table 2.11 lists the Comparison of Pin Configuration of the External Bus, and Table 2.12 lists the Comparison of Bus Registers.

Table 2.6 Comparison of Bus Specifications

Bus Type		RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
CPU bus	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, expansion RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, expansion RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to code flash memory	Connected to code flash memory
	Memory bus 3	Reserved area	Connected to expansion RAM
Internal main bus	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC, DTC, and extended bus master (EDMAC and SDSI) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC, DTC, and extended bus master (EDMAC, GLCDC, DRW2D, and SDSI) • Connected to on-chip memory (RAM, expansion RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)

Bus Type		RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Internal peripheral bus	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	• Reserved area	• Connected to peripheral modules (GLCDC, DRW2D) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash (in P/E) • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to the SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)

Table 2.7 Comparison of Addresses Assigned for Each Bus

Address	RX65N (CF ≤ 1 Mbyte)		RX65N (CF ≥ 1.5 Mbytes)	
	On-Chip ROM Enabled	On-Chip ROM Disabled	On-Chip ROM Enabled	On-Chip ROM Disabled
0000 0000h to 0007 FFFFh	Memory bus 1		Memory bus 1	
0008 0000h to 0008 7FFFh	Internal peripheral bus 1		Internal peripheral bus 1	
0008 8000h to 0009 FFFFh	Internal peripheral bus 2		Internal peripheral bus 2	
000A 0000h to 000B FFFFh	Internal peripheral bus 3		Internal peripheral bus 3	
000C 0000h to 000D FFFFh	Internal peripheral bus 4		Internal peripheral bus 4	
000E 0000h to 000F FFFFh	Reserved area		Internal peripheral bus 5	
0010 0000h to 007F FFFFh	Internal peripheral bus 6	Reserved area	Internal peripheral bus 6	Reserved area
0080 0000h to 00FF FFFFh	Reserved area		Memory bus 3	
0100 0000h to 07FF FFFFh	External bus		External bus	
0800 0000h to 0FFF FFFFh				
1000 0000h to 7FFF FFFFh	Reserved area		Reserved area	
8000 0000h to FEFF FFFFh	Memory bus 2	Reserved area	Memory bus 2	Reserved area
FF00 0000h to FFFF FFFFh		External bus		External bus

Table 2.8 Comparison of Bus Master Priorities

Priority	Internal Main Bus	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
High ↑ Low	—	EXDMAC	EXDMAC
	2	Extended bus master (1)	Extended bus master (2)
		DMAC	DMAC
		DTC	DTC
	1	CPU	CPU

Notes: 1. With RX65N (CF ≤ 1 Mbyte), the extended bus master consists of EDMAC and SDSI.
2. With RX65N (CF ≥ 1.5 Mbytes), the extended bus master consists of EDMAC, GLCDC, DRW2D, and SDSI.

Table 2.9 Comparison of Peripheral Modules Connected to Internal Peripheral Buses

Bus Type	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Internal peripheral bus 1	DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section	DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section
Internal peripheral bus 2	Peripheral modules other than those connected to internal peripheral buses 1, 3, 4, and 5	Peripheral modules other than those connected to internal peripheral buses 1, 3, 4, and 5
Internal peripheral bus 3	USBb, PDC, and standby RAM	USBb, PDC, and standby RAM
Internal peripheral bus 4	EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES	EDMAC, ETHERC, MTU3, SCIi, RSPI
Internal peripheral bus 5	Reserved area	GLCDC, DRW2D
Internal peripheral bus 6	Code flash memory (in P/E)	Code flash memory (in P/E) or data flash memory

Table 2.10 Comparison of External Bus Specifications

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
External address space	• An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. Separate bus: An 8 or 16-bit bus space is selectable. Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.	• An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • Bus width can be set for each area. Separate bus: An 8, 16, or 32-bit bus space is selectable. Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • An endian mode can be specified for each area.
CS area controller	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following: Timing of assertion and negation for chip-select signals (CS0# to CS7#) Timing of assertion of the read signal (RD#) and write signals (WR0#/WR# and WR1) Timing to start/end outputting data • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.	• Recovery cycles can be inserted. Read recovery: Up to 15 cycles Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles) • Wait control can be used to set up the following: Timing of assertion and negation for chip-select signals (CS0# to CS7#) Timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR3#) Timing to start/end outputting data • Write access mode: Single write strobe mode/byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
SDRAM area controller	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles	• Multiplexing output of row address/column address (8, 9, 10, or 11 bits) • Self-refresh and auto-Refresh selectable • CAS latency can be specified from one to three cycles
Write buffer function	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.	When write data from the bus master has been written to the write buffer, write access by the bus master is completed.
Frequency	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK). • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).	• The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK). • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Table 2.11 Comparison of Pin Configuration of the External Bus

Pin Name	I/O	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
A23 to A0	Output	Address output pins	Address output pins
D31 to D0	I/O	Data input/output pins D15 to D0 pins are enabled when the 16-bit bus space is specified. D7 to D0 pins are enabled when the 8-bit bus space is specified.	Data input/output pins D31 to D0 pins are enabled when the 32-bit bus space is specified. D15 to D0 pins are enabled when the 16-bit bus space is specified. D7 to D0 pins are enabled when the 8-bit bus space is specified.
BC0#	Output	The BC0# pin is enabled in single write strobe mode. The BC0# signal is a strobe signal and when the BC0# signal is low (accessing an external address space), it means that D7 to D0 are valid. When an 8-bit bus space is specified, this output pin is always held low regardless of write access mode.	The BC0# pin is enabled in single write strobe mode. The BC0# signal is a strobe signal and when the BC0# signal is low (accessing an external address space), it means that D7 to D0 are valid. When an 8-bit bus space is specified, this output pin is always held low regardless of write access mode.
BC1#	Output	The BC1# pin is enabled in single write strobe mode. The BC1# signal is a strobe signal and when the BC1# signal is low (accessing an external address space), it means that D15 to D8 are valid. This pin is not used when the 8-bit bus space is specified.	The BC1# pin is enabled in single write strobe mode. The BC1# signal is a strobe signal and when the BC1# signal is low (accessing an external address space), it means that D15 to D8 are valid. This pin is not used when the 8-bit bus space is specified.
BC2#	Output	—	The BC2# pin is enabled in single write strobe mode. The BC2# signal is a strobe signal and when the BC2# signal is low (accessing an external address space), it means that D23 to D16 are valid. This pin is not used when the 8- or 16-bit bus space is specified.
BC3#	Output	—	The BC3# pin is enabled in single write strobe mode. The BC3# signal is a strobe signal and when the BC3# signal is low (accessing an external address space), it means that D31 to D24 are valid. This pin is not used when the 8- or 16-bit bus space is specified.
CS0#	Output	A chip select signal for area 0 (CS0)	A chip select signal for area 0 (CS0)
CS1#	Output	A chip select signal for area 1 (CS1)	A chip select signal for area 1 (CS1)
CS2#	Output	A chip select signal for area 2 (CS2)	A chip select signal for area 2 (CS2)
CS3#	Output	A chip select signal for area 3 (CS3)	A chip select signal for area 3 (CS3)
CS4#	Output	A chip select signal for area 4 (CS4)	A chip select signal for area 4 (CS4)
CS5#	Output	A chip select signal for area 5 (CS5)	A chip select signal for area 5 (CS5)
CS6#	Output	A chip select signal for area 6 (CS6)	A chip select signal for area 6 (CS6)
CS7#	Output	A chip select signal for area 7 (CS7)	A chip select signal for area 7 (CS7)

Pin Name	I/O	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
RD#	Output	A strobe signal indicating that reading from an external address space (CS0 to CS7) is in progress	A strobe signal indicating that reading from an external address space (CS0 to CS7) is in progress
WR0#/WR#	Output	The WR0# pin is enabled in byte strobe mode. The WR0# signal is a strobe signal and when the WR0# signal is low (writing to an external address space), it means that D7 to D0 are valid. The WR# pin is enabled in single write strobe mode. The WR# signal is a strobe signal and indicates writing to an external address space is in progress. When an 8-bit bus space is specified, this output pin is held low during a write access regardless of write access mode.	The WR0# pin is enabled in byte strobe mode. The WR0# signal is a strobe signal and when the WR0# signal is low (writing to an external address space), it means that D7 to D0 are valid. The WR# pin is enabled in single write strobe mode. The WR# signal is a strobe signal and indicates writing to an external address space is in progress. When an 8-bit bus space is specified, this output pin is held low during a write access regardless of write access mode.
WR1#	Output	The WR1# pin is enabled in byte strobe mode. The WR1# signal is a strobe signal and when the WR1# signal is low (writing to an external address space), it means that D15 to D8 are valid. This pin is disabled in single write strobe mode. This pin is not used when the 8-bit bus space is specified.	The WR1# pin is enabled in byte strobe mode. The WR1# signal is a strobe signal and when the WR1# signal is low (writing to an external address space), it means that D15 to D8 are valid. This pin is disabled in single write strobe mode. This pin is not used when the 8-bit bus space is specified.
WR2#	Output	—	The WR2# pin is enabled in byte strobe mode. The WR2# signal is a strobe signal and when the WR2# signal is low (writing to an external address space), it means that D23 to D16 are valid. This pin is disabled in single write strobe mode. This pin is not used when the 8- or 16-bit bus space is specified.
WR3#	Output	—	The WR3# pin is enabled in byte strobe mode. The WR3# signal is a strobe signal and when the WR3# signal is low (writing to an external address space), it means that D31 to D24 are valid. This pin is disabled in single write strobe mode. This pin is not used when the 8- or 16-bit bus space is specified.
ALE	Output	Address latch signal when address/data multiplexed bus is selected.	Address latch signal when address/data multiplexed bus is selected.
WAIT#	Input	A wait request signal when accessing the external address space (CS0 to CS7) (Low: Wait request)	A wait request signal when accessing the external address space (CS0 to CS7) (Low: Wait request)

Pin Name	I/O	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
SDCLK	Output	SDRAM clock	SDRAM clock
CKE	Output	SDRAM clock enable signal	SDRAM clock enable signal
SDCS#	Output	SDRAM chip select signal	SDRAM chip select signal
RAS#	Output	SDRAM low address strobe signal	SDRAM low address strobe signal
CAS#	Output	SDRAM column address strobe signal	SDRAM column address strobe signal
WE#	Output	SDRAM write enable signal	SDRAM write enable signal
DQM0	Output	SDRAM I/O data mask enable signal for D7 to D0	SDRAM I/O data mask enable signal for D7 to D0
DQM1	Output	SDRAM I/O data mask enable signal for D15 to D8	SDRAM I/O data mask enable signal for D15 to D8
DQM2	Output	—	SDRAM I/O data mask enable signal for D23 to D16
DQM3	Output	—	SDRAM I/O data mask enable signal for D31 to D24

Table 2.12 Comparison of Bus Registers

Register	Bit Symbol	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
CSnCR	BSIZE[1:0]	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	External Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: A 32-bit bus space is selected 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
SDCCR	BSIZE[1:0]	SDRAM Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: Setting prohibited 1 0: An 8-bit bus space is selected 1 1: Setting prohibited	SDRAM Bus Width Select b5 b4 0 0: A 16-bit bus space is selected 0 1: A 32-bit bus space is selected 1 0: An 8-bit bus space is selected 1 1: Setting prohibited
EBMAPCR	—	—	Extended Bus Master Priority Control Register

2.6 I/O Ports

Table 2.13 lists the Comparison of I/O Port Functions and Table 2.14 lists the Comparison of I/O Port Registers.

Table 2.13 Comparison of I/O Port Functions

Port Symbol	Port	RX65N (CF ≤ 1 Mbyte)				RX65N (CF ≥ 1.5 Mbytes)			
		Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
PORT0	P00 to P02	✓	✓	Normal drive/ high drive/high-speed interface high-drive	—	✓	✓	Normal drive/ high drive/high-speed interface high-drive	—
	P03, P05	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P07	✓	✓	Fixed to high driving ability output	✓	✓	✓	Fixed to high driving ability output	✓
PORT1	P10	—	—	—	—	✓	✓	Fixed to high driving ability output	—
	P11	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓
	P12 to P14	✓	✓	Fixed to high driving ability output	✓	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓
	P15, P16	✓	✓	Fixed to high driving ability output	✓	✓	✓	Fixed to high driving ability output	✓
	P17	✓	✓	Fixed to high driving ability output	✓	✓	✓	High drive/high-speed interface high-drive	✓
PORT2	P20, P21	✓	✓	Fixed to high driving ability output	✓	✓	✓	High drive/high-speed interface high-drive	✓
	P22, P23	✓	✓	Fixed to high driving ability output	—	✓	✓	High drive/high-speed interface high-drive	—
	P24 to P26	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P27	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high speed interface high-drive	—
PORT3	P30, P31	✓	✓	High drive/high-speed interface high-drive	✓	✓	✓	High drive/high-speed interface high-drive	✓
	P32, P33	✓	✓	Fixed to high driving ability output	✓	✓	✓	Fixed to high driving ability output	✓

Port Symbol	Port	RX65N (CF ≤ 1 Mbyte)				RX65N (CF ≥ 1.5 Mbytes)			
		Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
PORT3	P34, P37	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P35	—	—	—	—	—	—	—	—
	P36	✓	✓	Fixed to normal output	—	✓	✓	Fixed to normal output	—
PORT4	P40 to P47	✓	✓	Fixed to normal output	—	✓	✓	Fixed to normal output	—
PORT5	P50 to P52, P56	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	P53	✓	✓	High drive/high-speed interface high-drive	—	✓	✓	High drive/high-speed interface high-drive	—
	P54, P55	✓	✓	High drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	P57	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORT6	P60 to P66	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P67	✓	✓	Fixed to high driving ability output	✓	✓	✓	Fixed to high driving ability output	✓
PORT7	P70, P73	✓	✓	High drive/high-speed interface high-drive	—	✓	✓	High drive/high-speed interface high-drive	—
	P71	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P72	✓	✓	Fixed to high driving ability output	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	P74 to P77	✓	✓	High drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORT8	P80 to P83	✓	✓	High drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	P84, P85	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—

Port Symbol	Port	RX65N (CF ≤ 1 Mbyte)				RX65N (CF ≥ 1.5 Mbytes)			
		Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
PORT8	P86	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—
	P87	✓	✓	Fixed to high driving ability output	—	✓	✓	High drive/high-speed interface high-drive	—
PORT9	P90 to P93	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	P94 to P97	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTA	PA0 to PA7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTB	PB0 to PB7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTC	PC0 to PC3	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓
	PC4 to PC7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTD	PD0 to PD7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTE	PE0 to PE7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTF	PF0 to PF4	—	—	—	—	✓	✓	Fixed to high driving ability output	—
	PF5	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—

Port Symbol	Port	RX65N (CF ≤ 1 Mbyte)				RX65N (CF ≥ 1.5 Mbytes)			
		Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
PORTG	PG0, PG1	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	PG2 to PG7	—	—	—	—	✓	✓	High drive/high-speed interface high-drive	—
PORTJ	PJ0 to PJ2	—	—	—	—	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
	PJ3, PJ5	✓	✓	Fixed to high driving ability output	—	✓	✓	Fixed to high driving ability output	—

Table 2.14 Comparison of I/O Port Registers

Port Symbol	Register	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
PORT1	DSCR	—	Drive Capacity Control Register
	DSCR2	—	Drive Capacity Control Register 2
PORT7	DSCR	—	Drive Capacity Control Register
PORT8	DSCR	—	Drive Capacity Control Register
PORT9	ODR1	—	Open-Drain Control Register 1
PORTF	ODR0	—	Open-Drain Control Register 0
PORTG	PDR	—	Port Direction Register
	PODR	—	Port Output Data Register
	PIDR	—	Port Input Register
	PMR	—	Port Mode Register
	ODR0	—	Open-Drain Control Register 0
	ODR1	—	Open-Drain Control Register 1
	PCR	—	Pull-Up Resistor Control Register
	DSCR	—	Drive Capacity Control Register
	DSCR2	—	Drive Capacity Control Register 2
PORTJ	DSCR	—	Drive Capacity Control Register
	DSCR2	—	Drive Capacity Control Register 2

2.7 Multi-Function Pin Controller

Table 2.15 lists the Comparison of Registers for the Multi-Function Pin Controller and Table 2.16 lists the Comparison of Settings for External Address Buses A16 to A23.

Table 2.15 Comparison of Registers for the Multi-Function Pin Controller

Register	Bit Name	MPC in RX65N (CF ≤ 1 Mbyte)	MPC in RX65N (CF ≥ 1.5 Mbytes)
PmnPFS	—	For details of the Pin Function Control register, refer to the User's Manual: Hardware listed in 5. Reference Documents.	
PFBCR0	DH32E	—	D16 to D31 Output Enable
	WR32BC32E	—	WR3#/BC3# and WR2#/BC2# Output Enable
PFBCR1	ALES	—	ALE Select
PFBCR2	—	—	External Bus Control Register 2
PFBCR3	—	—	External Bus Control Register 3

Table 2.16 Comparison of Settings for External Address Buses A16 to A23

PFBCR0		MPC in RX65N (CF ≤ 1 Mbyte)	MPC in RX65N (CF ≥ 1.5 Mbytes)
ADRHMS Bit	ADRHMS2 Bit		
0	0	Set PC0 to PC7.	Set PC0 to PC7.
0	1	Set PC0, PC1, P71, P72, P74, and PC5 to PC7.	Set PC0, PC1, P71, P72, P74, and PC5 to PC7.
1	0	Set P90 to P93. (No allocation of A20 to A23)	Set P90 to P97.
1	1	Setting prohibited.	Setting prohibited.

2.8 I²C-bus Interface

Table 2.17 lists the Comparison of Specifications for the I²C-bus Interface.

Table 2.17 Comparison of Specifications for the I²C-bus Interface

Item	RIICa in RX65N (CF ≤ 1 Mbyte)	RIICa in RX65N (CF ≥ 1.5 Mbytes)
Number of channels	2 channels	3 channels
Communications format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode Plus is supported (up to 1 Mbps)	Fast-mode Plus is supported (up to 1 Mbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (7-bit and 10-bit address fomats can be selected together). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (7-bit and 10-bit address fomats can be selected together). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of not-acknowledge. • For reception, the acknowledge bit is automatically transmitted. When selecting wait processing between the eighth and ninth clock cycles, response with the acknowledge field according to the received data can be controled by the software.	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of not-acknowledge. • For reception, the acknowledge bit is automatically transmitted. When selecting wait processing between the eighth and ninth clock cycles, response with the acknowledge field according to the received data can be controled by the software.
Wait function	In reception, the following periods of wait can be set by holding the SCL clock low: • Wait for the period between the eighth and ninth clock cycles • Wait for the period between the ninth clock cycle and the first clock cycle of the next transfer	In reception, the following periods of wait can be set by holding the SCL clock low: • Wait for the period between the eighth and ninth clock cycles • Wait for the period between the ninth clock cycle and the first clock cycle of the next transfer

Item	RIICa in RX65N (CF ≤ 1 Mbyte)	RIICa in RX65N (CF ≥ 1.5 Mbytes)
SDA output delay function	Output timing of the transmit data including the acknowledge bit can be delayed.	Output timing of the transmit data including the acknowledge bit can be delayed.
Arbitration	• For multi-master operation - The SCL clock can be synchronized if a conflict occurs with the SCL clock from another master. - When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. - In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of not-acknowledge due to non-matching of the internal signal for the SDA line and the level on the SDA line is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation - The SCL clock can be synchronized if a conflict occurs with the SCL clock from another master. - When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. - In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of not-acknowledge due to non-matching of the internal signal for the SDA line and the level on the SDA line is detectable. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events: Detection of arbitration, NACK, timeout, start condition including restart condition, or stop condition • Receive data full (including when slave addresses match) • Transmit data empty (including when slave addresses match) • Transmit end	Four sources: • Error in transfer or occurrence of events: Detection of arbitration, NACK, timeout, start condition including restart condition, or stop condition • Receive data full (including when slave addresses match) • Transmit data empty (including when slave addresses match) • Transmit end

Item	RIICa in RX65N (CF ≤ 1 Mbyte)	RIICa in RX65N (CF ≥ 1.5 Mbytes)
Low power consumption function	Transition to module stop state is available.	Transition to module stop state is available.
RIIC operating modes	• Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	• Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode
Event link function (output)	Four sources (RIIC0): • Error in transfer or occurrence of events: Detection of arbitration, NACK, timeout, start condition including restart condition, or stop condition • Receive data full (including when slave addresses match) • Transmit data empty (including when slave addresses match) • Transmit end	Four sources (RIIC0): • Error in transfer or occurrence of events: Detection of arbitration, NACK, timeout, start condition including restart condition, or stop condition • Receive data full (including when slave addresses match) • Transmit data empty (including when slave addresses match) • Transmit end

2.9 Boundary Scan

Table 2.18 lists the Comparison of Specifications for the Boundary Scan and Table 2.19 lists the Comparison of Registers for the Boundary Scan.

Table 2.18 Comparison of Specifications for the Boundary Scan

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Boundary scan enabled/disabled	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are dedicated for the JTAG when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). 145-pin TFLGA: P26/P27/P30/P31/P34	The following pins are dedicated for the JTAG when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). 177-pin TFLGA/176-pin LFBGA: PF0/PF1/PF2/PF3/PF4 145-pin TFLGA: P26/P27/P30/P31/P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.19 Comparison of Registers for the Boundary Scan

Register	Bit Name	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
JTIDR	DID[31:0]	ID code register Value after a reset: 0831 6447h	ID code register Value after a reset: 0835 9447h
JTBSR	—	For details on the boundary scan register (JTBSR), refer to the User's Manual: Hardware listed in 5. Reference Documents.	

2.10 RAM

Table 2.20 lists the Comparison of RAM Specifications and Table 2.21 lists the Comparison of RAM Registers.

Table 2.20 Comparison of RAM Specifications

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)	
	RAM	RAM	Expansion RAM
Capacity	256 Kbytes	256 Kbytes	384 Kbytes
Address	0000 0000h to 0003 FFFFh	0000 0000h to 0003 FFFFh	0080 0000h to 0085 FFFFh
Memory bus	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable	• Single-cycle access is possible for both reading and writing. • Enabling or disabling of the RAM is selectable.	
Data retention function	Not available in deep software standby mode	Not available in deep software standby mode	
Low power consumption function	The module-stop function can be spedified.	The module stop function can be specified separately for the RAM and expansion RAM	
Error checking	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	

Table 2.21 Comparison of RAM Registers

Register	Bit Name	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
EXRAMMODE	—	—	Expansion RAM Operating Mode Control Register
EXRAMSTS	—	—	Expansion RAM Error Status Register
EXRAMECAD	—	—	Expansion RAM Error Address Capture Register
EXRAMPRCR	—	—	Expansion RAM Protection Register

2.11 Flash Memory

Table 2.22 lists the Comparison of Specifications for the Code Flash Memory, Table 2.23 lists the Comparison of Specifications for the Data Flash Memory, Table 2.24 lists the Comparison of Registers for the Flash Memory, and Table 2.25 lists the Comparison of FCMDR Register Status after Receiving Commands.

Table 2.22 Comparison of Specifications for the Code Flash Memory

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Memory capacity	User area: 1 Mbyte max.	User area: 2 Mbytes max.
ROM cache	• Capacity: 256 Bytes max. • Mapping method: 8-way set associative • Replace method: LRU method • Line size: 16 bytes	• Capacity: 256 Bytes max. • Mapping method: 8-way set associative • Replace method: LRU method • Line size: 16 bytes
Read cycle	• When the cache is hit: One cycle • When the cache is missed while ROM cache operation is enabled, or when ROM cache operation is disabled: One cycle if ICLK ≤ 50 MHz Two cycles if 50 MHz < ICLK ≤ 100 MHz Three cycles if ICLK > 100 MHz	• When the cache is hit: One cycle • When the cache is missed while ROM cache operation is enabled, or when ROM cache operation is disabled: One cycle if ICLK ≤ 50 MHz Two cycles if 50 MHz < ICLK ≤ 100 MHz Three cycles if ICLK > 100 MHz
Value after erasure	FFh	FFh
Programming/erasing method	• Self-programming: The code flash memory can be programmed and erased, and the option-setting memory can be programmed with the FACI command specified in the area for issuing the FACI command (007E 0000h). • Serial programming: Programming and erasing by the serial programmer through the serial interface communication.	• Self-programming: The code flash memory can be programmed and erased, and the option-setting memory can be programmed with the FACI command specified in the area for issuing the FACI command (007E 0000h). • Serial programming: Programming and erasing by the serial programmer through the serial interface communication.
Security function	Protection against illicit tampering or reading the flash memory	Protection against illicit tampering or reading the flash memory
Protection	Protection against erroneous rewriting of the flash memory	Protection against erroneous rewriting of the flash memory
Dual bank function	—	The program can be updated safely with the dual bank structure even if programming is canceled. • Linear mode: The code flash memory is used as one area. • Dual mode: The code flash memory is divided into two areas.
Trusted memory (TM) function	Protection against illicit reading of the code flash memory: • Linear mode: blocks 8 and 9	Protection against illicit reading of the code flash memory • Linear mode: blocks 8 and 9 • Dual mode: blocks 8, 9 ,46, and 47

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Background operations (BGOs)	—	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.
Units of programming and erasure	Units of programming for the user area: 128 bytes Units of erasure for the user area: Block units	Units of programming for the user area: 128 bytes Units of erasure for the user area: Block units
Other functions	Interrupts can be accepted during self-programming	Interrupts can be accepted during self-programming.
	The startup area of the code flash memory is selectable from blocks 0 and 1.	The startup area of the code flash memory is selectable from blocks 0 and 1.
On-board programming (Serial programming/ Self-programming)	• Programming/erasure in boot mode (for the SCI interface) - The asynchronous serial interface (SCI1) is used - The transfer rate is adjusted automatically • Programming/erasure in boot mode (for the USB interface) - USBb is used - Dedicated hardware is not required, so direct connection to a PC is possible • Programming/erasure in boot mode (for the FINE interface) - FINE is used • Programming/erasure by self-programming - The code flash memory can be programmed and erased without resetting the system	• Programming/erasure in boot mode (for the SCI interface) - The asynchronous serial interface (SCI1) is used - The transfer rate is adjusted automatically • Programming/erasure in boot mode (for the USB interface) - USBb is used - Dedicated hardware is not required, so direct connection to a PC is possible • Programming/erasure in boot mode (for the FINE interface) - FINE is used • Programming/erasure by self-programming - The code flash memory can be programmed and erased without resetting the system
Off-board programming	Programming and erasure of the code flash memory and option-setting memory by using a parallel programmer is possible.	Programming and erasure of the code flash memory and option-setting memory by using a parallel programmer is possible.
Unique ID	16-byte ID code specific to each MCU	16-byte ID code specific to each MCU

Table 2.23 Comparison of Specifications for the Data Flash Memory

Item	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
Memory capacity	—	Data area: 32 Kbytes
Read cycle	—	Reading proceeds in every cycle of FCLK
Value after erasure	—	Undefined
Programming/erasing method	—	• Self-programming: The data flash memory can be programmed and erased with the FACI command specified in the area for issuing the FACI command (007E 0000h). • Serial programming: Programming and erasing by the serial programmer through the serial interface communication.
Security function	—	Protection against illicit tampering or reading the flash memory
Protection	—	Protection against erroneous rewriting of the flash memory
Background operations (BGOs)	—	• The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.
Units of programming and erasure	—	Unit of programming for the data area: 4 bytes Unit of erasure for the data area: 64/128/256 bytes
Other functions	—	Interrupts can be accepted during self-programming.
On-board programming (Serial programming/ Self-programming)	—	• Programming/erasure in boot mode (for the SCI interface) - The asynchronous serial interface (SCI1) is used. - The transfer rate is adjusted automatically. • Programming/erasure in boot mode (for the USB interface) - USBb is used. - Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (for the FINE interface) - FINE is used • Programming and erasure by self-programming - The flash memory can be programmed and erased without resetting the system.

Table 2.24 Comparison of Registers for the Flash Memory

Register	Bit Name	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
FWEPROR	FLWE[1:0]	Flash Programming and Erasure Enable b1 b0 0 0: Programming/erasure is disabled. 0 1: Programming/erasure is enabled. 1 0: Programming/erasure is disabled. 1 1: Programming/erasure is disabled.	Flash Programming and Erasure Enable b1 b0 0 0: Programming/erasure and blank checking are disabled. 0 1: Programming/erasure and blank checking are enabled. 1 0: Programming/erasure and blank checking are disabled. 1 1: Programming/erasure and blank checking are disabled.
FASTAT	DFAE	—	Data Flash Memory Access Violation Flag
FAEINT	DFAEIE	—	Data Flash Memory Access Violation Interrupt Enable
FEADDR	—	—	FACI Command End Address Register
FENTRYR	FENTRYD	—	Data Flash Memory P/E Mode Entry
FCMDR	CMDR[7:0] PCMDR[7:0]	Refer to Table 2.25 Comparison of FCMDR Register Status after Receiving Commands.	Refer to Table 2.25 Comparison of FCMDR Register Status after Receiving Commands.
FBCCNT	—	—	Data Flash Blank Check Control Register
FBCSTAT	—	—	Data Flash Blank Check Status Register
FPSADDR	—	—	Data Flash Programming Start Address Register
FSUACR	—	Start-Up Area Control Register	Start-Up Area Control Register Do not use this register when dual mode (MDE.BANKMD[2:0] = 000b) is selected. In dual mode, starting up proceeds from startup area 0.
EEPFCLK	—	—	Data Flash Memory Access Frequency Setting Register

Table 2.25 Comparison of FCMDR Register Status after Receiving Commands

Command	RX65N (CF ≤ 1 Mbyte)		RX65N (CF ≥ 1.5 Mbytes)	
	CMDR	FCMDR	CMDR	FCMDR
Programming	E8h	Previous command	E8h	Previous command
Block erase	D0h	20h	D0h	20h
Multi-block erase	—	—	D0h	21h
P/E suspend	B0h	Previous command	B0h	Previous command
P/E resume	D0h	Previous command	D0h	Previous command
Status clear	50h	Previous command	50h	Previous command
Forced stop	B3h	Previous command	B3h	Previous command
Blank check	—	—	D0h	71h
Configuration setting	40h	Previous command	40h	Previous command

3. Comparison of Pin Functions

Table 3.1 lists the Comparison of Pin Functions for 144/145 Pin Packages and Table 3.2 lists the Comparison of Pin Functions for 100 Pin Packages. The item which exists only in either of the product is indicated as blue text. Black text indicates there is no differences between the products.

Table 3.1 Comparison of Pin Functions for 144/145 Pin Packages

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
1	A1	AVSS0	AVSS0
2	B3	P05/IRQ13/DA1	P05/IRQ13/DA1
3	B1	AVCC1	AVCC1
4	D3	P03/IRQ11/DA0	P03/IRQ11/DA0
5	C1	AVSS1	AVSS1
6	C2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10/AN120
7	D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9 /AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9 /AN119
8	D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8 /AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8 /AN118
9	D2	PF5/IRQ4	PF5/IRQ4
10	E4	EMLE	EMLE
11	E3	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	A10	VSS	VSS
13	F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/C TS6#/RTS6/#SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/C TS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#
14	E2	VCL	VCL
15	F4	VBATT	VBATT
16	G3	MD/FINED	MD/FINED
17	F1	XCIN	XCIN
18	F2	XCOUT	XCOUT
19	G2	RES#	RES#
20	G1	P37/XTAL	P37/XTAL
21	C6	VSS	VSS
22	H1	P36/EXTAL	P36/EXTAL
23	B10	VCC	VCC
24	H4	P35/UPSEL/NMI	P35/UPSEL/NMI
25	J1	P34/TRST#/MTIOC0A/TMCI3/PO12/PO E10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/PO E10#/ET0_LINKSTA/SCK6/SCK0/IRQ4

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
26	J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/IRQ3-DS
27	J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS
28	K3	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	J4	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
30	K1	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
31	K2	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
32	L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SDHI_CD/HSYNC/ADTRG0#
33	L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SDHI_WP/PIXCLK
34	L2	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/SDHI_D1-C/PIXD7
35	M1	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/SDHI_D0-C/PIXD6
36	N1	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SDHI_CLK-C/PIXD5/IRQ9
37	N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SDHI_CMD-C/PIXD4/IRQ8
38	M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SDHI_D3-C/PIXD3/IRQ7/ADTRG1#
39	N3	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/PIXD2	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/SDHI_D2-C/PIXD2
40	L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0_OVRCURB/IRQ6/ADTRG0#
41	M3	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/PIXD1
42	K4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/CRX1-DS/PIXD0/IRQ5

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
43	N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
44	L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
45	M4	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
46	M5	VCC_USB	VCC_USB
47	N5	USB0_DM	USB0_DM
48	N6	USB0_DP	USB0_DP
49	M6	VSS_USB	VSS_USB
50	L6	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/SCK7
51	N7	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/CRX1/IRQ10	P55/TRDATA3/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/TXD7/SMOSI7/SSDA7/CRX1/IRQ10
52	K5	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	P54/TRDATA2/ALE/D1[A1/D1]/EDACK0/MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/RTS2#/SS2#/CTX1
53	K6	P53/BCLK	P53/BCLK
54	L7	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	K7	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
57	C13	VSS	VSS
58	L8	P83/TRCLK/EDACK1/MTIOC4C/ET0_CRS/RMII0_CRS_DV/SCK10/SS10#/CTS10#	P83/TRCLK/EDACK1/MTIOC4C/ET0_CRS/RMII0_CRS_DV/SCK10/SS10#/CTS10#
59	D5	VCC	VCC
60	N9	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/ET0_COL/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/MMC_D7-A/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/PO31/TOC0/CACREF/ET0_COL/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/MMC_D7-A/IRQ14
61	M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/MMC_D6-A/IRQ13
62	L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A/MMC_D5-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/ET0_ETXD2/SCK8/SCK10/RSPCKA-A/MMC_D5-A
63	N10	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/RMII0_TXD1/SMOSI10/SSDA10/TXD10/MMC_D4-A	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/ET0_ETXD1/RMII0_TXD1/SMOSI10/SSDA10/TXD10/MMC_D4-A
64	M9	P81/TRDATA1/EDACK0/MTIOC3D/PO27/ET0_ETXD0/RMII0_TXD0/SMISO10/SSCL10/RXD10/QIO3-A/SDHI_CD/MMC_D3-A	P81/TRDATA1/EDACK0/MTIOC3D/PO27/ET0_ETXD0/RMII0_TXD0/SMISO10/SSCL10/RXD10/QIO3-A/SDHI_CD/MMC_D3-A
65	K9	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/SDHI_WP/MMC_D2-A	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/ET0_TX_EN/RMII0_TXD_EN/SCK10/RTS10#/QIO2-A/SDHI_WP/MMC_D2-A

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
66	L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/SDSI_D1-A/MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/QMI-A/QIO1-A/SDHI_D1-A/SDSI_D1-A/MMC_D1-A
67	N11	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TCLKB/PO24/ET0_TX_ER/TXD5/SMOSI5/SSDA5/QMO-A/QIO0-A/SDHI_D0-A/SDSI_D0-A/MMC_D0-A
68	M10	P77/TRDATA7/CS7#/PO23/ET0_RX_ER/RMII0_RX_ER/SMOSI11/SSDA11/TXD11/QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/MMC_CLK-A	P77/TRDATA7/CS7#/PO23/ET0_RX_ER/RMII0_RX_ER/SMOSI11/SSDA11/TXD11/QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/MMC_CLK-A
69	K10	P76/TRDATA6/CS6#/PO22/ET0_RX_CLK/REF50CK0/SMISO11/SSCL11/RXD11/QSSL-A/SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A	P76/TRDATA6/CS6#/PO22/ET0_RX_CLK/REF50CK0/SMISO11/SSCL11/RXD11/QSSL-A/SDHI_CMD-A/SDSI_CMD-A/MMC_CMD-A
70	L11	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SSLA3-A/SDHI_D3-A/SDSI_D3-A/MMC_CD-A	PC2/A18/MTIOC4B/TCLKA/PO21/ET0_RX_DV/RXD5/SMISO5/SSCL5/SSLA3-A/SDHI_D3-A/SDSI_D3-A/MMC_CD-A
71	N12	P75/TRSYNC1/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/MMC_RES#-A	P75/TRSYNC1/CS5#/PO20/ET0_ERXD0/RMII0_RXD0/SCK11/RTS11#/SDHI_D2-A/SDSI_D2-A/MMC_RES#-A
72	N13	P74/TRDATA5/A20/CS4#/PO19/ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#	P74/TRDATA5/A20/CS4#/PO19/ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#
73	M12	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/ET0_ERXD2/SCK5/SSLA2-A/IRQ12
74	D11	VCC	VCC
75	M11	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/ET0_ERXD3/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14
76	E1	VSS	VSS
77	L12	P73/TRDATA4/CS3#/PO16/ET0_WOL	P73/TRDATA4/CS3#/PO16/ET0_WOL
78	K11	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SDSI_D1-B
79	K12	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SDSI_D0-B
80	K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/ET0_ETXD0/RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/ET0_ETXD0/RMII0_TXD0/SCK9/SCK11/SDSI_CLK-B/LCD_CLK-B
81	J11	PB4/A12/TIOCA4/PO28/ET0_TX_EN/RMII0_TXD_EN/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SDSI_CMD-B	PB4/A12/TIOCA4/PO28/ET0_TX_EN/RMII0_TXD_EN/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SDSI_CMD-B/LCD_TCON0-B
82	J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/LCD_TCON1-B

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
83	J12	PB2/A10/TIOCC3/TCLKC/PO26/ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B	PB2/A10/TIOCC3/TCLKC/PO26/ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/LCD_TCON2-B
84	J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/LCD_TCON3-B/IRQ4-DS
85	H10	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC
86	H11	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO
87	H12	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/LCD_DATA0-B/IRQ12
88	H13	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/LCD_DATA1-B
89	G11	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/SS5#/MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/SS5#/MOSIA-B/LCD_DATA2-B
90	G10	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_LINKSTA/RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_LINKSTA/RSPCKA-B/LCD_DATA3-B
91	G12	VCC	VCC
92	G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/SSLA0-B/LCD_DATA4-B/IRQ5-DS
93	F11	VSS	VSS
94	F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/SSCL5/LCD_DATA5-B/IRQ6-DS
95	F13	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/LCD_DATA6-B
96	F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/ET0_WOL/SCK5/SSLA2-B/LCD_DATA7-B/IRQ11
97	E10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/SSLA1-B	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/SSLA1-B/LCD_DATA8-B
98	E13	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/DQM1/CS7#/MTIOC7C/IRQ15
99	E11	P66/DQM0/CS6#/MTIOC7D	P66/DQM0/CS6#/MTIOC7D
100	E12	P65/CKE/CS5#	P65/CKE/CS5#
101	D10	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/MISOB-B/SDHI_WP/MMC_RES#-B/LCD_DATA9-B/IRQ7/AN105
102	D13	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
103	H2	VCC	VCC
104	C12	P70/SDCLK	P70/SDCLK
105	H3	VSS	VSS

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
106	D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/LCD_DATA11-B/IRQ5/AN103
107	B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/LCD_DATA12-B/AN102
108	A13	PE3/D11[A11/D11]/MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/RTS12#/SS12#/MMC_D7-B /AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/CTS12#/RTS12#/SS12#/MMC_D7-B/LCD_DATA13-B/AN101
109	B12	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/LCD_DATA14-B/IRQ7-DS/AN100
110	A12	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/LCD_DATA15-B/ANEX1
111	C11	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/LCD_DATA16-B/ANEX0
112	D9	P64/WE#/CS4#	P64/WE#/D3[A3/D3]/CS4#
113	C10	P63/CAS#/CS3#	P63/CAS#/D2[A2/D2]/CS3#
114	A11	P62/RAS#/CS2#	P62/RAS#/D1[A1/D1]/CS2#
115	B11	P61/SDCS#/CS1#	P61/SDCS#/D0[A0/D0]/CS1#
116	L13	VSS	VSS
117	D8	P60/CS0#	P60/CS0#
118	K8	VCC	VCC
119	C9	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B/LCD_DATA17-B/IRQ7/AN107
120	A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/IRQ6/AN106
121	D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/MMC_CLK-B/LCD_DATA19-B/IRQ5/AN113
122	B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/QSSL-B/SDHI_CMD-B/MMC_CMD-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/QSSL-B/SDHI_CMD-B/MMC_CMD-B/LCD_DATA20-B/IRQ4/AN112
123	C8	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/AN111
124	A8	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
125	C7	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109

144 Pin LFQFP	145 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
126	B8	PD0/D0[A0/D0]/POE4#/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/ LCD_EXTCLK-B/IRQ0/AN108
127	D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/ AN117
128	A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ AN116
129	B7	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
130	N8	VSS	VSS
131	A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/AN114
132	M13	VCC	VCC
133	B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	B4	VREFL0	VREFL0
141	A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	C3	VREFH0	VREFH0
143	B2	AVCC0	AVCC0
144	A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
-	G4	BSCANP	BSCANP

Table 3.2 Comparison of Pin Functions for 100 Pin Packages

100 Pin LFQFP	100 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
1	A2	AVCC1	AVCC1
2	B1	EMLE	EMLE
3	C2	AVSS1	AVSS1
4	C3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#
5	C1	VCL	VCL
6	D4	VBATT	VBATT
7	D3	MD/FINED	MD/FINED
8	D1	XCIN	XCIN
9	D2	XCOUT	XCOUT
10	E3	RES#	RES#
11	E1	P37/XTAL	P37/XTAL
12	E2	VSS	VSS
13	F1	P36/EXTAL	P36/EXTAL
14	F2	VCC	VCC
15	F3	P35/UPSEL/NMI	P35/UPSEL/NMI
16	E4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4
17	G1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/CRX0/IRQ3-DS
18	F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCIC2/RTCOUT/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	G2	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	G3	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	G4	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
22	H1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/MOSIB-A
23	H2	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	J1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN
25	K1	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/SS0#
26	K2	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	J2	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/IRQ9

100 Pin LFQFP	100 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
28	K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/ TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/ TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/ IRQ8
29	J3	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIO CB0/TCLKD/TMO1/PO15/POE8#/SCK1 /TXD3/SMOSI3/SSDA3/SDA2-DS/ IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIO CB0/TCLKD/TMO1/PO15/POE8#/SCK1 /TXD3/SMOSI3/SSDA3/SDA2-DS/ IRQ7/ADTRG1#
30	H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCL KC/TMO2/PO14/RTCOUT/TXD1/SMOS I1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0 _OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCL KC/TMO2/PO14/RTCOUT/TXD1/SMOS I1/SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/USB0_VBUSEN/USB0_VBUS/USB0 _OVRCURB/IRQ6/ADTRG0#
31	H4	P15/MTIOC0B/MTCLKB/TIOCB2/TCLK B/TMCI2/PO13/RXD1/SMISO1/SSCL1/ SCK3/CRX1-DS/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLK B/TMCI2/PO13/RXD1/SMISO1/SSCL1/ SCK3/CRX1-DS/IRQ5
32	K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLK A/TMRI2/PO15/CTS1#/RTS1#/SS1#/ CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLK A/TMRI2/PO15/CTS1#/RTS1#/SS1#/ CTX1/USB0_OVRCURA/IRQ4
33	J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TX D2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TX D2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#
34	F5	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2
35	J6	VCC_USB	VCC_USB
36	K5	USB0_DM	USB0_DM
37	K6	USB0_DP	USB0_DP
38	J5	VSS_USB	VSS_USB
39	H5	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/ ET0_EXOUT/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC 4D/TMO3/ET0_EXOUT/CRX1/IRQ10
40	H6	P54/ALE/EDACK0/MTIOC4B/TMCI1/ET 0_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B /TMCI1/ET0_LINKSTA/CTS2#/RTS2#/ SS2#/CTX1
41	G5	P53/BCLK	P53/BCLK
42	G6	P52/RD#/RXD2/SMISO2/SSCL2/ SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/ SSLB3-A
43	K7	P51/WR1#/BC1#/WAIT#/SCK2/ SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/ SSLB2-A
44	J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2 /SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2 /SSLB1-A
45	H7	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/IRQ14
46	H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/TM CI2/PO30/TIC0/ET0_ETXD3/RXD8/SMI SO8/SSCL8/SMISO10/SSCL10/RXD10/ MOSIA-A/IRQ13	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/M TCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/ SSCL10/RXD10/MOSIA-A/IRQ13
47	K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCL KD/TMRI2/PO29/ET0_ETXD2/SCK8/ SCK10/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIO C3B/MTCLKD/TMRI2/PO29/ET0_ETXD 2/SCK8/SCK10/RSPCKA-A
48	J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/TM CI1/PO25/POE0#/ET0_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/SS10#/CTS10#/ RTS10#/SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TM CI1/PO25/POE0#/ET0_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/SS10#/CTS10#/ RTS10#/SSLA0-A
49	K9	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5

100 Pin LFQFP	100 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
50	K10	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A
51	J10	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12
52	J9	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/ SSLA1-A/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/ SSLA1-A/IRQ14
53	H10	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0 _CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TIOCB5/PO31/ET0 _CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B
54	H9	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0 _ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0 _ETXD1/RMII0_TXD1/RXD9/SMISO9/ SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B
55	G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/RMII 0_TXD0/SCK9/SCK11/SDSI_CLK-B	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/RMII 0_TXD0/SCK9/SCK11/SDSI_CLK-B/ LCD_CLK-B
56	G8	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B
57	F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ ER/RMII0_RX_ER/SCK6/SDSI_D3-B	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ ER/RMII0_RX_ER/SCK6/SDSI_D3-B/ LCD_TCON1-B
58	F7	PB2/A10/TIOCC3/TCLKC/PO26/ET0_R X_CLK/REF50CK0/CTS6#/RTS6#/SS6# /SDSI_D2-B	PB2/A10/TIOCC3/TCLKC/PO26/ET0_R X_CLK/REF50CK0/CTS6#/RTS6#/SS6# /SDSI_D2-B/LCD_TCON2-B
59	G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/T MCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/T MCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD6/SMOSI6/SSDA6/LCD_TCON3-B/ IRQ4-DS
60	G10	VCC	VCC
61	F8	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_E RXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/ET0_E RXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/LCD_DATA0-B/IRQ12
62	F10	VSS	VSS
63	F9	PA7/A7/TIOCB2/PO23/ET0_WOL/ MISOA-B	PA7/A7/TIOCB2/PO23/ET0_WOL/ MISOA-B/LCD_DATA1-B
64	E7	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMC I3/PO22/POE10#/ET0_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMC I3/PO22/POE10#/ET0_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA-B/LCD_DATA2-B
65	E9	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_ LINKSTA/RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ET0_ LINKSTA/RSPCKA-B/LCD_DATA3-B
66	E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TM RI0/PO20/ET0_MDC/TXD5/SMOSI5/SS DA5/SSLA0-B/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TM RI0/PO20/ET0_MDC/TXD5/SMOSI5/SS DA5/SSLA0-B/LCD_DATA4-B/IRQ5-DS
67	E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/T CLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/T CLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B/IRQ6-DS
68	E6	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5 /SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5 /SSCL5/SSLA3-B/LCD_DATA6-B

100 Pin LFQFP	100 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
69	D9	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/ SSLA2-B/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/ SSLA2-B/LCD_DATA7-B/IRQ11
70	D10	PA0/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B	PA0/BC0#/A0/MTIOC4A/MTIOC6D/ TIOCA0/PO16/CACREF/ET0_TX_EN/R MII0_TXD_EN/SSLA1-B/LCD_DATA8-B
71	D8	PE7/D15[A15/D15]/MTIOC6A/TOC1/MI SOB-B/SDHI_WP/MMC_RES#-B/ IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6 A/TOC1/MISOB-B/ SDHI_WP/MMC_RES#-B/ LCD_DATA9-B/IRQ7/AN105
72	D7	PE6/D14[A14/D14]/MTIOC6C/TIC1/MO SIB-B/SDHI_CD/MMC_CD-B/ IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6 C/TIC1/MOSIB-B/SDHI_CD/MMC_CD-B/LCD_DATA10-B/IRQ6/AN104
73	C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B /ET0_RX_CLK/REF50CK0/RSPCKB-B/ IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4 C/MTIOC2B/ET0_RX_CLK/REF50CK0/ RSPCKB-B/LCD_DATA11-B/ IRQ5/AN103
74	C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A /PO28/ET0_ERXD2/SSLB0-B/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4 D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/LCD_DATA12-B/AN102
75	B10	PE3/D11[A11/D11]/MTIOC4B/PO26/TO C3/POE8#/ET0_ERXD3/CTS12#/RTS1 2#/SS12#/MMC_D7-B/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4 B/PO26/TOC3/POE8#/ET0_ERXD3/CT S12#/RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B/AN101
76	A10	PE2/D10[A10/D10]/MTIOC4A/PO23/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/ AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4 A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B/IRQ7-DS/AN100
77	A9	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO 18/TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/SSLB2-B/MMC_D5-B/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSD A12/TXDX12/SIOX12/SSLB2-B/ MMC_D5-B/LCD_DATA15-B/ANEX1
78	A8	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB 1-B/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B/ANEX0
79	B9	PD7/D7[A7/D7]/MTIC5U/POE0#/ SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/ SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B/IRQ7/ AN107
80	B8	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE 4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE 4#/SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B/ IRQ6/AN106
81	C8	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B/IRQ5/AN113
82	A7	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B/IRQ4/ AN112
83	B7	PD3/D3[A3/D3]/MTIOC8D/TOC2/ POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/TOC2/ POE8#/RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/LCD_DATA21-B/IRQ3/ AN111

100 Pin LFQFP	100 Pin TFLGA	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
84	C7	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/LCD_DATA22-B/IRQ2/AN110
85	B6	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/CTX0/LCD_DATA23-B/IRQ1/AN109
86	A6	PD0/D0[A0/D0]/POE4#/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/LCD_EXTCLK-B/IRQ0/AN108
87	C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	A4	VREFL0	VREFL0
95	B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	C4	VREFH0	VREFH0
97	B3	AVCC0	AVCC0
98	A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	B2	AVSS0	AVSS0
100	A1	P05/IRQ13/DA1	P05/IRQ13/DA1

4. Important Information when Replacing the MCU

4.1 Address Space

4.1.1 Code Flash Memory

RX65N (CF ≥ 1.5 Mbytes) has two modes for handling the code flash memory; linear mode which uses the code flash memory as one area and dual mode which divides the code flash memory into two areas. Note that dual mode is not included in RX65N (CF ≤ 1 Mbyte).

Table 4.1 lists the Comparison of Code Flash Memory.

Table 4.1 Comparison of Code Flash Memory

Mode	RX65N (CF ≤ 1 Mbyte)			RX65N (CF ≥ 1.5 Mbytes)	
	512 Kbytes	768 Kbytes	1 Mbyte	1.5 Mbytes	2 Mbytes
Linear mode	FFF8 0000h to FFFF FFFFh	FFF4 0000h to FFFF FFFFh	FFF0 0000h to FFFF FFFFh	FFE8 0000h to FFFF FFFFh	FFE0 0000h to FFFF FFFFh
Dual mode (BANKSEL.BANKSWP[2:0] (1) = 111b)	—			Bank 1: FFE4 0000h to FFEF FFFFh	Bank 1: FFE0 0000h to FFEF FFFFh
				Bank 0: FFF4 0000h to FFFF FFFFh	Bank 0: FFF0 0000h to FFFF FFFFh

Note: 1. BANKSEL is the bank select register of the option-setting memory.
Only RX65N (CF ≥ 1.5 Mbytes) can use the bank select register (BANKSEL). BANKSEL is a reserved area in RX65N (CF ≤ 1 Mbyte).

4.1.2 Data Flash Memory

Only RX65N (CF ≥ 1.5 Mbytes) has the data flash memory.

Table 4.2 lists the Comparison of Data Flash Memory.

Table 4.2 Comparison of Data Flash Memory

RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
—	32 Kbytes 0010 0000h to 0010 7FFFh

4.1.3 RAM

Only RX65N (CF ≥ 1.5 Mbytes) has the expansion RAM.

Table 4.3 lists the Comparison of the Expansion RAM.

Table 4.3 Comparison of the Expansion RAM

	RX65N (CF ≤ 1 Mbyte)	RX65N (CF ≥ 1.5 Mbytes)
RAM	256 Kbytes 0000 0000h to 0003 FFFFh	256 Kbytes 0000 0000h to 0003 FFFFh
Expansion RAM	—	384 Kbytes 0080 0000h to 0085 FFFFh

4.2 Notes on Pin Design

4.2.1 General Input/Output Ports

PORTG is include in RX65N (CF ≥ 1.5 Mbytes) only.
When using 177/176-pin package of RX65N (CF ≥ 1.5 Mbytes) and PORTG is not used, or when using 100/144/145-pin package of RX65N (CF ≥ 1.5 Mbytes), PORTG must be processed as an unused pin.
The PDR register for PORTG must not be accessed in RX65N (CF ≤ 1 Mbyte) as it does not have PORTG.
For processing unused pins, refer to the RX65N Group, RX651 Group User's Manual: Hardware listed in 5. Reference Documents.

4.2.2 A/D Conversion During Accessing an External Bus

When performing A/D conversion during accessing an external bus, the accuracy may become worse.

In this case, some measure has to be taken by the software, e.g., perform A/D conversion multiple times, discard the maximum and minimum values of the A/D conversion results, and then take the average of rest of the A/D conversion values.

With RX65N (CF ≥ 1.5 Mbytes), the accuracy of A/D conversion can be held in some measure by changing the assignment of the external data bus. For details, refer to the RX65N Group, RX651 Group User's Manual: Hardware listed in 5. Reference Documents.

4.3 Notes on Configuring Functions

4.3.1 Option-Setting Memory

For RX65N (CF ≤ 1 Mbyte), dual mode cannot be selected with the bank mode select bits (BANKMD[2:0]) in the endian select register (MDE). When programming these bits, write 111b (linear mode).

Also, the dual-bank TM enable bit (TMEFDB[2:0]) in the TM enable flag register (TMEF) are reserved bits in RX65N (CF ≤ 1 Mbyte). When reading these bits, the value programmed by the user is read. When programming these bits, write 111b.

The bank select register (BANKSEL) can be used only in RX65N (CF ≥ 1.5 Mbytes).

The bank select register (BANKSEL) is a reserved area in RX65N (CF ≤ 1 Mbyte).

For details on the option-setting memory, refer to the RX65N Group, RX651 Group User's Manual: Hardware listed in 5. Reference Documents.

4.3.2 Switching of Driving Ability

Switching of driving ability for pins may differ between RX65N (CF ≤ 1 Mbyte) and RX65N (CF ≥ 1.5 Mbytes) even for the same pin.

For details on switching of driving ability, refer to the RX65N Group, RX651 Group User's Manual: Hardware listed in 5. Reference Documents.

4.3.3 RAM Error Interrupt Function

With RX65N (CF ≥ 1.5 Mbytes), when either of the RAMSTS.RAMERR flag (indicates a parity check error) or the EXRAMSTS.EXRAMERR flag (indicates an expansion RAM parity check error) is changed to 1, the RAM error interrupt occurs.

With RX65N (CF ≤ 1 Mbyte), when the RAMSTS.RAMERR flag (indicates parity check error) is changed to 1 while the parity check is enabled, the RAM error interrupt occurs.

The RAM error interrupt is cleared by writing 0 to the flags described above.

4.3.4 Rewriting with Self-Programming

The BGO function is available only in RX65N (CF ≥ 1.5 Mbytes). If the MCU used does not support the BGO function, the program for rewriting needs to be transferred to the internal RAM or the external memory before executing the program.

For details on self-programming, refer to RX65N Group, RX651 Group User's Manual: Hardware and Flash Memory User's Manual: Hardware listed in 5. Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Rev.2.00 (R01UH0602)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates.

None

Website and Support

Renesas Electronics Website

http://www.renesas.com/

Inquiries

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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