RX630 Group

Independent Watchdog Timer (Autostart Mode)

R01AN0594EJ0100
Rev.1.00
Dec 13, 2011

Introduction

This application note describes setting up an independent watchdog timer (in autostart mode) for RX630 Group products.

Target Device

RX630 Group

This application note can also be used with other RX family microcontrollers that have the same I/O registers (peripheral unit control registers) as the RX630 Group products. Note, however, that since there are changes between devices, such as additional functionality in certain functions, these operations must be verified with the manual for the device actually used. When using the methods described in this application note, full testing in the actual user system is required.

Contents

1. Specifications

This sample program operates an independent watchdog timer (in autostart mode) using option selection memory.

Table 1.1 lists the peripheral functions used and their uses.

Table 1.1 Peripheral Functions and their Uses

Peripheral Function	Use
Independent watchdog timer	This watchdog timer operates independently of the earlier watchdog timer used to detect software runaway.
Option setting memory	Registers that select the microcontroller state after a reset.

2. Conditions of Checking the Operation of the Software

The sample code described in this application note has been confirmed to run normally under the operating conditions given below.

Table 2.1 Operating Conditions

Item	Description
MCU	RX630 (R5F5630EDDFP)
Memory used for evaluation	Xin clock: 12 MHz Subclock: 32.768 kHz
Operating voltage	3.3 V
Integrated development environment	Version 4.09.00.007
C compiler	RX Standard Toolchain (V.1.0.1.0) C/C++ compiler package for RX family V.1.01.00
	Compiler options: The default settings for the integrated development environment are used.
Operating mode	Single chip mode
Version of the sample code	Version 1.30
Board used	R0K505630C001BR

3. Software Description

3.1 Operation Overview

This sample program supports OFS0 (option function selection register 0) and the IWDT register.

This application shows the correspondence between the down counter that uses OFS0, reset or interrupt output control, and count stop control, and the IWDTCR (IWDT control register), IWDTRCR (IWDT reset control register), and IWDTCSTPR (IWDT count stop control register) registers. The enable/disable switching provided by OFS0 and IWDTCR, IWDTRCR, and IWDTCSTPR register control is controlled by the OFS0.IWDTSTRT bit (IWDT start mode selection bit) in option function selection register 0.

Note that the OFS0 register settings must remain fixed during IWDT operation.

3.2 File Structure

Table 3.1 lists the files used in the sample code.

Table 3.1 File Structure

File Name	Function	Notes
main_setclock.c	The main processing	
dbsct.c	B and R section settings	File automatically generated by the IDE
intprg.c	Interrupt handling (The SCI interrupt handler, which is used by this program, has been removed from this file.)	File automatically generated by the IDE
resetprg.c	Reset handling	File automatically generated by the IDE
sbrk.c	sbrk() function	File automatically generated by the IDE
vecttbl.c	Vector table related processing	File automatically generated by the IDE to which option and memory settings have been added
iodefine.h	I/O register related header file	
lowsrc.h	I/O streams related header file	File automatically generated by the IDE
sbrk.h	sbrk() function header file	File automatically generated by the IDE
stacksct.h	Stack area header file	File automatically generated by the IDE
typedefine.h	Integer type definitions header file	File automatically generated by the IDE
vect.h	Vector table related header file	File automatically generated by the IDE

3.3 Constants

Table 3.2 lists the constants used by the sample code.

Table 3.2 Constants Used in the Sample Code

Constant	Set Value	Description
Option function selection register 0	0xFFFFFFFD	• After a reset, the WDT will be in the stopped state. • After a reset, the IWDT automatically starts in autostart mode. • The IWDT timeout period is 16,384 cycles. • The IWDT clock divisor is 128. • The IWDT window end position is not set. • The IWDT window start position is not set. • Reset by the IWDT reset interrupt request is enabled. • IWDT sleep mode count stop control is enabled.

3.4 Variables

Table 3.3 lists the global variables.

Table 3.3 Global Variables

Type	Name	Description	Functions Where Used
None			

3.5 Functions

Table 3.4 lists the functions defined in the sample code.

Table 3.4 Functions

Function Name	Overview
Mcu_init	CPU initialization
opemode_init	Operating mode settings
clock_setting	CPU clock settings
peripheral_init	Peripheral function initialization
MTU3_init	16-bit timer MTU2A channel 3 initialization

3.6 Function Specifications

This section lists the specifications of the functions in the sample code.

Name	mcu_init
Overview	CPU initialization
Header	Iodefine.h
Declaration	void mcu_init(void)
Description	
Arguments	None
Return values	None
Notes	

Name	clock_setting
Overview	Sets the CPU clock.
Header	Iodefine.h
Declaration	void clock_setting(void)
Description	• Stops the subclock oscillator. • Stops the high-speed clock oscillator. • Sets the oscillator stabilization time for the main clock oscillator to 131,072 cycles. • Sets the PLL oscillator stabilization time to 4,194,304 cycles. • Sets the PLL frequency multiplier to 16x. • Sets the main clock oscillator to the operating state. • Sets the PLL circuit to the operating state. • Sets the system clock to divided by 2, the FlashIF clock to divided by 4, the external bus clock to divided by 4, and the peripheral module clock to divided by 4. • Sets the clock source to be the PLL circuit.
Arguments	None
Return values	None
Notes	

Name	peripheral_init
Overview	Peripheral function initialization
Header	Iodefine.h
Declaration	void peripheral_init(void)
Description	• Clears the MTU2A unit 0 module stop state. • Initializes the 16-bit timer MTU2A channel 3.
Arguments	None
Return values	None
Notes	

Name	MTU3_init
Overview	16-bit timer MTU2A channel 3 initialization
Header	Iodefine.h
Declaration	void MTU3_init(void)
Description	• Sets the P17 pin mode to MTU2A channel 3 output compare output. • Sets the MTU2A channel 3 count clock to be PLCK divided by 16, to count on rising edges, and to be cleared by compare match A. • Sets the MTU2A channel 3 compare match outputs such that compare match A has an initial output of 0 and is toggled by a compare match and compare match B output to be stopped. • Clears the MTU2A channel 3 timer counter. • Sets the MTU2A channel 3 compare match counter to 0xFFF0. • Sets the MTU2A channel 3 operating mode to normal operation. • Of the MTU2A channel 3 interrupts, enables TGR interrupt enable A. • Sets the MTU2A channel 3 TGR interrupt enable A interrupt level to level 4. • Starts MTU2A channel 3 operation.
Arguments	None
Return values	None
Notes	

3.7 Flowcharts

3.7.1 Main Processing

Figure 3.1 shows the main processing flowchart.

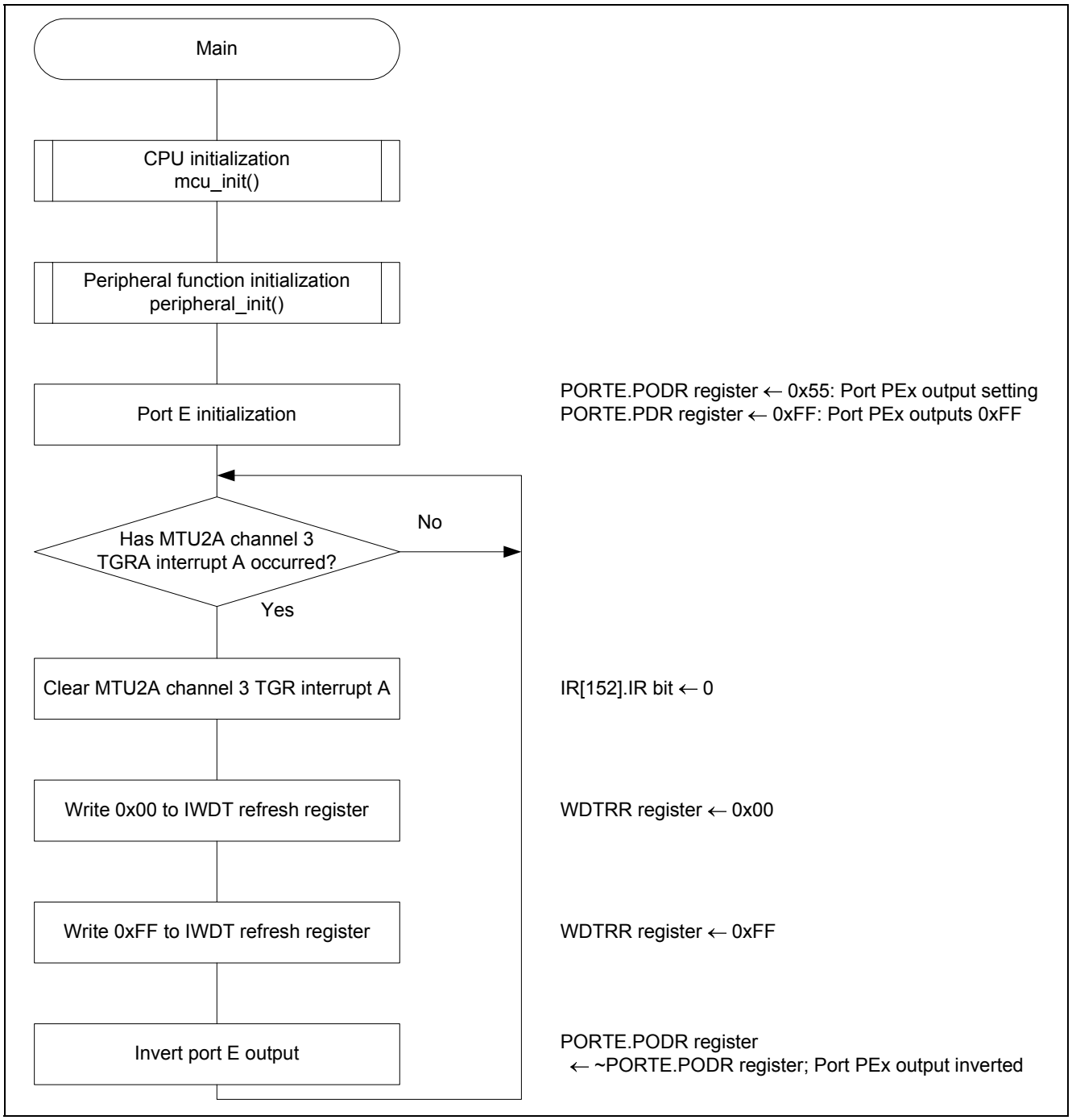

Figure 3.1 Main Processing

3.7.2 CPU Initialization

Figure 3.2 shows the flowchart for CPU initialization.

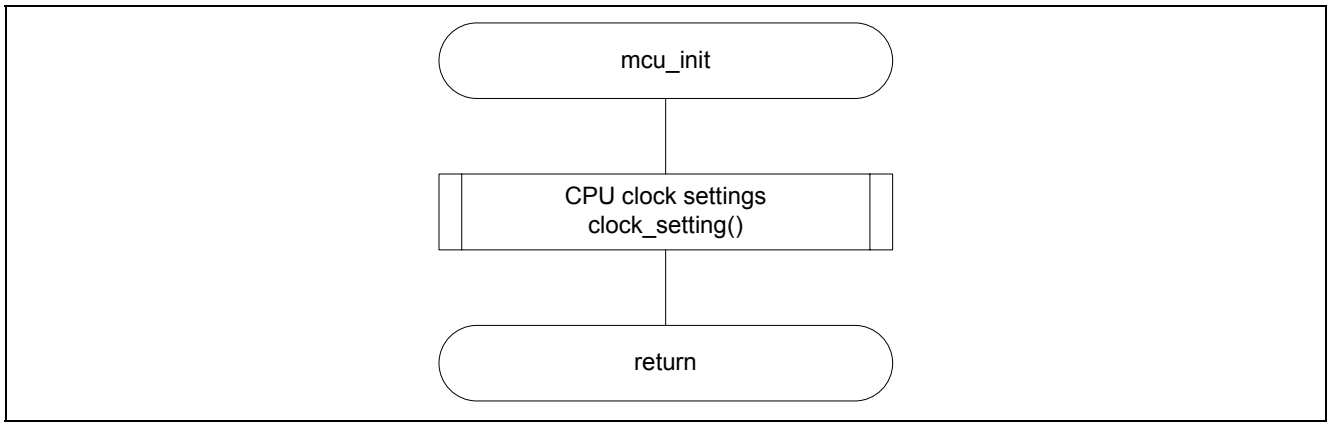

Figure 3.2 CPU Initialization

3.7.3 CPU Clock Settings

Figure 3.3 shows the flowchart for the CPU clock settings.

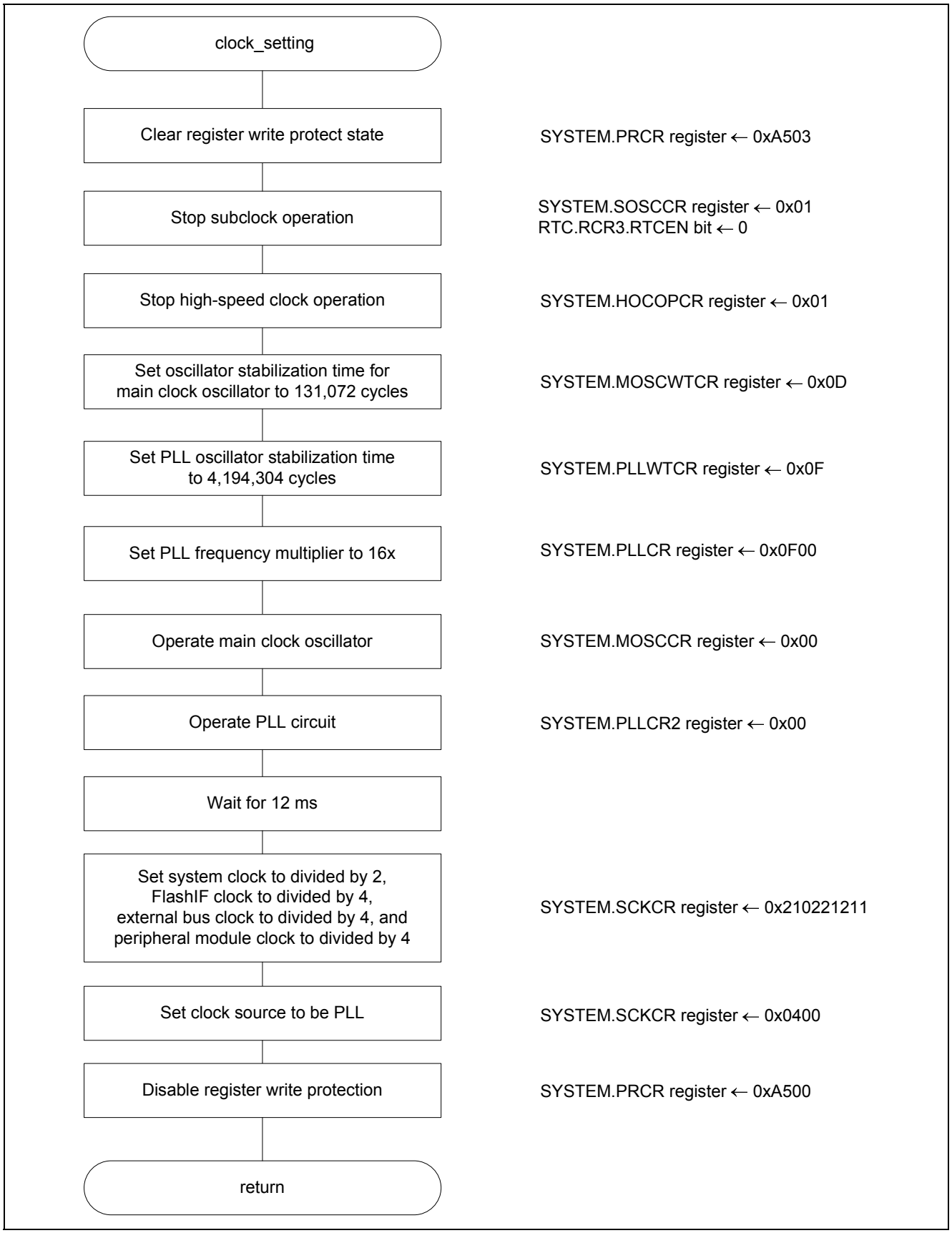

Figure 3.3 CPU Clock Settings

3.7.4 Peripheral Function Initialization

Figure 3.4 shows the flowchart for peripheral function initialization.

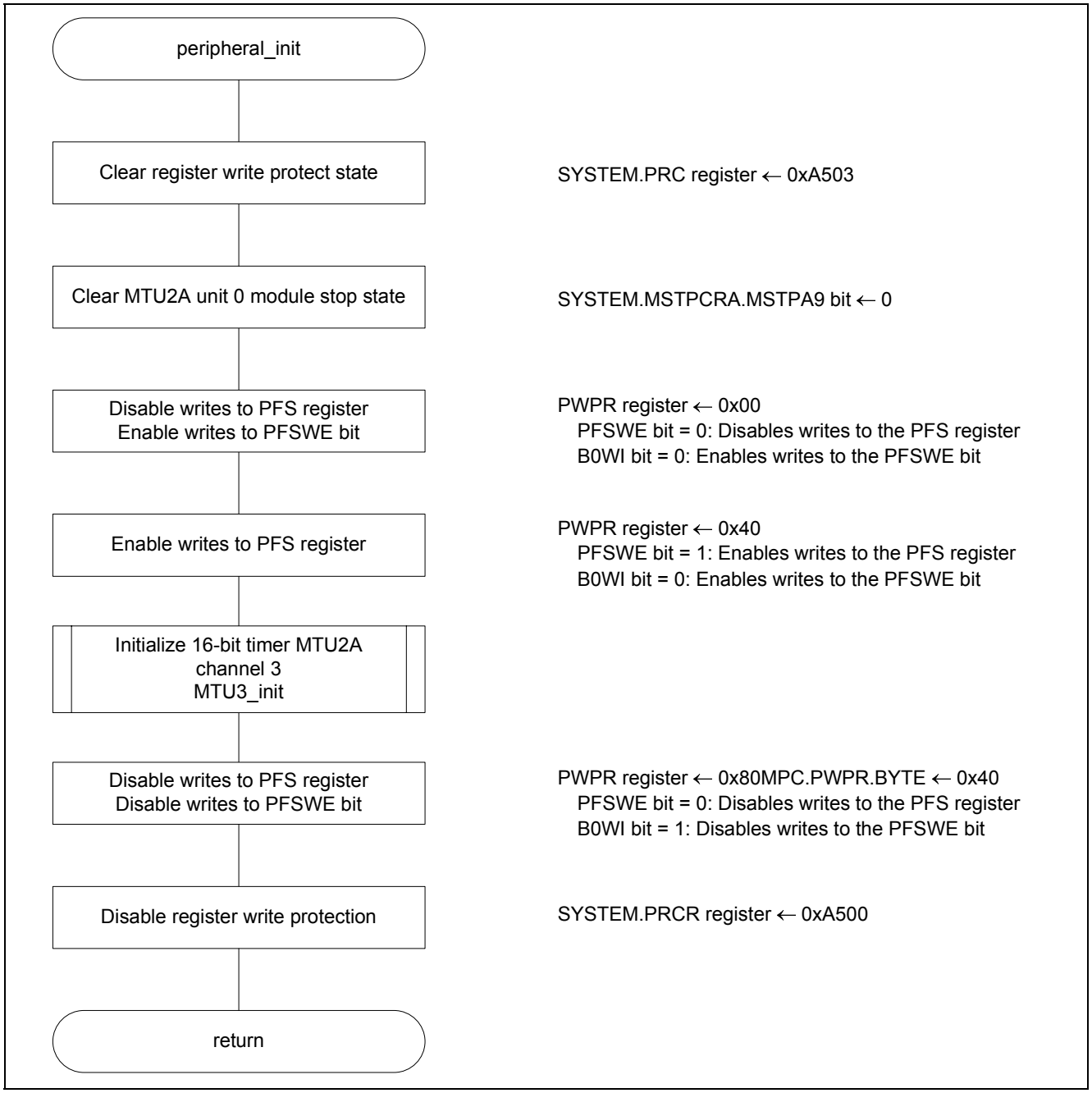

Figure 3.4 Peripheral Function Initialization

3.7.5 16-Bit Timer MTU2A Channel 3 Initialization

Figure 3.5 shows the flowchart for 16-bit timer MTU2A channel 3 initialization.

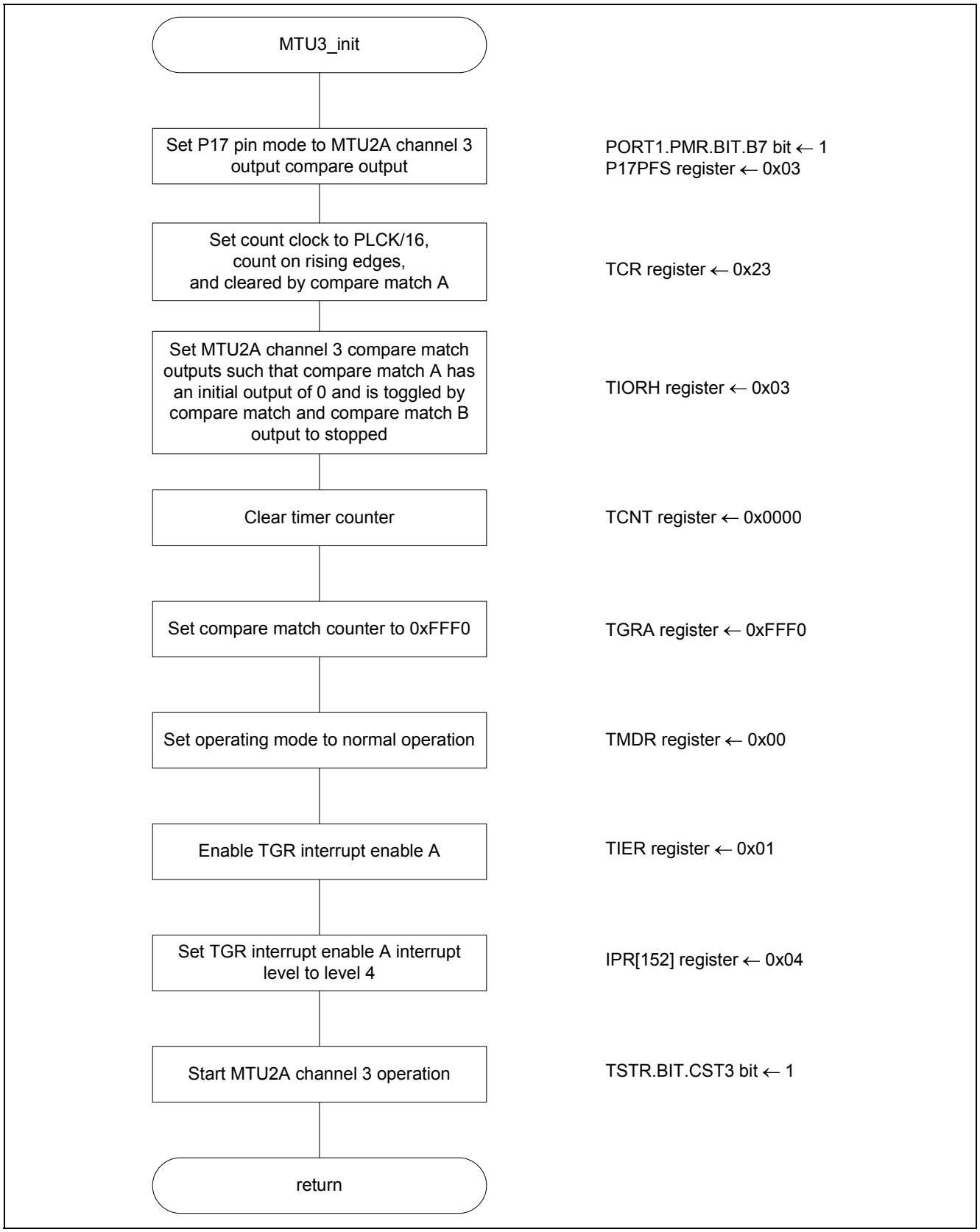

Figure 3.5 16-Bit Timer MTU2A Channel 3 Initialization

4. Sample Programs

The sample program can be downloaded from the Renesas Electronics Web site.

5. Reference Documents

- RX630 Group User's Manual: Hardware, Rev.1.00
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates/Technical News
  (The latest information can be downloaded from the Renesas Electronics Web site.)
- C Compiler Manual
  RX Family C/C++ Compiler Package User's Manual V.1.0.1.0
  (The latest version can be downloaded from the Renesas Electronics Web site.)

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.13.11	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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