RX62T Group, RX24T Group, RX24U Group

Migrating from the RX62T Group to the RX24T Group or RX24U Group

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Summary

This application note describes guidelines for migrating microcontroller code from the RX62T Group to the RX24T Group or RX24U Group.

Information is included for comparing specifications and confirming points of difference between microcontrollers in the RX62T Group and in the RX24T Group or RX24U Group with the package pin count indicated below.

100-pin package

The RX24T Group is available in two versions: A and B. The differences between these versions are summarized below. (Version B is available in a 100-pin package only.)

Function			Version B	Version A
Memory	ROM		256 KB/384 KB/512 KB	128 KB/256 KB
	RAM		32 KB	16 KB
Multi-function pin controller		MTU inverted I/O	Yes	No
Timer	Port output enable 3 • Version B: POE3A • Version A: POE3b		High-impedance control for MTU3 and GPT output pins	High-impedance control for MTU3 output pin
		I/O port switching control	Yes	No
		Independent setting of comparator sources	Yes	No
	GPT		16-bit × 4 channels	No
Communication	RSCAN		1 channel	No
Comparator		External reference voltage	No	CVREFC0 or CVREFC1 pin
		Internal reference voltage	DA0 or DA1 output selectable	Comparator C dedicated D/A converter
8-bit D/A			2 channels	1 channel
		External output	Yes	No (dedicated comparator C reference voltage generator)

The description of this application note applies mainly to version B.

This application note provides guidelines for smooth migration from the RX62T Group to the RX24T Group or RX24U Group. It does not cover all the details of the differences in the specifications of the above products.

Refer to the User's Manual: Hardware of each of the above products when migrating program code.

Target Devices

RX62T Group, RX24T Group, and RX24U Group

When not otherwise indicated, descriptions refer to the 100-pin package version of the RX62T Group, RX24T Group, and RX24U Group.

Contents

1. Overview for Migration Design

Compared to the RX62T Group, the RX24T Group and RX24U Group incorporate improvements that increase processing power and reduce power consumption.

There are some points to keep in mind about hardware and software when migrating from the RX62T Group to the RX24T Group or RX24U Group.

Section 2, Notes on the Pin Design describes notes on hardware. Section 3, Notes on the Function Settings describes notes on software.

2. Notes on the Pin Design

The range of frequencies to which the XTAL and EXTAL pins can be connected differs on the RX24T Group and RX24U Group. Notes on 100-pin package versions are presented below. For notes on 80-pin and 64-pin packages, refer to the tables listing the differences in pin functions and the differences in power supply, clock, and system control pins for the respective package pin counts in 4.2, Points of Difference between Pin Functions.

2.1 Main Clock Oscillator

On the RX24T Group and RX24U Group an oscillator (ceramic resonator or crystal oscillator) with an oscillation frequency of 1 MHz to 20 MHz may be connected to the EXTAL or XTAL pin. (This covers the entire allowable oscillation frequency range of the RX62T Group, which is 8 MHz to 12.5 MHz.)

In the crystal oscillator connection examples for the RX62T Group and for the RX24T Group and RX24U Group, the capacitor and damping resistor reference values differ. For detailed information on connecting a crystal oscillator, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

2.2 PLL Circuit Power Supply Pin

The RX62T Group has a dedicated power supply pin for the PLL circuit, but on the RX24T Group and RX24U Group no such pin is provided.

2.3 VCL Pin (External Capacity)

On the RX24T Group and RX24U Group, connect a 4.7µF smoothing capacitor to the VCL pin for internal power supply stabilization.

2.4 Mode Setting Pins

The pins for setting the mode after release from the reset state are MD0 and MD1 on the RX62T Group but MD only on the RX24T Group and RX24U Group. In addition, the endian setting is specified on the RX62T Group by using the MDE pin but on the RX24T Group and RX24U Group by using the MDE.MDE[2:0] bits in the option-setting memory.

2.5 General I/O Ports

Note that on the RX62T Group port 4 is an AVCC0-dependent input port and ports 5 and 6 are AVCC-dependent input ports, but on the RX24T Group and RX24U Group P40 to P43 are AVCC0-dependent I/O ports, P44 to P47 are AVCC1-dependent I/O ports, and ports 5 and 6 are AVCC2-dependent I/O ports. If these pins will not be used, either set them to input and connect each to the pin corresponding to the target port (AVCC0, AVCC1, or AVCC2) via a resistor (pull-up), or connect each to the pin corresponding to the target port (AVSS0, AVSS1, or AVSS2) via a resistor (pull-down).

In addition, although on the RX62T Group it was possible to leave pins open when the corresponding bit in PORTn.ICR was set to its initial value, on the RX24T Group and RX24U Group pins should be released after being set to output (PORTn.PDR bit = 1). When a pin is left open when set to output its setting reverts to input immediately after release from the reset state, causing an undefined pin voltage level while it is set to input and possibly resulting in an increase in the power supply current.

Note that RX24U Group microcontrollers have no ports P50 and P51. Any software that uses these ports must be modified to use other general I/O ports.

2.6 Comparator

The RX62T Group integrates comparator functionality into the 12-bit A/D converter, but the 12-bit A/D converter of the RX24T Group and RX24U Group does not include comparator functionality. Comparator C can be used instead. To accomplish this, use CMPCnm (n = channel number, m = 0 to 3) for analog input.

In addition, on the RX62T Group it is possible to select between using pin input (low side: AN003/CVREFL, high side: AN103/CVREFH) and using an internal voltage source (1/8 × AVCC0 to 7/8 × AVCC0) for reference voltages. On the RX24T Group and RX24U Group, in contrast, the reference voltage source is selectable between the output of on-chip D/A converter 0 and the output of on-chip D/A converter 1. Note that on version A of the RX24T Group either the input on the CVREFC0 or CVREFC1 pin or the output of on-chip D/A converter 0 may be selected as the reference voltage source.

2.7 Inputting an External Clock

On the RX62T Group it is permissible to input on the XTAL pin a signal that is the antiphase of the external clock signal input on the EXTAL pin. On the RX24T Group and RX24U Group, however, this is not allowed. Keep this in mind when designing your system.

When inputting an external clock to the RX24T Group or RX24U Group, it is necessary to set the main clock oscillator switch bit (MOSEL) in the main clock oscillator forced oscillation control register (MOFCR) to 1.

3. Notes on the Function Settings

Points related to function settings that differ between the RX62T Group and the RX24T Group and RX24U Group, which should be kept in mind when writing software, are touched on below.

For details on points of difference in modules and functions, see 4.3, Points of Difference between Modules and Functions.

When making use of this application note, make sure to perform thorough evaluation on the target system.

3.1 Memory Wait Cycle

RX24T Group and RX24U Group microcontrollers have a memory wait cycle setting register (MEMWAIT), but RX62T Group microcontrollers do not. To select a high-speed ICLK clock frequency of 32 MHz or higher on the RX24T Group or RX24U Group, set the MEMWAIT bits to 01b (wait states (ICLK ≤ 64 MHz)) or 10b (wait states (ICLK ≤ 80 MHz)). For details, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

3.2 Option-Setting Memory

On RX24T Group and RX24U Group microcontrollers the endian, independent watchdog timer, and other settings are specified in the option-setting memory. The option-setting memory is in the ROM, so it cannot be overwritten by executing instructions. It is therefore necessary to write appropriate settings when creating programs. For details, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

3.3 Clock Generation Circuit

The RX24T Group and RX24U Group add peripheral module clock A (PCLKA), which is supplied to the MTU and GPT (and to the SCI11 on the RX24U Group only); peripheral module clock D (PCLKD), which is supplied to the 12-bit A/D converter; the FlashIF clock (FCLK), which is supplied to the Flash interface; and the CAN clock (CANMCLK), which is supplied to the RSCAN. Also, there are changes to the frequency operating ranges.

For details on the points of difference, see 4.4.5, Clock Generation Circuit. For details, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

3.4 Low Power Consumption

Change deep software standby mode in the RX62T Group to software standby mode in the RX24T Group and RX24U Group. Current consumption of software standby mode is equal to that of deep software standby mode.

Change all-module clock stop mode in the RX62T Group to deep sleep mode in the RX24T Group and RX24U Group. Current consumption of deep sleep mode is equal to that of all-module clock stop mode.

3.5 Method of Specifying Pin Functions

The RX24T Group and RX24U Group are provided with a multi-function pin controller (MPC), so the method of specifying pin functions differs from that of the RX62T Group.

For details, refer to the User's Manual: Hardware of the RX24T Group and of the RX24U Group, which are listed in 5, Reference Documents.

3.6 Comparator

The RX62T Group integrates comparator functionality into the 12-bit A/D converter, but the 12-bit A/D converter of the RX24T Group and RX24U Group does not include comparator functionality. Comparator C can be used instead.

3.7 Supplemental Information on RAM Self-Diagnostics

The RX24T Group and RX24U Group provide a buffer to enable fast access between the RAM and CPU. When a write to RAM is followed by a read access to the same address, the data may be read not from the RAM but from the buffer in some cases. Such read and write operations present no problems in a buffered configuration, but programs that expect to actually read from the RAM the previously written data (for example, software that performs self-diagnostics on on-chip RAM) may not operate as expected (because the data is read from the buffer instead).

To ensure that data is actually read from the RAM, do the following.

When reading data from an address in RAM aligned with a 4-byte boundary*[1] after a write to RAM completes, first perform a write to another address that is different from that address aligned with a 4-byte boundary that you wish to read, then start the read from the desired address in RAM.

Note 1. An address aligned with a 4-byte boundary refers to an address whose lowest two bits have a value of 00b to 11b.

3.8 Flash Memory

The programming and erase time and unit for the flash memory in the RX62T Group differ from those for the flash memory in the RX24T Group or RX24U Group. Therefore, software that performs self-programming in single-chip mode will require changes.

In order to use FCU commands on the RX62T Group it is necessary to store the contents of the FCU firmware in the FCU RAM. This processing is not needed on the RX24T Group and RX24U Group.

On the RX62T Group the flash memory is programmed, erased, etc., by issuing FCU commands to the FCU. On the RX24T Group and RX24U Group, in contrast, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for programming and erasing the ROM and then issuing software commands.

Table 3.1 compares the specifications of FCU commands and software commands.

Table 3.1 Comparison of FCU Command and Software Command Specifications

Item	FCU Command (RX62T)	Software Command (RX24T and RX24U)
Command issue area	Program/erase address (00FC 0000h to 00FF FFFFh)	Program/erase address (FC18 0000h to FC1F FFFFh)
Usable commands	• Transition to program/erase normal mode • Transition to status read mode • Transition to lock bit read mode • Peripheral clock notify • Program • Block erase • Program/erase suspend • Program/erase resume • Status register clear • Lock bit read 2 • Program lock bit • Blank check	• Program • Block erase • All-block erase • Blank check • Program startup area information • Program access window information

4. Points of Difference

4.1 Points of Difference between Specifications in Outline

Table 4.1 lists points of difference between the specifications of the RX62T Group and of the RX24T Group and RX24U Group in outline. The specifications of 100-pin package (version B in the case of the RX24T) products are listed. The number of channels of each peripheral module varies with the pin count of the package.

Specifications that apply only to one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that apply to both groups are indicated in black.

Table 4.1 Points of Difference between Specifications in Outline

Item		RX62T	RX24T RX24U
CPU	Central processing unit	• Maximum operating frequency: 100 MHz • 32-bit RX CPU (RXv1) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 9 control registers (32 bits) 1 accumulator (64 bits) • Basic instructions: 73 • 8 floating-point instructions • 9 DSP instructions • 10 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits —	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Min. instruction execution time: 1 clock cycle per instruction • Address space: 4 GB, linear addressing • Register 16 general-purpose registers (32 bits) 10 control registers (32 bits) 2 accumulators (72 bits) • Basic instructions: 75, variable instruction length • 11 floating-point instructions • 23 DSP instructions • 11 addressing modes • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • 32-bit multiplier: 32-bit × 32-bit → 64 bits • Divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • ROM cache: 2 KB (disabled by default)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard

Item		RX62T	RX24T RX24U
Memory	ROM	• ROM Capacity: 64, 128, 256 KB	• ROM Capacity: (RX24T) 128, 256, 384, 512 KB (RX24U) 256, 384, 512 KB
		• No-wait memory access	• 32 MHz or less: no-wait memory access 32 to 80 MHz: Wait states
		• 2 on-board programming modes Boot mode (SCI interface) — User program mode	• 3 on-board programming modes Boot mode (SCI interface) Boot mode (FINE interface) Self-programming (single-chip mode)
		• Off-board programming Ability to program user MAT using a PROM writer	• Off-board programming Programming using a compatible flash programmer supported
	RAM	• Capacity: 8, 16 KB	• Capacity: (RX24T) 16, 32 KB (RX24U) 32 KB
		• No-wait memory access	• No-wait memory access
	Data flash (RX62T) E2 DataFlash (RX24T and RX24U)	• Data ROM capacity: 32, 8 KB	• Data ROM capacity: 8 KB
		• 30,000 erase cycles	• Program/erase cycles: 1,000,000
		• Background operation (BGO) supported	• Background operation (BGO) supported
MCU operating mode		Single-chip mode	Single-chip mode

Item	RX62T	RX24T RX24U
Clock generation circuits	• Main clock oscillator	• Main clock oscillator
	—	• Low-speed on-chip oscillators
	—	• High-speed on-chip oscillators
	• Comprises PLL frequency synthesizer and frequency divider circuits, allowing selection of operating frequencies	• PLL frequency synthesizer
	• Low-speed on-chip oscillator dedicated to IWDT	• IWDT-dedicated on-chip oscillator
	• Oscillation stop detection: Yes	• Oscillation stop detection: Yes
	—	• Clock frequency accuracy measurement circuit (CAC): Yes
	• Ability to independently set system clock (ICLK) and peripheral module (PCLK)	• Ability to independently set system clock (ICLK), peripheral module (PCLK), and FlashIF clock (FCLK)
	• The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the ICLK: 8 to 100 MHz	• The CPU and system sections such as other bus masters run in synchronization with the ICLK: Max. 80 MHz
	• PCLK synchronization of peripheral module: 8 to 50 MHz	• PCLKA synchronization of MTU3 and GPT: Max. 80 MHz
		• PCLKB synchronization of peripheral modules other than MTU3 and GPT: Max. 40 MHz
	—	• PCLKD synchronization of ADCLK of S12AD: Max. 40 MHz
	—	• The flash memory peripheral circuit runs in synchronization with the FCLK: Max. 32 MHz
Resets	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	Voltage monitoring reset	Voltage monitoring reset
	Watchdog timer reset	—
	Independent watchdog timer reset	Independent watchdog timer reset
	—	Software reset
	Deep software standby reset	—

Item	RX62T	RX24T RX24U
Voltage detection	LVD • Generation of internal reset or internal interrupt when VCC drops below voltage detection level (Vdet)	LVDAb Generation of internal reset or internal interrupt when VCC drops below voltage detection level (Vdet) Voltage detection 0: Ability to select voltage from among 3 detection voltage levels Voltage detection 1: Ability to select voltage from among 9 detection voltage levels Voltage detection 2: Ability to select voltage from among 4 detection voltage levels
Low power consumption functions	• Module stop function • 4 low-power states: Sleep mode All-module clock stop mode Software standby mode Deep software standby mode —	• Module stop function • 3 low-power states: Sleep mode — Software standby mode — Deep sleep mode
Function for lower operating power consumption	Not available	Operating power control modes • High-speed operating mode • Middle-speed operating mode

Item	RX62T	RX24T	RX24U
Interrupt controller	• Peripheral function interrupts: 101 sources • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 source (NMI pin, oscillation stop detection interrupt, and voltage monitoring interrupt) • 16 levels specifiable for the order of priority	• Interrupt vectors: 163 • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 source (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, IWDT interrupt) • 16 levels specifiable for the order of priority	• Interrupt vectors: 175 • External interrupts: 9 source (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 source (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, IWDT interrupt) • 16 levels specifiable for the order of priority
Data transfer controller	DTC • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupt, peripheral function interrupt • Chain transfer function	DTCa • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupt, peripheral function interrupt • Chain transfer function	

Item		RX62T	RX24T	RX24U
General I/O ports		112-pin/100-pin/80-pin (R5F562TxGDFF)/80-pin (other than R5F562TxGDFF)/64-pin • I/O: 61/55/44/44/37 • Input: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current output: 12/12/12/6/6(0) (MTU3 pins, GPT pins) (No large-current output pins on 5 V version of 64-pin products) • Pin states are always readable.	100-pin/ 80-pin/64-pin • I/O: 80/60/48 • Input: 1/1/1 • Pull-up resistors: 80/64/48 • Open-drain outputs: 60/45/37 • Large-current output: 15/14/14 • 5-V tolerant: 2/2/2 • Pin states are always readable.	144-pin/100-pin • I/O: 110/79 • Input: 1/1 • Pull-up resistors: 110/79 • Open-drain outputs: 90/61 • Large-current output: 15/15 • 5-V tolerant: 2/2 • Pin states are always readable.
Multi-function pin controller		Not available	Capable of selecting the input/output function from multiple pins	
Timers	Multi-function timer pulse unit 3	MTU3 • 16 bits × 8 channels • Support for max. 24 pulse I/O and 3 pulse input lines • Ability to select among six to eight count clocks (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) for each channel (4 count clocks for channel 5) • 35 general registers (Of these, 24 function as output compare and input capture registers.) • Counter clear operation (support for simultaneous clearing at compare match or input capture) • Writing synchronized with multiple timer counters (TCNT) • Counter-synchronous I/O with each register • Buffer operation	MTU3d • 16 bits × 9 channels • Support for max. 28 pulse I/O and 3 pulse input lines • Ability to select among 14 count clocks (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/32, PCLK/64, PCLKA/256, PCLK/1,024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, and MTIOC1A) for each channel (11 count clocks for channels 1, 3, 4, 6, and 7, 12 count clocks for channel 2, and 10 count clocks for channel 5) • 43 general registers (Of these, 28 function as output compare and input capture registers.) • Counter clear operation (support for simultaneous clearing at compare match or input capture) • Writing synchronized with multiple timer counters (TCNT) • Counter-synchronous I/O with each register • Buffer operation	

Item		RX62T	RX24T RX24U
Timers	Multi-function timer pulse unit 3	• Operation with cascade connection • 38 interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronous PWM • Complementary PWM mode Non-overlapping waveform output for 3-phase inverter control Automatic dead time setting Ability to set PWM duty ratio to 0 to 100% Delayed A/D conversion request function Peak/trough interrupt skipping function Double buffer function • Reset-synchronous PWM mode 3-phase output of forward- and reverse-phase PWM waveforms with user-defined duty ratio • Phase counting mode • Dead time compensation counter function • A/D converter conversion start trigger generation • A/D conversion start skipping function —	• Operation with cascade connection • 45 interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronous PWM • Complementary PWM mode Non-overlapping waveform output for 3-phase inverter control Automatic dead time setting Ability to set PWM duty ratio to 0 to 100% Delayed A/D conversion request function Peak/trough interrupt skipping function Double buffer function • Reset-synchronous PWM mode 3-phase output of forward- and reverse-phase PWM waveforms with user-defined duty ratio • Phase counting mode • Dead time compensation counter function • A/D converter conversion start trigger generation • A/D conversion start skipping function • Digital filtering of input capture and external count clock pins

Item		RX62T	RX24T	RX24U
Timers	Port output enable 3	POE3 • High-impedance control for MTU3 and GPT waveform output pins Activation by 5 input pins: POE0, POE4, POE8, POE10, and POE11 Activation by short-circuited output detection (detection of state in which large-current outputs are active level simultaneously) Activation by oscillation stop detection, 12-bit A/D analog input comparator detection, or software • Ability to select which output pins are put in high-impedance state when POE input and comparator detection occur	POE3A • MTU3 and GPT waveform output pin high-impedance/general I/O port switching control Activation by 6 input pins: POE0#, POE4#, POE8#, POE10#, POE11#, and POE12# Activation by short-circuited output detection (detection of state in which PWM outputs are active level simultaneously) Activation by oscillation stop detection, comparator C (CMPC) detection, or software • Ability to select which output pins are put in high-impedance state when POE input and comparator detection occur	
	General PWM timer	GPT • 16 bits × 4 channels — • Ability to select up-count or down-count (sawtooth wave) or up-down-count (triangular wave) operation on each counter • Ability to select among 4 count clock sources for each channel • 2 I/O pins per channel • 2 output compare/input capture registers per channel • For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used • Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation	GPTB • 16 bits × 4 channels • Support for cascade connection on 2 channels as a 32-bit timer • Ability to select up-count or down-count (sawtooth wave) or up-down-count (triangular wave) operation on each counter • Ability to select among 13 count clock sources for each channel • 2 I/O pins per channel • 2 output compare/input capture registers per channel • For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used • Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation	

Item		RX62T	RX24T RX24U
Timers	General PWM timer	• Frame cycle registers for each channel (ability to generate interrupts at overflow/ underflow) • Support for synchronous operation of each counter • Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support) • Ability to generate dead time during PWM operation • Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time automatically • Support for count start, clear, or stop by external or internal trigger • Ability to use comparator detection, software, or compare match as internal trigger source — • Ability to generate A/D converter start trigger • Ability to count edges of the frequency-divided IWDT dedicated low-speed on-chip oscillator clock using a count clock produced by frequency dividing the system clock (ICLK) (oscillation error detection)	• Frame cycle registers for each channel (ability to generate interrupts at overflow/ underflow) • Support for synchronous operation of each counter • Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support) • Ability to generate dead time during PWM operation • Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time • Support for count start, clear, or stop by external or internal trigger • Ability to use comparator detection, MTU3 count start, software, or compare match as internal trigger source • Noise filtering function activated by input capture, external trigger pin, or external count clock pin • Ability to generate A/D converter start trigger —
	Compare match timer	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer	• 18 bits × 1 channel • Select from among eight count clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Ability to switch between watchdog timer mode and interval timer mode	Not available

Item		RX62T	RX24T RX24U
Timers	Independent watchdog timer	IWDT • 14 bits × 1 channel • Count clock: IWDT-dedicated low-speed on-chip oscillator	IWDTa • 14 bits × 1 channel • Count clock: IWDT-dedicated on-chip oscillator
	8-bit timer	Not available	• (8 bits × 2 channels) × 4 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Ability to generate A/D converter start trigger • Ability to generate baud rate clock for SCI5 and SCI6
Communication function	Serial communications interfaces	SCIb • 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor communication function • Ability to select any bit rate using on-chip baud rate generator • Choice of LSB-first or MSB-first transfer • Noise canceling function (enabled only during asynchronous operation) — — — — —	SCIg • 3 channels (RX24T) 4 channels (RX24U) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor communication function • Ability to select any bit rate using on-chip baud rate generator • Choice of LSB-first or MSB-first transfer • Noise canceling function (enabled only during asynchronous operation) Average transfer rate clock can be input from TMR timers for SCI5 and SCI6 Simple I^2C Simple SPI Support for 9-bit transfer mode Support for bit rate modulation

Item		RX62T	RX24T RX24U
Communication function	I^2C bus interface	RIIC • 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Fast mode support	RIICa • 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Fast mode support
	CAN module	CAN • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes	RSCAN • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 16 mailboxes
	Serial peripheral interface	RSPI • 1 unit • RSPI transfer facility • Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Support for serial communication in master or slave mode • Data formats Ability to switch between MSB-first and LSB-first bit order The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffer configuration • Double buffers for both transmission and reception	RSPIb • 1 channel • RSPI transfer facility • Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock synchronous operation (three lines) • Support for serial communication in master or slave mode • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffer configuration • Double buffers for both transmission and reception
	LIN module	• 1 channel • Compatible with LIN protocol revisions 1.3, 2.0, and 2.1	Not availble

Item		RX62T	RX24T RX24U
A/D converter	12-bit A/D converter	S12ADA	S12ADF
		• 12 bits 4 channels × 2 units	• 12 bits (RX24T): 5 channels × 2 units, 12 channels × 1 unit (RX24U): 5 channels × 2 units, 10 channels × 1 unit
		• 12-bit resolution	• 12-bit resolution
		• Conversion time: 1.0 μs per channel (when A/D converter clock ADCLK = 50 MHz and AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (when A/D converter clock ADCLK = 25 MHz and AVCC0 = 3.0 to 3.6 V)	• Conversion time: 1.0 μs per channel (when ADCLK = 40 MHz)
		• 2 operating modes Single mode Scan mode —	• Operating modes — Scan mode Group A priority control (only for 3-group scan mode)
		• Scan mode Single-cycle scan mode Continuous scan mode — 2-channel scan mode (ability to divide inputs in each unit into 2 groups and select a separate conversion startup source for each group)	• Scan mode Single scan mode Continuous scan mode 3-group scan mode —
		• Sample-and-hold function Sample and hold circuit common to all units Individual sample and hold circuit in addition to the above (3 channels/1 unit)	• Sample-and-hold function Sample and hold circuit common to all units Individual sample and hold circuit in addition to the above (3 channels/1 unit)
		• Separate A/D conversion registers for each input pin	• Separate A/D conversion registers for each input pin
		• 2-stage conversion result registers for 1 analog input only per unit (AN000/AN100)	• 1 register per unit for A/D-converted data duplication in double trigger mode, and 2 registers per unit for A/D-converted data duplication during extended operation in double trigger mode
		—	• Analog input cutoff detection assist function
		• A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT), an external trigger signal	• A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), an external trigger signal

Item		RX62T	RX24T	RX24U
A/D converter	12-bit A/D converter	• Support for output at 8- or 10-bit accuracy Ability to select 2-bit or 4-bit right-shifting of conversion result output	—	
		• Self-diagnostic function Ability to generate 3 analog input voltages (VREFL0, VREFH0 × 1/2, and VREFH0) for use by self-diagnostic function	• Self-diagnostic function For each unit, ability to generate 3 analog input voltages (RX24T): 0, AVCC0 to AVCC2 × 1/2, AVCC0 to AVCC2, (RX24U): 0, VREFH0 to VREFH2 × 1/2, VREFH0 to VREFH2) for use by self-diagnostic function	
		• Input signal amplification function using programmable gain amplifier (3 channels/unit 1)	• Input signal amplification function using programmable gain amplifier (3 channels/unit 1)	
		• Amplification ratio: 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, 4.444×,5.0×, 5.714×, 6.667×, 10.0×, or 13.333× (total 11 steps)	• Amplification ratio: (RX24T): 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, or 4.444× (total 6 steps) (RX24U): 2.0×, 2.5×, 3.077×, 3.636×, 4.0×, 4.444×, 5.0×, 6.667×, 8×, 10.0×, or 13.333× (total 11 steps)	
		• Window comparator function (3 channels/1 unit)	—	

Item		RX62T	RX24T	RX24U
A/D converter	10-bit A/D converter	10 bits (12 channels × 1 unit) • 10-bit resolution • Conversion time: 1.0 μs per channel (when A/D converter clock ADCLK = 50 MHz and AVCC0 = 4.0 to 5.5 V) 2.0 μs per channel (when A/D converter clock ADCLK = 25 MHz and AVCC0 = 3.0 to 3.6 V) • 2 operating modes Single mode and scan mode • Scan mode Single-cycle scan mode Continuous scan mode • Sample and hold function Sample and hold circuit common to all units • A/D conversion registers for each input pin • 3 A/D conversion start methods Software trigger, timer (MTU3 or GPT) trigger, and external trigger • Support for 8-bit precision output Ability to select 2-bit right-shifting of conversion result output • Self-diagnostic function Ability to generate 3 analog input voltages (AVSS, VREF × 1/2, and VREF) for use by self-diagnostic function	Not available	
Comparator C		Not available	• 4 channels • Reference voltage and analog input voltage • Reference voltage: Selectable among 2 • Analog input voltage: Selectable among 4 inputs	

Item	RX62T	RX24T	RX24U
8-bit D/A converter	Not available	2 channels • 8-bit resolution • Output voltage: 0 V to VREF • Support for external output, support for use as comparator C reference voltage	2 channels • 8-bit resolution • Output voltage: 0 V to AVCC2 • Support for external output, support for use as comparator C reference voltage
Memory protection unit	• Protected areas: Ability to specify up to 8 areas within range from 0000 0000h to FFFF FFFFh • Minimum protection unit: 16 bytes • Ability to specify read, write, or run access for each area • Generation of address exception when access to a non-specified area is detected	• Protected areas: Ability to specify up to 8 areas within range from 0000 0000h to FFFF FFFFh • Minimum protection unit: 16 bytes • Ability to specify read, write, or run access for each area • Generation of address exception when access to a non-specified area is detected	
Register write protection	Not available	Ability to prohibit write access to important registers to protect against program runaway	
CRC calculator	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.	
Clock frequency accuracy measurement circuit	Not available	Ability to monitor for errors in output clock frequencies of main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, IWDT dedicated on-chip oscillator, and PCLKB	
Data Operation Circuit	Not available	Function for comparing, adding, or subtracting 16 bits of data	

Item	RX62T	RX24T	RX24U
Power supply voltages/ operating frequencies	ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz (Not dependent on power supply voltage.) • 3 V product VCC = PLLVCC = 2.7 to 3.6 V AVCC0 = AVCC = 3.0 to 3.6 V, or 4.0 to 5.5 V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5 V product VCC = PLLVCC = 4.0 to 5.5 V AVCC0 = AVCC = 4.0 to 5.5 V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC	VCC = 2.7 to 5.5 V ICLK: Max. 80 MHz PCLKA: Max. 80 MHz PCLKB: Max. 40 MHz PCLKD: Max. 40 MHz FCLK: Max. 32 MHz	
Operating ambient temperature	D version: –40 to +85°C G version: –40 to +105°C	D version: –40 to +85°C —	
Packages	112-pin LFQFP 0.5 mm pitch 100-pin LFQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 64-pin LFQFP 0.5 mm pitch 64-pin LQFP 0.8 mm pitch	100-pin LFQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 80-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch	144-pin LFQFP 0.5 mm pitch 100-pin LQFP 0.5 mm pitch

4.2 Points of Difference between Pin Functions

Points of difference between pin functions and between pins for power supplies, clocks, and system control are listed below. Items that apply only to one group or the other are indicated in blue. Items that are different between groups are indicated in red. Items that apply to both groups are indicated in black.

4.2.1 100-Pin Package

Table 4.2 lists points of difference between the pin functions for the 100-pin package. Table 4.3 lists points of difference between pins for power supplies, clocks, and system control for the 100-pin package.

Table 4.2 Points of Difference between Pin Functions for 100-Pin Package

I/O Port	RX62T	RX24T	RX24U
P00	— (No I/O port)	IRQ2, ADST1	IRQ2, ADST1
P01	— (No I/O port)	POE12#, IRQ4, ADST2	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, MTIOC9D#, CTS1#, RTS1#, SS1#, IRQ5, ADST0	MTIOC9D, MTIOC9D#, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD-B, IRQ0-A	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0
P11	MTCLKC-B, IRQ1-A	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3, IRQ1	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3, IRQ1
P20	ADTRG0#-B, MTCLKB-B, IRQ7	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4, IRQ7, ADTRG0#, AN016	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4, IRQ7, ADTRG0#, AN016
P21	ADTRG1#-B, MTCLKA-B, IRQ6	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4, IRQ6, ADTRG1#, AN116	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4, IRQ6, ADTRG1#, AN116
P22	ADTRG#, CRX-B, LRX, MISO-A	MTIC5W, MTIC5W#, TMRI2, TMO4, MISOA, ADTRG2#, COMP2	MTIC5W, MTIC5W#, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	CTX-B, LTX, MOSI-A	MTIC5V, MTIC5V#, TMO2, CACREF, MOSIA, COMP1, DA1	MTIC5V, MTIC5V#, TMO2, CACREF, MOSIA, COMP1, DA1
P24	RSPCK-A	MTIC5U, MTIC5U#, TMCI2, TMO6, RSPCKA, COMP0, DA0	MTIC5U, MTIC5U#, TMCI2, TMO6, RSPCKA, COMP0, DA0
P27	— (No I/O port)	— (No I/O port)	MTIOC1A, MTIOC1A#
P30	MTIOC0B-B, MTCLKD-A, SSL0-A	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6, SSLA0, IRQ7, COMP3	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6, SSLA0, IRQ7, COMP3
P31	MTIOC0A-B, MTCLKC-A, SSL1-A	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6, SSLA1, IRQ6	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6, SSLA1, IRQ6
P32	MTIOC3C, MTCLKB-A, SSL2-A	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6, SSLA2	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6, SSLA2

I/O Port	RX62T	RX24T	RX24U
P33	MTIOC3A, MTCLKA-A, SSL3-A	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0, SSLA3	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0, SSLA3
P36	— (No I/O port)	—	—
P37	— (No I/O port)	—	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001	AN001
P42	AN002	AN002	AN002
P43	AN003, CVREFL	AN003	AN003
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	AN103	AN103
P50	AN6	AN206	— (No I/O port)
P51	AN7	AN207	— (No I/O port)
P52	AN8	AN208, IRQ0	AN208, IRQ0
P53	AN9	AN209, IRQ1	AN209, IRQ1
P54	AN10	AN210, IRQ2	AN210, IRQ2
P55	AN11	AN211, IRQ3	AN211, IRQ3
P60	AN0	AN200, IRQ4	AN200, IRQ4
P61	AN1	AN201, IRQ5	AN201, IRQ5
P62	AN2	AN202, IRQ6	AN202, IRQ6
P63	AN3	AN203, IRQ7	AN203, IRQ7
P64	AN4	AN204	AN204
P65	AN5	AN205	AN205
P70	IRQ5, POE0#	POE0#, IRQ5	POE0#, IRQ5
P71	MTIOC3B, GTIOC0A-A	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#
P72	MTIOC4A, GTIOC1A-A	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#
P73	MTIOC4B, GTIOC2A-A	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#
P74	MTIOC3D, GTIOC0B-A	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#
P75	MTIOC4C, GTIOC1B-A	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#
P76	MTIOC4D, GTIOC2B-A	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#
P80	MTIC5W, RXD2-B	MTIC5W, MTIC5W#, TMRI4, RXD6, SMISO6, SSCL6	MTIC5W, MTIC5W#, TMRI4, RXD6, SMISO6, SSCL6
P81	MTIC5V, TXD2-B	MTIC5V, MTIC5V#, TMCI4, TXD6, SMOSI6, SSDA6	MTIC5V, MTIC5V#, TMCI4, TXD6, SMOSI6, SSDA6
P82	MTIC5U, SCK2-B	MTIC5U, MTIC5U#, TMO4, SCK6	MTIC5U, MTIC5U#, TMO4, SCK6
P90	MTIOC7D	MTIOC7D, MTIOC7D#	MTIOC7D, MTIOC7D#
P91	MTIOC7C	MTIOC7C, MTIOC7C#	MTIOC7C, MTIOC7C#
P92	MTIOC6D	MTIOC6D, MTIOC6D#	MTIOC6D, MTIOC6D#

I/O Port	RX62T	RX24T	RX24U
P93	MTIOC7B	MTIOC7B, MTIOC7B#	MTIOC7B, MTIOC7B#
P94	MTIOC7A	MTIOC7A, MTIOC7A#	MTIOC7A, MTIOC7A#
P95	MTIOC6B	MTIOC6B, MTIOC6B#	MTIOC6B, MTIOC6B#
P96	IRQ4, POE4#	POE4#, IRQ4	POE4#, IRQ4
PA0	MTIOC6C, SSL3-B	MTIOC6C, MTIOC6C#, TMO2, SSLA3, CTXD0	MTIOC6C, MTIOC6C#, TMO2, SSLA3, CTXD0
PA1	MTIOC6A, SSL2-B	MTIOC6A, MTIOC6A#, TMO4, SSLA2, CRXD0, ADTRG0#	MTIOC6A, MTIOC6A#, TMO4, SSLA2, CRXD0, ADTRG0#
PA2	MTIOC2B, SSL1-B	MTIOC2B, MTIOC2B#, TMO7, GTADSM1, CTS6#, RTS6#, SS6#, SSLA1	MTIOC2B, MTIOC2B#, TMO7, GTADSM1, CTS6#, RTS6#, SS6#, SSLA1
PA3	MTIOC2A, SSL0-B	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0, SSLA0	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0, SSLA0
PA4	ADTRG0#-A, MTIOC1B, RSPCK-B	MTIOC1B, MTIOC1B#, TMCI7, SCK6, RSPCKA, ADTRG0#	MTIOC1B, MTIOC1B#, TMCI7, SCK6, RSPCKA, ADTRG0#
PA5	ADTRG1#-A, MTIOC1A, MISO-B	MTIOC1A, MTIOC1A#, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#	MTIOC1A, MTIOC1A#, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#
PB0	MTIOC0D, MOSI-B	MTIOC0D, MTIOC0D#, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#	MTIOC0D, MTIOC0D#, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#
PB1	MTIOC0C, RXD0, SCL	MTIOC0C, MTIOC0C#, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0	MTIOC0C, MTIOC0C#, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B-A, TXD0, SDA	MTIOC0B, MTIOC0B#, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0	MTIOC0B, MTIOC0B#, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	MTIOC0A-A, SCK0	MTIOC0A, MTIOC0A#, CACREF, SCK6, RSPCKA	MTIOC0A, MTIOC0A#, CACREF, SCK6, RSPCKA
PB4	GTETRG, IRQ3, POE8#	POE8#, GTETRG, GTECLKD, CTS5#, RTS5#, SS5#, IRQ3	POE8#, GTETRG, GTECLKD, CTS5#, RTS5#, SS5#, IRQ3
PB5	CTX-A, TXD2-A, TRSYNC	GTIOC2B, GTIOC2B#, TXD5, SMOSI5, SSDA5	GTIOC2B, GTIOC2B#, TXD5, SMOSI5, SSDA5
PB6	CRX-A, RXD2-A, TRDATA0	GTIOC2A, GTIOC2A#, RXD5, SMISO5, SSCL5, IRQ5	GTIOC2A, GTIOC2A#, RXD5, SMISO5, SSCL5, IRQ5
PB7	SCK2-A, TRDATA1	GTIOC1B, GTIOC1B#, SCK5	GTIOC1B, GTIOC1B#, SCK5
PD0	GTIOC3B, RSPCK-C, TRDATA2	TMO6, GTIOC1A, GTIOC1A#, RSPCKA	TMO6, GTIOC1A, GTIOC1A#, RSPCKA
PD1	GTIOC3A, MISO-C, TRDATA3	TMO2, GTIOC0B, GTIOC0B#, MISOA	TMO2, GTIOC0B, GTIOC0B#, MISOA
PD2	GTIOC2B-B, MOSI-C, TRCLK	TMCI1, TMO4, GTIOC0A, GTIOC0A#, SCK5, MOSIA	TMCI1, TMO4, GTIOC0A, GTIOC0A#, SCK5, MOSIA
PD3	GTIOC2A-B, TXD1, TDO	TMO0, GTECLKC, TXD1, SMOSI1, SSDA1	TMO0, GTECLKC, TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11
PD4	GTIOC1B-B, SCK1, TCK	TMCI0, TMCI6, GTECLKB, SCK1, IRQ2	TMCI0, TMCI6, GTECLKB, SCK1, SCK11, IRQ2
PD5	GTIOC1A-B, RXD1, TDI	TMRI0, TMRI6, GTECLKA, RXD1, SMISO1, SSCL1, IRQ3	TMRI0, TMRI6, GTECLKA, RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11, IRQ3

I/O Port	RX62T	RX24T	RX24U
PD6	GTIOC0B-B, SSL0-C, TMS	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#, CTS1#, RTS1#, SS1#, SSLA0, IRQ5, ADST0	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#, CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0, IRQ5, ADST0
PD7	GTIOC0A-B, CTX-C, SSL1-C, TRST#	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#, TXD5, SMOSI5, SSDA5, SSLA1	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#, TXD5, SMOSI5, SSDA5, SSLA1
PE0	CRX-C, SSL2-C	MTIOC9B, MTIOC9B#, TMCI1, TMCI5, RXD5, SMISO5, SSCL5, SSLA2	MTIOC9B, MTIOC9B#, TMCI1, TMCI5, RXD5, SMISO5, SSCL5, SSLA2
PE1	SSL3-C	MTIOC9D, MTIOC9D#, TMO5, CTS5#, RTS5#, SS5#, SSLA3	MTIOC9D, MTIOC9D#, TMO5, CTS5#, RTS5#, SS5#, SSLA3
PE2	NMI, POE10#-A	POE10#, NMI	POE10#, NMI
PE3	MTCLKD-C, IRQ2-A, POE11#	MTCLKD, MTCLKD#, POE11#, IRQ2	MTCLKD, MTCLKD#, POE11#, IRQ2
PE4	MTCLKC-C, IRQ1-B, POE10#-B	MTCLKC, MTCLKC#, POE10#, IRQ1	MTCLKC, MTCLKC#, POE10#, IRQ1
PE5	IRQ0-B	IRQ0	IRQ0

Table 4.3 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 100-Pin Package

Pin Number	RX62T	RX24T	RX24U
2	EMLE	— (P02)	— (P02)
3	VSS	VSS	VSS
4	MDE	— (P00)	— (P00)
5	VCL	VCL	VCL
6	MD1	MD	MD
7	MD0	— (P01)	— (P01)
10	RES#	RES#	RES#
11	XTAL	XTAL (P37)	XTAL (P37)
12	VSS	VSS	VSS
13	EXTAL	EXTAL (P36)	EXTAL (P36)
14	VCC	VCC	VCC
29	PLLVCC	VCC	VCC
31	PLLVSS	VSS	VSS
42	VCC	VCC	VCC
44	VSS	VSS	VSS
60	VCC	VCC	VCC
62	VSS	VSS	VSS
71	AVCC	AVCC2	— (P64)
72	VREF	VREF	AVCC2
73	AVSS	AVSS2	AVSS2
86	— (P45)	— (P45)	PGAVSS1
91	— (P40)	— (P40)	PGAVSS0
92	AVCC0	AVCC1	AVCC1
93	VREFH0	AVCC0	AVCC0
94	VREFL0	AVSS0	AVSS0
95	AVSS0	AVSS1	AVSS1

4.2.2 80-Pin Package

Table 4.4 lists points of difference between the pin functions for the 80-pin package. Table 4.5 lists points of difference between pins for power supplies, clocks, and system control for the 80-pin package.

Table 4.4 Points of Difference between Pin Functions for 80-Pin Package

I/O Port	RX62T	RX24T
P00	— (No I/O port)	IRQ2, ADST1
P01	— (No I/O port)	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD-B, IRQ0-A	MTIOC9B, MTCLKD, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0
P11	MTCLKC-B, IRQ1-A	MTIOC3A, MTCLKC, TMO3, IRQ1
P20	ADTRG0#-B, MTCLKB-B, IRQ7	MTCLKB, MTIOC9C, TMRI4, IRQ7, ADTRG0#, AN016, CVREFC0
P21	ADTRG1#-B, MTCLKA-B, IRQ6	MTCLKA, MTIOC9A, TMCI4, IRQ6, ADTRG1#, AN116, CVREFC1
P22	ADTRG#, CRX-B, LRX, MISO-A	MTIC5W, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	CTX-B, LTX, MOSI-A	MTIC5V, TMO2, CACREF, MOSIA, COMP1
P24	RSPCK-A	MTIC5U, TMCI2, TMO6, RSPCKA, COMP0
P30	MTIOC0B-B, MTCLKD-A, SSL0-A	MTIOC0B, MTCLKD, TMCI6, SSLA0, IRQ7, COMP3
P31	MTIOC0A-B, MTCLKC-A, SSL1-A	MTIOC0A, MTCLKC, TMRI6, SSLA1, IRQ6
P32	MTIOC3C, MTCLKB-A, SSL2-A	— (No I/O port)
P33	MTIOC3A, MTCLKA-A, SSL3-A	— (No I/O port)
P36	— (No I/O port)	—
P37	— (No I/O port)	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001
P42	AN002	AN002
P43	AN003, CVREFL	AN003
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	AN103
P50	— (No I/O port)	AN206
P51	— (No I/O port)	AN207
P52	— (No I/O port)	AN208, IRQ0
P53	— (No I/O port)	AN209, IRQ1
P54	— (No I/O port)	AN210, IRQ2
P55	— (No I/O port)	AN211, IRQ3
P60	AN0	— (No I/O port)
P61	AN1	— (No I/O port)
P62	AN2	AN202, IRQ6
P63	AN3	— (No I/O port)
P70	IRQ5, POE0#	POE0#, IRQ5

I/O Port	RX62T	RX24T
P71	MTIOC3B, GTIOC0A-A	MTIOC3B
P72	MTIOC4A, GTIOC1A-A	MTIOC4A
P73	MTIOC4B, GTIOC2A-A	MTIOC4B
P74	MTIOC3D, GTIOC0B-A	MTIOC3D
P75	MTIOC4C, GTIOC1B-A	MTIOC4C
P76	MTIOC4D, GTIOC2B-A	MTIOC4D
P90	— (No I/O port)	MTIOC7D
P91	MTIOC7C	MTIOC7C
P92	MTIOC6D	MTIOC6D
P93	MTIOC7B	MTIOC7B
P94	MTIOC7A	MTIOC7A
P95	MTIOC6B	MTIOC6B
P96	IRQ4, POE4#	POE4#, IRQ4
PA2	MTIOC2B, SSL1-B	— (No I/O port)
PA3	MTIOC2A, SSL0-B	MTIOC2A, TMRI7, SSLA0
PA4	ADTRG0#-A, MTIOC1B, RSPCK-B	— (No I/O port)
PA5	ADTRG1#-A, MTIOC1A, MISO-B	MTIOC1A, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#
PB0	MTIOC0D, MOSI-B	MTIOC0D, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#
PB1	MTIOC0C, RXD0, SCL	MTIOC0C, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B-A, TXD0, SDA	MTIOC0B, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	MTIOC0A-A, SCK0	MTIOC0A, CACREF, SCK6, RSPCKA
PB4	GTETRG, IRQ3, POE8#	POE8#, CTS5#, RTS5#, SS5#, IRQ3
PB5	CTX-A, TXD2-A	TXD5, SMOSI5, SSDA5
PB6	CRX-A, RXD2-A	RXD5, SMISO5, SSCL5, IRQ5
PB7	SCK2-A	— (No I/O port)
PD2	— (No I/O port)	TMCI1, TMO4, SCK5, MOSIA
PD3	GTIOC2A-B, TXD1, TDO	TMO0, TXD1, SMOSI1, SSDA1
PD4	GTIOC1B-B, SCK1, TCK	TMCI0, TMCI6, SCK1, IRQ2
PD5	GTIOC1A-B, RXD1, TDI	TMRI0, TMRI6, RXD1, SMISO1, SSCL1, IRQ3
PD6	GTIOC0B-B, TMS	MTIOC9C, TMO1, CTS1#, RTS1#, SS1#, SSLA0, IRQ5, ADST0
PD7	GTIOC0A-B, CTX-C, TRST#	MTIOC9A, TMRI1, TMRI5, SSLA1
PE0	CRX-C	— (No I/O port)
PE2	NMI, POE10#-A	POE10#, NMI
PE3	MTCLKD-C, IRQ2-A, POE11#	MTCLKD, POE11#, IRQ2
PE4	MTCLKC-C, IRQ1-B, POE10#-B	MTCLKC, POE10#, IRQ1

Table 4.5 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 80-Pin Package

Pin Number	RX62T	RX24T
1	EMLE	— (P02)
2	VSS	VSS
3	MDE	— (P00)
4	VCL	VCL
5	MD1	MD
6	MD0	— (P01)
9	RES#	RES#
10	XTAL	XTAL (P37)
11	VSS	VSS
12	EXTAL	EXTAL (P36)
13	VCC	VCC
23	— (PB5)	VCC
24	PLLVCC	— (PB4)
25	— (PB4)	VSS
26	PLLVSS	— (PB3)
32	— (PA2)	VCC
33	VCC	— (P96)
34	— (P96)	VSS
35	VSS	— (P95)
48	— (P33)	VCC
50	VCC	VSS
52	VSS	— (P24)
57	— (P21)	AVCC2
58	— (P20)	VREF
59	AVCC	AVSS2
60	AVSS	— (P62)
73	AVCC0	— (P41)
74	VREFH0	— (P40)
75	VREFL0	AVCC1
76	AVSS0	AVCC0
77	— (P11)	AVSS0
78	— (P10)	AVSS1

4.2.3 80-Pin Package (R5F562TxGDFF)

Table 4.6 lists points of difference between the pin functions for the 80-pin package (R5F562TxGDFF). Table 4.7 lists points of difference between pins for power supplies, clocks, and system control for the 80-pin package (R5F562TxGDFF).

Table 4.6 Points of Difference between Pin Functions for 80-Pin Package (R5F562TxGDFF)

I/O Port	RX62T	RX24T
P00	— (No I/O port)	IRQ2, ADST1
P01	— (No I/O port)	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD-B, IRQ0-A	MTIOC9B, MTCLKD, TMRI3, POE12#, CTS6#, RTS6#, SS6#, IRQ0
P11	— (No I/O port)	MTIOC3A, MTCLKC, TMO3, IRQ1
P20	ADTRG0#-B, MTCLKB-B, IRQ7	MTCLKB, MTIOC9C, TMRI4, IRQ7, ADTRG0#, AN016, CVREFC0
P21	— (No I/O port)	MTCLKA, MTIOC9A, TMCI4, IRQ6, ADTRG1#, AN116, CVREFC1
P22	ADTRG#, CRX-B, LRX, MISO-A	MTIC5W, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	CTX-B, LTX, MOSI-A	MTIC5V, TMO2, CACREF, MOSIA, COMP1
P24	RSPCK-A	MTIC5U, TMCI2, TMO6, RSPCKA, COMP0
P30	MTIOC0B-B, MTCLKD-A, SSL0-A	MTIOC0B, MTCLKD, TMCI6, SSLA0, IRQ7, COMP3
P31	MTIOC0A-B, MTCLKC-A, SSL1-A	MTIOC0A, MTCLKC, TMRI6, SSLA1, IRQ6
P32	MTIOC3C, MTCLKB-A, SSL2-A	— (No I/O port)
P33	MTIOC3A, MTCLKA-A, SSL3-A	— (No I/O port)
P36	— (No I/O port)	—
P37	— (No I/O port)	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001
P42	AN002	AN002
P43	AN003, CVREFL	AN003
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	AN103
P50	— (No I/O port)	AN206
P51	— (No I/O port)	AN207
P52	— (No I/O port)	AN208, IRQ0
P53	— (No I/O port)	AN209, IRQ1
P54	— (No I/O port)	AN210, IRQ2
P55	— (No I/O port)	AN211, IRQ3
P60	AN0	— (No I/O port)
P61	AN1	— (No I/O port)
P62	AN2	AN202, IRQ6

I/O Port	RX62T	RX24T
P63	AN3	— (No I/O port)
P70	IRQ5, POE0#	POE0#, IRQ5
P71	MTIOC3B, GTIOC0A-A	MTIOC3B
P72	MTIOC4A, GTIOC1A-A	MTIOC4A
P73	MTIOC4B, GTIOC2A-A	MTIOC4B
P74	MTIOC3D, GTIOC0B-A	MTIOC3D
P75	MTIOC4C, GTIOC1B-A	MTIOC4C
P76	MTIOC4D, GTIOC2B-A	MTIOC4D
P80	MTIC5W, RXD2-B	— (No I/O port)
P81	MTIC5V, TXD2-B	— (No I/O port)
P82	MTIC5U, SCK2-B	— (No I/O port)
P90	MTIOC7D	MTIOC7D
P91	MTIOC7C	MTIOC7C
P92	MTIOC6D	MTIOC6D
P93	MTIOC7B	MTIOC7B
P94	MTIOC7A	MTIOC7A
P95	MTIOC6B	MTIOC6B
P96	IRQ4, POE4#	POE4#, IRQ4
PA3	MTIOC2A	MTIOC2A, TMRI7, SSLA0
PA5	ADTRG1#-A, MTIOC1A	MTIOC1A, TMCI3, RXD6, SMISO6, SSCL6, MISOA, IRQ1, ADTRG1#
PB0	MTIOC0D	MTIOC0D, TMO0, TXD6, SMOSI6, SSDA6, MOSIA, ADTRG2#
PB1	MTIOC0C, RXD0, SCL	MTIOC0C, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B-A, TXD0, SDA	MTIOC0B, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	MTIOC0A-A, SCK0	MTIOC0A, CACREF, SCK6, RSPCKA
PB4	GTETRG, IRQ3, POE8#	POE8#, CTS5#, RTS5#, SS5#, IRQ3
PB5	CTX-A, TXD2-A	TXD5, SMOSI5, SSDA5
PB6	CRX-A, RXD2-A	RXD5, SMISO5, SSCL5, IRQ5
PB7	SCK2-A	— (No I/O port)
PD2	GTIOC2B-B	TMCI1, TMO4, SCK5, MOSIA
PD3	GTIOC2A-B, TXD1, TDO	TMO0, TXD1, SMOSI1, SSDA1
PD4	GTIOC1B-B, SCK1, TCK	TMCI0, TMCI6, SCK1, IRQ2
PD5	GTIOC1A-B, RXD1, TDI	TMRI0, TMRI6, RXD1, SMISO1, SSCL1, IRQ3
PD6	GTIOC0B-B, TMS	MTIOC9C, TMO1, CTS1#, RTS1#, SS1#, SSLA0, IRQ5, ADST0
PD7	GTIOC0A-B, TRST#	MTIOC9A, TMRI1, TMRI5, SSLA1
PE2	NMI, POE10#-A	POE10#, NMI
PE3	MTCLKD-C, IRQ2-A, POE11#	MTCLKD, POE11#, IRQ2
PE4	MTCLKC-C, IRQ1-B, POE10#-B	MTCLKC, POE10#, IRQ1

Table 4.7 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 80-Pin Package (R5F562TxGDFF)

Pin Number	RX62T	RX24T
1	EMLE	— (P02)
2	VSS	VSS
3	MDE	— (P00)
4	VCL	VCL
5	MD1	MD
6	MD0	— (P01)
9	RES#	RES#
10	XTAL	XTAL (P37)
11	VSS	VSS
12	EXTAL	EXTAL (P36)
13	VCC	VCC
23	— (PB5)	VCC
24	PLLVCC	— (PB4)
25	— (PB4)	VSS
26	PLLVSS	— (PB3)
32	— (PA3)	VCC
33	VCC	— (P96)
34	— (P96)	VSS
35	VSS	— (P95)
48	— (P70)	VCC
50	— (P32)	VSS
51	VCC	— (P30)
53	VSS	— (P23)
57	— (P22)	AVCC2
58	— (P20)	VREF
59	AVCC	AVSS2
60	AVSS	— (P62)
73	AVCC0	— (P41)
74	VREFH0	— (P40)
75	VREFL0	AVCC1
76	AVSS0	AVCC0
77	— (P82)	AVSS0
78	— (P81)	AVSS1

4.2.4 64-Pin Package

Table 4.8 lists points of difference between the pin functions for the 64-pin package. Table 4.9 lists points of difference between pins for power supplies, clocks, and system control for the 64-pin package.

Table 4.8 Points of Difference between Pin Functions for 64-Pin Package

I/O Port	RX62T	RX24T
P00	— (No I/O port)	IRQ2, ADST1
P01	— (No I/O port)	POE12#, IRQ4, ADST2
P02	— (No I/O port)	MTIOC9D, CTS1#, RTS1#, SS1#, IRQ5, ADST0
P10	MTCLKD-B, IRQ0-A	— (No I/O port)
P11	MTCLKC-B, IRQ1-A	MTIOC3A, MTCLKC, TMO3, IRQ1
P21	— (No I/O port)	MTCLKA, MTIOC9A, TMCI4, IRQ6, ADTRG1#, AN116, CVREFC1
P22	CRX-B, LRX, MISO-A	MTIC5W, TMRI2, TMO4, MISOA, ADTRG2#, COMP2
P23	CTX-B, LTX, MOSI-A	MTIC5V, TMO2, CACREF, MOSIA, COMP1
P24	RSPCK-A	MTIC5U, TMCI2, TMO6, RSPCKA, COMP0
P30	MTIOC0B-B, MTCLKD-A, SSL0-A	MTIOC0B, MTCLKD, TMCI6, SSLA0, IRQ7, COMP3
P31	MTIOC0A-B, MTCLKC-A, SSL1-A	MTIOC0A, MTCLKC, TMRI6, SSLA1, IRQ6
P32	MTIOC3C, MTCLKB-A, SSL2-A	— (No I/O port)
P33	MTIOC3A, MTCLKA-A, SSL3-A	— (No I/O port)
P36	— (No I/O port)	—
P37	— (No I/O port)	—
P40	AN000	AN000, CMPC00, CMPC01, CMPC22, CMPC23
P41	AN001	AN001
P42	AN002	AN002
P43	AN003, CVREFL	— (No I/O port)
P44	AN100	AN100, CMPC10, CMPC11, CMPC32, CMPC33
P45	AN101	AN101, CMPC02, CMPC03, CMPC20, CMPC21
P46	AN102	AN102, CMPC12, CMPC13, CMPC30, CMPC31
P47	AN103, CVREFH	— (No I/O port)
P50	— (No I/O port)	AN206
P51	— (No I/O port)	AN207
P52	— (No I/O port)	AN208, IRQ0
P53	— (No I/O port)	AN209, IRQ1
P54	— (No I/O port)	AN210, IRQ2
P70	IRQ5, POE0#	POE0#, IRQ5
P71	MTIOC3B, GTIOC0A-A	MTIOC3B
P72	MTIOC4A, GTIOC1A-A	MTIOC4A
P73	MTIOC4B, GTIOC2A-A	MTIOC4B
P74	MTIOC3D, GTIOC0B-A	MTIOC3D
P75	MTIOC4C, GTIOC1B-A	MTIOC4C
P76	MTIOC4D, GTIOC2B-A	MTIOC4D

I/O Port	RX62T	RX24T
P90	— (No I/O port)	MTIOC7D
P91	MTIOC7C	MTIOC7C
P92	MTIOC6D	MTIOC6D
P93	MTIOC7B	MTIOC7B
P94	MTIOC7A	MTIOC7A
P95	— (No I/O port)	MTIOC6B
P96	— (No I/O port)	POE4#, IRQ4
PA2	MTIOC2B, SSL1-B	— (No I/O port)
PA3	MTIOC2A, SSL0-B	— (No I/O port)
PA4	ADTRG0#-A, MTIOC1B, RSPCK-B	— (No I/O port)
PA5	ADTRG1#-A, MTIOC1A, MISO-B	— (No I/O port)
PB0	MTIOC0D, MOSI-B	— (No I/O port)
PB1	MTIOC0C, RXD0, SCL	MTIOC0C, TMCI0, ADSM1, RXD6, SMISO6, SSCL6, SCL0
PB2	MTIOC0B-A, TXD0, SDA	MTIOC0B, TMRI0, ADSM0, TXD6, SMOSI6, SSDA6, SDA0
PB3	MTIOC0A-A, SCK0	MTIOC0A, CACREF, SCK6, RSPCKA
PB4	GTETRG, IRQ3, POE8#	POE8#, CTS5#, RTS5#, SS5#, IRQ3
PB5	CTX-A, TXD2-A	TXD5, SMOSI5, SSDA5
PB6	CRX-A, RXD2-A	RXD5, SMISO5, SSCL5, IRQ5
PB7	SCK2-A	— (No I/O port)
PD3	GTIOC2A-B, TXD1, TDO	TMO0, TXD1, SMOSI1, SSDA1
PD4	GTIOC1B-B, SCK1, TCK	TMCI0, TMCI6, SCK1, IRQ2
PD5	GTIOC1A-B, RXD1, TDI	TMRI0, TMRI6, RXD1, SMISO1, SSCL1
PD6	GTIOC0B-B, TMS	MTIOC9C, TMO1, CTS1#, RTS1#, SS1#
PD7	GTIOC0A-B, TRST#	MTIOC9A, TMRI1, TMRI5, SSLA1
PE2	NMI, POE10#-A	POE10#, NMI

Table 4.9 Points of Difference between Pins for Power Supplies, Clocks, and System Control for 64-Pin Package

Pin Number	RX62T	RX24T
1	EMLE	— (P02)
2	MDE	— (P00)
3	VCL	VCL
4	MD1	MD
5	MD0	— (P01)
6	RES#	RES#
7	XTAL	XTAL (P37)
8	VSS	VSS
9	EXTAL	EXTAL (P36)
10	VCC	VCC
20	PLLVCC	— (PB3)
22	PLLVSS	— (PB1)
23	— (PB3)	VCC
25	— (PB1)	VSS
39	— (P70)	VCC
41	— (P32)	VSS
42	VCC	— (P30)
44	VSS	— (P23)
47	— (P23)	AVCC2/VREF
48	— (P22)	AVSS2
57	AVCC	— (P42)
58	VREFH0	— (P41)
59	VREFL0	— (P40)
60	AVSS0	AVCC1
61	— (P11)	AVCC0
62	— (P10)	AVSS0
63	— (PA5)	AVSS1

4.3 Points of Difference between Modules and Functions

Table 4.10 lists points of difference between modules and functions. This table lists points of difference for the specifications of the 100-pin package. For points of difference between individual modules and functions refer to 4.4, Points of Difference between Specifications in Detail, and the User's Manual: Hardware of each group, listed in 5, Reference Documents.

Table 4.10 Points of Difference between Modules and Functions

No.	Module or Function Name	RX62T	RX24T	RX24U
1	Operating modes	△	△	△
2	Resets	△	△	△
3	Option-setting memory	—	○	○
4	Voltage detection circuit (LVD/LVDAb/LVDAb)	△	△	△
5	Clock generation circuit	△	△	△
6	Clock frequency accuracy measurement circuit (CAC)	—	○	○
7	Low power consumption	△	△	△
8	Register write protection function	—	○	○
9	Interrupt controller (ICU/ICUb/ICUb)	△	△	△
10	Buses	△	△	△
11	Memory-protection unit (MPU)	△	△	△
12	Data transfer controller (DTC/DTCa/DTCa)	△	△	△
13	I/O ports	△	△	△
14	Multi-function pin controller (MPC)	—	○	○
15	Multi-function timer pulse unit 3 (MTU3/MTU3d/MTU3d)	△	△	△
16	Port output enable 3 (POE3/POE3b*1/POE3A)	△	△	△
17	General PWM timer (GPT/GPTB/GPTB)	△	△	△
18	8-bit timer (TMR)	—	○	○
19	Compare match timer (CMT)	◎	◎	◎
20	Watchdog timer (WDT)	○	—	—
21	Independent watchdog timer (IWDT/IWDTa/IWDTa)	△	△	△
22	Serial communications interface (SCIb/SCIg/SCIg)	△	△	△
23	I^2C bus interface (RIIC/RIICa/RIICa)	△	△	△
24	CAN module (CAN/RSCAN/RSCAN)	△	△	△
25	Serial peripheral interface (RSPI/RSPIb/RSPIb)	△	△	△
26	LIN module (LIN)	○	—	—
27	CRC calculator (CRC)	◎	◎	◎
28	12-bit A/D converter (S12ADA/S12ADF/S12ADF)	△	△	△
29	10-bit A/D converter (ADA)	○	—	—
30	D/A converter (DAa)	—	○	○
31	Comparator C (CMPC)	—	○	○
32	Data operation circuit (DOC)	—	○	○
33	RAM	△	△	△
34	Flash memory	△	△	△

Note 1. POE3b on RX24T (version A), POE3A on RX24T (version B)

Legend

◎: All groups have this module or function.

○ or —: Not all groups have this module or function.

○ means that the module or function is available on the group indicated.

— means that the module or function is not available on the group indicated.

△: All groups have this module or function, but the specifications differ between groups.

Where the module symbols differ, indications are as follows: Module or symbol name (symbol for RX62T/symbol for RX24T/symbol for RX24U).

4.4 Points of Difference between Specifications in Detail

Points of difference between specifications in detail are listed below. Specifications that apply only to one group or the other are indicated in blue. Specifications that are different between groups are indicated in red. Specifications that have no difference between the two groups are not described.

4.4.1 CPU

Table 4.11 lists the points of difference between the CPUs.

Table 4.11 Points of Difference between CPUs

Item	RX62T	RX24T and RX24U
Instruction architecture	RXv1	RXv2
CPU register set	• 16 general-purpose registers (32 bits) 9 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PC (BPSW) Fast interrupt vector register (FINTV) Floating-point status word (FPSW) — • 1 accumulator (64 bits) in single-chip mode (ACC)	• 16 general-purpose registers (32 bits) 10 control registers (32 bits) Interrupt stack pointer (ISP) User stack pointer (USP) Interrupt table register (INTB) Program counter (PC) Processor status word (PSW) Backup PC (BPC) Backup PSW (BPSW) Fast interrupt vector register (FINTV) Floating-point status word (FPSW) Exception table register (EXTB) • 2 accumulators (72 bits) in single-chip mode (ACC0, ACC1)
Addressing modes	10 addressing modes: Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative —	11 modes Immediate Register direct Register indirect Register relative Post-increment register indirect Pre-decrement register indirect Indexed register indirect Control register direct PSW direct Program counter relative Accumulator direct
Basic instructions	73 basic instructions — —	75 basic instructions Storing with LI flag clear (MOVCO) Loading with LI flag set (MOVLI)
Floating-point instructions	8 floating-point instructions — — —	11 floating-point instructions Floating-point square root (FSQRT) Floating point to integer conversion (FTOU) Integer to floating-point conversion (UTOF)

Item	RX62T	RX24T and RX24U
DSP instructions	9 DSP instructions Multiply-accumulate upper 16 bits (MACHI) Multiply-accumulate lower 16 bits (MACLO) Multiply upper 16 bits (MULHI) Multiply lower 16 bits (MULOL) Move upper 32 bits from accumulator (MVFACHI) Move accumulator middle 32 bits from accumulator (MVFACMI) Move accumulator lower 32 bits from accumulator (MVTACLO) Round 16-bit signed value in accumulator (RACW) — — — — — — — — — — — — — —	23 DSP instructions Multiply-accumulate upper 16 bits (MACHI) Multiply-accumulate lower 16 bits (MACLO) Multiply upper 16 bits (MULHI) Multiply lower 16 bits (MULOL) Move upper 32 bits from accumulator (MVFACHI) Move accumulator middle 32 bits from accumulator (MVFACMI) Move accumulator lower 32 bits from accumulator (MVTACLO) Round 16-bit signed value in accumulator (RACW) 32-bit multiply-accumulate (EMACA) 32-bit multiply-subtract (EMSBA) 32-bit multiply (EMULA) Multiply-accumulate upper 16 bits/lower 16 bits (MACLH) Multiply-accumulate upper 16 bits (MSBHI) Multiply-accumulate upper 16 bits/lower 16 bits (MSBLH) Multiply-accumulate lower 16 bits (MSBLO) Multiply upper 16 bits/lower 16 bits (MULLH) Move guard bits from accumulator (MVFACGU) Move lower 32 bits from accumulator (MVFACLO) Move guard bits to accumulator (MVTACGU) Round signed value in accumulator (RACL) Round signed value in accumulator (RADCL) Round 16-bit signed value in accumulator (RDACW)
Vector table	• Fixed vector table • Relocatable vector table	• Exception vector table • Interrupt vector table

4.4.2 Operating Modes

Table 4.12 lists the points of difference between the operating modes, and Table 4.13 lists the points of difference between the I/O registers related to the operating modes.

Table 4.12 Points of Difference between Operating Modes

Item	RX62T	RX24T and RX24U
Operating modes	• Single-chip mode • Boot mode SCI interface —	• Single-chip mode • Boot mode SCI interface FINE interface
Pins for setting a mode	MD1 and MD0	MD and UB (PC7)

Table 4.13 Points of Difference between I/O Registers Related to Operating Modes

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
MDMONR	MD0	MD0 pin status flag	Reserved
	MD	Reserved	MD pin status flag
	MD1	MD1 pin status flag	Reserved
	MDE	MDE pin status flag	Reserved
MDSR	—	Mode status register	Register not available
SYSCR0	—	System control register 0	Register not available

4.4.3 Resets

Table 4.14 lists the points of difference between the resets, and Table 4.15 lists the points of difference between the I/O registers related to the resets.

Table 4.14 Points of Difference between Resets

Item		RX62T	RX24T and RX24U
Types of resets	RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
	Power-on reset	VCC rises or falls (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
	Voltage monitoring reset	VCC falls (voltage detection: Vdet1 and Vdet2).	VCC falls (voltage detection: Vdet0, Vdet1, and Vdet2).
	Deep software standby reset	Deep software standby mode is canceled by an interrupt.	Not available
	Independent watchdog timer reset	The independent watchdog timer underflows.	The independent watchdog timer underflows or refresh error.
	Watchdog timer reset	The watchdog timer overflows.	Not available
	Software reset	Not available	Register settings

Table 4.15 Points of Difference between I/O Registers Related to Resets

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
RSTSR0	—	Register not available	Reset status register 0
RSTSR1	—	Register not available	Reset status register 1
RSTSR2	—	Register not available	Reset status register 2
SWRR	—	Register not available	Software reset register
RSTSR	—	Reset status register	Register not available
RSTCSR	—	Reset control/status register	Register not available
IWDTSR	REFEF	Reserved	Refresh error flag

4.4.4 Voltage Detection Circuit

Table 4.16 lists the points of difference between the voltage detection circuits, and Table 4.17 lists the points of difference between the I/O registers related to the voltage detection circuits.

Table 4.16 Points of Difference between Voltage Detection Circuits

Item		RX62T		RX24T and RX24U		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet1.	Voltage falls lower than Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	Fixed	Fixed	Selectable from three levels using OFS1.VDSEL [1:0] bits.	Selectable from nine levels using LVDLVLR. LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR. LVD2LVL[1:0] bits.
	Monitor flag	Not available	Not available	Not available	LVD1SR. LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR. LVD2MON flag: Monitors if higher or lower than Vdet2.
		Not available	Not available		LVD1SR. LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR. LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet1 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet1	Reset when Vdet2 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet2	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.

Item		RX62T		RX24T and RX24U		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
		Interrupt request when Vdet1 > VCC	Interrupt request when Vdet2 > VCC		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.

Table 4.17 Points of Difference between I/O Registers Related to Voltage Detection Circuits

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
RSTSR	—	Reset status register	Register not available
LVDKEYR	—	Key code register for low-voltage detection control	Register not available
LVDCR	—	Low-voltage detection control register	Register not available
LVD1CR1	—	Register not available	Voltage monitoring 1 circuit control register 1
LVD1SR	—	Register not available	Voltage monitoring 1 circuit status register
LVD2CR1	—	Register not available	Voltage monitoring 2 circuit control register 1
LVD2SR	—	Register not available	Voltage monitoring 2 circuit status register
LVCMPCR	—	Register not available	Voltage monitoring circuit control register
LVDLVLR	—	Register not available	Voltage detection level select register
LVD1CR0	—	Register not available	Voltage monitoring 1 circuit control register 0
LVD2CR0	—	Register not available	Voltage monitoring 2 circuit control register 0

4.4.5 Clock Generation Circuit

Table 4.18 lists the points of difference between the clock generation circuits, and Table 4.19 lists the points of difference between the I/O registers related to the clock generation circuits.

Table 4.18 Points of Difference between Clock Generation Circuits

Item	RX62T	RX24T and RX24U
Uses	• Generates the system clock (ICLK) supplied to the CPU, DTC, MTU3, GPT, ROM, and RAM. • Generates the peripheral module clocks (PCLK) supplied to the peripheral modules. • Generates the on-chip oscillator clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the RSCAN.
Operating frequencies	• ICLK: 8 MHz to 100 MHz • PCLK: 8 MHz to 50 MHz (Common to all peripheral modules) — • IWDTCLK: 125 kHz	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CANMCLK: 20 MHz (max.) • CACCLK: Same frequency as each oscillator • IWDTCLK: 15 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 12.5 MHz • External clock input frequency: 8 MHz to 12.5 MHz • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source is switched to an internally generated clock, and the MTU3 and GPT pins can be forcedly driven to high-impedance. —	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When main clock oscillation stop is detected, the system clock source is switched to LOCO, and MTU3 and GPT pin output can be stopped. • Drive capacity switching function

Item	RX62T	RX24T and RX24U
PLL	• Input clock source: Main clock —	• Input clock source: Main clock Clock with frequency of HOCO (32 MHz) divided by 4
	—	• Input division ratio: Selectable among 1, 2, and 4
	• Input frequency: 8 MHz to 12.5 MHz	• Input frequency: 4 MHz to 12.5 MHz
	• Frequency multiplication ratio: 8	• Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5)
	• Oscillation frequency: 64 MHz to 100 MHz	• Oscillation frequency: 40 MHz to 80 MHz
High-speed on-chip oscillator (HOCO)	—	Oscillation frequency: 32 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz
Internal oscillator circuit used when main clock oscillator is stopped	Oscillation frequency of internal oscillator circuit when oscillation stop detected: 0.5 MHz to 7.0 MHz	Not available (LOCO is used when oscillation stop is detected.)

Table 4.19 Points of Difference between I/O Registers Related to Clock Generation Circuits

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
SCKCR	PCK[3:0] (RX62T) PCKB[3:0] (RX24T and RX24U)	Peripheral module clock select bits	Peripheral module clock B (PCLKB) select bits
	PCKA[3:0]	Reserved	Peripheral module clock A (PCLKA) select bits
	PCKD[3:0]	Reserved	Peripheral module clock D (PCLKD) select bits
	FCK[3:0]	Reserved	FlashIF clock (FCLK) select bits
SCKCR3	—	Register not available	System clock control register 3
PLLCR	—	Register not available	PLL control register
PLLCR2	—	Register not available	PLL control register 2
MOSCCR	—	Register not available	Main clock oscillator control register
LOCOCR	—	Register not available	Low-speed on-chip oscillator control register
ILOCOCR	—	Register not available	IWDT-dedicated on-chip oscillator control register
HOCOCR	—	Register not available	High-speed on-chip oscillator control register
HOCOCR2	—	Register not available	High-speed on-chip oscillator control register 2
HOCOWTCR	—	Register not available	High-speed on-chip oscillator wait control register
OSCOVFSR	—	Register not available	Oscillation stabilization flag register
OSTDCR	OSTDIE	Reserved	Oscillation stop detection interrupt enable bit
	OSTDF	Oscillation stop detection flag	Reserved
	OSTDE	Oscillation stop detection function enable bit	Oscillation stop detection function enable bit
		Value after a reset differs.	
	KEY[7:0]	OSTDCR key code	Not available (as register is one byte in size)
OSTDSR	—	Register not available	Oscillation stop detection status register
MOSCWTCR	—	Register not available	Main clock oscillator wait control register
MOFCR	—	Register not available	Main clock oscillator forced oscillation control register
MEMWAIT	—	Register not available	Memory wait cycle setting register

4.4.6 Low Power Consumption

Table 4.20 lists the points of difference between the low power consumption functions, and Table 4.21 lists the points of difference between the I/O registers related to the low power consumption functions.

Table 4.20 Points of Difference between Low Power Consumption Functions

Item	RX62T	RX24T and RX24U
Reducing power consumption by switching clock signals	Ability to set division ratio separately • System clock (ICLK) • Peripheral module clock (PCLK)	Ability to set division ratio separately • System clock (ICLK) • High-speed peripheral module clock (PCLKA) • Peripheral module clock (PCLKB) • S12AD clock (PCLKD) • FlashIF clock (FCLK)
Low power consumption modes	Sleep mode All-module clock stop mode Software standby mode Deep software standby mode —	Sleep mode — Software standby mode — Deep sleep mode
Function for lower operating power consumption	Not available	Two operating power control modes • High-speed operating mode • Middle-speed operating mode

Table 4.21 Points of Difference between I/O Registers Related to Low Power Consumption Functions

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
SBYCR	STS[4:0]	Standby timer select bits Value after a reset differs.	Reserved
MSTPCRA	MSTPA2	Reserved	8-bit timer 7 and 6 (unit 3) module stop bit
	MSTPA3	Reserved	8-bit timer 5 and 4 (unit 2) module stop bit
	MSTPA4	Reserved	8-bit timer 3 and 2 (unit 1) module stop bit
	MSTPA5	Reserved	8-bit timer 1 and 0 (unit 0) module stop bit
	MSTPA16	12-bit A/D converter (unit 1) module stop bit	12-bit A/D converter 1 module stop bit
	MSTPA17	12-bit A/D converter (unit 0) module stop bit	12-bit A/D converter module stop bit
	MSTPA19	Reserved	8-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	12-bit A/D converter 2 module stop bit
	MSTPA24	12-bit A/D converter control section module stop bit	Reserved
	ACSE	All-module clock stop mode enable bit	Reserved
MSTPCRB	MSTPB0	CAN module stop bit	RSCAN module stop bit
	MSTPB6	Reserved	DOC module stop bit
	MSTPB7	LIN module stop bit	Reserved
	MSTPB10	Reserved	Comparator C module stop bit
	MSTPB17	Serial peripheral interface module stop bit	Serial peripheral interface 0 module stop bit
	MSTPB21	I^2C bus interface module stop bit	I^2C bus interface 0 module stop bit
	MSTPB25	Reserved	Serial communication interface 6 module stop bit
	MSTPB26	Reserved	Serial communication interface 5 module stop bit
	MSTPB29	Serial communication interface 2 module stop bit	Reserved
	MSTPB31	Serial communication interface 0 module stop bit	Reserved

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
MSTPCRC	MSTPC19	Reserved	Clock frequency accuracy measurement circuit module stop bit
	MSTPC24	Reserved	(RX24U only) Serial communication interface 11 module stop bit
	MSTPC26	Reserved	(RX24U only) Serial communication interface 9 module stop bit
	MSTPC27	Reserved	(RX24U only) Serial communication interface 8 module stop bit
	DSLPE	Reserved	Deep sleep mode enable bit
DPSBYCR	—	Deep standby control register	Register not available
DPSWCR	—	Deep standby wait control register	Register not available
DPSIER	—	Deep standby interrupt enable register	Register not available
DPSIFR	—	Deep standby interrupt flag register	Register not available
DPSIEGR	—	Deep standby interrupt edge register	Register not available
RSTSR	—	Reset status register	Register not available
DPSBKRy (y=0 to 31)		Deep standby backup register	Register not available
OPCCR	—	Register not available	Operating power control register

4.4.7 Interrupt Controller

Table 4.22 the points of difference between the interrupt controllers, and Table 4.23 lists the points of difference between the I/O registers related to the interrupt controllers.

Table 4.22 Points of Difference between Interrupt Controllers

Item		RX62T	RX24T and RX24U
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Sources: 101 • Interrupt detection: Edge detection/level detection • Edge detection or level detection is fixed for each source of the connected peripheral modules.	• Interrupts from peripheral modules • Sources: 163 (RX24T), 175 (RX24U) • Interrupt detection: Edge detection/level detection • Edge detection or level detection is fixed for each source of the connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source.	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported
	DTC control	DTC activation sources: 87 (78 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	DTC activation sources: 118 (RX24T), 124 (RX24U) (109 (RX24T) or 115 (RX24U) peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	IWDT underflow/ refresh error	Not available	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
Return from low power consumption modes		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. —	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source.
		• All-module clock stop mode: Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or WDT interrupts	—
		• Software standby mode: Return is initiated by non-maskable interrupts or IRQ0 to IRQ7 interrupts	• Software standby mode: Return is initiated by non-maskable interrupts or IRQ0 to IRQ7 interrupts

Table 4.23 Points of Difference between I/O Registers Related to Interrupt Controllers

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
IRQFLTE0	—	Register not available	IRQ pin digital filter enable register 0
IRQFLTC0	—	Register not available	IRQ pin digital filter setting register 0
NMISR	LVDST	Voltage monitoring interrupt status flag (b1)	Not available
	OSTST	Oscillation stop detection interrupt status flag (b2)	Oscillation stop detection interrupt status flag (b1)
	IWDTST	Reserved	IWDT underflow/refresh error status flag
	LVD1ST	Reserved	Voltage monitoring 1 interrupt status flag
	LVD2ST	Reserved	Voltage monitoring 2 interrupt status flag
NMIER	LVDEN	Voltage monitoring interrupt enable bit (b1)	Not available
	OSTEN	Oscillation stop detection interrupt enable bit (b2)	Oscillation stop detection interrupt enable bit (b1)
	IWDTEN	Reserved	IWDT underflow/refresh error enable bit
	LVD1EN	Reserved	Voltage monitoring 1 interrupt enable bit
	LVD2EN	Reserved	Voltage monitoring 2 interrupt enable bit
NMICLR	OSTCLR	OST clear bit (b2)	OST clear bit (b1)
	IWDTCLR	Reserved	IWDT clear bit
	LVD1CLR	Reserved	LVD1 clear bit
	LVD2CLR	Reserved	LVD2 clear bit
NMIFLTE	—	Register not available	NMI digital filter enable register
NMIFLTC	—	Register not available	NMI digital filter setting register

Headings in Table 4.24 indicate as follows.

- Vector No.: Vector number for the interrupt
- RX62T/RX24T/RX24U: Applies to RX62T Group, RX24T Group, or RX24U Group, as indicated.
- Source of interrupt request generation: Name of the source for generation of the interrupt request
- Name: Name of the interrupt
- Interrupt detection: “Edge” or “level” as the method for detection of the interrupt
- CPU interrupt: “○” in this column indicates that the source can be used for the CPU interrupt.
- DTC activation: “○” in this column indicates that the source can be used for DTC activation.
- sstb return: “○” in this column indicates that the source can be used for return from software-standby mode.
- sacs return: “○” in this column indicates that the source can be used for return from all-module clock stop mode.
- IER: IER register and bit corresponding to the vector number
- IPR: IPR register corresponding to the interrupt source
- DTCER: DTCER register corresponding to the DTC activation source

Table 4.24 Points of differences between Interrupt Vector Tables

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
0	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
1	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
2	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
3	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
4	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
5	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
6	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
7	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—
8	RX62T RX24T RX24U	—	Reserved Unconditional trap only	—	×	×	×	×	—	—	—

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
9	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
10	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
11	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
12	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
13	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
14	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
15	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U		Unconditional trap only								
21	RX62T	FCUIF	FIFERR	Level	○	×	×	×	IER02.IEN5	IPR01	—
	RX24T RX24U	—	Reserved	—	×				—	—	
32	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CAC	FERRF	Level	○				IER04.IEN0	IPR032	
33	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CAC	MENDF	Level	○				IER04.IEN1	IPR033	
34	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CAC	OVFF	Level	○				IER04.IEN2	IPR034	
40	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT	ETGIN	Edge	○				IER05.IEN0	IPR040	
41	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT	ETGIP	Edge	○				IER05.IEN1	IPR041	
44	RX62T	RSPI0	SPEI0	Level	○	×	×	×	IER05.IEN4	IPR14	—
	RX24T RX24U									IPR044	

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
45	RX62T	RSPI0	SPRI0	Edge	○	○	×	×	IER05.IEN5	IPR14	DTCER045
	RX24T									IPR044	
	RX24U										
46	RX62T	RSPI0	SPTI0	Edge	○	○	×	×	IER05.IEN6	IPR14	DTCER046
	RX24T									IPR044	
	RX24U										
47	RX62T	RSPI0	SPII0	Level	○	×	×	×	IER05.IEN7	IPR14	—
	RX24T									IPR044	
	RX24U										
48	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIA0	Edge	○	○			IER06.IEN0	IPR048	DTCER048
	RX24U										
49	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIB0	Edge	○	○			IER06.IEN1	IPR049	DTCER049
	RX24U										
50	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIC0	Edge	○	○			IER06.IEN2	IPR050	DTCER050
	RX24U										
51	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCID0	Edge	○	○			IER06.IEN3	IPR051	DTCER051
	RX24U										
52	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GDTE0	Edge	○				IER06.IEN4	IPR052	
	RX24U										
53	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIE0	Edge	○	○			IER06.IEN5	IPR053	DTCER053
	RX24U										
54	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIF0	Edge	○	○			IER06.IEN6	IPR054	DTCER054
	RX24U										
55	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT0	GTCIV0	Edge	○	○			IER06.IEN7	IPR055	DTCER055
	RX24U										
56	RX62T	CAN0	ERS0	Edge	○	×	×	×	IER07.IEN0	IPR18	—
	RX24T	GPT0	GTCIU0			○				IPR056	DTCER056
	RX24U										
57	RX62T	CAN0	RXF0	Edge	○	×	×	×	IER07.IEN1	IPR18	—
	RX24T	DOC	DOPCF	Level						IPR057	
	RX24U										
58	RX62T	CAN0	TXF0	Edge	○	×	×	×	IER07.IEN2	IPR18	—
	RX24T	—	Reserved	—	×				—	—	
	RX24U										

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
59	RX62T	CAN0	RXM0	Edge	○	×	×	×	IER07.IEN3	IPR18	—
	RX24T RX24U	RSCAN	COMFRXINT			○				IPR059	DTCER059
60	RX62T	CAN0	TXM0	Edge	○	×	×	×	IER07.IEN4	IPR18	—
	RX24T RX24U	RSCAN	RXFINT	Level						IPR060	
61	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	RSCAN	TXINT	Level	○				IER07.IEN5	IPR061	
62	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	RSCAN	CHERRINT	Level	○				IER07.IEN6	IPR062	
63	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	RSCAN	GLERRINT	Level	○				IER07.IEN7	IPR063	
64	RX62T	External pin	IRQ0	Edge/	○	○	○	○	IER08.IEN0	IPR20	DTCER064
	RX24T RX24U	ICU		Level				×		IPR064	
65	RX62T	External pin	IRQ1	Edge/	○	○	○	○	IER08.IEN1	IPR21	DTCER065
	RX24T RX24U	ICU		Level				×		IPR065	
66	RX62T	External pin	IRQ2	Edge/	○	○	○	○	IER08.IEN2	IPR22	DTCER066
	RX24T RX24U	ICU		Level				×		IPR066	
67	RX62T	External pin	IRQ3	Edge/	○	○	○	○	IER08.IEN3	IPR23	DTCER067
	RX24T RX24U	ICU		Level				×		IPR067	
68	RX62T	External pin	IRQ4	Edge/	○	○	○	○	IER08.IEN4	IPR24	DTCER068
	RX24T RX24U	ICU		Level				×		IPR068	
69	RX62T	External pin	IRQ5	Edge/	○	○	○	○	IER08.IEN5	IPR25	DTCER069
	RX24T RX24U	ICU		Level				×		IPR069	
70	RX62T	External pin	IRQ6	Edge/	○	○	○	○	IER08.IEN6	IPR26	DTCER070
	RX24T RX24U	ICU		Level				×		IPR070	
71	RX62T	External pin	IRQ7	Edge/	○	○	○	○	IER08.IEN7	IPR27	DTCER071
	RX24T RX24U	ICU		Level				×		IPR071	
88	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	LVD	LVD1	Edge	○		○		IER0B.IEN0	IPR088	

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
89	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	LVD	LVD2	Edge	○		○		IER0B.IEN1	IPR089	
96	RX62T	WDT	WOVI	Edge	○	×	×	○	IER0C.IEN0	IPR40	—
	RX24T RX24U	—	Reserved	—	×			×	—	—	
98	RX62T	AD0	ADI0	Edge	○	○	×	×	IER0C.IEN2	IPR44	DTCER098
	RX24T RX24U	GPT1	GTCIA1							IPR098	
99	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIB1	Edge	○	○			IER0C.IEN3	IPR099	DTCER099
100	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIC1	Edge	○	○			IER0C.IEN4	IPR100	DTCER100
101	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCID1	Edge	○	○			IER0C.IEN5	IPR101	DTCER101
102	RX62T	S12AD0	S12ADI0	Edge	○	○	×	×	IER0C.IEN6	IPR48	DTCER102
	RX24T RX24U	S12AD	S12ADI							IPR102	
103	RX62T	S12AD1	S12ADI1	Edge	○	○	×	×	IER0C.IEN7	IPR48	DTCER103
	RX24T RX24U	S12AD	GBADI							IPR103	
104	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD	GCADI	Edge	○	○			IER0D.IEN0	IPR104	DTCER104
105	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD1	S12ADI1	Edge	○	○			IER0D.IEN1	IPR105	DTCER105
106	RX62T	Comparator	CMPI	Edge	○	○	×	×	IER0D.IEN2	IPR49	DTCER106
	RX24T RX24U	S12AD1	GBADI1							IPR106	
107	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD1	GCADI1	Edge	○	○			IER0D.IEN3	IPR107	DTCER107
108	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CMPC0	CMPC0	Edge	○	○			IER0D.IEN4	IPR108	DTCER108
109	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CMPC1	CMPC1	Edge	○	○			IER0D.IEN5	IPR109	DTCER109

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
110	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	CMPC2	CMPC2	Edge	○	○			IER0D.IEN6	IPR110	DTCER110
111	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	S12ADI2	Edge	○	○			IER0D.IEN7	IPR111	DTCER111
112	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	GBADI2	Edge	○	○			IER0E.IEN0	IPR112	DTCER112
113	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	S12AD2	GCADI2	Edge	○	○			IER0E.IEN1	IPR113	DTCER113
114	RX62T RX24T RX24U	MTU0	TGIA0	Edge	○	○	×	×	IER0E.IEN2	IPR51 IPR114	DTCER114
115	RX62T RX24T RX24U	MTU0	TGIB0	Edge	○	○	×	×	IER0E.IEN3	IPR51 IPR114	DTCER115
116	RX62T RX24T RX24U	MTU0	TGIC0	Edge	○	○	×	×	IER0E.IEN4	IPR51 IPR114	DTCER116
117	RX62T RX24T RX24U	MTU0	TGID0	Edge	○	○	×	×	IER0E.IEN5	IPR51 IPR114	DTCER117
118	RX62T RX24T RX24U	MTU0	TCIV0	Edge	○	×	×	×	IER0E.IEN6	IPR52 IPR118	—
119	RX62T RX24T RX24U	MTU0	TGIE0	Edge	○	×	×	×	IER0E.IEN7	IPR52 IPR118	—
120	RX62T RX24T RX24U	MTU0	TGIF0	Edge	○	×	×	×	IER0F.IEN0	IPR52 IPR118	—
121	RX62T RX24T RX24U	MTU1	TGIA1	Edge	○	○	×	×	IER0F.IEN1	IPR53 IPR121	DTCER121
122	RX62T RX24T RX24U	MTU1	TGIB1	Edge	○	○	×	×	IER0F.IEN2	IPR53 IPR121	DTCER122
123	RX62T RX24T RX24U	MTU1	TCIV1	Edge	○	×	×	×	IER0F.IEN3	IPR54 IPR123	—

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
124	RX62T RX24T RX24U	MTU1	TCIU1	Edge	○	×	×	×	IER0F.IEN4	IPR54 IPR123	—
125	RX62T RX24T RX24U	MTU2	TGIA2	Edge	○	○	×	×	IER0F.IEN5	IPR55 IPR125	DTCER125
126	RX62T RX24T RX24U	MTU2	TGIB2	Edge	○	○	×	×	IER0F.IEN6	IPR55 IPR125	DTCER126
127	RX62T RX24T RX24U	MTU2	TCIV2	Edge	○	×	×	×	IER0F.IEN7	IPR56 IPR127	—
128	RX62T RX24T RX24U	MTU2	TCIU2	Edge	○	×	×	×	IER10.IEN0	IPR56 IPR127	—
129	RX62T RX24T RX24U	MTU3	TGIA3	Edge	○	○	×	×	IER10.IEN1	IPR57 IPR129	DTCER129
130	RX62T RX24T RX24U	MTU3	TGIB3	Edge	○	○	×	×	IER10.IEN2	IPR57 IPR129	DTCER130
131	RX62T RX24T RX24U	MTU3	TGIC3	Edge	○	○	×	×	IER10.IEN3	IPR57 IPR129	DTCER131
132	RX62T RX24T RX24U	MTU3	TGID3	Edge	○	○	×	×	IER10.IEN4	IPR57 IPR129	DTCER132
133	RX62T RX24T RX24U	MTU3	TCIV3	Edge	○	×	×	×	IER10.IEN5	IPR58 IPR133	—
134	RX62T RX24T RX24U	MTU4	TGIA4	Edge	○	○	×	×	IER10.IEN6	IPR59 IPR134	DTCER134
135	RX62T RX24T RX24U	MTU4	TGIB4	Edge	○	○	×	×	IER10.IEN7	IPR59 IPR134	DTCER135
136	RX62T RX24T RX24U	MTU4	TGIC4	Edge	○	○	×	×	IER11.IEN0	IPR59 IPR134	DTCER136
137	RX62T RX24T RX24U	MTU4	TGID4	Edge	○	○	×	×	IER11.IEN1	IPR59 IPR134	DTCER137

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
138	RX62T RX24T RX24U	MTU4	TCIV4	Edge	○	○	×	×	IER11.IEN2	IPR5A IPR138	DTCER138
139	RX62T RX24T RX24U	MTU5	TGIU5	Edge	○	○	×	×	IER11.IEN3	IPR5B IPR139	DTCER139
140	RX62T RX24T RX24U	MTU5	TGIV5	Edge	○	○	×	×	IER11.IEN4	IPR5B IPR139	DTCER140
141	RX62T RX24T RX24U	MTU5	TGIW5	Edge	○	○	×	×	IER11.IEN5	IPR5B IPR139	DTCER141
142	RX62T RX24T RX24U	MTU6	TGIA6	Edge	○	○	×	×	IER11.IEN6	IPR5C IPR142	DTCER142
143	RX62T RX24T RX24U	MTU6	TGIB6	Edge	○	○	×	×	IER11.IEN7	IPR5C IPR142	DTCER143
144	RX62T RX24T RX24U	MTU6	TGIC6	Edge	○	○	×	×	IER12.IEN0	IPR5C IPR142	DTCER144
145	RX62T RX24T RX24U	MTU6	TGID6	Edge	○	○	×	×	IER12.IEN1	IPR5C IPR142	DTCER145
146	RX62T RX24T RX24U	MTU6	TCIV6	Edge	○	×	×	×	IER12.IEN2	IPR5D IPR146	—
149	RX62T RX24T RX24U	MTU7	TGIA7	Edge	○	○	×	×	IER12.IEN5	IPR5E IPR149	DTCER149
150	RX62T RX24T RX24U	MTU7	TGIB7	Edge	○	○	×	×	IER12.IEN6	IPR5E IPR149	DTCER150
151	RX62T RX24T RX24U	MTU7	TGIC7	Edge	○	○	×	×	IER12.IEN7	IPR5F IPR151	DTCER151
152	RX62T RX24T RX24U	MTU7	TGID7	Edge	○	○	×	×	IER13.IEN0	IPR5F IPR151	DTCER152
153	RX62T RX24T RX24U	MTU7	TCIV7	Edge	○	○	×	×	IER13.IEN1	IPR60 IPR153	DTCER153

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
159	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIA9	Edge	○	○			IER13.IEN7	IPR159	DTCER159
160	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIB9	Edge	○	○			IER14.IEN0	IPR159	DTCER160
161	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIC9	Edge	○	○			IER14.IEN1	IPR159	DTCER161
162	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGID9	Edge	○	○			IER14.IEN2	IPR159	DTCER162
163	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TCIV9	Edge	○				IER14.IEN3	IPR163	
164	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIE9	Edge	○				IER14.IEN4	IPR163	
165	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	MTU9	TGIF9	Edge	○				IER14.IEN5	IPR163	
168	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	POE	OEI1	Level	○				IER15.IEN0	IPR168	
169	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	POE	OEI2	Level	○				IER15.IEN1	IPR168	
170	RX62T	POE	OEI1	Level	○	×	×	×	IER15.IEN2	IPR67	—
	RX24T RX24U		OEI3							IPR168	
171	RX62T	POE	OEI2	Level	○	×	×	×	IER15.IEN3	IPR67	—
	RX24T RX24U		OEI4							IPR168	
172	RX62T	POE	OEI3	Level	○	×	×	×	IER15.IEN4	IPR67	—
	RX24T RX24U		OEI5							IPR168	
173	RX62T	POE	OEI4	Level	○	×	×	×	IER15.IEN5	IPR67	—
	RX24T RX24U	CMPC3	CMPC3	Edge		○				IPR173	DTCER173
174	RX62T	GPT0	GTCIA0	Edge	○	○	×	×	IER15.IEN6	IPR68	DTCER174
	RX24T RX24U	TMR0	CMIA0							IPR174	

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
175	RX62T	GPT0	GTCIB0	Edge	○	○	×	×	IER15.IEN7	IPR68	DTCER175
	RX24T RX24U	TMR0	CMIB0							IPR174	
176	RX62T	GPT0	GTCIC0	Edge	○	○	×	×	IER16.IEN0	IPR68	DTCER176
	RX24T RX24U	TMR0	OVI0			×				IPR174	—
177	RX62T	GPT0	GTCIE0	Edge	○	○	×	×	IER16.IEN1	IPR69	DTCER177
	RX24T RX24U	TMR1	CMIA1							IPR177	
178	RX62T	GPT0	GTCIV0	Edge	○	○	×	×	IER16.IEN2	IPR69	DTCER178
	RX24T RX24U	TMR1	CMIB1							IPR177	
179	RX62T	GPT0	LOCO1	Edge	○	○	×	×	IER16.IEN3	IPR69	DTCER179
	RX24T RX24U	TMR1	OVI1			×				IPR177	—
180	RX62T	GPT1	GTCIA1	Edge	○	○	×	×	IER16.IEN4	IPR6A	DTCER180
	RX24T RX24U	TMR2	CMIA2							IPR180	
181	RX62T	GPT1	GTCIB1	Edge	○	○	×	×	IER16.IEN5	IPR6A	DTCER181
	RX24T RX24U	TMR2	CMIB2							IPR180	
182	RX62T	GPT1	GTCIC1	Edge	○	○	×	×	IER16.IEN6	IPR6A	DTCER182
	RX24T RX24U	TMR2	OVI2			×				IPR180	—
183	RX62T	GPT1	GTCIE1	Edge	○	○	×	×	IER16.IEN7	IPR6B	DTCER183
	RX24T RX24U	TMR3	CMIA3							IPR183	
184	RX62T	GPT1	GTCIV1	Edge	○	○	×	×	IER17.IEN00	IPR6B	DTCER184
	RX24T RX24U	TMR3	CMIB3							IPR183	
185	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	TMR3	OVI3	Edge	○				IER17.IEN1	IPR183	
186	RX62T	GPT2	GTCIA2	Edge	○	○	×	×	IER17.IEN2	IPR6C	DTCER186
	RX24T RX24U	TMR4	CMIA4							IPR186	
187	RX62T	GPT2	GTCIB2	Edge	○	○	×	×	IER17.IEN3	IPR6C	DTCER187
	RX24T RX24U	TMR4	CMIB4							IPR186	
188	RX62T	GPT2	GTCIC2	Edge	○	○	×	×	IER17.IEN4	IPR6C	DTCER188
	RX24T RX24U	TMR4	OVI4			×				IPR186	—

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
189	RX62T	GPT2	GTCIE2	Edge	○	○	×	×	IER17.IEN5	IPR6D	DTCER189
	RX24T RX24U	TMR5	CMIA5							IPR189	
190	RX62T	GPT2	GTCIV2	Edge	○	○	×	×	IER17.IEN6	IPR6D	DTCER190
	RX24T RX24U	TMR5	CMIB5							IPR189	
191	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	TMR5	OVI5	Edge	○				IER17.IEN7	IPR189	
192	RX62T	GPT3	GTCIA3	Edge	○	○	×	×	IER18.IEN0	IPR6E	DTCER192
	RX24T RX24U	TMR6	CMIA6							IPR192	
193	RX62T	GPT3	GTCIB3	Edge	○	○	×	×	IER18.IEN1	IPR6E	DTCER193
	RX24T RX24U	TMR6	CMIB6							IPR192	
194	RX62T	GPT3	GTCIC3	Edge	○	○	×	×	IER18.IEN2	IPR6E	DTCER194
	RX24T RX24U	TMR6	OVI6			×				IPR192	—
195	RX62T	GPT3	GTCIE3	Edge	○	○	×	×	IER18.IEN3	IPR6F	DTCER195
	RX24T RX24U	TMR7	CMIA7							IPR195	
196	RX62T	GPT3	GTCIV3	Edge	○	○	×	×	IER18.IEN4	IPR6F	DTCER196
	RX24T RX24U	TMR7	CMIB7							IPR195	
197	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	TMR7	OVI7	Edge	○				IER18.IEN5	IPR195	
202	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GDTE1	Edge	○				IER19.IEN2	IPR202	
203	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIE1	Edge	○	○			IER19.IEN3	IPR203	DTCER203
204	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIF1	Edge	○	○			IER19.IEN4	IPR204	DTCER204
205	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIV1	Edge	○	○			IER19.IEN5	IPR205	DTCER205
206	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT1	GTCIU1	Edge	○	○			IER19.IEN6	IPR206	DTCER206

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
207	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIA2	Edge	○	○			IER19.IEN7	IPR207	DTCER207
208	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIB2	Edge	○	○			IER1A.IEN0	IPR208	DTCER208
209	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIC2	Edge	○	○			IER1A.IEN1	IPR209	DTCER209
210	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCID2	Edge	○	○			IER1A.IEN2	IPR210	DTCER210
211	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GDTE2	Edge	○				IER1A.IEN3	IPR211	
212	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIE2	Edge	○	○			IER1A.IEN4	IPR212	DTCER212
213	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT2	GTCIF2	Edge	○	○			IER1A.IEN5	IPR213	DTCER213
214	RX62T	SCI0	ERI0	Level	○	×	×	×	IER1A.IEN6	IPR80	—
	RX24T RX24U	GPT2	GTCIV2	Edge		○				IPR214	DTCER214
215	RX62T	SCI0	RXI0	Edge	○	○	×	×	IER1A.IEN7	IPR80	DTCER215
	RX24T RX24U	GPT2	GTCIU2							IPR215	
216	RX62T	SCI0	TXI0	Edge	○	○	×	×	IER1B.IEN0	IPR80	DTCER216
	RX24T RX24U	GPT3	GTCIA3							IPR216	
217	RX62T	SCI0	TEI0	Level	○	×	×	×	IER1B.IEN1	IPR80	—
	RX24T RX24U	GPT3	GTCIB3	Edge		○				IPR217	DTCER217
218	RX62T	SCI1	ERI1	Level	○	×	×	×	IER1B.IEN2	IPR81	—
	RX24T RX24U									IPR218	
219	RX62T	SCI1	RXI1	Edge	○	○	×	×	IER1B.IEN3	IPR81	DTCER219
	RX24T RX24U									IPR218	
220	RX62T	SCI1	TXI1	Edge	○	○	×	×	IER1B.IEN4	IPR81	DTCER220
	RX24T RX24U									IPR218	

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
221	RX62T	SCI1	TEI1	Level	○	×	×	×	IER1B.IEN5	IPR81	—
	RX24T									IPR218	
	RX24U										
222	RX62T	SCI2	ERI2	Level	○	×	×	×	IER1B.IEN6	IPR82	—
	RX24T	SCI5	ERI5							IPR222	
	RX24U										
223	RX62T	SCI2	RXI2	Edge	○	○	×	×	IER1B.IEN7	IPR82	DTCER223
	RX24T	SCI5	RXI5							IPR222	
	RX24U										
224	RX62T	SCI2	TXI2	Edge	○	○	×	×	IER1C.IEN0	IPR82	DTCER224
	RX24T	SCI5	TXI5							IPR222	
	RX24U										
225	RX62T	SCI2	TEI2	Level	○	×	×	×	IER1C.IEN1	IPR82	—
	RX24T	SCI5	TEI5							IPR222	
	RX24U										
226	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	SCI6	ERI6	Level	○				IER1C.IEN2	IPR226	
	RX24U										
227	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	SCI6	RXI6	Edge	○	○			IER1C.IEN3	IPR226	DTCER227
	RX24U										
228	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	SCI6	TXI6	Edge	○				IER1C.IEN4	IPR226	DTCER228
	RX24U										
229	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	SCI6	TEI6	Level	○				IER1C.IEN5	IPR226	
	RX24U										
238	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT3	GTCIC3	Edge	○	○			IER1D.IEN6	IPR238	DTCER238
	RX24U										
239	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT3	GTCID3	Edge	○	○			IER1D.IEN7	IPR239	DTCER239
	RX24U										
240	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT3	GDTE3	Edge	○				IER1E.IEN0	IPR240	
	RX24U										
241	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT3	GTCIE3	Edge	○	○			IER1E.IEN1	IPR241	DTCER241
	RX24U										
242	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T	GPT3	GTCIF3	Edge	○	○			IER1E.IEN2	IPR242	DTCER242
	RX24U										

Vector No.	RX62T/ RX24T and RX24U	Source of Interrupt Request Generation	Name	Interrupt Detection	CPU Interrupt	DTC Activation	sstb Return	sacs Return	IER	IPR	DTCER
243	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT3	GTCIV3	Edge	○	○			IER1E.IEN3	IPR243	DTCER243
244	RX62T	—	Reserved	—	×	×	×	×	—	—	—
	RX24T RX24U	GPT3	GTCIU3	Edge	○	○			IER1E.IEN4	IPR244	DTCER244
246	RX62T	RIIC0	ICEEI0	Level	○	×	×	×	IER1E.IEN6	IPR88	—
	RX24T RX24U		EEI0							IPR246	
247	RX62T	RIIC0	ICRXI0	Edge	○	○	×	×	IER1E.IEN7	IPR89	DTCER247
	RX24T RX24U		RXI0							IPR247	
248	RX62T	RIIC0	ICTXI0	Edge	○	○	×	×	IER1F.IEN0	IPR8A	DTCER248
	RX24T RX24U		TXI0							IPR248	
249	RX62T	RIIC0	ICTEI0	Level	○	×	×	×	IER1F.IEN1	IPR8B	—
	RX24T RX24U		TEI0							IPR249	
250	RX62T RX24T	—	Reserved	—	×	×	×	×	—	—	—
	RX24U	SCI11	ERI11	Level	○				IER1F.IEN2	IPR250	
251	RX62T RX24T	—	Reserved	—	×	×	×	×	—	—	—
	RX24U	SCI11	RXI11	Edge	○	○			IER1F.IEN3	IPR250	DTCER251
252	RX62T RX24T	—	Reserved	—	×	×	×	×	—	—	—
	RX24U	SCI11	TXI11	Edge	○	○			IER1F.IEN4	IPR250	DTCER252
253	RX62T RX24T	—	Reserved	—	×	×	×	×	—	—	—
	RX24U	SCI11	TEI11	Level	○				IER1F.IEN5	IPR250	
254	RX62T	LIN0	LIN0	Edge	○	×	×	×	IER1F.IEN6	IPR90	—
	RX24T RX24U	—	Reserved	—	×				—	—	

4.4.8 Buses

Table 4.25 lists the points of difference between the buses, and Table 4.26 lists the points of difference in between the I/O registers related to the buses.

Table 4.25 Points of Difference between Buses

Item		RX62T	RX24T and RX24U
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (bus error monitoring section, interrupt controller, etc.) • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, bus error monitoring section, interrupt controller, etc.) • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules (WDT, CMT, CRC, SCI, etc.) • Operates in synchronization with the peripheral module clock (PCLK).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 3	—	• Connected to peripheral modules (RSCAN and CMPC). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3, GPT). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (MTU3, GPT, and SCI11 (RX24U)) • Operates in synchronization with the peripheral module clock (PCLKA).
	Internal peripheral bus 6	• Connected to the on-chip ROM (P/E) and data flash memory. • Operates in synchronization with the peripheral module clock (PCLK).	• Connected to the flash control module and E2 DataFlash. • Operates in synchronization with the FlashIF clock (FCLK).

Table 4.26 Points of Difference between I/O Registers Related to Buses

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
BEREN	TOEN	Reserved	Timeout detection enable bit
BERSR1	TO	Reserved	Timeout bit
BUSPRI	—	Register not available	Bus priority control register

4.4.9 Memory-Protection Unit

Table 4.27 lists the points of difference between the I/O registers related to the memory-protection units.

Table 4.27 Points of Difference between I/O Registers Related to the Memory-Protection Units

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
MPESTS	IA (RX62T) IMPER (RX24T and RX24U)	Instruction memory-protection error generated bit	Instruction memory-protection error generated bit
	DA (RX62T) DMPER (RX24T and RX24U)	Data memory-protection error generated bit	Data memory-protection error generated bit

4.4.10 Data Transfer Controller

Table 4.28 lists the points of difference between the data transfer controllers and Table 4.29 lists the points of difference between the I/O registers related to the data transfer controllers.

Table 4.28 Points of Difference between Data Transfer Controllers

Item	RX62T	RX24T and RX24U
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. The maximum repeat size is 256 data units. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 255 data units.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. The maximum repeat size is 256 data units. • Block transfer mode A single activation leads to the transfer of a single block. The maximum block size is 256 data units.
Data transfer units	• 1 data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Number of data units per block: 1 to 255	• 1 data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Number of data units per block: 1 to 256

Table 4.29 Points of Difference between I/O Registers Related to Data Transfer Controllers

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
DTCVBR	—	DTC vector base address (lower 12 bits)	DTC vector base address (lower 10 bits)
	—	DTC vector base address (upper 20 bits)	DTC vector base address (lower 22 bits)

4.4.11 I/O Ports

Table 4.30 lists the points of difference between the I/O ports and Table 4.31 lists the points of difference between the I/O registers related to the I/O ports.

Table 4.30 Points of Difference between I/O Ports

Item	Port Symbol	RX62T	RX24T	RX24U
Ports	PORT0	Not available	P00, P01, P02	
	PORT2	P20, P21, P22, P23, P24, —		P20, P21, P22, P23, P24, P27
	PORT3	P30, P31, P32, P33	P30, P31, P32, P33, P36, P37	
	PORT5	P50, P51, P52, P53, P54, P55		—, —, P52, P53, P54, P55
Input pull-up function	PORT0	Not available	P00 to P02 Available	
	PORT1	P10, P11 Not available	P10, P11 Available	
	PORT2	P20 to P24, — Not available	P20 to P24, — Available	P20 to P24, P27 Available
	PORT3	P30 to P33 Not available	P30 to P33, P36, P37 Available	
	PORT4	P40 to P47 Not available	P40 to P47 Available	
	PORT5	P50, P51, P52 to P55 Not available	P50, P51, P52 to P55 Available	—, —, P52 to P55 Available
	PORT6	P60 to P65 Not available	P60 to P65 Available	
	PORT7	P70 to P76 Not available	P70 to P76 Available	
	PORT8	P80 to P82 Not available	P80 to P82 Available	
	PORT9	P90 to P96 Not available	P90 to P96 Available	
	PORTA	PA0 to PA5 Not available	PA0 to PA5 Available	
	PORTB	PB0 to PB7 Not available	PB0 to PB7 Available	
	PORTD	PD0 to PD7 Not available	PD0 to PD7 Available	
	PORTE	PE0, PE1, PE3 to PE5 Not available	PE0, PE1, PE3 to PE5 Available	
Open drain output	PORT0	Not available	P00 to P02 Available	
	PORT1	P10, P11 Not available	P10, P11 Available	
	PORT2	P20 to P24, — Not available	P20 to P24, — Available	P20 to P24, P27 Available
	PORT3	P30 to P33, —, — Not available	P30 to P33, P36, P37 Available	

Item	Port Symbol	RX62T	RX24T	RX24U
Open drain output	PORT7	P70 to P76 Not available	P70 to P76 Available	
	PORT8	P80 to P82 Not available	P80 to P82 Available	
	PORT9	P90 to P96 Not available	P90 to P96 Available	
	PORTA	PA0 to PA5 Not available	PA0 to PA5 Available	
	PORTB	PB0 to PB7 Not available However, open drain output is available on PB1 for SCL only and on PB2 for SDA only. Available	PB0 to PB7 Available	
	PORTD	PD0 to PD7 Not available	PD0 to PD7 Available	
	PORTE	PE0, PE1, PE3 to PE5 Not available	PE0, PE1, PE3 to PE5 Available	
Drive Capacity Switching	PORT0	Not available	P00 to P02 Available	
	PORT1	P10, P11 Not available	P10, P11 Available	
	PORT2	P20 to P24, — Not available	P20 to P24, — Available	P20 to P24, P27 Available
	PORT3	P30 to P33 Not available	P30 to P33 Available	
	PORT7	P70 Not available	P70 Available	
	PORT8	P80, P82 Not available	P80, P82 Available	
	PORT9	P96 Not available	P96 Available	
	PORTA	PA0 to PA5 Not available	PA0 to PA5 Available	
	PORTB	PB0, PB3, PB4, PB6, PB7 Not available	PB0, PB3, PB4, PB6, PB7 Available	
	PORTD	PD0 to PD2, PD4 to PD7 Not available	PD0 to PD2, PD4 to PD7 Available	
	PORTE	PE0, PE1, PE3 to PE5 Not available	PE0, PE1, PE3 to PE5 Available	
Large-current pins	PORT8	P81 Not available	P81 Available	
	PORTB	PB5 Not available	PB5 Available	
	PORTD	PD3 Not available	PD3 Available	
5 V tolerant	PORTB	PB1, PB2 Not available	PB1, PB2 Available	

Table 4.31 Points of Difference between I/O Registers Related to I/O Ports

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
PDR	—	Register not available	Port direction register
PODR	—	Register not available	Port output data register
PIDR	—	Register not available	Port input register
PMR	—	Register not available	Port mode register
ODR0	—	Register not available	Open-drain control register 0
ODR1	—	Register not available	Open-drain control register 1
PCR	—	Register not available	Pull-up control register
DSCR	—	Register not available	Drive capacity control register
DDR	—	Data direction register	Register not available
DR	—	Data register	Register not available
PORT	—	Port register	Register not available
ICR	—	Input buffer control register	Register not available
PF8IRQ	—	Port function register 8	Register not available
PFAADC	—	Port function register A	Register not available
PFCMTU	—	Port function register C	Register not available
PFDGPT	—	Port function register D	Register not available
PFFSCI	—	Port function register F	Register not available
PFGSPI	—	Port function register G	Register not available
PFHSPI	—	Port function register H	Register not available
PFJCAN	—	Port function register J	Register not available
PFKLIN	—	Port function register K	Register not available
PFMPOE	—	Port function register M	Register not available
PFNPOE	—	Port function register N	Register not available

4.4.12 Multi-Function Timer Pulse Unit 3

Table 4.32 lists the points of difference between the multi-function timer pulse unit 3 modules, and Table 4.33 lists the points of difference between the I/O registers related to the multi-function timer pulse unit 3 modules.

Table 4.32 Points of Difference between Multi-Function Timer Pulse Unit 3 Modules

Item	RX62T	RX24T and RX24U
Pulse input/output	Maximum 24	Maximum 28
Count clocks	6 to 8 clocks for each channel (4 clocks for channel 5)	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and 4 clocks for MTU1 and MTU2 (LWA = 1))
Operating frequency	8 to 100 MHz	Up to 80 MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output on compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, and MTU9] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing on compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, and MTU7] Buffer operation specifiable	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9] Buffer operation specifiable
	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available	[MTU1 and MTU2] • Phase counting mode can be specified independently. • Cascade connection operation available • MTU1 and MTU2 interlocked operation in 32-bit phase counting mode is available (TMDR3.LWA = 1).
	—	[MTU6 and MTU7] An AC asynchronous motor (brushless DC motor) drive mode using interlocked operation with MTU9 in complementary PWM or reset PWM operation is available, selectable between two types of waveform output (chopping or level).
Interrupt sources	38	45

Table 4.33 Points of Difference between I/O Registers Related to Multi-Function Timer Pulse Unit 3 Modules

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
TCR2	—	Register not available	Timer control register 2
TMDR1	BFE	Buffer operation E bit 0: MTU0.TGRE and MTU0.TGRF operate normally. 1: MTU0.TGRE and MTU0.TGRF are used together for buffer operation.	Buffer operation E bit 0: MTU0.TGRE and MTU9.TGRE, and MTU0.TGRF and TU9.TGRF operate normally. 1: MTU0.TGRE and MTU9.TGRE, and MTU0.TGRF and TU9.TGRF are used together for buffer operation.
TMDR2n (n = A or B)	—	Register not available	Timer mode register 2
TMDR3	—	Register not available	Timer mode register 3
TSR	TGFA	Input capture/output compare flag A	Reserved
	TGFB	Input capture/output compare flag B	Reserved
	TGFC	Input capture/output compare flag C	Reserved
	TGFD	Input capture/output compare flag D	Reserved
	TCFV	Overflow flag	Reserved
	TCFU	Underflow flag	Reserved
TSR2	—	Timer status register 2	Register not available
TBTM	TTSE	Timing select E bit 0: When compare match E occurs in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE 1: When MTU0.TCNT is cleared, data is transferred from MTU0.TGRF to MTU0.TGRE.	Timing select E bit 0: When compare match E occurs in MTU0 or MTU9, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE. 1: When MTU0.TCNT or MTU9.TCNT is cleared, data is transferred from MTU0.TGRF to MTU0.TGRE or MTU9.TGRF to MTU9.TGRE.
TCNTLW	—	Register not available	Timer longword counter
TGRnLW (n = A or B)	—	Register not available	Timer longword general register
TSTRA	CST9	Reserved	Counter start 9 bit
TSYRA	SYNC9	Reserved	Timer sync 9 bit
TCSYSTR	SCH9	Reserved	Synchronous start 9 bit
TGCRB	—	Register not available	Timer gate control register B
NFCRn (n = 0 to 4, 6, 7, 9, C)	—	Register not available	Noise filter control register n
NFCR5	—	Register not available	Noise filter control register 5
TADSTRGR0	—	Register not available	A/D conversion start request select register 0
TADSTRGR1	—	Register not available	A/D conversion start request select register 1

4.4.13 Port Output Enable 3

Table 4.34 lists the points of difference between the port output enable 3 modules, and Table 4.35 lists the points of difference between the I/O registers related to the port output enable 3 modules.

Table 4.34 Points of Difference between Port Output Enable 3 Modules

Item	RX62T	RX24T and RX24U
Target pins to be placed in high-impedance state (RX24T and RX24U also selectable as general I/O)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — • GPT output pins GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B)
Conditions for high-impedance state (RX24T and RX24U also selectable as general I/O)	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, or POE11# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D 4. MTIOC6B and MTIOC6D 5. MTIOC7A and MTIOC7C 6. MTIOC7B and MTIOC7D 7. GTIOC0A-A and GTIOC0B-A 8. GTIOC1A-A and GTIOC1B-A 9. GTIOC2A-A and GTIOC2B-A • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (S12ADA)	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: 1. MTIOC3B and MTIOC3D 2. MTIOC4A and MTIOC4C 3. MTIOC4B and MTIOC4D 4. MTIOC6B and MTIOC6D 5. MTIOC7A and MTIOC7C 6. MTIOC7B and MTIOC7D 7. GTIOC0A and GTIOC0B 8. GTIOC1A and GTIOC1B 9. GTIOC2A and GTIOC2B • When a register setting is made • When clock generation circuit oscillation stop is detected • When comparator detection occurs in the comparator (CMPC)

Item	RX62T	RX24T and RX24U
Functions (Ability to select high-impedance state and general I/O ports on RX24T and RX24U)	• Each of the POE0#, POE4#, POE8#, POE10#, or POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.	• Each of the POE0#, POE4# POE8#, POE10#, POE11#, or POE12# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling.
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, or POE11# pin falling-edge or low-level sampling.	• Each of the POE0#, POE4# POE8#, POE10#, POE11#, or POE12# input pins can be set for falling edge, or for low-level sampling, halting output on all pins subject to control.
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state when the oscillation-stop detection circuit in the clock pulse generator detects stopped oscillation.	• Output can be stopped on all pins subject to control when clock generation circuit oscillation stop is detected.
	• Pins for the MTU complementary PWM output or the GPT large-current output pins can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins or the GPT large-current output pins are compared and simultaneous active-level output continues for one cycle or more.	• Output can be halted on the MTU complementary PWM output pins when simultaneous active-level output continues for 1 cycle or longer by comparing the output level of the MTU complementary PWM output pins or the GPT large-current output pins.
		• Output can be halted on the GPT output pins when simultaneous active-level output continues for 1 cycle or longer by comparing the output level of the GPT output pins (GPT0, GPT1, and GPT2).
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state in response to comparator detection by the 12-bit A/D converter (S12ADA).	• Output on all pins subject to control can be stopped in response to comparator detection by the 12-bit A/D converter (S12ADA).
	• Pins for the MTU complementary PWM output, MTU0, and GPT pins can be placed in the high-impedance state by modifying settings in the POE3 registers.	• By making settings to the POE3 register, output can be halted on all pins subject to control.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.

Table 4.35 Points of Difference between I/O Registers Related to Multi-Function Timer Pulse Unit 3 Modules

Register Symbol	Bit Symbol	RX62T	RX24T	RX24U
ICSR3	POE8E	POE8 high-impedance enable bit	POE8 output disable bit	
ICSR4	POE10E	POE10 high-impedance enable bit	POE10 output disable bit	
ICSR5	POE11E	POE11 high-impedance enable bit	POE11 output disable bit	
ICSR6	—	Register not available	Input level control/status register 6	
ICSR7	—	Register not available	Input level control/status register 7	
OCSR1	OCE1	Output short high-impedance enable 1 bit	Simultaneous conduction output disable 1 bit	
OCSR2	OCE2	Output short high-impedance enable 2 bit	Simultaneous conduction output disable 2 bit	
OCSR3	—	Register not available		Output level control/status register 3
ALR1	OLSG0A	MTIOC3B/GTIOC0A-A active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit	
	OLSG0B	MTIOC3D/GTIOC0B-A active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit	
	OLSG1A	MTIOC4A/GTIOC1A-A active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit	
	OLSG1B	MTIOC4C/GTIOC1B-A active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit	
	OLSG2A	MTIOC4B/GTIOC2A-A active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit	
	OLSG2B	MTIOC4D/GTIOC2B-A active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit	
ALR2	—	Register not available	Active level register 2	
ALR3	—	Register not available		Active level register 3
SPOER	MTUCH34HIZ	MTU3, MTU4 output high-impedance enable bit	MTU3, MTU4/GPT0 to GPT2 pin output disable bit	
	MTUCH67HIZ	MTU6, MTU7 output high-impedance enable bit	MTU6, MTU7 pin output disable bit	
	MTUCH0HIZ	MTU0 output high-impedance enable bit	MTU0 pin output disable bit	
	GPT01HIZ (RX62T) GPT02HIZ (RX24U)	GPT0, GPT1 output high-impedance enable bit	Reserved	GPT0 to GPT2/MTU3, MTU4 pin output disable bit
	GPT23HIZ (RX62T) GPT03HIZ (RX24T/RX24U)	GPT2, GPT3 output high-impedance enable bit	GPT0 to GPT3 pin output disable bit	
	MTUCH9HIZ	Reserved	MTU9 output disable bit	

Register Symbol	Bit Symbol	RX62T	RX24T	RX24U
POECR1	MTU0AZE	MTU CH0A high-impedance enable bit	MTIOC0A (PB3) pin high-impedance enable bit	
	MTU0BZE	MTU CH0B high-impedance enable bit	MTIOC0B (PB2) pin high-impedance enable bit	
	MTU0CZE	MTU CH0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit	
	MTU0DZE	MTU CH0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit	
	MTU0A1ZE	Reserved	MTIOC0A (P31) pin high-impedance enable bit	
	MTU0B1ZE	Reserved	MTIOC0B (P30) pin high-impedance enable bit	
POECR2	MTU7BDZE	MTU CH7BD high-impedance enable bit	MTIOC7B/MTIOC7D pin high-impedance enable bit	
	MTU7ACZE	MTU CH7AC high-impedance enable bit	MTIOC7A/MTIOC7C pin high-impedance enable bit	
	MTU6BDZE	MTU CH6BD high-impedance enable bit	MTIOC6B/MTIOC6D pin high-impedance enable bit	
	MTU4BDZE	MTU CH4BD high-impedance enable bit	MTIOC4B/MTIOC4D (P73/P76) pin high-impedance enable bit	
	MTU4ACZE	MTU CH4AC high-impedance enable bit	MTIOC4A/MTIOC4C (P72/P75) pin high-impedance enable bit	
	MTU3BDZE	MTU CH3BD high-impedance enable bit	MTIOC3B/MTIOC3D (P71/P74) pin high-impedance enable bit	
POECR3	GPT0ABZE (RX62T) GPT0AZE (RX24U)	GPT CH0AB high-impedance enable bit	Reserved	GTIOC0A (P12) pin high-impedance enable bit
		Initial value after a reset differs.		
	GPT1ABZE (RX62T) GPT0BZE (RX24U)	GPT CH1AB high-impedance enable bit	Reserved	GTIOC0B (P15) pin high-impedance enable bit
		Initial value after a reset differs.		
	GPT1AZE	Reserved		GTIOC1A (P13) pin high-impedance enable bit
	GPT1BZE	Reserved		GTIOC1B (P16) pin high-impedance enable bit
	GPT2AZE	Reserved		GTIOC2A (P14) pin high-impedance enable bit
	GPT2BZE	Reserved		GTIOC2B (P17) pin high-impedance enable bit

Register Symbol	Bit Symbol	RX62T	RX24T RX24U
POECR3	GPT2ABZE (RX62T) GPT0A1ZE (RX24T/RX24U)	GPT CH2AB high-impedance enable bit Initial value after a reset differs.	GTIOC0A (PD2) pin high-impedance enable bit
	GPT3ABZE (RX62T) GPT0B1ZE (RX24T/RX24U)	GPT CH3AB high-impedance enable bit Initial value after a reset differs.	GIOC0B (PD1) pin high-impedance enable bit
	GPT1A1ZE	Reserved	GTIOC1A (PD0) pin high-impedance enable bit
	GPT1B1ZE	Reserved	GTIOC1B (PB7) pin high-impedance enable bit
	GPT2A1ZE	Reserved	GTIOC2A (PB6) pin high-impedance enable bit
	GPT2B1ZE	Reserved	GTIOC2B (PB5) pin high-impedance enable bit
	GPT3A1ZE	Reserved	GTIOC3A high-impedance enable bit
	GPT3B1ZE	Reserved	GTIOC3B high-impedance enable bit
POECR4	CMADDMT34ZE	MTU CH34 high-impedance CFLAG add bit	MTU3, MTU4 output disabling condition CFLAG add bit
	IC2ADDMT34ZE	MTU CH34 high-impedance POE4F add bit	MTU3, MTU4 output disabling condition POE4F add bit
	IC3ADDMT34ZE	MTU CH34 high-impedance POE8F add bit	MTU3, MTU4 output disabling condition POE8F add bit
	IC4ADDMT34ZE	MTU CH34 high-impedance POE10F add bit	MTU3, MTU4 output disabling condition POE10F add bit
	IC5ADDMT34ZE	MTU CH34 high-impedance POE11F add bit	MTU3, MTU4 output disabling condition POE11F add bit
	IC6ADDMT34ZE	Reserved	MTU3, MTU4 output disabling condition POE12F add bit
	CMADDMT67ZE	MTU CH67 high-impedance CFLAG add bit	MTU6, MTU7 output disabling condition CFLAG add bit
	IC1ADDMT67ZE	MTU CH67 high-impedance POE0F add bit	MTU6, MTU7 output disabling condition POE0F add bit
	IC3ADDMT67ZE	MTU CH67 high-impedance POE8F add bit	MTU6, MTU7 output disabling condition POE8F add bit
	IC4ADDMT67ZE	MTU CH67 high-impedance POE10F add bit	MTU6, MTU7 output disabling condition POE10F add bit
	IC5ADDMT67ZE	MTU CH67 high-impedance POE11F add bit	MTU6, MTU7 output disabling condition POE11F add bit
	IC6ADDMT67ZE	Reserved	MTU6, MTU7 output disabling condition POE12F add bit
POECR5	CMADDMT0ZE	MTU CH0 high-impedance CFLAG add bit	MTU0 output disabling condition CFLAG add bit
	IC1ADDMT0ZE	MTU CH0 high-impedance POE0F add bit	MTU0 output disabling POE0F add bit
	IC2ADDMT0ZE	MTU CH0 high-impedance POE4F add bit	MTU0 output disabling POE4F add bit
	IC4ADDMT0ZE	MTU CH0 high-impedance POE10F add bit	MTU0 output disabling POE10F add bit

Register Symbol	Bit Symbol	RX62T	RX24T	RX24U
POECR5	IC5ADDMT0ZE	MTU CH0 high-impedance POE11F add bit	MTU0 output disabling POE11F add bit	
	IC6ADDMT0ZE	Reserved	MTU0 output disabling POE12F add bit	
POECR6	CMADDGPT01ZE (RX62T) CMADDGPT02ZE (RX24U)	GPT CH01 high-impedance CFLAG add bit	Reserved	GPT0 to GPT2 output disabling condition CFLAG add bit
	IC1ADDGPT01ZE (RX62T) IC1ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE0F add bit	Reserved	GPT0 to GPT2 output disabling condition POE0F add bit
	IC2ADDGPT01ZE (RX62T) IC2ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE4F add bit	Reserved	GPT0 to GPT2 output disabling condition POE4F add bit
	IC3ADDGPT01ZE (RX62T) IC3ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE8F add bit	Reserved	GPT0 to GPT2 output disabling condition POE8F add bit
	IC5ADDGPT01ZE (RX62T) IC5ADDGPT02ZE (RX24U)	GPT CH01 high-impedance POE11F add bit	Reserved	GPT0 to GPT2 output disabling condition POE11F add bit
	IC6ADDGPT02ZE	Reserved		GPT0 to GPT2 output disabling condition POE12F add bit
	CMADDGPT23ZE (RX62T) CMADDGPT03ZE (RX24T/RX24U)	GPT CH23 high-impedance CFLAG add bit	GPT0 to GPT3 output disabling condition CFLAG add bit	
	IC1ADDGPT23ZE (RX62T) IC1ADDGPT03ZE (RX24T/RX24U)	GPT CH23 high-impedance POE0F add bit	GPT0 to GPT3 output disabling condition POE0F add bit	
	IC2ADDGPT23ZE (RX62T) IC2ADDGPT03ZE (RX24T/RX24U)	GPT CH23 high-impedance POE4F add bit	GPT0 to GPT3 output disabling condition POE4F add bit	
	IC3ADDGPT23ZE (RX62T) IC3ADDGPT03ZE (RX24T/RX24U)	GPT CH23 high-impedance POE8F add bit	GPT0 to GPT3 output disabling condition POE8F add bit	

Register Symbol	Bit Symbol	RX62T	RX24T	RX24U
POECR6	IC4ADDGPT23ZE (RX62T) IC4ADDGPT03ZE (RX24T/RX24U)	GPT CH23 high-impedance POE10F add bit	GPT0 to GPT3 output disabling condition POE10F add bit	
	IC6ADDGPT03ZE	Reserved	GPT0 to GPT3 output disabling condition POE12F add bit	
POECR7	MTU9AZE	Register not available	MTIOC9A (PD7) pin high-impedance enable bit	
	MTU9BZE		MTIOC9B (PE0) pin high-impedance enable bit	
	MTU9CZE		MTIOC9C (PD6) pin high-impedance enable bit	
	MTU9DZE		MTIOC9D (PE1) pin high-impedance enable bit	
	MTU9A1ZE		MTIOC9A (P21) pin high-impedance enable bit	
	MTU9B1ZE		MTIOC9B (P10) pin high-impedance enable bit	
	MTU9C1ZE		MTIOC9C (P20) pin high-impedance enable bit	
	MTU9D1ZE		MTIOC9D (P02) pin high-impedance enable bit	
	MTU9A2ZE		Reserved	MTIOC9A (P26) pin high-impedance enable bit
	MTU9C2ZE		Reserved	MTIOC9C (P25) pin high-impedance enable bit
POECR8	—	Register not available	Port output enable control register 8	
PMMCR0	—	Register not available	Port mode mask control register 0	
PMMCR1	—	Register not available	Port mode mask control register 1	
PMMCR2	GPT0AME	Register not available	Reserved	GTIOC0A/MTIOC3B (P12) pin port mode mask enable bit
	GPT0BME		Reserved	GTIOC0B/MTIOC3D (P15) pin port mode mask enable bit
	GPT1AME		Reserved	GTIOC1A/MTIOC4A (P13) pin port mode mask enable bit

Register Symbol	Bit Symbol	RX62T	RX24T	RX24U
PMMCR2	GPT1BME	Register not available	Reserved	GTIOC1B/MTIOC4C (P16) pin port mode mask enable bit
	GPT2AME		Reserved	GTIOC2A/MTIOC4B (P14) pin port mode mask enable bit
	GPT2BME		Reserved	GTIOC2B/MTIOC4D (P17) pin port mode mask enable bit
PWMCR3	MTU9A2ME	Register not available	Reserved	MTIOC9A (P26) pin port mode mask enable bit
	MTU9C2ME		Reserved	MTIOC9C (P25) pin port mode mask enable bit
POECMPFR	—	Register not available	Port output enable comparator output detection flag register	
POECMPSEL	—	Register not available	Port output enable comparator request select register	
POECMPEXm (m = 0 to 2, 4, 5) (RX24T) (m = 0 to 5) (RX24U)	—	Register not available	Port output enable comparator request extended selection register m	

4.4.14 General PWM Timer

Table 4.36 lists the points of difference between the general PWM timers, and Table 4.37 lists the points of difference between the I/O registers related to the general PWM timers.

Table 4.36 Points of Difference between General PWM Timers

Item	RX62T	RX24T and RX24U
Functions	• 16 bits × 4 channels	• Selectable among 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels
	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter
	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3
	• Independently selectable clock source for each channel (4 internal clocks)	• Independently selectable clock source for each channel (9 internal clocks and 4 external clocks)
	• 2 I/O pins per channel	• 2 I/O pins per channel
	—	• Ability to select noise filter for each input path
	• 2 output compare/input capture registers per channel	• 2 output compare/input capture registers per channel
	• For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used	• For each channel, 4 registers that function as buffer register for the 2 output compare/input capture registers and that can be used as compare registers when buffering is not used
	• Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation	• Generation of asymmetrical left/right PWM waveforms allowing peak and trough buffering during output compare operation
	• Frame cycle registers for each channel (ability to generate interrupts at overflow/underflow)	• Frame cycle registers for each channel (ability to generate interrupts at overflow/underflow)
	• Support for synchronous operation of each counter	• Support for synchronous operation of each counter
	• Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support)	• Synchronous operation mode (synchronous or precisely at user-defined timing (phase shifting support)
	• Ability to generate dead time during PWM operation	• Ability to generate dead time during PWM operation
	• Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time	• Ability to combine 3 counters to generate 3-phase PWM waveforms with dead time
	• Starting, clearing, and stopping counters in response to external or internal trigger	• Starting, stopping, and clearing counters in response to external or internal trigger

Item	RX62T	RX24T and RX24U
Functions	• Ability to use comparator detection, software, or compare match as internal trigger source • Ability to count edges of the frequency-divided IWDT dedicated low-speed on-chip oscillator clock using a count clock produced by frequency dividing the system clock (ICLK) (oscillation error detection)	• Ability to use comparator detection, MTU3 count start, software, or compare match as internal trigger source —

Table 4.37 Points of Difference between I/O Registers Related to General PWM Timers

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTSTR	CST1	GPT1.GTCNT count start bit	GPT1.GTCNT/GPT01.GTCNTLW count start bit
	CST3	GPT3.GTCNT count start bit	GPT3.GTCNT/GPT23.GTCNTLW count start bit
NFCR	—	Register not available	Noise filter control register
GTHSCR General PWM Timer hardware source start control register (RX62T) General PWM timer hardware source start/stop control register (RX24T/RX24U)	CSHW1[1:0]	GPT1.GTCNT hardware source count start bits	GPT1.GTCNT/GPT01.GTCNTLW hardware source count start bits
	CSHW3[1:0]	GPT3.GTCNT hardware source count start bits	GPT3.GTCNT/GPT23.GTCNTLW hardware source count start bits
	CPHW1[1:0]	GPT1.GTCNT hardware source count stop bits	GPT1.GTCNT/GPT01.GTCNTLW hardware source count stop bits
	CPHW3[1:0]	GPT3.GTCNT hardware source count stop bits	GPT3.GTCNT/GPT23.GTCNTLW hardware source count stop bits
GTHCCR	CCHW1[1:0]	GPT1.GTCNT hardware source counter clear bits	GPT1.GTCNT/GPT01.GTCNTLW hardware source counter clear bits
	CCHW3[1:0]	GPT3.GTCNT hardware source counter clear bits	GPT3.GTCNT/GPT23.GTCNTLW hardware source counter clear bits
	CCSW1	GPT1.GTCNT counter clear bit	GPT1.GTCNT/GPT01.GTCNTLW counter clear bit
	CCSW3	GPT3.GTCNT counter clear bit	GPT3.GTCNT/GPT23.GTCNTLW counter clear bit

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHSSR	CSHSL0[3:0]	GPT0.GTCNT hardware counter start source select bits b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input — — Settings other than the above are prohibited.	GPT0.GTCNT hardware counter start source select bits b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHSSR	CSHSL1[3:0]	GPT1.GTCNT hardware counter start source select bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input — — Settings other than the above are prohibited.	GPT1.GTCNT/GPT01.GTCNTLW hardware counter start source select bits b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHSSR	CSHSL2[3:0]	GPT2.GTCNT hardware counter start source select bits b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input — — Settings other than the above are prohibited.	GPT2.GTCNT hardware counter start source select bits b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHSSR	CSHSL3[3:0]	GPT3.GTCNT hardware counter start source select bits b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: Setting prohibited 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input — — Settings other than the above are prohibited.	GPT3.GTCNT/GPT23.GTCNTLW hardware counter start source select bits b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output 0 0 1 0: MTU0 count start 0 0 1 1: MTU1 count start 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output 0 1 1 0: MTU2 count start 0 1 1 1: MTU4 count start 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input 1 1 0 1: MTU7 count start 1 1 1 0: MTU9 count start Settings other than the above are prohibited when count operation is started by a hardware source.
GTHPSR	CSHPL0[3:0]	GPT0.GTCNT hardware count stop/clear source select bits b3 b0 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited.	GPT0.GTCNT hardware count stop/clear source select bits b3 b0 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHPSR	CSHPL1[3:0]	GPT1.GTCNT hardware count stop/clear source select bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited.	GPT1.GTCNT/GPT01.GTCNTLW hardware count stop/clear source select bits b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.
	CSHPL2[3:0]	GPT2.GTCNT hardware count stop/clear source select bits b11 b8 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited.	GPT2.GTCNT hardware count stop/clear source select bits b11 b8 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTHPSR	CSHPL3[3:0]	GPT3.GTCNT hardware count stop/clear source select bits b15 b12 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input Settings other than the above are prohibited.	GPT3.GTCNT/GPT01.GTCNTLW hardware count stop/clear source select bits b15 b12 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input Settings other than the above are prohibited when count operation is started by a hardware source.
GTWP	WP0	GPT0 register write enable bit	GPT0 register write disable bit
	WP1	GPT1 register write enable bit	GPT1/GPT01 register write disable bit
	WP2	GPT2 register write enable bit	GPT2 register write disable bit
	WP3	GPT3 register write enable bit	GPT3/GPT23 register write disable bit
GTSYNC	SYNC0[1:0]	GPT0.GTCNT counter synchronous clear source select bits b1 b0 0 0: Synchronous clear is not performed. 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT0.GTCNT counter synchronous clear source select bits b1 b0 0 0: Synchronous clear is not performed. 0 1: GPT0.GTCNT counter is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT counter is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT counter is synchronously cleared by a GPT3/GPT23 clearing source.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTSYNC	SYNC1[1:0]	GPT1.GTCNT counter synchronous clear source select bits b5 b4 0 0: GPT1.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: Synchronous clear is not performed. 1 0: GPT1.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT1.GTCNT/GPT01.GTCNTLW counter synchronous clear source select bits b5 b4 0 0: GPT1.GTCNT counter is synchronously cleared by a GPT0 clearing source. 0 1: Synchronous clear is not performed. 1 0: GPT1.GTCNT/GPT01.GTCNTLW counter is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT/GPT01.GTCNTLW counter is synchronously cleared by a GPT3/GPT23 clearing source.
	SYNC2[1:0]	GPT2.GTCNT counter synchronous clear source select bits b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: Synchronous clear is not performed. 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.	GPT2.GTCNT counter synchronous clear source select bits b9 b8 0 0: GPT2.GTCNT counter is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT counter is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: Synchronous clear is not performed. 1 1: GPT2.GTCNT counter is synchronously cleared by a GPT3 clearing source.
	SYNC3[1:0]	GPT3.GTCNT counter synchronous clear source select bits b13 b12 0 0: GPT3.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: Synchronous clear is not performed.	GPT3.GTCNT/GPT01.GTCNTLW counter synchronous clear source select bits b13 b12 0 0: GPT3.GTCNT/GPT23.GTCNTLW counter is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT/GPT23.GTCNTLW counter is synchronously cleared by a GPT1/GPT01 clearing source. 1 0: GPT3.GTCNT counter is synchronously cleared by a GPT2 clearing source. 1 1: Synchronous clear is not performed.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTETINT	ETIPF	External trigger rising input interrupt request flag	Reserved (Value after a reset is undefined.)
	ETINF	External trigger falling input interrupt request flag	Reserved (Value after a reset is undefined.)
	GTENFCS [1:0]	Reserved	GTETRG noise filter sampling clock select bits
	GTETRGEN	Reserved	GTETRG noise filter enable bit
GTBDR	BD0[0] (RX62T) BD00 (RX24T/ RX24U)	GPT0.GTCCR buffer operation disable bit	GPT0.GTCCR buffer operation disable bit
	BD0[1] (RX62T) BD01 (RX24T/ RX24U)	GPT0.GTPR buffer operation disable bit	GPT0.GTPR buffer operation disable bit
	BD0[2] (RX62T) BD02 (RX24T/ RX24U)	GPT0.GTADTR buffer operation disable bit	GPT0.GTADTR buffer operation disable bit
	BD0[3] (RX62T) BD03 (RX24T/ RX24U)	GPT0.GTDV buffer operation disable bit	GPT0.GTDV buffer operation disable bit
	BD1[0] (RX62T) BD10 (RX24T/ RX24U)	GPT1.GTCCR buffer operation disable bit	GPT1.GTCCR/ GPT01.GTCCRLW buffer operation disable bit
	BD1[1] (RX62T) BD11 (RX24T/ RX24U)	GPT1.GTPR buffer operation disable bit	GPT1.GTPR/GPT01.GTPRLW buffer operation disable bit
	BD1[2] (RX62T) BD12 (RX24T/ RX24U)	GPT1.GTADTR buffer operation disable bit	GPT1.GTADTR/ GPT01.GTADTRLW buffer operation disable bit
	BD1[3] (RX62T) BD13 (RX24T/ RX24U)	GPT1.GTDV buffer operation disable bit	GPT1.GTDV/GPT01.GTDVLW buffer operation disable bit
	BD2[0] (RX62T) BD20 (RX24T/ RX24U)	GPT2.GTCCR buffer operation disable bit	GPT2.GTCCR buffer operation disable bit
	BD2[1] (RX62T) BD21 (RX24T/ RX24U)	GPT2.GTPR buffer operation disable bit	GPT2.GTPR buffer operation disable bit
	BD2[2] (RX62T) BD22 (RX24T/ RX24U)	GPT2.GTADPR buffer operation disable bit	GPT2.GTADPR buffer operation disable bit

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTBDR	BD2[3] (RX62T) BD23 (RX24T/ RX24U)	GPT2.GTDV buffer operation disable bit	GPT2.GTDV buffer operation disable bit
	BD3[0] (RX62T) BD30 (RX24T/ RX24U)	GPT3.GTCCR buffer operation disable bit	GPT3.GTCCR/ GPT23.GTCCRLW buffer operation disable bit
	BD3[1] (RX62T) BD31 (RX24T/ RX24U)	GPT3.GTPR buffer operation disable bit	GPT3.GTPR/GPT23.GTPRLW buffer operation disable bit
	BD3[2] (RX62T) BD32 (RX24T/ RX24U)	GPT3.GTADTR buffer operation disable bit	GPT3.GTADTR/ GPT23.GTADTRLW buffer operation disable bit
	BD3[3] (RX62T) BD33 (RX24T/ RX24U)	GPT3.GTDV buffer operation disable bit	GPT3.GTDV/GPT23.GTDVLW buffer operation disable bit
LCCR	—	LOCO count control register	Register not available
LCST	—	LOCO count status register	Register not available
LCNT	—	LOCO count value register	Register not available
LCNTA	—	LOCO count result average register	Register not available
LCNTn (n = 00 to 15)	—	LOCO count result register n	Register not available
LCNTDU	—	LOCO count upper permissible deviation register	Register not available
LCNTDL	—	LOCO count lower permissible deviation register	Register not available
GTCWP	—	Register not available	General PWM timer clearing write-protection register
GTCMNWP	—	Register not available	General PWM timer common register write-protection register
GTMDR	—	Register not available	General PWM timer mode register
GTECNFCR	—	Register not available	General PWM timer external clock noise filter control register
GTADSMR	—	Register not available	General PWM timer A/D conversion start request signal monitor register
GTINTAD	GTINTA	GTCCRA compare match/input capture interrupt enable bit	GTCCRA(LW) compare match/input capture interrupt enable bit
	GTINTB	GTCCRB compare match/input capture interrupt enable bit	GTCCRB(LW) compare match/input capture interrupt enable bit
	GTINTC	GTCCRC compare match interrupt enable bit	GTCCRC(LW) compare match/input capture interrupt enable bit

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTINTAD	GTINTD	GTCCRD compare match interrupt enable bit	GTCCRD(LW) compare match/input capture interrupt enable bit
	GTINTE	GTCCRE compare match interrupt enable bit	GTCCRE(LW) compare match/input capture interrupt enable bit
	GTINTF	GTCCRF compare match interrupt enable bit	GTCCRF(LW) compare match/input capture interrupt enable bit
	GTINTPR[1:0]	GTPR compare match interrupt enable bits	GTPR(LW) compare match interrupt enable bits
	ADTRAUEN	GTADTRA compare match (up-counting) A/D converter start request enable bit	GTADTRA(LW) compare match (up-counting) A/D converter start request enable bit
	ADTRADEN	GTADTRA compare match (down-counting) A/D converter start request enable bit	GTADTRA(LW) compare match (down-counting) A/D converter start request enable bit
	ADTRBUEN	GTADTRB compare match (up-counting) A/D converter start request enable bit	GTADTRB(LW) compare match (up-counting) A/D converter start request enable bit
	ADTRBDEN	GTADTRB compare match (down-counting) A/D converter start request enable bit	GTADTRB(LW) compare match (down-counting) A/D converter start request enable bit
GTCR	TPCS[1:0] (RX62T) TPCS[3:0] (RX24T/ RX24U)	Timer prescaler select bits b9 b8 0 0: ICLK (system clock) 0 1: ICLK/2 (system clock/2) 1 0: ICLK/4 (system clock/4) 1 1: ICLK/8 (system clock/8)	Timer prescaler select bits b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD
GTBER	CCRA[1:0]	GTCCRA buffer operation bits b1 b0 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	GTCCRA(LW) buffer operation bits b1 b0 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRA(LW) register ↔ GTCCRC(LW) register) 1 x: Double buffer operation (GTCCRA(LW) register ↔ GTCCRC(LW) register ↔ GTCCRD(LW) register)

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTBER	CCRB[1:0]	GTCCRB buffer operation bits b3 b2 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	GTCCRB(LW) buffer operation bits b3 b2 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTCCRB(LW) register ↔ GTCCRE(LW) register) 1 x: Double buffer operation (GTCCRB(LW) register ↔ GTCCRE(LW) register ↔ GTCCRF(LW) register)
	PR [1:0]	GTPR buffer operation bits b5 b4 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Double buffer operation (GTPDBR → GTPBR → GTPR)	GTPR(LW) buffer operation bits b5 b4 0 0: Buffer operation is not performed. 0 1: Single buffer operation (GTPBR(LW) register → GTPR(LW) register) 1 x: Double buffer operation (GTPDBR(LW) register → GTPBR(LW) register → GTPR(LW) register)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit Writing 1 to this bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit is automatically cleared to 0 after 1 is written to it. This bit is read as 0.	GTCCRA(LW) and GTCCRB(LW) forcible buffer operation bit Writing 1 to this bit forcibly performs buffer transfer of GTCCRA(LW) and GTCCRB(LW). This bit is automatically cleared to 0 after 1 is written to it. This bit is read as 0.
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits • Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at peak 1 0: Transfer at trough 1 1: Transfer at both peak and trough • Saw waves b9 b8 0 0: No transfer Value other than 0 0: Transfer at underflow (during down-counting) or overflow (during up-counting)	GTADTRA(LW) buffer transfer timing select bits • Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at peak 1 0: Transfer at trough 1 1: Transfer at both peak and trough • Saw waves b9 b8 0 0: No transfer Value other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clearing
	ADTDA	GTADTRA double buffer select bit	GTADTRA(LW) double buffer select bit
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits	GTADTRB(LW) buffer transfer timing select bits

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTBER	ADTDB	GTADTRB double buffer operation bit	GTADTRB(LW) double buffer operation bit
GTUDC	OADTY[1:0]	Reserved	GTIOCA pin output duty setting bits
	OADTYF	Reserved	GTIOCA pin output duty forced setting bit
	OADTYR	Reserved	Output after release of GTIOCA pin output 0%/100% duty cycle setting bit
	OBDTY[1:0]	Reserved	GTIOCB pin output duty setting bits
	OBDTYF	Reserved	GTIOCB pin output duty forced setting bit
	OBDTYR	Reserved	Output after release of GTIOCB pin output 0%/100% duty cycle setting bit
GTITC	ITLA	GTCCRA compare match/input capture interrupt link bit	GTCCRA(LW) compare match/input capture interrupt link bit
	ITLB	GTCCRB compare match/input capture interrupt link bit	GTCCRB(LW) compare match/input capture interrupt link bit
	ITLC	GTCCRC compare match interrupt link bit	GTCCRC(LW) compare match interrupt link bit
	ITLD	GTCCRD compare match interrupt link bit	GTCCRD(LW) compare match interrupt link bit
	ITLE	GTCCRE compare match interrupt link bit	GTCCRE(LW) compare match interrupt link bit
	ITLF	GTCCRF compare match interrupt link bit	GTCCRF(LW) compare match interrupt link bit
	ADTAL	GTADTRA A/D converter start request link bit	GTADTRA(LW) A/D converter start request link bit
	ADTBL	GTADTRB A/D converter start request link bit	GTADTRB(LW) A/D converter start request link bit
GTST	TCFA	Input capture/compare match flag A	Reserved (Value after a reset is undefined.)
	TCFB	Input capture/compare match flag B	Reserved (Value after a reset is undefined.)
	TCFC	Compare match flag C	Reserved (Value after a reset is undefined.)
	TCFD	Compare match flag D	Reserved (Value after a reset is undefined.)
	TCFE	Compare match flag E	Reserved (Value after a reset is undefined.)
	TCFF	Compare match flag F	Reserved (Value after a reset is undefined.)
	TCFPO	Overflow flag	Reserved (Value after a reset is undefined.)
	TCFPU	Underflow flag	Reserved (Value after a reset is undefined.)
	ITCNT[2:0]	GTCIV interrupt skipping count counter	GTCIV/GTCIU interrupt skipping count counter

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTCNTLW	—	Register not available	General PWM timer longword counter register
GTCCRmLW (m = A to F)	—	Register not available	General PWM timer longword compare capture register
GTPRLW	—	Register not available	General PWM timer longword period setting register
GTPBRLW	—	Register not available	General PWM timer longword period setting buffer register
GTPDBRLW	—	Register not available	General PWM timer longword period setting double buffer register
GTADTRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing register m
GTADTBRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing buffer register m
GTADTDBRmLW (m = A or B)	—	Register not available	Longword A/D converter start request timing double buffer register m
GTONCR	NFS[3:0]	GTIOC output negate source select bits b7 b4 0 0 0 0: AN000 comparator detection 0 0 0 1: AN001 comparator detection 0 0 1 0: AN002 comparator detection 0 0 1 1: Setting prohibited 0 1 0 0: AN100 comparator detection 0 1 0 1: AN101 comparator detection 0 1 1 0: AN102 comparator detection 0 1 1 1: GTETRG pin input 1 x x x: Software control (control through SWN bit)	GTIOC output negate source select bits b7 b4 0 0 0 0: CMPC0 comparator output 0 0 0 1: CMPC1 comparator output — — 0 1 0 0: CMPC2 comparator output 0 1 0 1: CMPC3 comparator output — 0 1 1 1: GTETRG pin input 1 x x x: Software control (control through SWN bit) Settings other than the above are prohibited when negate control is enabled by the NEA or NEB bit.

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTDTCR	TDE	Negative-phase waveform setting bit 0: The GTCCRB register is set individually without using the GTDVU and GTDVD registers. 1: The GTDVU and GTDVD registers are used to set the compare match value for negative-phase waveforms with dead time automatically in the GTCCRB register.	Negative-phase waveform setting bit 0: The GTCCRB(LW) register is set individually without using the GTDVU(LW) and GTDVD(LW) registers. 1: The GTDVU(LW) and GTDVD(LW) registers are used to set the compare match value for negative-phase waveforms with dead time automatically in the GTCCRB(LW) register.
	TDBUE	GTDVU buffer operation enable bit 0: GTDVU register buffer operation is disabled. 1: GTDVU register buffer operation is enabled.	GTDVU(LW) buffer operation enable bit 0: GTDVU(LW) register buffer operation is disabled. 1: GTDVU(LW) register buffer operation is enabled.
	TDBDE	GTDVD buffer operation enable bit 0: GTDVD register buffer operation is disabled. 1: GTDVD register buffer operation is enabled.	GTDVD(LW) buffer operation enable bit 0: GTDVD(LW) register buffer operation is disabled. 1: GTDVD(LW) register buffer operation is enabled.
	TDFER	GTDVD setting bit 0: The GTDVU and GTDVD registers are set individually. 1: The value written to the GTDVU register is set automatically in the GTDVD register.	GTDVD(LW) setting bit 0: The GTDVU(LW) and GTDVD(LW) registers are set individually. 1: The value written to the GTDVU(LW) register is set automatically in the GTDVD(LW) register.
GTSOS	SOS [1:0]	Output protection function status bits b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 set during transfer at trough or peak) 1 0: Protected state (GTCCRA ≥ GTPR set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR set during transfer at peak)	Output protection function status bits b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA(LW) register = 0 set during transfer at trough or peak) 1 0: Protected state (GTCCRA(LW) register ≥ GTPR(LW) register set during transfer at trough) 1 1: Protected state (GTCCRA(LW) register ≥ GTPR(LW) register set during transfer at peak)
GTDVmLW (m = U or D)	—	Register not available	General PWM timer longword dead time value register m
GTDBmLW (m = U or D)	—	Register not available	General PWM timer longword dead time buffer register m

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
GTDLYCR	—	PWM output delay control register	Register not available
GTDLYRA	—	GTIOCA rising output delay register	Register not available
GTDLYFA	—	GTIOCA falling output delay register	Register not available
GTDLYRB	—	GTIOCB rising output delay register	Register not available
GTDLYFB	—	GTIOCB falling output delay register	Register not available

4.4.15 Independent Watchdog Timer

Table 4.38 lists the points of difference between the independent watchdog timers, and Table 4.39 lists the points of difference between the I/O registers related to the independent watchdog timers.

Table 4.38 Points of Difference between Independent Watchdog Timers

Item	RX62T	RX24T and RX24U
Conditions for starting the counter	— • Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Counting starts automatically after a reset (auto-start mode). • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows is generated.	• Reset (The down-counter and other registers return to their initial values.) • A counter underflows or a refresh error is generated. Counting restarts. (In auto-start mode, counting restarts automatically after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after a refresh.)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow —	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Non-maskable interrupt sources	—	• Down-counter underflow • Refresh occurring outside the refresh-permitted period (refresh error)
Output signals (internal signals)	• Reset output — —	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62T	RX24T and RX24U
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) — — — —	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 4.39 Points of Difference between I/O Registers Related to Independent Watchdog Timers

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
IWDTCR	TOPS[1:0]	Timeout period selection bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Timeout period selection bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	CKS[3:0]	Clock select bits b7 b4 0 0 - -: IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 - - - : IWDTCLK/256 Initial value after a reset differs.	Clock divide ratio select bits b7 b4 0 0 0 0: No division 0 0 1 0: Divide-by-16 0 0 1 1: Divide-by-32 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 0 1: Divide-by-256
	RPES[1:0]	Reserved	Window end position select bits
	RPSS[1:0]	Reserved	Window start position select bits
IWDTSR	REFEF	Reserved	Refresh error flag
IWDTRCR	—	Register not available	IWDT reset control register
IWDTCSTPR	—	Register not available	IWDT count stop control register

4.4.16 Serial Communications Interface

Table 4.40 lists the points of difference between the serial communications interfaces, and Table 4.41 lists the points of difference between the I/O registers related to the serial communications interfaces.

Table 4.40 Points of Difference between Serial Communications Interfaces

Item	RX62T	RX24T	RX24U
Number of channels	3 channels	3 channels	4 channels
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface — —	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	
I/O pins	• SCI/SMCI I/O pins SCK0, RXD0, TXD0, SCK1, RXD1, TXD1, SCK2, RXD2, TXD2	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK1, RXD1, TXD1, CTS1#/RTS1#, SCK5, RXD5, TXD5, CTS5#/RTS5#, SCK6, RXD6, TXD6, CTS6#/RTS5# (channel 11 available on RX24U only) SCK11, RXD11, TXD11, CTS11#/RTS11# • SCI I/O pins (simple I²C mode) SSCL1, SSDA1, SSCL5, SSDA5, SSCL6, SSDA6 (channel 11 available on RX24U only) SSCL11, SSDA11 • SCI I/O pins (simple SPI mode) SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6# (channel 11 available on RX24U only) SCK11, SMISO11, SMOSI11, SS11#	
Data transfer	Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.	
Interrupt sources	Transmit end, transmit data empty, receive data full, or receive error	Transmit end, transmit data empty, receive data full, receive error Completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	

Item		RX62T	RX24T RX24U
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Clock source	An internal or external clock can be selected. —	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
Clock synchronous mode	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	Fast mode is supported.
	Noise canceler	—	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	—	Selectable among four clock phase and clock polarity settings.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 4.41 Points of Difference between I/O Registers Related to Serial Communications Interfaces

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
RDRH	—	Register not available	Receive data register H
RDRL	—	Register not available	Receive data register L
RDRHL	—	Register not available	Receive data register HL
TDRH	—	Register not available	Transmit data register H
TDRL	—	Register not available	Transmit data register L
TDRHL	—	Register not available	Transmit data register HL
SMR (SCMR.SMIF = 0)	CHR	Character length bit (valid only in asynchronous mode) 0: Transmit/receive using 8-bit data length 1: Transmit/receive using 7-bit data length	Character length bit (valid only in asynchronous mode) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive using 9-bit data length 0 1: Transmit/receive using 9-bit data length 1 0: Transmit/receive using 8-bit data length 1 1: Transmit/receive using 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
SCR (SCMR.SMIF = 0)	CKE[1:0]	Clock enable bits (asynchronous mode) b1 b0 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock • When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. — (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.	SCI5 or SCI6: Clock enable bits (asynchronous mode) b1 b0 0 0: On-chip baud rate generator SCKn pin can function as I/O port, based on I/O port settings. 0 1: On-chip baud rate generator Clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock • When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency 8 times the bit rate when the SEMR.ABCS bit is set to 1. • TMR clock can be used. The SCKn pin functions as an I/O port according to the I/O port settings when the TMR clock is in use. (Clock synchronous mode) 0 x: Internal clock: SCKn functions as clock output pin. 1 x: External clock SCKn functions as clock input pin.
SCMR	CHR1	Reserved	Character length 1 bit
MDDR	—	Register not available	Modulation duty register
SEMR	ACS0	Reserved	Asynchronous mode clock source select bit
	BRME	Reserved	Bit rate modulation enable bit
	BGDM	Reserved	Baud rate generator double-speed mode select bit
SNFR	—	Register not available	Noise filter setting register
SIMR1	—	Register not available	I^2C mode register 1
SIMR2	—	Register not available	I^2C mode register 2
SIMR3	—	Register not available	I^2C mode register 3
SISR	—	Register not available	I^2C status register
SPMR	—	Register not available	SPI mode register

4.4.17 I²C Bus Interface

Table 4.42 lists the points of difference between the I/O registers related to the I²C bus interfaces.

Table 4.42 Points of Difference between I/O Registers Related to I²C Bus Interfaces

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
ICMR2	TMWE	Timeout internal counter write enable	Reserved
TMOCNT	—	Timeout internal counter	Register not available

4.4.18 CAN Module

Table 4.43 lists the points of difference between the CAN modules, and Table 4.44 lists the points of difference between the I/O registers related to the CAN modules.

Table 4.43 Points of Difference between CAN Modules

Item	RX62T	RX24T and RX24U
Bit rate	Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Up to 1 Mbps
Message boxes	32 mailboxes: 2 selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, 4 FIFO stages can be configured for transmission and 4 FIFO stages for reception.	16 message boxes • Each channel dedicated: 4 buffers (4 buffers per channel) Transmit buffer: 4 buffer per channel • Shared among channels: 16 buffers Receive buffers: 0 to 16 buffers Receive FIFO buffers: 2 (up to 16 buffers allocatable to each) Transmit/receive FIFO buffers: 1 per channel (up to 16 buffers allocatable to each)

Item	RX62T	RX24T and RX24U
Reception	• Ability to receive data frames and remote frames • Ability to select ID format used for reception (standard ID only, extended ID only, or both standard and extended IDs) • Selectable one-shot reception function • Ability to select overwrite mode (message overwritten) or overrun mode (message discarded) • Ability to enable or disable receive end interrupt for each mailbox — — —	• Ability to receive data frames and remote frames • Ability to select ID format used for reception (standard ID only, extended ID only, or both) — — — • Ability to enable or disable interrupts for each FIFO • Mirror function (to receive messages transmitted from own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Acceptance filtering	• 8 acceptance masks (individual mask for every 4 mailboxes) • Ability to individually enable or disable masks for each mailbox	• Refer to reception filtering function.
Reception filtering function	—	• Ability to select receive messages using a total of 16 receive rules • Ability to set the number of receive rules (0 to 16) for each channel • Acceptance filtering: Ability to set ID and mask for each receive rule • DLC filter processing: Ability to specify DLC filter checking for each receive rule
Receive message transfer function	—	• Routing function Ability to transfer receive messages to user-defined buffers (max. transfer buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, or transmit/receive FIFO buffer • Label addition function Ability to simultaneously store label information when storing a message in a receive buffer and FIFO buffer

Item	RX62T	RX24T and RX24U
Transmission	• Ability to transmit data frames and remote frames • Ability to select ID format used for transmission (standard ID only, extended ID only, or both standard and extended IDs) • Selectable one-shot transmission function • Ability to select ID priority transmission mode or mailbox number priority mode • Ability to abort transmission requests (and ability to confirm abort completion with a flag) • Ability to enable or disable transmit complete interrupt individually by mailbox	• Ability to transmit data frames and remote frames • Ability to select ID format used for transmission (standard ID only, extended ID only, or both) • One-shot transmission function • Ability to select ID priority transmission or transmit buffer number priority transmission • Transmit abort function (with ability to confirm abort completion with a flag) • Ability to enable or disable transmit complete interrupt individually by transmit buffer or transmit/receive FIFO buffer
Interval transmission function	—	Ability to set the message transmission interval time (transmit mode of transmit/receive FIFO buffers)
Transmit history function	—	Function for storing history information for transmitted messages
Error status monitoring	• Monitoring of CAN bus errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, and ACK delimiter errors) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Error counter reading —	• Monitoring of CAN protocol errors (stuff errors, form errors, ACK errors, CRC errors, bit errors, ACK delimiter errors, and bus dominant locking) • Detection of error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Error counter reading • Monitors DLC errors
Time stamp function	• Time stamp function using 16-bit counter • Ability to select reference clock among 1-, 2-, 4-, and 8-bit time periods	• Time stamp function using 16-bit counter • Time stamp clock source division function

Item	RX62T	RX24T and RX24U
Interrupt function	5 interrupt sources (receive end interrupt, transmit complete interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	5 sources • Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channels (3 sources per channel) — Channel transmit interrupts Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Transmit/receive FIFO receive interrupt — Channel error interrupt
CAN sleep mode	Ability to reduce current consumption by stopping the CAN clock	—
Software support units	3 software support units • Acceptance filtering support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
CAN clock source	Peripheral module clock (PCLK)	CAN clock (CANMCLK)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) —	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)

Table 4.44 Points of Difference between I/O Registers Related to CAN Modules

Register Symbol	Bit Symbol	RX62T	RX24/24U
CTLR	—	Control register	Register not available
BCR	—	Bit configuration register	Register not available
MKRi	—	Mask register i (i = 0 to 7)	Register not available
FIDCR0	—	FIFO received ID compare register 0	Register not available
FIDCR1	—	FIFO received ID compare register 1	Register not available
MKIVLR	—	Mask invalid register	Register not available
MBj	—	Mailbox register j (j = 0 to 31)	Register not available
MIER	—	Mailbox interrupt enable register	Register not available
MCTLj	—	Message control register j (j = 0 to 31)	Register not available
RFCR	—	Receive FIFO control register	Register not available
RFPCR	—	Receive FIFO pointer control register	Register not available
TFCR	—	Transmit FIFO control register	Register not available
TFPCR	—	Transmit FIFO pointer control register	Register not available
STR	—	Status register	Register not available
MSMR	—	Mailbox search mode register	Register not available
MSSR	—	Mailbox search status register	Register not available
CSSR	—	Channel search support register	Register not available
AFSR	—	Acceptance filter support register	Register not available
EIER	—	Error interrupt enable register	Register not available
EIFR	—	Error interrupt source judge register	Register not available
RECR	—	Receive error count register	Register not available
TECR	—	Transmit error count register	Register not available
ECSR	—	Error code store register	Register not available
TSR	—	Time stamp register	Register not available
TCR	—	Test control register	Register not available
CFGL	—	Register not available	Bit configuration register L
CFGH	—	Register not available	Bit configuration register H
CTRL	—	Register not available	Control register L
CTRH	—	Register not available	Control register H
STSL	—	Register not available	Status register L
STSH	—	Register not available	Status register H
ERFLL	—	Register not available	Error flag register L
ERFLH	—	Register not available	Error flag register H
GCFGL	—	Register not available	Global configuration register L
GCFGH	—	Register not available	Global configuration register H
GCTRL	—	Register not available	Global control register L
GCTRH	—	Register not available	Global control register H
GSTS	—	Register not available	Global status register
GERFLL	—	Register not available	Global error flag register

Register Symbol	Bit Symbol	RX62T	RX24/24U
GTINTSTS	—	Register not available	Global transmit interrupt status register
GTSC	—	Register not available	Timestamp register
GAFLCFG	—	Register not available	Receive rule number configuration register
GAFLIDLj	—	Register not available	Receive rule entry register jAL (j = 0 to 15)
GAFLIDHj	—	Register not available	Receive rule entry register jAH (j = 0 to 15)
GAFLMLj	—	Register not available	Receive rule entry register jBL (j = 0 to 15)
GAFLMHj	—	Register not available	Receive rule entry register jBH (j = 0 to 15)
GAFLPLj	—	Register not available	Receive rule entry register jCL (j = 0 to 15)
GAFLPHj	—	Register not available	Receive rule entry register jCH (j = 0 to 15)
RMNB	—	Register not available	Receive buffer number configuration register
RMND0	—	Register not available	Receive buffer receive complete flag register
RMIDLn	—	Register not available	Receive buffer register nAL (n = 0 to 15)
RMIDHn	—	Register not available	Receive buffer register nAH (n = 0 to 15)
RMTSn	—	Register not available	Receive buffer register nBL (n = 0 to 15)
RMPTRn	—	Register not available	Receive buffer register nBH (n = 0 to 15)
RMDF0n	—	Register not available	Receive buffer register nCL (n = 0 to 15)
RMDF1n	—	Register not available	Receive buffer register nCH (n = 0 to 15)
RMDF2n	—	Register not available	Receive buffer register nDL (n = 0 to 15)
RMDF3n	—	Register not available	Receive buffer register nDH (n = 0 to 15)
RFCCm	—	Register not available	Receive FIFO control register m (m = 0 or 1)
RFSTSm	—	Register not available	Receive FIFO status register m (m = 0 or 1)
RFPCTRm	—	Register not available	Receive FIFO pointer control register m (m = 0 or 1)
RFIDLm	—	Register not available	Receive FIFO access register mAL (m = 0 or 1)
RFIDHm	—	Register not available	Receive FIFO access register mAH (m = 0 or 1)
RFTSm	—	Register not available	Receive FIFO access register mBL (m = 0 or 1)
RFPTRm	—	Register not available	Receive FIFO access register mBH (m = 0 or 1)

Register Symbol	Bit Symbol	RX62T	RX24/24U
RFDF0m	—	Register not available	Receive FIFO access register mCL (m = 0 or 1)
RFDF1m	—	Register not available	Receive FIFO access register mCH (m = 0 or 1)
RFDF2m	—	Register not available	Receive FIFO access register mDL (m = 0 or 1)
RFDF3m	—	Register not available	Receive FIFO access register mDH (m = 0 or 1)
CFCCL0	—	Register not available	Transmit/receive FIFO control register 0L
CFCCH0	—	Register not available	Transmit/receive FIFO control register 0H
CFSTS0	—	Register not available	Transmit/receive FIFO status register 0
CFPCTR0	—	Register not available	Transmit/receive FIFO pointer control register 0
CFIDL0	—	Register not available	Transmit/receive FIFO access register 0AL
CFIDH0	—	Register not available	Transmit/receive FIFO access register 0AH
CFTS0	—	Register not available	Transmit/receive FIFO access register 0BL
CFPTR0	—	Register not available	Transmit/receive FIFO access register 0BH
CFDF00	—	Register not available	Transmit/receive FIFO access register 0CL
CFDF10	—	Register not available	Transmit/receive FIFO access register 0CH
CFDF20	—	Register not available	Transmit/receive FIFO access register 0DL
CFDF30	—	Register not available	Transmit/receive FIFO access register 0DH
RFMSTS	—	Register not available	Receive FIFO message lost status register
CFMSTS	—	Register not available	Transmit/receive FIFO message lost status register
RFISTS	—	Register not available	Receive FIFO interrupt status register
CFISTS	—	Register not available	Transmit/receive FIFO receive interrupt status register
TMCp	—	Register not available	Transmit buffer control register p (p = 0 to 3)
TMSTSp	—	Register not available	Transmit buffer status register p (p = 0 to 3)
TMTRSTS	—	Register not available	Transmit buffer transmit request status register
TMTCSTS	—	Register not available	Transmit buffer transmit complete status register
TMTASTS	—	Register not available	Transmit buffer transmit abort status register
TMIEC	—	Register not available	Transmit buffer interrupt enable register

Register Symbol	Bit Symbol	RX62T	RX24/24U
TMIDLp	—	Register not available	Transmit buffer register pAL (p = 0 to 3)
TMIDHp	—	Register not available	Transmit buffer register pAH (p = 0 to 3)
TMPTRp	—	Register not available	Transmit buffer register pBH (p = 0 to 3)
TMDF0p	—	Register not available	Transmit buffer register pCL (p = 0 to 3)
TMDF1p	—	Register not available	Transmit buffer register pCH (p = 0 to 3)
TMDF2p	—	Register not available	Transmit buffer register pDL (p = 0 to 3)
TMDF3p	—	Register not available	Transmit buffer register pDH (p = 0 to 3)
THLCC0	—	Register not available	Transmit history buffer control register
THLSTS0	—	Register not available	Transmit history buffer status register
THLACC0	—	Register not available	Transmit history buffer access register
THLPCTR0	—	Register not available	Transmit history buffer pointer control register
GRWCR	—	Register not available	Global RAM window control register
GTSTCFG	—	Register not available	Global test configuration register
GTSTCTRL	—	Register not available	Global test control register
GLOCKK	—	Register not available	Global test protection unlock register
RPGACCr	—	Register not available	RAM test register r (r = 0 to 127)

4.4.19 Serial Peripheral Interface

Table 4.45 lists the points of difference between the serial peripheral interfaces, and Table 4.46 lists the points of difference between the I/O registers related to the serial peripheral interfaces.

Table 4.45 Points of Difference between Serial Peripheral Interfaces

Item	RX62T	RX24T and RX24U
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 4 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection —	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. —	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources: Receive buffer full interrupt Transmit buffer empty interrupt RSPI error interrupt (mode fault, overrun, parity error) RSPI idle interrupt (RSPI idle)	Interrupt sources: Receive buffer full interrupt Transmit buffer empty interrupt RSPI error interrupt (mode fault, overrun, underrun, parity error) RSPI idle interrupt (RSPI idle)
Other functions	— • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function

Table 4.46 Points of Difference between I/O Registers Related to Serial Peripheral Interfaces

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
SPSR	UDRF	Reserved	Underrun error flag
SPDCR	SLSEL[1:0]	SSL pin output select bits	Reserved
SPCR2	SCKASE	Reserved	RSPCK auto-stop function enable bit

4.4.20 12-Bit A/D Converter

Table 4.47 lists the points of difference between the 12-bit A/D converters, and Table 4.48 lists the points of difference between the I/O registers related to the 12-bit A/D converters.

Table 4.47 Points of Difference between 12-Bit A/D Converters

Item	RX62T	RX24T and RX24U
Number of units	2 units	3 units
Input channels	8 channels (4 channels × 2 units)	22 channels (20 channels on 100-pin version of RX24U)
Extended analog function	—	Internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• 1.0 µs per channel (when operating with A/D conversion clock ADCLK = 50 MHz and AVCC0 = 4.0 V to 5.5 V) • 2.0 µs per channel (when operating with A/D conversion clock ADCLK = 25 MHz and AVCC0 = 3.0 V to 3.6 V)	• 1.0 µs per channel (when operating with A/D conversion clock ADCLK = 40 MHz)
A/D conversion clock	Settable to PCLK divided by 1, 2, 4, or 8 (ADCSR.CKS[1:0]).	Settable to system clock divided by 1, 2, 4, 8, 16, 32, or 64 (SCKCR.PCKD[3:0]). Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLK:ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.

Item	RX62T	RX24T and RX24U
Data register	• 10 registers for analog input	• 22 registers for analog input, 1 for A/D-converted data duplication in double trigger mode, and 2 for A/D-converted data duplication during extended operation in double trigger mode
	—	• 1 register for internal reference voltage
	• 1 register per unit for self-diagnostics	• 1 register per unit for self-diagnostics
	• The results of A/D conversion are stored in 12-bit A/D data registers.	• The results of A/D conversion are stored in 12-bit A/D data registers.
	• Output with 12-bit accuracy supported for A/D conversion results.	• Output with 12-bit accuracy supported for A/D conversion results.
	—	• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode.
	—	• Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
	—	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single mode: Analog inputs of one channel are converted only once.	—
	• Single-cycle scan mode: Analog inputs of up to four channels are converted only once.	• Single scan mode: A/D conversion is performed only once on the analog inputs of user-selected channels. A/D conversion is performed only once on the internal reference voltage (S12AD2).
	• Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 4 channels.	• Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of user-selected channels.

Item	RX62T	RX24T and RX24U
Operating mode	• 2-channel scan mode: Channels in each unit are divided into two groups and the conversion startup source can be selected separately for each group.	• Group scan mode: Either two (A and B) or three (A, B, and C) groups may be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) The user-selected channels are divided among group A and group B or among group A, group B, and group C, and and A/D conversion of the analog inputs selected on a group basis is performed only once. The scanning start conditions (synchronous triggers) can be selected independently for group A, group B, and group C, allowing conversion to start at a different time for each group.
	—	• Group scan mode (with group priority control selected): If a trigger for a higher-priority group occurs when A/D conversion on a lower-priority group is in progress, scanning of the lower-priority group is stopped and scanning of the higher-priority group starts. Regarding the priority sequence, a setting is available to specify whether or not scanning of the lower-priority group restarts (rescan) after scanning finishes of group A (high priority), group B (middle priority), and group C (low priority). For rescanning, a setting is available to specify whether to start from the first of the selected channels or from the next unscanned channel after the last channel on which A/D conversion completed.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit 3 (MTU3) or the general PWM timer (GPT). • Asynchronous trigger A/D conversion can be externally triggered from the ADTRG0# pin for S12AD0 and from the ADTRG1# pin for S12AD1.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit 3 (MTU3d), the general PWM timer (GPT), or the 8-bit timer (TMR). • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (separately for each of three units).

Item	RX62T	RX24T and RX24U
Functions	• Channel-dedicated sample-and-hold function (3 channels per unit)	• Channel-dedicated sample-and-hold function (3 channels on S12AD1 only)
	—	• Variable sampling state count
	• Self-diagnostic function for 12-bit A/D converter	• Self-diagnostic function for 12-bit A/D converter
	• Input signal amplification function using programmable gain amplifier (3 channels per unit)	• Input signal amplification function using programmable gain amplifier (1 channel/S12AD, 3 channels/S12AD1)
	• Window comparator function (3 channels per unit)	—
	—	• Selectable A/D-converted value adding mode or averaging mode
	—	• Analog input disconnection assist detection function (discharge function/precharge function)
	—	• Double trigger mode (duplication of A/D conversion data)
	—	• Automatic clear function for A/D data registers

Item	RX62T	RX24T and RX24U
Interrupt source	• An interrupt request (S12ADI) can be generated on completion of A/D conversion in each unit.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a single scan (separately for each of three units). • In double trigger mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan (separately for each of three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI, GBADI1, or GBADI2) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (GCADI, GCADI1, or GCADI2) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, GBADI2/GCADI2) can be generated.
	• A S12ADI interrupt can activate the data transfer controller (DTC).	• The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).
	• An interrupt request (CMPI) can be generated when comparator detection occurs (can also be used for a POE source).	—

Table 4.48 Points of Difference between I/O Registers Related to 12-Bit A/D Converters

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
ADDBLDR	—	Register not available	A/D data duplication register
ADDBLDRA	—	Register not available	A/D data duplication register A
ADDBLDRB	—	Register not available	A/D data duplication register B
ADOCDR	—	Register not available	A/D internal reference voltage data register
ADCSR	DBLANS[4:0]	Not available	Double trigger channel select bits
	GBADIE	Not available	Group B scan end interrupt enable bit
	DBLE	Not available	Double trigger mode select bit
	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	Clock select bits (b3 b2)	Not available
	ADIE	A/D conversion end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS[1:0]	A/D conversion mode select bits b6 b5 0 0: Single mode 0 1: Single-cycle scan mode 1 0: Continuous scan mode 1 1: 2-channel scan mode	Scan mode select bits b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited
	ADST	A/D start bit (b7)	A/D conversion start bit (b15)
ADANS	—	A/D channel select register	Register not available
ADANSA0	—	Register not available	A/D channel select register A0
ADANSA1	—	Register not available	A/D channel select register A1
ADANSB0	—	Register not available	A/D channel select register B0
ADANSB1	—	Register not available	A/D channel select register B1
ADANSC0	—	Register not available	A/D channel select register C0
ADANSC1	—	Register not available	A/D channel select register C1
ADADS0	—	Register not available	A/D-converted value addition/average function channel select register 0
ADADS1	—	Register not available	A/D-converted value addition/average function channel select register 1
ADADC	—	Register not available	A/D-converted value addition/average count select register
ADCER	SHBYP	Dedicated sample-and-hold circuit select bit	Reserved
	ADPRC[1:0]	A/D data register bit precision set bits	Reserved
	ACE	Automatic clearing enable bit	A/D data register automatic clearing enable bit
	ADIE2	2-channel scan interrupt select bit	Reserved
	ADIEW	Double trigger interrupt select bit	Reserved

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
ADSTRGR	ADSTRS0[4:0]	A/D start trigger group 0 select bits (b0-b4)	Not available
	TRSB[5:0]	Not available	A/D conversion start trigger for group B select bits (b0-b5)
	ADSTRS1[4:0]	A/D start trigger group 1 select bits (b8-b12)	Not available
	TRSA[5:0]	Not available	A/D conversion start trigger select bits (b8-b13)
ADPG	—	A/D programmable gain amplifier register	Register not available
ADCMPMD0	—	Comparator operating-mode selection register 0	Register not available
ADCMPMD1	—	Comparator operating-mode selection register 1	Register not available
ADCMPNR0	—	Comparator filter-mode register 0	Register not available
ADCMPNR1	—	Comparator filter-mode register 1	Register not available
ADCMPFR	—	Comparator detection flag register	Register not available
ADCMPSEL	—	Comparator interrupt selection register	Register not available
ADEXICR	—	Register not available	A/D conversion extended input control register
ADGCTRGR	—	Register not available	A/D group C trigger select register
ADSHCR	—	Register not available	A/D sample-and-hold circuit control register
ADDISCR	—	Register not available	A/D disconnection detection control register
ADGSPCR	—	Register not available	A/D group scan priority control register
ADPGACR	—	Register not available	A/D programmable gain amplifier control register
ADPGAGS0	—	Register not available	A/D programmable gain amplifier gain setting register 0

4.4.21 RAM

Table 4.49 lists the points of difference between the RAM modules.

Table 4.49 Points of Difference between RAM Modules

Item	RX62T	RX24T and RX24U
RAM capacity	16 KB or 8 KB	32 KB or 16 KB*[1]
RAM address	—	0000 0000h to 0000 7FFFh (32 KB)
	0000 0000h to 0000 3FFFh (16 KB)	0000 0000h to 0000 3FFFh (16 KB)
	0000 0000h to 0000 1FFFh (8 KB)	—

Note 1. RX24T Group only

4.4.22 Flash Memory

Table 4.50 lists the points of difference between the flash memory modules, and Table 4.51 lists the points of difference between the I/O registers related to the flash memory modules.

Table 4.50 Points of Difference between Flash Memory Modules

	RX62T		RX24T and RX24U	
Item	Flash Memory for Code Storage	Flash Memory for Data Storage	ROM	E2 DataFlash
Memory space	User area: 256 KB 128 KB 64 KB	Data area: 32 KB 8 KB	User area: 512 KB 384 KB 256 KB (RX24T only) 128 KB	Data area: 8 KB
ROM cache	—	—	Capacity: 2 KB	
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	A read operation in word or byte units takes 3 cycles of PCLK.	No ROM wait cycles when ICLK ≤ 32 MHz, ROM wait cycle when ICLK > 32 MHz	—
Value after erase	Can be read as FFFF FFFFh in 32-bit access.	—	FFh	FFh
Interrupt	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, lock bit read 2, peripheral clock notify).	A flash ready interrupt request (FRDYI) is generated upon completion of FCU command execution (program, P/E suspend, blank check, peripheral clock notify).	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	
Programming /erasing method	• On-chip dedicated sequencer (FCU) for programming of the ROM • Programming and erasing the ROM are handled by issuing commands to the FCU. • The ROM in the erased state can be read as FFFF FFFFh in 32-bit access.		Software commands • The following software commands are implemented: Program, blank check, block erase, all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window information program	
Background operation (BGO) function	• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • Execution of program code from the ROM is possible while the data flash memory is being programmed or erased.		• The CPU is able to execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • It is possible to run a program located in the ROM while the E2 DataFlash is being programmed.	
Suspension and resumption functions	• The CPU is able to execute program code from the ROM when programming or erasure of the ROM is suspended. • Programming and erasure of the ROM can be restarted (resumed) after suspension.		—	

Item	RX62T		RX24T and RX24U	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**ROM**	**E2 DataFlash**
Units of programming and erasure	• Unit of programming for the user area: 256 bytes • Units of erasure for the user area: 4 KB (8 blocks), 16 KB (when the ROM size is 256 KB: 14 blocks, when the ROM size is 128 KB: 6 blocks, and when the ROM size is 64 KB: 2 blocks)	• Unit of programming for the data area: 8 or 128 bytes • Unit of erasure for the data area: 2 KB (32 KB data flash: 16 blocks; 8 KB data flash: 4 blocks)	• Unit of programming for the user area: 8 bytes • Unit of erasure for the user area: 2 KB	• Unit of programming for the data area: 1 byte • Unit of erasure for the data area: 1 KB
On-board programming	Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. — Programming by a routine for ROM/data flash programming within the user program • Ability to overwrite ROM/data flash without resetting the system		Programming in boot mode • The asynchronous serial interface (SCI1) is used. • The transfer rate is adjusted automatically. Boot mode (FINE interface) • FINE is used • Ability to overwrite user area and data area Self-programming • Ability to overwrite the user area and data area can be overwritten by means of a flash programming routine in a user program, without resetting the system	
Off-board programming	A PROM programmer can be used to program the user area.	—	The user area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the RX24T Group.	
Software-controlled protection function	The FENTRYR.FENTRY0 bit, FWEPROR.FLWE[1:0] bits, and lock bits can be used to prevent unintentional programming.	The FENTRYR.FENTRYD bit, FWEPROR.FLWE[1:0] bits, and DFLREk and DFLWEk registers, can be used to prevent unintentional programming (k = 0 or 1).	The FENTRYR.FENTRY0 bit can be used to prevent unintentional programming.	The FENTRYR.FENTRYD bit can be used to prevent unintentional programming.
Error protection function	Prevents further programming or erasure after the detection of abnormal operation during programming or erasure.		—	

Item	RX62T		RX24T and RX24U	
	Flash Memory for Code Storage	Flash Memory for Data Storage	ROM	E2 DataFlash
ID code protection	• This function can be used to prevent reading, writing, or erasing by the host. • ID codes can be used for control when connected to an on-chip debugging emulator. —		• Connection with the serial programmer in boot mode can be enabled or disabled using ID codes in boot mode. • ID codes can be used for control when connected to an on-chip debugging emulator. • Control by ROM code is possible when connecting a parallel programmer.	
Start-up program protection function	—	—	This function is used to safely rewrite blocks 0 to 7.	
Area protection	—	—	This function enables rewriting only the selected blocks in the user area and disables writing to the other blocks during self-programming.	

Table 4.51 Points of Difference between I/O Registers Related to Flash Memory Modules

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
FMODR	—	Flash mode register	Register not available
FASTAT	—	Flash access status register	Register not available
FAEINT	—	Flash access error interrupt enable register	Register not available
FCURAME	—	FCU RAM enable register	Register not available
FSTATR0	PRGSPD	Programming suspend status bit (b0)	Not available
	ERERR	Not available	Erase error flag (b0)
	ERSSPD	Erasure suspend status bit (b1)	Not available
	PRGERR	Programming error bit (b4)	Program error flag (b1)
	SUSRDY	Suspend ready bit (b3)	Not available
	BCERR	Not available	Blank check error flag (b3)
	ERSERR	Erasure error bit (b5)	Not available
	EILGLERR	Not available	Extra area illegal command error flag (b5)
	ILGLERR	Illegal command error bit (b6)	Reserved
	FRDY	Flash ready bit (b7)	Reserved
FSTATR1	FLOCKST	Lock bit status bit	Reserved
	FRDY	Reserved	Flash ready flag
	FCUERR	FCU error bit (b7)	Not available
	EXRDY	Not available	Extra area ready flag (b7)
FRDYIE	—	Flash ready interrupt enable register	Register not available
FENTRYR	FENTRYD	Data flash P/E mode entry bit	E2 DataFlash P/E mode entry bit
FPROTR	—	Flash protection register	Register not available
FRESETR	FRKEY[7:0]	Key code	Reserved
FCMDR	—	FCU command register	Register not available
FCPSR	—	FCU processing switching register	Register not available
FPESTAT	—	Flash P/E status register	Register not available

Register Symbol	Bit Symbol	RX62T	RX24T and RX24U
PCKAR	—	Peripheral clock notification register	Register not available
FWEPROR	—	Flash write erase protection register	Register not available
DFLRE0	—	Data flash read enable register 0	Register not available
DFLRE1	—	Data flash read enable register 1	Register not available
DFLWE0	—	Data flash programming/erasure enable register 0	Register not available
DFLWE1	—	Data flash programming/erasure enable register 1	Register not available
DFLBCCNT	—	Data flash blank check control register	Register not available
DFLBCSTAT	—	Data flash blank check status register	Register not available
DFLCTL	—	Register not available	E2 DataFlash control register
FPR	—	Register not available	Protection unlock register
FPSR	—	Register not available	Protection unlock status register
FPMCR	—	Register not available	Flash P/E mode control register
FISR	—	Register not available	Flash initial setting register
FASR	—	Register not available	Flash area select register
FCR	—	Register not available	Flash control register
FEXCR	—	Register not available	Flash extra area control register
FSARH	—	Register not available	Flash processing start address register H
FSARL	—	Register not available	Flash processing start address register L
FEARH	—	Register not available	Flash processing end address register H
FEARL	—	Register not available	Flash processing end address register L
FWBn (n = 0 to 3)	—	Register not available	Flash write buffer n register
FEAMH	—	Register not available	Flash error address monitor register H
FEAML	—	Register not available	Flash error address monitor register L
FSCMR	—	Register not available	Flash start-up setting monitor register
FAWSMR	—	Register not available	Flash access window start address monitor register
FAWEMR	—	Register not available	Flash access window end address monitor register
UIDRn (n = 0 to 3)	—	Register not available	Unique ID register n
ROMCE	—	Register not available	ROM cache enable register
ROMCIV	—	Register not available	ROM cache disable register

5. Reference Documents

User's Manual: Hardware

RX62T Group, RX62G Group User's Manual: Hardware Rev.2.00 (R01UH0034EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24U Group User's Manual: Hardware Rev.1.00 (R01UH0658EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

Compatibility with Technical Updates

This application note reflects the content of the following technical update.

TN-RX*-A173A/J

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Nov. 07, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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