RX24T Group

Motor Control Function Migration Guide (RX62T or RX63T to RX24T)

R01AN3668EJ0100
Rev.1.00
Mar 03, 2017

Introduction

When migrating motor control functions from the RX62T or RX63T to the RX24T, there are a number of points regarding hardware and software that should be borne in mind.

The points related to hardware are described in 1, Points Regarding Pin Settings, and the points related to software are described in 2, Points Regarding Function Settings.

For points of difference regarding registers, refer to the separate application note “Points of Difference Between RX24T Group and RX62T Group” (R01AN2836EJxxxx). (The revision number is represented by “xxxx”. Make sure to refer to the latest revision of the application note.)

This application note applies to the 100-pin versions of the above products.

Target Device

RX24T

Contents

1. Points Regarding Pin Settings

1.1 Clock

1.1.1 Oscillator Pin

The main clock frequency of the RX24T may be in the range 1 MHz to 20 MHz.

When migrating from the RX62T or RX63T, the previous setting may be used unchanged.

The main clock frequency ranges of the three microcontrollers are shown below.

	RX62T	RX63T	RX24T
Main clock frequency	8 MHz to 12.5 MHz	8 MHz to 12.5 MHz	1 MHz to 20 MHz

1.2 VCL Pin (External Capacitor)

On the RX62T and RX63T the VCL pin should be connected to a 0.1 μF smoothing capacitor for internal power supply stabilization, and on the RX24T it should be connected to a 4.7 μF smoothing capacitor for this purpose.

The capacitor should be located near the VCL pin.

1.3 PLLVCC Pin

On the RX62T a 22 μF bypass capacitor should be inserted between the PLLVCC (pin number 29) and PLLVSS (pin number 31) pins. The RX24T does not have a PLLVCC pin.

On the RX24T a 0.1 μF bypass capacitor should be inserted between the VCC (pin number 29) and VSS (pin number 31) pins.

In both cases, the bypass capacitor should be located as close as possible to the power supply pins, and the connecting pattern lines should be as short and as thick as possible.

1.4 12-Bit A/D Converter

Important points when migrating software that uses up to eight A/D input pin channels on the RX62T or RX63T to the RX24T are described below.

1.4.1 A/D Input Pins

The 12-bit A/D converter module of the RX24T comprises three units. Unit 0 has five analog input channels assigned to pins AN000 to AN003 and AN016, unit 1 has five analog input channels assigned to pins AN100 to AN103 and AN116, and unit 2 has 12 analog input channels assigned to pins AN200 to AN211.

The 12-bit A/D converter module comprises three units, and unit 0 (S12AD), unit 1 (S12AD1), and unit 2 (S12AD2) can operate independently. The input channels of S12AD, S12AD1, and S12AD2 can also be divided into three groups during operation.

When migrating, pins AN000 to AN003 and AN100 to AN103 on the RX24T can be used in the same manner as pins AN000 to AN003 and AN100 to AN103 on the RX62T or RX63T. There are some functional points of difference, however, and caution is therefore necessary.

A list of the 12-bit A/D converter input pin assignments of the three microcontrollers is shown below.

	Pin Assignment		
Pin Function	**RX62T**	**RX63T**	**RX24T**
AN000	P40	P40	P40
AN001	P41	P41	P41
AN002	P42	P42	P42
AN003	P43	P43	P43
AN016	—	—	P20
AN100	P44	P44	P44
AN101	P45	P45	P45
AN102	P46	P46	P46
AN103	P47	P47	P47
AN116	—	—	P21
AN200	—	—	P60
AN201	—	—	P61
AN202	—	—	P62
AN203	—	—	P63
AN204	—	—	P64
AN205	—	—	P65
AN206	—	—	P50
AN207	—	—	P51
AN208	—	—	P52
AN209	—	—	P53
AN210	—	—	P54
AN211	—	—	P55

1.4.2 ADST Bit Status Output Pins

The ADST bit status output pin functionality has been extended on the RX24T.

The ADST bit (A/D conversion start bit) indicates whether A/D conversion is stopped (0) or started (1). The following pins can be used to check the AD conversion state.

P02/ADST0 Pin, PD6/ADST0 Pin, P00/ADST1 Pin, and P01/ADST2 Pin

For details of ADST bit change conditions, refer to section 29, 12-Bit A/D Converter (S12ADF), in RX24T Group User's Manual: Hardware.

1.4.3 A/D Converter Input Clock

On the RX63T and RX24T the peripheral module clock (S12AD clock) (PCLKD) is used as the A/D conversion clock (ADCLK).

The RX62T does not have a peripheral module clock D (PCLKD), so when migrating to the RX24T it is necessary to add settings for peripheral module clock D (PCLKD).

1.4.4 Pins Supporting Channel-Dedicated Sample-and-Hold Function

On the RX24T pins AN100 to AN102 support the channel-dedicated sample-and-hold function.

On the RX62T and RX63T it is possible to use the channel-dedicated sample-and-hold function on both channels 0 to 2 (AN000 to AN002) of S12AD0 and channels 0 to 2 (AN100 to AN102) of S12AD1, but on the RX24T it is not possible in such cases to use the channel-dedicated sample-and-hold function on channels 0 to 2 (AN000 to AN002) of S12AD0.

1.4.5 Pins Supporting Designation for Group Priority Control

The RX24T supports group priority control.

During basic operation in group scan mode, all other trigger inputs are ignored during scan operation on group A, group B, or group C. During group priority operation, in contrast, if a trigger input for a higher-priority group is received during scan operation on a lower-priority group, scanning of the lower-priority group halts so that scanning of the higher-priority group can proceed.

The priority order of the groups is group A > group B > group C.

The RX63T supports group priority control, but this function is not supported on the RX62T.

1.5 Timers

Important points when migrating software that performs two-motor PWM output control using the complementary PWM mode of the multi-function timer pulse unit (MTU) of the RX62T or RX63T to the RX24T are described below.

1.5.1 PWM Output Pins

When migrating software, the same PWM output pins used for complementary PWM mode on the RX62T or RX63T can be used on the RX24T.

The PWM output pins used in complementary PWM mode are listed below.

Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1’ (PWM output 1 negative-phase waveform output)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2’ (PWM output 2 negative-phase waveform output)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3’ (PWM output 3 negative-phase waveform output)
MTU6	MTIOC6B	PWM output pin 4
	MTIOC6D	PWM output pin 4’ (PWM output 4 negative-phase waveform output)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5’ (PWM output 5 negative-phase waveform output)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6’ (PWM output 6 negative-phase waveform output)

The port assignments on the three microcontrollers of the PWM output pins in complementary PWM mode are listed below.

		Port Assignment		
Channel	Output Pin	RX62T	RX63T	RX24T
MTU3	MTIOC3B	P71	P71	P71
	MTIOC3D	P74	P74	P74
MTU4	MTIOC4A	P72	P72	P72
	MTIOC4C	P75	P75	P75
	MTIOC4B	P73	P73	P73
	MTIOC4D	P76	P76	P76
MTU6	MTIOC6B	P95	P95	P95
	MTIOC6D	P92	P92	P92
MTU7	MTIOC7A	P94	P94	P94
	MTIOC7C	P91	P91	P91
	MTIOC7B	P93	P93	P93
	MTIOC7D	P90	P90	P90

1.5.2 A/D Conversion Start Request Frame Synchronization Signal Output Pins

On the RX24T the functionality of the A/D conversion start request frame synchronization signal output pins has been extended.

The A/D conversion start request frame synchronization signal allows monitoring, using an external pin, of the timing of the generation of A/D conversion start request signals. The pins that can be used to check the timing of the generation of A/D conversion start request signals are as follows:

PB2/ADSM0 Pin and PB1/ADSM1 Pin

After the A/D conversion start request signal to be monitored is selected in A/D conversion start request select register 0 (TADSTRGR0) or A/D conversion start request select register 1 (TADSTRGR1) of the multi-function timer pulse unit (MTU), a high-level pulse signal is output on the ADSM0 or ADSM1 pin, respectively, when an A/D conversion start request signal is generated, and a low-level pulse signal is output on the ADSM0 or ADSM1 pin, respectively, on the timer cycle used to generate the A/D conversion start request signal.

1.6 Protection Functions

1.6.1 POE Input Pins

The important points when migrating software that performs two-motor PWM output control using the complementary PWM mode of the multi-function timer pulse unit (MTU), and input on pins POE0# and POE4#, from the RX62T or RX63T to the RX24T, are described below.

When migrating from the RX62T or RX63T to the RX24T, pins POE0# and POE4# can be used in the same manner.

The pin assignments of the POE input pins of the three microcontrollers are listed below.

	Port Assignment		
Input Pin	**RX62T**	**RX63T**	**RX24T**
POE0#	P70	P70	P70
POE4#	P96	P96	P96
POE8#	PB4	PB4	PB4
POE10#	PE2/PE4	PE2/PE4	PE2/PE4
POE11#	PE3	PE3	PE3
POE12#	—	—	P01 P10

Note that on the RX62T, RX63T, and RX24T high-impedance control by POE takes effect regardless of the setting of the port mode register (PMR).

The high-impedance target pins in case of POE detection on the three microcontrollers are listed below.

POE Detection	High-Impedance Target Pins		
	RX62T	**RX63T**	**RX24T**
POE0	MTU complementary PWM output pins (GPT0, GPT1, and GPT2 multi-use pins) (MTIOC3B/GTIOC0A-A, MTIOC3 D/GTIOC0B-A, MTIOC4A/GTIOC1A-A, MTIOC4C/GTIOC1B-A, MTIOC4B/GTIOC2A-A, MTIOC4D/GTIOC2B-A) *1	MTU complementary PWM output pins (GPT0, GPT1, and GPT2 multi-use pins) (MTIOC3B/GTIOC0A, MTIOC3D/GTIOC0B, MTIOC4A/GTIOC1A, MTIOC4C/GTIOC1B, MTIOC4B/GTIOC2A, MTIOC4D/GTIOC2B) *2	MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D) *3
POE4	MTU complementary PWM output pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D) *4	MTU complementary PWM output pins (GPT4, GPT5, and GPT6 multi-use pins) (MTIOC6B/GTIOC4A, MTIOC6D/GTIOC4B MTIOC7A/GTIOC5A MTIOC7C/GTIOC5B MTIOC7B/GTIOC6A MTIOC7D/GTIOC6B) *5	MTU complementary PWM output pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, MTIOC7D) *6
POE8	MTU0 pins (MTIOC0A-A, MTIOC0A-B, MTIOC0B-A, MTIOC0B-B, MTIOC0C, MTIOC0D) *7	MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) *8	MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) *9
POE10	GPT0 and GPT1 pins (GTIOC0A-B, GTIOC0B-B, GTIOC1A-B, GTIOC1B-B) *10	GPT0 and GPT1 pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B) *11	*12
POE11	GPT2 and GPT3 pins (GTIOC2A-B, GTIOC2B-B, GTIOC3A, GTIOC3B) *13	GPT2 and GPT3 pins (GTIOC2A, GTIOC2B, GTIOC3A, GTIOC3B) *14	*12
POE12	—		MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) *15

Note 1. By means of register settings, the MTU complementary PWM output pins (pins MTU6 and MTU7), MTU0 pin, and GPT pin can be put in the high-impedance state.

Note 2. By means of register settings, the MTU0 pin, MTU complementary PWM output pins (pins MTU6 and MTU7), and GPT pin can be put in the high-impedance state.

Note 3. By means of register settings, the MTU0 pin, the MTU complementary PWM output pins (pins MTU6 and MTU7) and the MTU9 pin can be put in the high-impedance state.

Note 4. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4), the MTU0 pin, and the GPT pin can be put in the high-impedance state.

Note 5. By means of register settings, the MTU0 pin, the MTU complementary PWM output pins (pins MTU3 and MTU4) and the GPT pin can be put in the high-impedance state.

Note 6. By means of register settings, the MTU0 pin, the MTU complementary PWM output pins (pins MTU3 and MTU4), and the MTU9 pin can be put in the high-impedance state.

Note 7. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), and the GPT pin can be put in the high-impedance state.

Note 8. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), and the GPT pin can be put in the high-impedance state.

Note 9. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, or pins MTU6 and MTU7), and the MTU9 pin can be put in the high-impedance state.

Note 10. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), the MTU0 pin, the GPT2 pin, and the GPT3 pin can be put in the high-impedance state.

Note 11. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), the MTU0 pin, the GPT2 pin, the GPT3 pin, the GPT6 pin, and the GPT7 pin can be put in the high-impedance state.

Note 12. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, or pins MTU6 and MTU7), the MTU0 pin, and the MTU9 pin can be put in the high-impedance state.

Note 13. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), the MTU0 pin, the GPT0 pin, and the GPT1 pin can be put in the high-impedance state.

Note 14. By means of register settings, the MTU complementary PWM output pins (pins MTU3 and MTU4, and pins MTU6 and MTU7), the MTU0 pin, the GPT0 pin, the GPT1 pin, the GPT6 pin, and the GPT7 pin can be put in the high-impedance state.

Note 15. The PWM output pins (pins MTU3 and MTU4, or pins MTU6 and MTU7) and the MTU0 pin can be put in the high-impedance state.

1.6.2 LVD Input Pin

On the RX62T, RX63T, and RX24T the VCC pin is used as the input pin of the voltage detection circuit (LVD).

1.6.3 Comparator Input Pins

The reference voltage setting input pins CVREFL and CVREFH of the RX62T and RX63T are not present on the RX24T. In addition, on the RX24T pins AN000 to AN002 and AN100 to AN102 cannot be used as comparator detection input pins, and AVCC0 cannot be used as a reference voltage setting input pin.

On the RX24T the comparator detection input pins are CMPC00 to CMPC03, CMPC10 to CMPC13, and CMPC20 to CMPC23; the reference voltage setting input pins are CVREFC0 and CVREFC1; and the on-chip D/A converter output voltage must be changed.

Also, if AN000 and AN100 to AN102 are assigned as comparator detection input pins, these pin function settings must be changed to CMPC00 to CMPC03, CMPC10 to CMPC13, and CMPC20 to CMPC23.

The comparator input pins of the three microcontrollers are listed below.

	RX62T		RX63T		RX24T	
Type	Pin	Port Assignment	Pin	Port Assignment	Pin	Port Assignment
Comparator detection input pins	AN000	P40	AN000	P40	CMPC00/ CMPC01/ CMPC22/ CMPC23 (AN000)	P40
	AN001	P41	AN001	P41	—	—
	AN002	P42	AN002	P42	—	—
	AN100	P44	AN100	P44	CMPC10/ CMPC11/ CMPC32/ CMPC33 (AN100)	P44
	AN101	P45	AN101	P45	CMPC02/ CMPC03/ CMPC20/ CMPC21 (AN101)	P45
	AN102	P46	AN102	P46	CMPC12/ CMPC13/ CMPC30/ CMPC31 (AN101)	P46
Reference voltage setting input pins	CVREFL	P43	CVREFL	P43	CVREFC0 (AN016)	P20
	CVREFH	P47	CVREFH	P47	CVREFC1 (AN116)	P21
	3-bit D/A converter output voltage	—	3-bit D/A converter output voltage	—	On-chip 8-bit D/A converter output voltage	—

2. Points Regarding Function Settings

2.1 Clocks

2.1.1 Main Clock Oscillator

On the RX62T, RX63T, and RX24T the available methods of supplying a clock signal to the main clock oscillator are connection to a resonator and input of an external clock signal.

When migrating software, keep in mind that on the RX62T and RX63T it was not possible to change the main clock oscillator oscillation source by means of a register setting, whereas on the RX24T the oscillation source can be changed using the MOSEL (main clock oscillator switch) bit in the main clock oscillator forced oscillation control register (MOFCR).

On the RX62T the main clock oscillator is the clock source of the system clock (ICLK) and peripheral module clock (PCLK).

On the RX24T, as on the RX63T, either the main clock oscillator or the on-chip oscillator clock can be selected as the clock source of the system clock (ICLK), peripheral module clock (PCLK), etc.

On the RX24T clock source selection is accomplished by setting the CKSEL[2:0] (clock source select) bits in system clock control register 3 (SCKCR3).

The on-chip oscillator clock oscillation frequencies that can be used as the clock source on the RX63T and RX24T are listed below.

	RX62T	RX63T	RX24T
Low-speed on-chip oscillator (LOCO)	—	125 KHz	4 MHz

On the RX24T the system clock (ICLK) setting requires that a setting be made to the MEMWAIT (memory wait cycle setting) bits in the memory wait cycle setting register (MEMWAIT).

On the RX62T a single peripheral module clock (PCLK) was supplied to all peripheral modules, but on the RX24T, as on the RX63T, the peripheral module clock functionality has been extended.

The applications of the peripheral module clock of the RX24T are listed below.

Peripheral Module Clock Type	Application
Peripheral module clock A (PCLKA)	Multi-function timer pulse unit (MTU)
Peripheral module clock B (PCLKB)	Peripheral clock for modules other than the multi-function timer pulse unit (MTU) and 12-bit A/D converter (S12AD)
Peripheral module clock D (PCLKD)	12-bit A/D converter (S12AD)

On the RX62T the division ratios of the system clock (ICLK) and the peripheral module clock (PCLK) were specified by the settings of ICK[3:0] and PCK[3:0] in the system clock control register (SCKCR), but on the RX24T the division ratios of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB, and PCLKD) are specified by the settings of ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0], respectively, in the peripheral module clock system clock control register (SCKCR).

For details, refer to section 9, Clock Generation Circuit, in RX24T Group User's Manual: Hardware.

2.1.2 Memory Wait Cycles

On the RX24T the system clock (ICLK) setting requires that a setting be made to the MEMWAIT (memory wait cycle setting) bits in the memory wait cycle setting register (MEMWAIT).

The memory wait cycle setting register (MEMWAIT) controls ROM wait cycles.

The MEMWAIT setting conditions stipulate that the MEMWAIT[1:0] bits must not be set to 00b (no wait states) when a system clock (ICLK) frequency higher than 32 MHz is selected.

Also, it is not necessary to set the MEMWAIT[1:0] bits to 01b (wait states (ICLK ≤ 64 MHz)) when a system clock (ICLK) frequency of 32 MHz or lower is selected.

When a system clock (ICLK) frequency of higher than 64 MHz is selected, the MEMWAIT[1:0] bits must not be set to 01b (wait states (ICLK ≤ 64 MHz)). Also, it is not necessary to set the MEMWAIT[1:0] bits to 10b (wait states (ICLK ≤ 80 MHz)) when a system clock (ICLK) frequency of 64 MHz or lower is selected.

For details of the setting restrictions for the MEMWAIT bits, refer to section 9, Clock Generation Circuit, in RX24T Group User's Manual: Hardware.

The setting restrictions for the MEMWAIT bits are summarized below.

	Operating Power Control State			
	High-Speed Operating Mode			
MEMWAIT[1:0] Bits	**ICLK ≤ 32 MHz**	**32 MHz < ICLK ≤ 64 MHz**	**64 MHz < ICLK ≤ 80 MHz**	**Middle-Speed Operating Mode**
00b	Can be set.	Cannot be set.	Cannot be set.	Can be set.
01b	Can be set.	Can be set.	Cannot be set.	Cannot be set.
10b	Can be set.	Can be set.	Can be set.	Cannot be set.
Other than above	Cannot be set.			

2.1.3 ROM Cache

The ROM cache functionality has been extended on the RX24T. When the ROM cache is operating, data is served from the ROM cache when a cache hit occurs.

To enable the ROM cache, set the ROM cache operation enable (ROMCEN) bit in the ROM cache enable register (ROMCE) to 1 (ROM cache operation enabled).

The default setting of the ROM cache enable register (ROMCE) is 0 (ROM cache operation disabled). Setting the ROMCEN bit to 1 (ROM cache operation enabled) will improve the processing speed.

2.2 Port Settings

The I/O ports of the RX24T can function as general I/O ports, I/O for peripheral functions, or as interrupt input pins.

Each port can also function as a peripheral module I/O pin, interrupt input pin, etc. After a reset it becomes an input port, but the function can be changed by means of register settings. The settings of the various ports are determined by the I/O port registers and the on-chip peripheral module registers.

On the RX24T, as on the RX63T, port function settings are made in the pin function control registers of the multi-function pin controller (MPC) and the I/O port mode register (PMR). On the RX62T the priority level of output port functions is determined by the various functions, and input ports transfer signals to all functions for which the input setting is selected.

For details of the supported settings of each port of the RX24T, refer to section 19, Multi-Function Pin Controller (MPC), in RX24T Group User's Manual: Hardware.

2.3 A/D Conversion

Operation settings can be entered independently for each unit. Therefore, separate register settings are required for each unit (S12AD, S12AD1, and S12AD2).

2.3.1 Single-Shunt Current Detection

The settings necessary to perform A/D conversion at two user-defined locations, during the timer counter peak to trough or trough to peak interval, are described below.

Note that since it is necessary to give priority to shunt current detection over other A/D conversion operations, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, group priority control is enabled, and double trigger mode is selected for the A/D conversion trigger.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In the A/D control register (ADCSR), set the double trigger mode select (DBLE) bit to 1 (double trigger mode selected) and the double trigger channel select (DBLANS [4:0]) bits to specify a channel as the analog input to be used as the double trigger target.
3. To select the A/D conversion start trigger for group A to match the MTU used for PWM output, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 001011b (compare match of MTU4.TADCORA and MTU4.TCNT or compare match of MTU4.TADCORB and MTU4.TCNT) or to 001111b (compare match of MTU7.TADCORA and MTU7.TCNT or compare match of MTU7.TADCORB and MTU7.TCNT).
4. Set the trigger start enable (TRGE) bit in the A/D control register (ADCSR) to 1 (start of A/D conversion by synchronous or asynchronous trigger enabled).
5. In the timer A/D converter start request cycle set buffer register of MTU4 or MTU7 (TADCOBRA or TADCOBRB), set the counter value for A/D conversion start requests.
6. In the timer A/D converter start request control register (TADCR) of MTU4 or MTU7, set the MTU4.TADCOBRA/B transfer timing select (BF[1:0]) bits or MTU7.TADCOBRA/B transfer timing select (BF[1:0]) bits to specify the A/D conversion start request cycle timing of transfers from the timer A/D converter start request cycle set buffer register (TADCOBRA or TADCOBRB) to the timer A/D converter start request cycle set register (TADCORA or TADCORB).
7. In the timer A/D converter start request control register (TADCR) of MTU4 or MTU7, set bits DT4BE, UT4BE, DT4AE, and UT4AE, or bits DT7BE, UT7BE, DT7AE, and UT7AE, to specify the A/D conversion start request cycle.
8. Set the group priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group priority control).

2.3.2 Three-Shunt Current Detection

The settings necessary to perform A/D conversion using unit 1 (S12AD1) of the 12-bit A/D converter (S12ADF), during timer counter peak to trough or trough to peak, are described below.

Note that since it is necessary to give priority to shunt current detection over other A/D conversion operations, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, and group priority control is enabled.

1. In A/D channel select register A0 (ADANSA0), select analog inputs AN100 to AN102 as channels on which A/D conversion will be performed for group A.

2. Set the channel-dedicated sample-and-hold circuit bypass select (SHANS[2:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify that the channel-dedicated sample-and-hold circuits are used for AN100 to AN102.

3. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).

4. When A/D conversion takes place at timer counter peaks, to match the MTU used for PWM output in group A, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000100b (MTU3.TGRA compare match/input capture (peak)) or 000110b (MTU6.TGRA compare match/input capture (peak)).
   When A/D conversion takes place at timer counter troughs, to match the MTU used for PWM output in group A, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000101b (MTU4.TGRA compare match/input capture, or MTU4.TCNT underflow (trough) in complementary PWM mode) or 000111b (MTU7.TGRA compare match/input capture, or MTU7.TCNT underflow (trough) in complementary PWM mode).

5. When A/D conversion takes place at timer counter peaks, set the A/D converter start request enable (TTGE) bit in the timer interrupt enable register (TIER) of MTU3 or MTU6 to 1 (A/D conversion start request generation enabled).
   When A/D conversion takes place at timer counter troughs, set the A/D converter start request enable 2 (TTGE2) bit in the timer interrupt enable register (TIER) of MTU4 or MTU7 to 1 (A/D conversion start request generation by MTUn.TCNT underflow (trough) enabled).

6. Set the channel-dedicated sample-and-hold circuit sampling time setting (SSTSH[7:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify the sampling time.

7. Set the trigger start enable (TRGE) bit in the A/D control register (ADCSR) to 1 (start of A/D conversion by synchronous or asynchronous trigger enabled).

8. Set the group priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group priority control).

2.3.3 Bus Voltage

Obtaining the bus voltage involves A/D conversion in continuous scan mode.

The settings necessary to perform bus voltage A/D conversion using different A/D conversion triggers than in shunt current detection are described below.

Note that since the priority of bus voltage A/D conversion is lower than that for shunt current detection, etc., and since the A/D conversion trigger settings used differ from those for shunt current detection, group scan mode is selected as the scan mode, the shunt current analog input is assigned to group A, group priority control is enabled, and the bus voltage is assigned to group C.

For shunt current detection settings, refer to 2.3.1, Single-Shunt Current Detection, and 2.3.2, Three-Shunt Current Detection.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In A/D channel select register C0 (ADANSC0) or A/D channel select register C1 (ADANSC1), select the analog input channels on which A/D conversion will be performed for group C.
3. Set the group C A/D conversion start trigger select (TRSC[5:0]) bits in the A/D group C trigger select register (ADGCTRGR) to 111111b (trigger source deselection state).
4. Set the group C A/D conversion operation enable (GRCE) bit in the A/D conversion start trigger select register (ADSTRGR) to 1 (group C is used).
5. Set the group priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group priority control).
6. Set the low-priority group restart setting (GBRSCN) bit in the A/D group scan priority control register (ADGSPCR) to 1 (scanning for the group is restarted after having been discontinued due to group priority control).
7. Set the single scan continuous start setting (GBRP) bit in the A/D group scan priority control register (ADGSPCR) to 1 (single scan for the lowest-priority group is continuously activated).
8. Set the restart channel select (LGRRS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (scanning from the channel on which A/D conversion is not completed is restarted).

2.3.4 Channel-Dedicated Sample-and-Hold Function

The channel-dedicated sample-and-hold function is used to perform A/D conversion of analog input on all selected channels once only after sample-and-hold takes place.

This allows simultaneous sampling of multiple channels, for example for three-shunt current detection.

On the RX24T the channel-dedicated sample-and-hold function can be used on analog input channels AN100 to AN102.

The channel-dedicated sample-and-hold settings are described below.

1. Set the channel-dedicated sample-and-hold circuit bypass select (SHANS[2:0]) bits in the sample-and-hold circuit control register (ADSHCR) to enable use of the channel-dedicated sample-and-hold circuit for the channels on which the function is to be enabled.
2. Set the channel-dedicated sample-and-hold circuit sampling time setting (SSTSH[7:0]) bits in the sample-and-hold circuit control register (ADSHCR) to specify the sampling time.

2.3.5 Group Priority Control

During basic operation in group scan mode, all other trigger inputs are ignored during scan operation on group A, group B, or group C. During group priority operation, in contrast, if a trigger input for a higher-priority group is received during scan operation on a lower-priority group, scanning of the lower-priority group halts so that scanning of the higher-priority group can proceed.

The number of groups that operate in group scan mode can be specified as two (groups A and B) or as three (groups A, B, and C) by setting the group C A/D conversion operation enable (GRCE) bit in the A/D group C trigger select register (ADGCTRGR).

The settings for enabling group priority control using unit 0 of the 12-bit A/D converter (S12ADF) are described below.

1. Set the scan mode select (ADCS[1:0]) bits in the A/D control register (ADCSR) to 01b (group scan mode).
2. In A/D channel select register A0 (ADANSA0) or A/D channel select register (ADANSA1), select the analog input channels on which A/D conversion will be performed for group A.
3. In A/D channel select register B0 (ADANSB0) or A/D channel select register (ADANSB1), select the analog input channels on which A/D conversion will be performed for group B.
4. In A/D channel select register C0 (ADANSC0) or A/D channel select register (ADANSC1), select the analog input channels on which A/D conversion will be performed for group C.
5. Set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to specify the A/D conversion start trigger for group A.
6. Set the group B A/D conversion start trigger select (TRSB[5:0]) bits in A/D conversion start trigger select register (ADSTRGR) to specify the A/D conversion start trigger for group B.
7. Set the group C A/D conversion start trigger select (TRSC[5:0]) bits in the A/D group C trigger select register (ADGCTRGR) to specify the A/D conversion start trigger for group C.
8. Set the group C A/D conversion operation enable (GRCE) bit in the A/D conversion start trigger select register (ADSTRGR) to 1 (group C is used).
9. Set the group priority control setting (PGS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (operation with group priority control).
10. Set the low-priority group restart setting (GBRSCN) bit in the A/D group scan priority control register (ADGSPCR) to 1 (scanning for the group is restarted after having been discontinued due to group priority control).
11. Set the restart channel select (LGRRS) bit in the A/D group scan priority control register (ADGSPCR) to 1 (scanning from the channel on which A/D conversion is not completed is restarted).

As the group scan mode trigger settings, set the ADSTRGR.TRSA[5:0] bits to select a synchronous trigger for group A, set the ADSTRGR.TRSB[5:0] bits to select a synchronous trigger for group B that is different from that selected for group A, and set the ADGCTRGR.TRSC[5:0] bits to select a synchronous trigger for group C that is different from those selected for groups A and B.

The scan operation is controlled by the setting of the low-priority group restart setting (GBRSCN) bit in the A/D group scan priority control register (ADGSPCR), as summarized below.

Scan Operation	**Trigger Input**	**ADGSPCR.GBRSCN = 0 Scanning for the group is not restarted after having been discontinued due to group priority control.**	**ADGSPCR.GBRSCN = 1 Scanning for the group is restarted after having been discontinued due to group priority control.**
Group A scan in progress	Group A trigger input	Trigger input disabled	Trigger input disabled
	Group B trigger input	Trigger input disabled	After group A scan finishes, group B scan takes place.
	Group C trigger input	Trigger input disabled	After group A scan finishes, group C scan takes place.
Group B scan in progress	Group A trigger input	Group B scan halts, and group A scan starts.	• Group B scan halts, and group A scan starts. • After group A scan finishes, group B scan takes place.
	Group B trigger input	Trigger input disabled	Trigger input disabled
	Group C trigger input	Trigger input disabled	After group B scan finishes, group C scan takes place.
Group C scan in progress	Group A trigger input	Group C scan halts, and group A scan starts.	• Group C scan halts, and group A scan starts. • After group A scan finishes, group C scan takes place.
	Group B trigger input	Group C scan halts, and group B scan starts.	• Group C scan halts, and group B scan starts. • After group B scan finishes, group C scan takes place.
	Group C trigger input	Trigger input disabled	Trigger input disabled

The correspondence of the three-group (group A, B, and C) group priority operation settings and operating modes is summarized below

Register Bit Descriptions

- Low-priority group restart setting (GBRSCN) bit
  0: Scanning for the group is not restarted after having been discontinued due to group priority control.
  1: Scanning for the group is restarted after having been discontinued due to group priority control.

- Restart channel select (LGRRS) bit
  0: Scanning is restarted from the scan start channel.
  1: Scanning from the channel on which A/D conversion is not completed is restarted.

- Single scan continuous start setting (GBRP) bit
  0: Single scan is not continuously activated.
  1: Single scan for the lowest-priority group is continuously activated

ADGSPCR			
GBRSCN	**LGRRS**	**GBRP**	**Operation Types**
0	X	0	Three-group (group A, B, and C) group priority operation • When the group A trigger is input, group B scan ends (and does not resume). • When the group A or group B trigger is input, group C scan ends (and does not resume).
0	X	1	Three-group (group A, B, and C) group priority operation • When the group A trigger is input, group B scan ends (and does not resume). • Continuous single scan takes place on group C with no start trigger input. After group C scan is halted, scan resumes from the channel specified in the ADANSC0 or ADANSC1 register after group A or B scanning finishes.
1	0	0	Three-group (group A, B, and C) group priority operation • After group B scan is halted, scan resumes from the channel specified in the ADANSB0 or ADANSB1 register after group A scanning finishes. • After group C scan is halted, scan resumes from the channel specified in the ADANSC0 or ADANSC1 register after group A or B scanning finishes.
1	1	0	Three-group (group A, B, and C) group priority operation • After group B scan is halted, after group A scanning finishes scan resumes from the channel specified in the ADANSB0 or ADANSB1 register on which scanning was halted. • After group C scan is halted, after group A or B scanning finishes scan resumes from the channel specified in the ADANSC0 or ADANSC1 register on which scanning was halted.
1	0	1	Three-group (group A, B, and C) group priority operation • After group B scan is halted, scan resumes from the channel specified in the ADANSB0 or ADANSB1 register after group A scanning finishes. • Continuous single scan takes place on group C with no start trigger input. After group C scan is halted, scan resumes from the channel specified in the ADANSC0 or ADANSC1 register after group A or B scanning finishes.

ADGSPCR			
GBRSCN	**LGRRS**	**GBRP**	**Operation Types**
1	1	1	Three-group (group A, B, and C) group priority operation • After group B scan is halted, after group A scanning finishes scan resumes from the channel specified in the ADANSB0 or ADANSB1 register on which scanning was halted. • Continuous single scan takes place on group C with no start trigger input. After group C scan is halted, after group A or B scanning finishes scan resumes from the channel specified in the ADANSC0 or ADANSC1 register on which scanning was halted.

2.3.6 A/D Conversion Status Output (ADST Bit Status Output)

On the RX24T the ADST bit status output pins can be used to check the A/D conversion status.

To enable ADST bit status output (pin P02/ADST0, PD6/ADST0, P00/ADST1, or P01/ADST2), set the pin function select bits in the pin function select register of the multi-function pin controller (MPC), and set the pin mode control bit in the port mode register (PMR) of the I/O port to 1 (use pin as I/O port for peripheral functions).

2.4 Timer (MTU)

2.4.1 Complementary PWM

In complementary PWM mode it is possible to specify dead time for output PWM waveforms. The dead time is the period during which the upper and lower arm transistors are set to the inactive level in order to prevent short-circuiting of the arms. Three sets of (positive-phase and negative-phase) PWM waveforms, or six phases in total, can be output with dead time by combining MTU3 and MTU4 or MTU6 and MTU7. PWM waveforms without dead time can also be output.

In complementary PWM mode, pins MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D or pins MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D function as PWM output pins, and the MTIOC3A or MTIOC6A pin can be set to toggle output synchronized with the PWM cycle.

MTU3.TCNT and MTU4.TCNT or MTU6.TCNT and MTU7.TCNT function as up/down-counters.

To enable complementary PWM mode on the RX24T, as on the RX62T and RX63T, in the timer mode register of MTU3 or MTU6 set the mode select (MD[3:0]) bits to a value of 1101b to 1111b, the buffer operation A (BFA) bit to 1 (TGRA and TGRC registers used together for buffer operation), and the buffer operation B (BFB) bit to 1 (TGRB and TGRD registers used together for buffer operation).

To produce left-right asymmetric PWM output in complementary PWM mode on the RX24T, it is necessary to set the double buffer select (DRS) bit in timer mode register 2 (TMDR2A) to 1 (double buffer function enabled) and to specify different values for buffer register B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF or MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) and buffer register A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD or MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD).

Note that settings should be made for buffer register A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD or MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD) and for buffer register B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF or MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) at the same time.

When transferring buffer register data, write to MTU4.TGRD (MTU7.TGRD) last.

For details of setting values, refer to section 20, Multi-Function Timer Pulse Unit (MTU3d), in RX24T Group User's Manual: Hardware.

2.4.2 Timer A/D Conversion Start Request

In complementary PWM mode on the RX24T, as on the RX62T and RX63T, MTU3.TGRA compare match (peak), MTU4.TCNT underflow (trough), MTU6.TGRA compare match, MTU7.TCNT underflow (trough), or MTU3, MTU4, MTU6, or MTU7 compare match can be used as the A/D conversion start request.

To perform A/D conversion at two user-defined locations, during the MTU4 timer counter peak to trough or trough to peak interval, make one of the following combinations of settings to bits DT4BE, UT4BE, DT4AE, and UT4AE in the MTU4 timer A/D conversion start request control register (TADCR).

Combined Settings for MTU4

	DT4BE Down-Count TRG4BN Enable Bit	UT4BE Up-Count TRG4BN Enable Bit	DT4AE Down-Count TRG4AN Enable Bit	UT4AE Up-Count TRG4AN Enable Bit
Combination 1	Enabled (1)	Disabled (0)	Enabled (1)	Disabled (0)
Combination 2	Enabled (1)	Disabled (0)	Disabled (0)	Enabled (1)
Combination 3	Disabled (0)	Enabled (1)	Enabled (1)	Disabled (0)
Combination 4	Disabled (0)	Enabled (1)	Disabled (0)	Enabled (1)

To perform A/D conversion at two user-defined locations, during the MTU7 timer counter peak to trough or trough to peak interval, make one of the following combinations of settings to bits DT7BE, UT7BE, DT7AE, and UT7AE in the MTU7 timer A/D conversion start request control register (TADCR).

Combined Settings for MTU7

	DT7BE Down-Count TRG7BN Enable Bit	UT7BE Up-Count TRG7BN Enable Bit	DT7AE Down-Count TRG7AN Enable Bit	UT7AE Up-Count TRG7AN Enable Bit
Combination 1	Enabled (1)	Disabled (0)	Enabled (1)	Disabled (0)
Combination 2	Enabled (1)	Disabled (0)	Disabled (0)	Enabled (1)
Combination 3	Disabled (0)	Enabled (1)	Enabled (1)	Disabled (0)
Combination 4	Disabled (0)	Enabled (1)	Disabled (0)	Enabled (1)

It is also necessary to specify the A/D conversion start trigger by making the settings specified in step 3, and to specify the A/D conversion start request cycle by making the settings specified in step 5, of 2.3.1, Single-Shunt Current Detection.

The settings for performing A/D conversion at either the peak or trough of the timer counter are described below.

Performing A/D Conversion at the Peak of the Timer Counter

Set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000100b (MTU3.TGRA compare match/input capture (peak)) to specify the A/D conversion start trigger, and set the A/D converter start request enable (TTGE) bit in the MTU3 timer interrupt enable register (TIER) to 1 (A/D conversion start request generation enabled).

Alternatively, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000110b (MTU6.TGRA compare match/input capture (peak)) to specify the A/D conversion start trigger, and set the A/D converter start request enable (TTGE) bit in the MTU6 timer interrupt enable register (TIER) to 1 (A/D conversion start request generation enabled).

Performing A/D Conversion at the Trough of the Timer Counter

Set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000101b (MTU4.TGRA compare match/input capture, or MTU4.TCNT underflow (trough) in complementary PWM mode) to specify the A/D conversion start trigger, and set the A/D converter start request enable 2 (TTGE2) bit in the MTU4 timer interrupt enable register (TIER) to 1 (A/D conversion request at MTU4.TCNT underflow (trough) enabled).

Alternatively, set the A/D conversion start trigger select (TRSA[5:0]) bits in the A/D conversion start trigger select register (ADSTRGR) to 000111b (MTU7.TGRA compare match/input capture, or MTU7.TCNT underflow (trough) in complementary PWM mode) to specify the A/D conversion start trigger, and set the A/D converter start request enable 2 (TTGE2) bit in the MTU7 timer interrupt enable register (TIER) to 1 (A/D conversion request at MTU7.TCNT underflow (trough) enabled).

2.4.3 A/D Conversion Start Request Frame Synchronization Signal Output

The RX24T can output an A/D conversion start request frame synchronization signal.

The A/D conversion start request frame synchronization signal enables external pins to be used to monitor the A/D conversion start request signal generation timing. Make the following settings to enable A/D conversion start request frame synchronization signal output (on pin PB2/ADSM0 or PB1/ADSM1).

1. Set the appropriate pin function select bit in the pin function select register of the multi-function pin controller (MPC).

2. Set the pin mode control bit in the port mode register (PMR) of the I/O port to 1 (peripheral function).

3. Set the A/D conversion start request select for ADSM0 pin output frame synchronization signal generation (TADSTRS0[4:0]) bits in A/D conversion start request select register 0 (TADSTRGR0) of the multi-function timer pulse unit (MTU) to specify the A/D conversion start request to be used to generate output of the frame synchronization signal on the ADSM0 pin.
   Alternatively, set the A/D conversion start request select for ADSM1 pin output frame synchronization signal generation (TADSTRS0[4:0]) bits in A/D conversion start request select register 1 (TADSTRGR1) of the multi-function timer pulse unit (MTU) to specify the A/D conversion start request to be used to generate output of the frame synchronization signal on the ADSM1 pin.

For details of setting values, refer to section 20, Multi-Function Timer Pulse Unit (MTU3d), in RX24T Group User's Manual: Hardware.

2.5 Protection Functions

2.5.1 POE

The port output enable (POE) function can be used to place output pins of the MTU in the high-impedance state under various conditions.

The conditions under which MTU output pins can be placed in the high-impedance state using the port output enable (POE) function on the RX24T are summarized below.

Condition
Change of input pin state. • Input received on POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# pin.
Shorting of output pins. • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC3B and MTIOC3D (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC4A and MTIOC4C (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC4B and MTIOC4D (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC6B and MTIOC6D (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC7A and MTIOC7C (indicating a short). • Output signal level (active level) matched for one cycle or more on MTU complementary PWM output pins MTIOC7B and MTIOC7D (indicating a short).
Bit in software port output enable register (SPOER) set to 1 (place pins in high-impedance state).
Clock generation circuit oscillation stop detected.
Comparator detection by comparator (CMPC).

The above functionality can be used in the same manner when migrating from the RX62T or RX63T to the RX24T.

To enable high-impedance control by comparing the output level of MTU3 pins (MTIOC3B/MTIOC3D) or MTU4 pins (MTIOC4A and MTIOC4C or MTIOC4B and MTIOC4D) in complementary PWM mode on the RX24T, set the pin output active level in active level register 1 (ALR1) and enable high-impedance control for MTU3 or MTU4 pins in port output enable control register 2 (POECR2).

To enable high-impedance control by comparing the output level of MTU6 pins (MTIOC6B/MTIOC6D) or MTU7 pins (MTIOC7A and MTIOC7C or MTIOC7B and MTIOC7D) in complementary PWM mode, set the pin output active level in active level register 2 (ALR2) and enable high-impedance control for MTU6 or MTU7 pins in port output enable control register 2 (POECR2).

Among the registers used by the POE function, the following can be written to only once after a reset.

It is necessary to use byte or word access when making settings.

- Input level control/status registers 1, 2, 3, 4, 5, 6, and 7 (ICSR1, ICSR2, ICSR3, ICSR4, ICSR5, ICSR6, and ICSR7)
- Output level control/status registers 1 and 2 (OCSR1 and OCSR2)
- Active level registers 1 and 2 (ALR1 and ALR2)
- Port output enable control registers 1, 2, 4, 5, 7, and 8 (POECR1, POECR2, POECR4, POECR5, POECR7, and POECR8)
- Port output enable comparator request select register (POECMPSEL)

For details of POE register settings, refer to section 21, Port Output Enable 3 (POE3b), in RX24T Group User's Manual: Hardware.

2.5.2 LVD

The voltage detection circuit (LVD) monitors the voltage input on the VCC pin. The VCC input voltage can be monitored using a software program.

It is possible to generate an internal reset or interrupt when a specified detection voltage value is detected.

The voltage detection circuit of the RX24T supports three LVD functions: voltage monitoring 0, voltage monitoring 1, and voltage monitoring 2.

The specifications of the voltage detection circuit of the RX24T are listed below.

Item		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0.	When voltage rises above or drops below Vdet1.	When voltage rises above or drops below Vdet2.
	Detection voltage	Voltage selectable from 2 levels using OFS1 register.	Voltage selectable from 9 levels using LVDLVLR.LVD1LVL[3:0] bits.	Voltage selectable from 4 levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	None	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Vdet1 passage detection.	LVD2SR.LVD2DET flag: Vdet2 passage detection.
Processing when voltage detected	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified duration when VCC > Vdet0.	Reset when Vdet1 > VCC: CPU restart after specified duration when VCC > Vdet1 or Vdet1 > VCC (selectable).	Reset when Vdet2 > VCC: CPU restart after specified duration when VCC > Vdet2 or Vdet2 > VCC (selectable).
	Interrupts	None	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt.	Selectable between non-maskable or maskable interrupt.
			Interrupt request issued both when Vdet1 > VCC and when VCC > Vdet1, or when Vdet1 > VCC or VCC > Vdet1.	Interrupt request issued both when Vdet2 > VCC and when VCC > Vdet2, or when Vdet2 > VCC or VCC > Vdet2.

When migrating software from the RX62T, be aware that on the RX24T adds a new monitoring function (voltage monitoring 0) to the two supported on the RX62T (voltage monitoring 1 and voltage monitoring 2). On the RX24T monitoring by the voltage monitoring 1 and voltage monitoring 2 functions can be checked using the voltage monitoring 1 circuit status register (LVD1SR) and voltage monitoring 2 circuit control register 1 (LVD2CR1), respectively.

When migrating software that uses the voltage detection circuit (LVD) of the RX62T or RX63T, it is necessary to change the detection voltage level settings on the RX24T.

On the RX24T the voltage monitoring 0 detection voltage level can be set in option function select register 1 (OFS1). The voltage detection 1 and voltage detection 2 detection voltage levels can be set in the voltage detection level select register (LVDLVLR).

For details of the voltage detection circuit (LVD), refer to section 7, Option-Setting Memory, and section 8, Voltage Detection Circuit (LVDAb), in RX24T Group User's Manual: Hardware.

The detection voltage level settings supported by the three microcontrollers are listed below.

Detection Voltage Level	RX62T	RX63T	RX24T
Voltage monitoring 0 detection voltage level	Function not implemented.	Fixed at 1 level	Selectable from 2 levels
Voltage monitoring 1 detection voltage level	Fixed at 1 level	Selectable from 3 levels (Pins 48 and 64 are fixed at 1 level.)	Selectable from 9 levels
Voltage monitoring 2 detection voltage level	Fixed at 1 level	Selectable from 3 levels (Pins 48 and 64 are fixed at 1 level.)	Selectable from 4 levels

2.5.3 Comparator Reference Voltage

On the RX24T comparator C (CMPC) compares the reference input voltage and analog input voltage. The reference input voltage and analog input voltage comparison result can be read by software or output to an external pin. It is also possible to generate an interrupt request when the comparison result changes.

The comparator C reference input voltage of the RX24T is selectable from the inputs to pins CVREFC0 and CVREFC1, and the output of the on-chip D/A converter.

To switch the reference input voltage on the RX24T, set the CVRS[1:0] (reference input voltage select) bits in the comparator reference voltage select register (CMPSEL1).

Note that when the CVRS[1:0] (reference input voltage select) bits in the comparator reference voltage select register (CMPSEL1) are set to 10b (on-chip D/A converter output voltage selected as reference input voltage), it is also necessary to make settings to the D/A converter for generating comparator C reference voltage (DA).

The D/A converter for generating comparator C reference voltage (DA) outputs an 8-bit conversion result based on the VREF pin input voltage and the value of D/A data register 0 (DADR0), using the following formula.

Formula: (DADR0 register value ÷ 256) × VREF

D/A conversion starts when the D/A output enable 0 (DAOE0) bit in the D/A control register (DACR) of the D/A converter for generating comparator C reference voltage (DA) is set to 1 (D/A conversion enabled).

For details, refer to section 30, D/A Converter for Generating Comparator C Reference Voltage (DA), and section 31, Comparator C (CMPC), in RX24T Group User's Manual: Hardware.

3. Points of Difference

3.1 Comparison of Functions

A comparative listing of the functions of the RX62T, RX63T, and RX24T is presented below.

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Clocks	Clock generation circuit	Oscillator	Main clock oscillator	8 MHz to 12.5 MHz	8 MHz to 12.5 MHz	1 MHz to 20 MHz
			High-speed on-chip oscillator (HOCO)	—	—	32/64 MHz
			Low-speed on-chip oscillator (LOCO)	—	125 KHz	4 MHz
			PLL frequency synthesizer	○	○	○
			IWDT-dedicated on-chip oscillator	125 KHz	125 KHz	15 KHz
		Settings	System clock (ICLK)	○	○	○
			Peripheral module clock (PCLK)	○	—	—
			Peripheral module clock (PCLKA)	—	○	○
			Peripheral module clock (PCLKB)	—	○	○
			AD clock (PCLKC)	—	○	—
			S12AD clock (PCLKD)		○	○
			FlashIF clock (FCLK)	—	○	○
			External bus clock (BCLK)	—	○	—
		Operating frequency	System clock (ICLK)	100 MHz max.	100 MHz max	80 MHz max.
			Peripheral module clock (PCLK)	50 MHz max.	—	—
			Peripheral module clock (PCLKA)	—	100 MHz max.	80 MHz max.
			Peripheral module clock (PCLKB)	—	50 MHz max.	40 MHz max.
			AD clock (PCLKC)		100 MHz max.	—
			S12AD clock (PCLKD)		50 MHz max.	40 MHz max.
			FlashIF clock (FCLK)	—	50 MHz max.	32 MHz max.
			External bus clock (BCLK)	—	50 MHz max.	—
			Main clock oscillator wait control	—	○	○
	ROM	ROM cache	ROM cache enable	—	—	○
		ROM access wait	ROM access wait setting	—	—	○

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Interrupts	Interrupt controller (ICU)	Symbol		ICU	ICUb	ICUb
		Interrupt sources	External interrupt sources (IRQ pins)	8	8	8
			Software interrupt sources	1	1	1
			Non-maskable interrupt sources (NMI pins)	3	6	5
		Non-maskable interrupts	NMI pin interrupt	○	○	○
			Oscillation stop detection interrupt	○	○	○
			Voltage monitoring interrupt	○	—	—
			Voltage monitoring 1 interrupt		○	○
			Voltage monitoring 2 interrupt		○	○
			WDT underflow/ refresh error	—	○	—
			IWDT underflow/ refresh error	—	○	○
		Priority setting	Support for 16 interrupt priority levels	○	○	○
I/O ports	General I/O ports	Ports	Input/output	55	57	80
			Input	21	21	1
			Open-drain output	2	16	60
			Large-current output	12	12	15
			5 V tolerant	—	—	2
			Pull-up resistors	—	—	80
Multi-function pin controller	Multi-function pin controller (MPC)	I/O functions	Support for selecting from multiple pins for I/O functions	—	○	○
Timer	Multi-function timer pulse unit (MTU)	Symbol		MTU3	MTU3	MTU3d
		Channels	16 bits/channel	8 channels	8 channels	9 channels
		Pulse I/O	Pulse I/O channels (max. supported pulse I/O channels)	24	24	28
			Pulse input channels (max. supported pulse input channels)	3	3	3

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Timer	Multi-function timer pulse unit (MTU)	Division ratio	Clock pin	ICLK	PCLKA	PCLKA
			Divide-by-1	○	○	○
			Divide-by-2	—	—	○
			Divide-by-4	○	○	○
			Divide-by-8	—	—	○
			Divide-by-16	○	○	○
			Divide-by-32	—	—	○
			Divide-by-64	○	○	○
			Divide-by-256	○	○	○
			Divide-by-1024	○	○	○
		External clock input	MTCLKA	○	○	○
			MTCLKB	○	○	○
			MTCLKC	○	○	○
			MTCLKD	○	○	○
			MTIOC1A	—	—	○
		Input capture function	Transfer of TCNT value to TGR at input edge detection	○	○	○
		Output compare function	0 output, 1 output, toggle output	○	○	○
		Synchronous operation	Simultaneous overwriting of multiple TCNT values (synchronous preset)	○	○	○
		Buffer operation	Use of TGRC and TGRD registers as buffer registers	○	○	○
		Cascade connection operation	Connection of 16-bit counters from different channels to function as a 32-bit counter	○	○	○
		PWM mode	Output of PWM waveforms from output pins	○	○	○
		Phase counting mode	16-bit mode	○	○	○
			32-bit mode	○	○	○
		Reset-synchronized PWM mode	PWM waveforms (positive-phase and negative-phase) that share a common wave transition point	○	○	○

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Timer	Multi-function timer pulse unit (MTU)	Complementary PWM output mode	Output of non-overlapping waveforms for 3-phase inverter control	○	○	○
			Automatic dead time setting	○	○	○
			Support for setting PWM duty ratio to any value from 0 to 100%	○	○	○
			A/D conversion request delaying function	○	○	○
			Peak/trough interrupt skipping function	○	○	○
			Double buffer function	○	○	○
		External pulse width measurement	External pulse width measurement	○	○	○
		Dead time compensation counter	Measurement of delay in output waveforms and application to duty ratio	○	○	○
		Trigger generation	A/D converter conversion start trigger generation	○	○	○
			A/D conversion start skipping function	○	○	○
		A/D conversion start timing measurement	A/D conversion start request frame synchronization signal	—	—	○
		Interrupt sources	Interrupt sources	38	38	45
	Port output enable (POE)	Symbol		POE3	POE3	POE3b
		High-impedance control	High-impedance control of MTU waveforms output pins	○	○	○
			High-impedance control of GPT waveforms output pins	○	○	—

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Timer	Port output enable (POE)	Activation sources	Activation by POE0 input pin	○	○	○
			Activation by POE4 input pin	○	○	○
			Activation by POE8 input pin	○	○	○
			Activation by POE10 input pin	○	○	○
			Activation by POE11 input pin	○	○	○
			Activation by POE12 input pin	—	○	○
			Activation at detection of clock generation circuit oscillation stop	○	○	○
			Activation by comparison of output level of MTU complementary PWM output pins	○	○	○
			Activation at detection of output short (GPT large-current pins)	○	—	—
			Activation at detection of output short (GPT output pins)	—	○	—
			Activation by event signal of event link controller (ELC)	—	—	—
			Activation at comparator detection	○	○	○
			Activation by software (register)	○	○	○
	General PWM timer (GPT)	Symbol		GPT	GPT	—
		Channels	16 bits/channel	4 channels	8 channels	—
		I/O	Input pins	1	2	—
			I/O pins	8	16	—
		Division ratio	Clock pin	ICLK	PCLKA	—
			Divide-by-1	○	○	—
			Divide-by-2	○	○	—
			Divide-by-4	○	○	—
			Divide-by-8	○	○	—
		External clock input		○	○	—
		Count operation	Up-count or down-count (saw-wave)	○	○	—
			Up/down-count (triangle-wave)	○	○	—
		Output compare/ input capture registers	Output compare registers that also function as input capture registers	○	○	—

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Timer	General PWM timer (GPT)	Compare/ buffer registers	Support for setting compare match registers as buffer registers	○	○	—
		Cycle set registers/ buffer registers	Support for setting cycle set registers as buffer registers	○	○	—
		Input capture function	Transfer of count values to GTCCRA or GTCCRB at input edge detection	○	○	—
		Synchronous operation	Support for simultaneous count clear or start on multiple channels	○	○	—
		Phase shift start	Support for setting count value of channels before count operation start and starting count operation with phase differential	○	○	—
		Automatic dead time setting function	Automatic setting of compare match value for negative-phase waveforms with dead time based on compare match value and dead time value for positive-phase waveforms	○	○	—
		PWM mode	Output of PWM waveforms on output pins	○	○	—
		Buffer operation	Support for compare match using buffer registers	○	○	—
		One-shot operation	Support for with fixed buffer operation	○	○	—
		Trigger generation	A/D conversion start trigger	○	○	—
		PWM delay generation function	Support for controlling PWM output rise/fall timing at resolution of 1/32 of PCLKA	—	○	—

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Timer	8-bit timer (TMR)	Symbol		—	—	TMR
		Channels	8 bits/channel	—	—	2 channels × 4 units
		Division ratio	Clock pin	—	—	PCLK
			Divide-by-1	—	—	○
			Divide-by-2	—	—	○
			Divide-by-8	—	—	○
			Divide-by-32	—	—	○
			Divide-by-64	—	—	○
			Divide-by-1024	—	—	○
			Divide-by-8192	—	—	○
		Output	Support for pulse output or PWM output with user-specified duty ratio	—	—	○
		Cascade connection operation	Support for use as 16-bit timer using cascade connection of 2 channels	—	—	○
		A/D conversion trigger	Support for generation of A/D converter conversion start trigger	—	—	○
		SCI baud rate clock generation	SCI5	—	—	○
			SCI6	—	—	○
			SCI12	—	—	—
		Event link function	Output	—	—	—
			Input	—	—	—
	Compare match timer (CMT)	Symbol		CMT	CMT	CMT
		Units	(16-bit × 2 channels) × number of units	2	2	2
		Count clock	Input count clock	PCLK	PCLK	PCLK
			Divide-by-8	○	○	○
			Divide-by-32	○	○	○
			Divide-by-128	○	○	○
			Divide-by-512	○	○	○
		Event link function	Output	—	—	—
			Input	—	—	—

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
A/D converters	12-bit A/D converter (S12AD)	Symbol		S12ADA	S12ADB	S12ADF
		Channels × units	Channels	4 channels × 2 units	4 channels × 2 units	5 channels × 2 units 12 channels × 1 unit
		Resolution	Bit width	12-bit	12-bit	12-bit
		Conversion time per channel	When A/D conversion clock When ADCLK = 50 MHz and AVCC0 = 4.0 V to 5.5 V	1.0 µs	1.0 µs	—
			When ADCLK = 40 MHz	—	—	1.0 µs
			When A/D conversion clock ADCLK = 25 MHz and AVCC0 = 3.0 V to 3.6 V	2.0 µs	2.0 µs	—
		Division ratio	A/D conversion clock	PCLK	ADCLK	ADCLK
			Divide-by-1	○	ADCLK is set by the clock generation circuit (CPG).	ADCLK is set by the clock generation circuit (CPG).
			Divide-by-2	○		
			Divide-by-4	○		
			Divide-by-8	○		
		Operating modes	Single mode	○	—	—
			Single-cycle scan mode	○	○	○
			Continuous scan mode	○	○	○
			Group scan mode	○	○	○
			Group priority control (group scan mode only)	—	○	○
			Group priority control groups	—	2	3
		Data register	For analog input	10	8	22
			Double data (for A/D conversion data duplication in double trigger mode)	2	1	1
			For A/D conversion data duplication in double trigger mode extended operation	—	2	2
			For temperature sensor	—	—	—
			For internal reference voltage	—	—	1
			For self-diagnostics	—	—	1
		Sample-and-hold function	Sample-and-hold function (simultaneous sampling)	○	○	○
		Variable sampling function	Support for per-channel setting of sampling time	○	○	○
		A/D conversion register	Support for an A/D conversion register for each input pin	○	○	○

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
A/D converters	12-bit A/D converter (S12AD)	Disconnection detection function	Analog input disconnection detection assist function	—	○	○
		A/D conversion data duplication function	Double data/double trigger mode	○	○	○
		A/D conversion start method	Triggering by software	○	○	○
			Triggering by multi-function timer pulse unit (MTU)	○	○	○
			Triggering by general PWM timer (GPT)	○	○	—
			Triggering by 8-bit timer (TMR)	—	—	○
			External triggering by ADTRG0# pin	○	○	○
			Triggering by temperature sensor	—	—	—
			Triggering by event link controller (ELC)	—	—	—
		A/D conversion accuracy	Support for specifying A/D data register bit accuracy (storage at 12-bit, 10-bit, or 8-bit accuracy)	○	○	— (12-bit fixed)
			Support for A/D data register format selection (flush-right or flush-left)	○	○	○
			A/D-converted value addition function	—	○	○
		Self-diagnostic functions	Internal self-diagnostics using analog input voltage (VREFL0)	○	○	○
			Internal self-diagnostics using analog input voltage (VREFH0 × 1/2)	○	○	○
			Internal self-diagnostics using analog input voltage (VREFH0 × 1)	○	○	○

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
A/D converters	12-bit A/D converter (S12AD)	Programmable gain amplifiers		3 channels × 2 units	3 channels × 2 units	4 channels (1 channel for unit 0 and 3 channels for unit 1)
		Input signal amplification function using programmable gain amplifier	Gain: 2.0×	○	○	○
			Gain: 2.5×	○	○	○
			Gain: 3.077×	○	○	○
			Gain: 3.636×	○	○	○
			Gain: 4.0×	○	○	○
			Gain: 4.444×	○	○	○
			Gain: 5.0×	○	○	—
			Gain: 5.714×	○	○	—
			Gain: 6.667×	○	○	—
			Gain: 10.0×	○	○	—
			Gain: 13.333×	○	○	—
Comparator	Comparator	Symbol		—	—	CMPC
		Comparators		3 channels × 2 units	3 channels × 2 units	4 channels
		Function settings	Low-level comparator	○	○	—
			High-level comparator	○	○	—
			Window comparator	○	○	—
		Response speed	REFH response time (tCR)	1 µs	500 ns	—
			REFL response time (tCF)	1 µs	500 ns	—
			[Comparator A] Comparator output delay time Falling edge VI = LVREF − 110 mV	—	—	—
			[Comparator A] Comparator output delay time Falling edge VI < LVREF − 1V	—	—	—
			[Comparator A] Comparator output delay time Rising edge VI = LVREF + 160 mV	—	—	—
			[Comparator A] Comparator output delay time Rising edge VI > LVREF + 1V	—	—	—

Type	Module/Function	Item	Description	RX62T [100-Pin Version]	RX63T [100-Pin Version]	RX24T [100-Pin Version]
Comparator	Comparator	Response speed	[Comparator B] Comparator output delay time VI = VREF + 100 mV	—	—	—
			[CMPC] VOD = 100 mV t CMPCTL.CDFS = 0 tcr	—	—	200 ns
			[CMPC] VOD = 100 mV t CMPCTL.CDFS = 0 tcf	—	—	200 ns

4. Sample Code

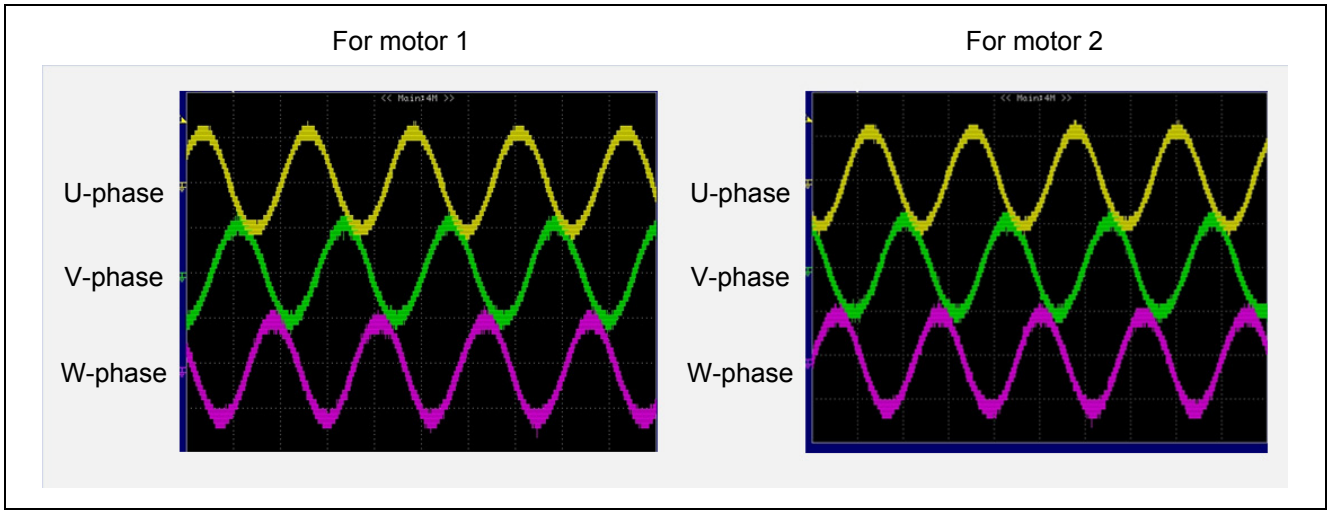
4.1 Summary

The sample code is provided to illustrate, when creating a program that uses the RX24T to control two motors, how to generate left-right symmetric (for motor 2) and left-right asymmetric (for motor 1) PWM output using complementary PWM mode 3 of the MTU; how to make settings for A/D conversion using the group scan function, with different timings for group A, group B, and group C; and how to make settings for the protection functions.

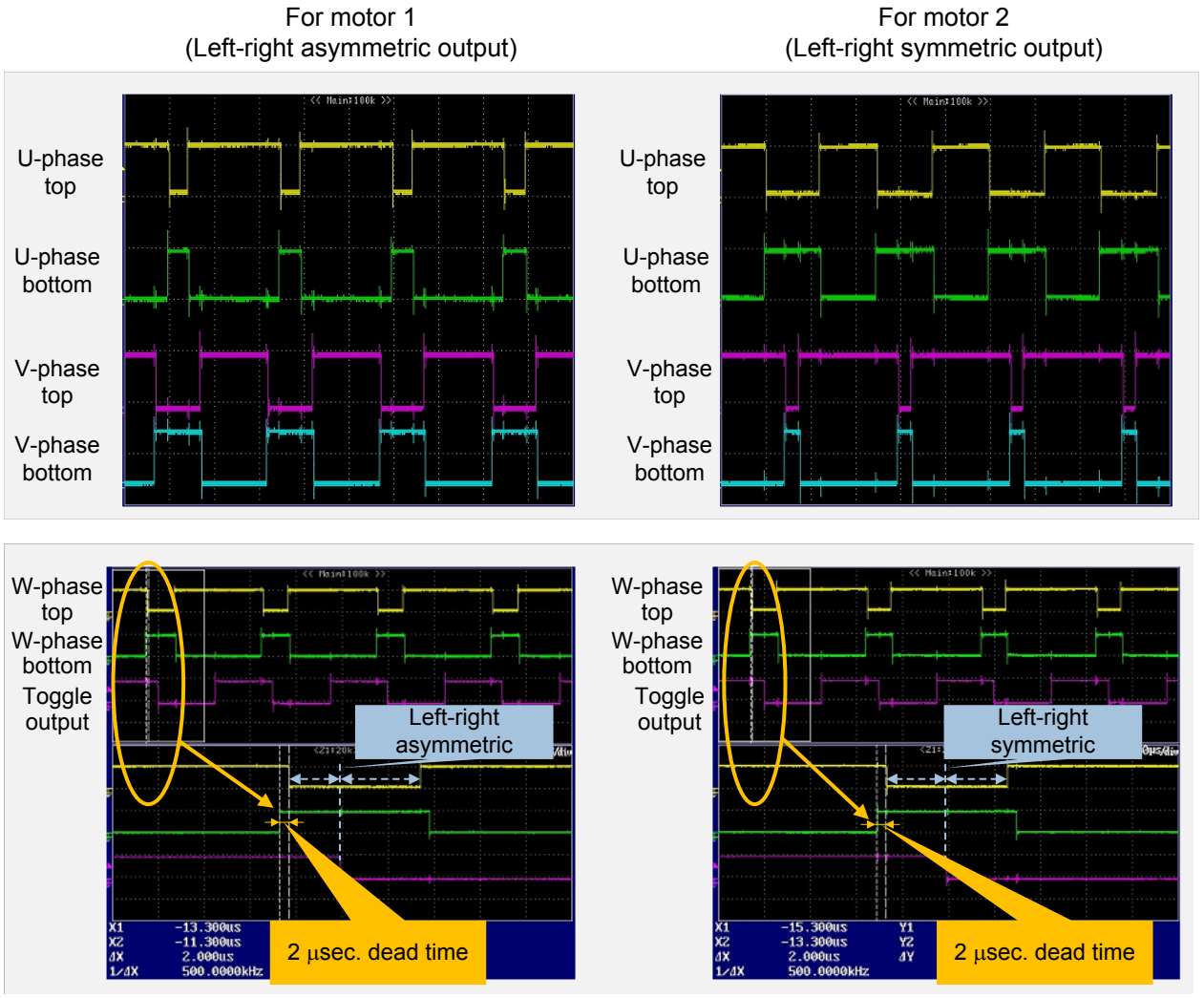
Note that the settings used in the sample code are such that the data results in sine waves when each PWM output phase undergoes CR filtering. The output waveforms are shown below.

The sample code is intended only for reference, and Renesas makes no guarantee regarding its operation. When making use of the sample code, make sure to perform sufficient testing in a suitable environment.

< Sine Wave After CR Filtering >



< PWM Output Waveforms >



Note: Toggle output: Toggles waveform output in synchronization with the PWM cycle.

4.2 Development and Operation Confirmation Environment

The development and operation confirmation environment of the sample code is summarized below.

< CS+ >

tem	Description
MCU used	R5F524TAADFP (Package: PLQP0100KB-A)
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation CS+ for CC V4.01.00 [05 Sep 2016]
C compiler	Renesas Electronics Corporation CC - RX V2.05.0
	Compiler options: -isa=rxv2 –fpu -lang=c99 -include=Include -output=obj -debug -optimize=max –speed -nologo -Xcref=%BuildModeName%
iodefine.h version	Version 1.1 (2015-07-13)
Board used	Renesas Starter Kit for RX24T (Product No.: RTK500524TC01000BR)

< e^2 studio >

Item	Description
MCU used	R5F524TAADFP (Package: PLQP0100KB-A)
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation e^2studio Version: 5.2.0.020
C compiler	Renesas Electronics Corporation CC - RX V2.05.0
	Compiler options: -isa=rxv2 –fpu -include="C:\PROGRA~1\Renesas\RX\2_5_0/include" -debug -optimize=max -speed -nologo -define=__RX -nomessage -alias=noansi
iodefine.h version	Version 1.1 (2015-07-13)
Board used	Renesas Starter Kit for RX24T (Product No.: RTK500524TC01000BR)
Remarks	Sample code created with reference to Software Migration Guide: CS+ to e^2 studio Migration.

4.3 Peripheral Functions

The peripheral function used in the sample code and their applications are listed below.

Peripheral Function	Application
Ports	• Test port output (for processing timing measurement) • SW1 input (PWM output start switch) • SW2 input (PWM output stop switch) • ADST bit (A/D conversion start bit) status output • A/D conversion start request frame synchronization signal (ADSM0 and ADSM1) output
Multi-function timer pulse unit 3 (MTU3d)	• Toggle waveform output synchronized with the PWM cycle • Complementary PWM output (motor 1: left-right asymmetric, motor 2: left-right symmetric)
12-bit A/D converter (S12ADF)	For A/D value acquisition (acquisition of shunt current, bus voltage, and other A/D values)
D/A converter for generating comparator C reference voltage (DA)	Generates reference input voltage for comparator C (CMPC).
Comparator C (CMPC)	Outputs comparator detection result when overvoltage is detected.
Port output enable 3 (POE3b)	Puts PWM output pins in high-impedance state when overcurrent or overvoltage is detected.
Voltage detection circuit (LVDAb)	Applies a reset when a voltage drop is detected.

(1) Ports

1. Test port output (for processing timing measurement)
   Outputs high at start, and low at finish, of MTU3 or MTU6 peak interrupt processing.
2. SW1 input (PWM output start switch) and SW2 input (PWM output stop switch)
   Starts and stops PWM output in response to SW1 and SW2 input, respectively.
3. ADST bit (A/D conversion start bit) status output
   Used to check the A/D conversion status.
4. A/D conversion start request frame synchronization signals (ADSM0 and ADSM1)
   Used to check the timing of A/D conversion start request signal generation.

(2) Multi-function timer pulse unit 3 (MTU3d)

Toggles waveform output in synchronization with the PWM cycle (MTIOC3A and MTIOC6A).
Uses complementary PWM mode 3 to generate six-phase PWM output with triangle-wave modulation and dead time (motor 1: MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, and MTIOC4D; motor 2: MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D).
The sample code generates PWM output with a 6 µsec. cycle, low-active, and 2 µsec. dead time.
For motor 1, the double buffer function is enabled and different values are set for buffer A and buffer B , resulting in left-right asymmetric PWM output.
For motor 2, the double buffer function is disabled, resulting in left-right symmetric PWM output.

(3) 12-bit A/D converter (S12ADF)

The group scan function is used, with the shunt current value assigned to group A and the bus voltage value and other A/D values assigned to group C, and A/D conversion is performed with different timing for each.
For motor 1, group A is set to double trigger mode, A/D conversion takes places with two different timings on the selected channel, and the converted values are stored in different registers (redundant registers for A/D data).
For motor 2, the channel-dedicated sample-and-hold function is used on group A, and sampling is performed on three channels with the same timing.

(4) D/A converter for generating comparator C reference voltage (DA)
VREF is used as the input, and a value equal to 90% of the input value is output as the comparator reference voltage.

(5) Comparator C (CMPC)
The output from the D/A converter for generating comparator C reference voltage (DA) is used as the input, and when it exceeds the CMPC analog input voltage, the comparator detection result is output and a POE control signal is output.

(6) Port output enable 3 (POE3b)
Overcurrent detection (falling-edge detection on POE0# or POE4 pin), comparator detection, or output short detection occurs, the pins on which PWM output is in progress are put into the high-impedance state.

(7) Voltage detection circuit (LVDAb)
A reset is generated when the power supply voltage drops to 2.51 V or less. The reset source can be acquired from reset status register 0 (RSTSR0).

4.4 Sample Code Specifications

The basic specifications of the sample code are listed below.

No.	Category	Item		Setting
1	Clock settings	Resonator		20 MHz
		PCLKA (max. 40 MHz)		80 MHz
		PCLKB (max. 40 MHz)		40 MHz
		PCLKD (max. 40 MHz)		40 MHz
		ICLK (max. 40 MHz)		80 MHz
		FCLK (max. 32 MHz)		20 MHz
		Memory wait cycles		Wait cycles enabled
		ROM cache		Cache operation enabled
2	Ports	SW1		PWM output start
		SW2		PWM output stop
3	MTU3	Operation mode		Complementary PWM mode 3 (transfer at peaks and/or troughs) (MTU3 and MTU4, MTU6 and MTU7)
		Double buffer function		Enabled (MTU3 and MTU4 only)
		Carrier frequency		8 KHz
		Dead time		2 µsec.
		PWM active output		Low-active
		PWM output values (MTU3 and MTU4)		Use table that generates left-right asymmetric (6 µsec. gap between left and right) output of U-phase, V-phase, and W-phase (motor 1).
		PWM output values (MTU6 and MTU7)		Use table that generates left-right symmetric output of U-phase, V-phase, and W-phase (motor 2).
4	ADC	Unit 0	Double trigger mode	Enabled
			Group scan mode	Enabled
				Group A: AN002 Group B: AN001 Group C: AN003
			Group priority control	Enabled
			A/D conversion triggers	Group A: A/D conversion start request (TRG4AN) at MTU4.TCNT down-count, A/D conversion start request (TRG4BN) at MTU4.TCNT down-count Group B: MTU3.TGRA compare match/input capture Group C: Continuous scan
			Buffer register update timing	MTU4.TADCORA and MTU4.TADCORB updated from cycle set buffer register at peaks
			ADST bit status output (ADST0)	Enabled
		Unit 1	Double trigger mode	Disabled
			Group scan mode	Enabled
				Group A: AN100, AN101, AN102 Group B: AN103 Group C: AN116

No.	Category	Item		Setting
4	ADC	Unit 1	Group priority control	Enabled
			A/D conversion triggers	Group A: MTU7.TGRA compare match/input capture, or MTU7.TCNT underflow (trough) in complementary PWM mode Group B: MTU6.TGRA compare match/input capture Group C: Continuous scan
			Channel-dedicated sample-and-hold	Enabled: AN100, AN101, AN102
			Sampling time	0.4 µsec.
			ADST bit status output (ADST1)	Enabled
		Unit 2	Double trigger mode	Disabled
			Group scan mode	Enabled
				Group A: AN200, AN201, AN202 Group B: AN203, AN204, AN205 Group C: AN206, AN207, AN208, AN209, AN210, AN211
			Group priority control	Enabled
			A/D conversion triggers	Group A: MTU3.TGRA compare match/input capture Group B: MTU6.TGRA compare match/input capture Group C: Continuous scan
		Common	AD conversion start request frame synchronization signal output (ADSM0)	Compare match of MTU4.TADCORB and MTU4.TCNT
			AD conversion start request frame synchronization signal output (ADSM1)	MTU7.TGRA compare match/input capture, or MTU7.TCNT underflow (trough) in complementary PWM mode
5	Comparator	Reference voltage		Input by on-chip D/A converter
		Operation when detected		POE control signal output
				Comparator external pin output enabled
6	POE	Detection condition		POE#0 or POE#4 falling edge detection
				Comparator detection
		Operation when detected		Put MTU ports in high-impedance state
7	LVD	Detection condition		Voltage drop (2.51 V) detection (using voltage monitoring 0)
		Operation when detected		Reset

4.5 Hardware

4.5.1 Pins Used

The pins used by the sample code are listed below.

Pin Name	Pin	I/O	Description
MTIOC3B	P71	Output	PWM output pin 1
MTIOC3D	P74	Output	PWM output pin 1’ (PWM output 1 negative-phase waveform output)
MTIOC4A	P72	Output	PWM output pin 2
MTIOC4C	P75	Output	PWM output pin 2’ (PWM output 2 negative-phase waveform output)
MTIOC4B	P73	Output	PWM output pin 3
MTIOC4D	P76	Output	PWM output pin 3’ (PWM output 3 negative-phase waveform output)
MTIOC6B	P95	Output	PWM output pin 4
MTIOC6D	P92	Output	PWM output pin 4’ (PWM output 4 negative-phase waveform output)
MTIOC7A	P94	Output	PWM output pin 5
MTIOC7C	P91	Output	PWM output pin 5’’ (PWM output 5 negative-phase waveform output)
MTIOC7B	P93	Output	PWM output pin 6
MTIOC7D	P90	Output	PWM output pin 6’ (PWM output 6 negative-phase waveform output)
ADST0	PD6	Output	ADST bit status output pin 1
ADST1	P00	Output	ADST bit status output pin 2
ADSM0	PB2	Output	A/D conversion start request frame synchronization signal pin 1
ADSM1	PB1	Output	A/D conversion start request frame synchronization signal pin 2
COMP0	P24	Output	Comparator output pin
—	P22	Output	Test port output pin 1
—	PB3	Output	Test port output pin 2
MTIOC3A	P11	Output	Toggle output synchronized with the PWM cycle pin 1
MTIOC6A	PA1	Output	Toggle output synchronized with the PWM cycle pin 2
AN001	P41	Input	Motor 1 bus voltage detection A/D pin
AN002	P42	Input	Motor 1 shunt current detection AD pin
AN003	P43	Input	Motor 1 group B A/D pin
AN100	P44	Input	Motor 2 shunt current detection A/D pin 1
AN101	P45	Input	Motor 2 shunt current detection A/D pin 2
AN102	P46	Input	Motor 2 shunt current detection A/D pin 3
AN103	P46	Input	A/D pin motor 2 group B A/D pin
AN116	P21	Input	Motor 2 bus voltage detection
AN206	P50	Input	Unit 2 group C A/D pin 1
AN207	P51	Input	Unit 2 group C A/D pin 2
AN208	P52	Input	Unit 2 group C A/D pin 3
AN209	P53	Input	Unit 2 group C A/D pin 4
AN210	P54	Input	Unit 2 group C A/D pin 5
AN211	P55	Input	Unit 2 group C A/D pin 6
AN200	P60	Input	Unit 2 group A A/D pin 1
AN201	P61	Input	Unit 2 group A A/D pin 2
AN202	P62	Input	Unit 2 group A A/D pin 3
AN203	P63	Input	Unit 2 group B A/D pin 1
AN204	P64	Input	Unit 2 group B A/D pin 2
AN205	P65	Input	Unit 2 group B A/D pin 3
—	P10	Input	SW1: PWM output start
—	P02	Input	SW2: PWM output stop
POE0#	P70	Input	POE0# input pin
POE4#	P96	Input	POE4# input pin
CMPC00	P40	Input	Comparator input pin

4.6 Software

4.6.1 Operation Overview

The sample code starts PWM output when SW1 is pressed following a reset, and stops PWM output when SW2 is pressed.

The 8 kHz carrier frequency of the complementary PWM output waveforms has dead time of 2 µsec.

The complementary PWM output for motor 1 consists of three-phase left-right asymmetric (6 µsec. gap between left and right) waveforms output by MTU3 and MTU4.

The complementary PWM output for motor 2 consists of three-phase left-right symmetric waveforms output by MTU6 and MTU7.

The MTU and 12-bit A/D converter are used in combination to perform A/D conversion processing.

The group scan function is used with the three 12-bit A/D converter units to accomplish A/D conversion using different timings for group A, group B, and group C. The A/D conversion to obtain the shunt current for motor 1 uses the double trigger mode on group A of unit 0, A/D conversion takes places with two different timings on the selected channel, and the converted values are stored in different registers (redundant registers for A/D data).

The A/D conversion to obtain the shunt current for motor 2 uses simultaneous sampling on three channels at the underflow (trough) of MTU7.TCNT on group A of unit 1.

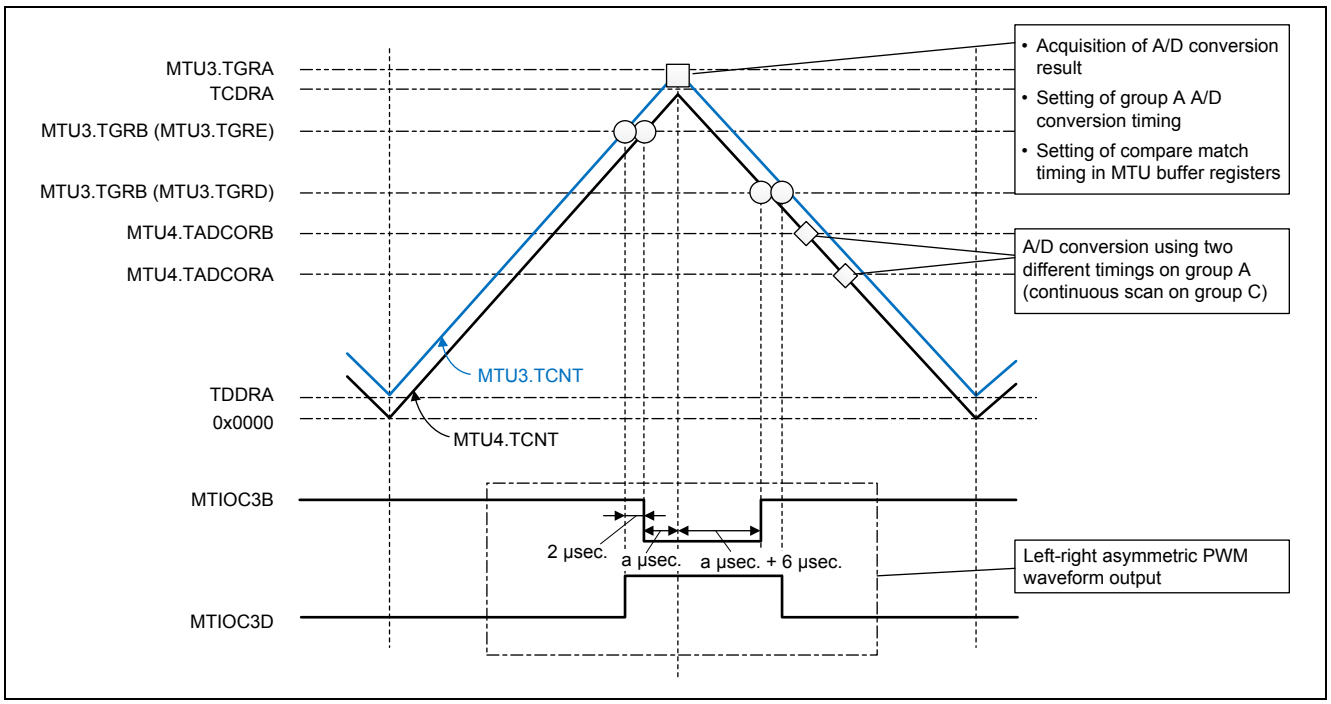
The POE function puts the PWM output pins in the high-impedance state when POE0# or POE4# input occurs and when comparator output is detected.

The LVD function generates a reset when the voltage drops below 2.51 V.

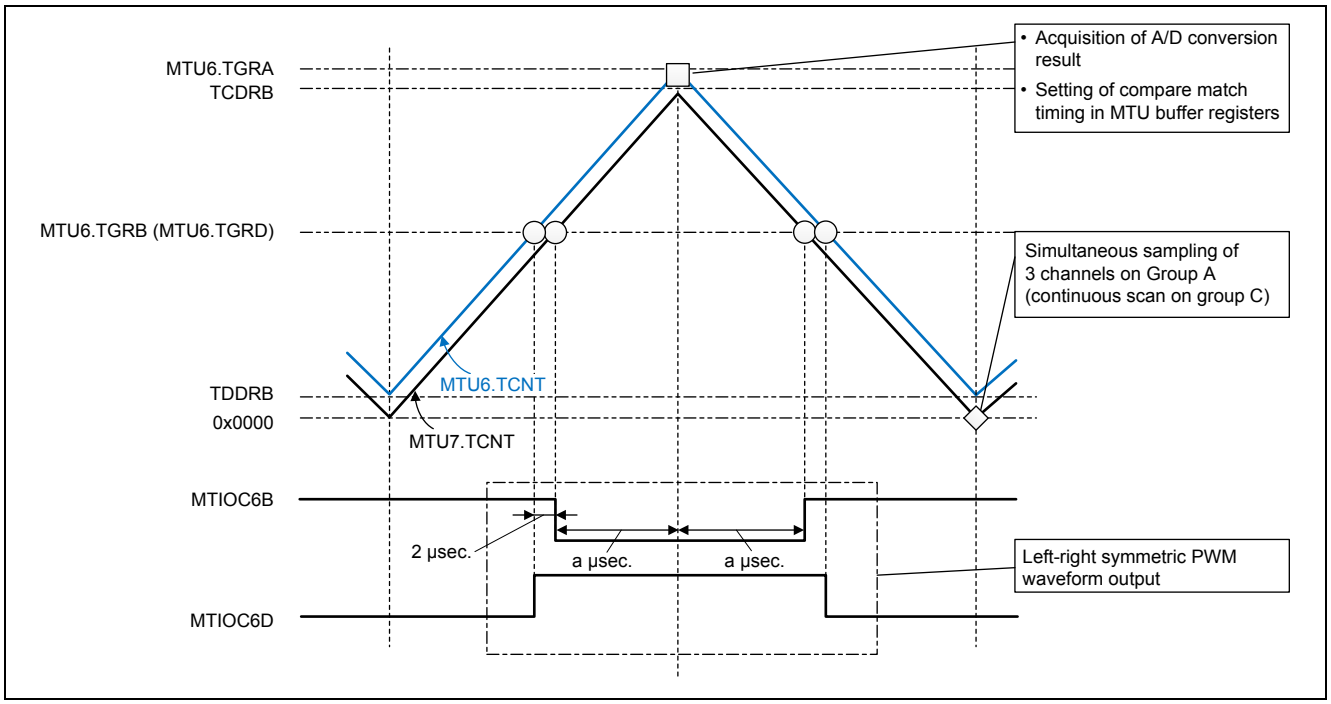
In addition, reset status register 0 (RSTSR0) can be used to obtain the reset source.

The A/D conversion timing and PWM output of the sample code (for motor 1 and motor 2) are shown below.

< For motor 1 >



< For motor 2 >



4.6.2 File Configuration

File Name	Description	Remarks
app.h	reg.c and app.c header file	
reg.c	Register access processing	
app.c	Main processing routine, setting of PWM duty	
intprg.c	Interrupt handler	
dbsct.c	Section definition file	
vecttbl.c	Vector table definition file	
iodefine.h	Register definition header file	
typedefine.h	Type definition header file	
vect.h	Vector definition header file	
stacksct.h	Stack definition header file	

4.6.3 List of Constants

Constants are listed below.

Constant Name	Setting Value	Description
DEF_FLAG_OFF	0	Flag state: off
DEF_FLAG_ON	1	Flag state: on
DEF_CLOCK_FREQ_Hz	80000000	Clock frequency
DEF_CARRIER_FREQ_Hz	8000	PWM cycle
DEF_DEADTIME_CNT_NUM	DEF_CLOCK_FREQ_NUM * 2 / 1000000	Dead time setting value
DEF_CARRIER_COUNT_NUM	DEF_CLOCK_FREQ_NUM/ DEF_CARRIER_FREQ_NUM	PWM cycle count value
DEF_HALF_CARRIER_COUNT_NUM	DEF_CARRIER_COUNT_NUM / 2	Value equal to 1/2 of PWM cycle count value
MTU_AD_GET_TIMING1	600	Shunt current acquisition timing 1
MTU_AD_GET_TIMING2	4500	Shunt current acquisition timing 2
DEF_PWM_TABLE_MAX	360	PWM table element count

Constant tables are listed below.

Constant Name	Description
g_table_pwm_duty_u_1	U-phase PWM output timing table 1
g_table_pwm_duty_u_2	U-phase PWM output timing table 2 (single-shunt only)
g_table_pwm_duty_v_1	V-phase PWM output timing table 1
g_table_pwm_duty_v_2	V-phase PWM output timing table 2 (single-shunt only)
g_table_pwm_duty_w_1	W-phase PWM output timing table 1
g_table_pwm_duty_w_2	W-phase PWM output timing table 2 (single-shunt only)

4.6.4 List of Variables

Global variables are listed below.

Type	Variable Name	Description
unsigned char	g_val_reset_fact	For reset source storage
unsigned short	g_val_pwm_duty_table_case_num	Motor 1 PWM duty table setting count
unsigned short	g_val_pwm_duty_table_case_num2	Motor 2 PWM duty table setting count
unsigned short	g_val_dc_voltage	For unit 0 bus voltage A/D storage (group C) (AN001)
unsigned short	g_val_dc_voltage2	For unit 1 bus voltage A/D storage (group C) (AN116)
unsigned long	g_val_enable_flag	PWM control flag
unsigned short	g_val_shunt_ad_1	For unit 0 shunt current A/D value 1 storage (group A) (single-shunt) (AN002)
unsigned short	g_val_shunt_ad_2	For unit 0 shunt current A/D value 2 storage (group A) (single-shunt) (AN002)
unsigned short	g_val_ad_gb_an003	For unit 0 group B A/D value storage (AN003)
unsigned short	g_val_shunt_ad2_1	For unit 1 shunt current A/D value 1 storage (group A) (3-shunt) (AN100)
unsigned short	g_val_shunt_ad2_2	For unit 1 shunt current A/D value 2 storage (group A) (3-shunt) (AN101)
unsigned short	g_val_shunt_ad2_3	For unit 1 shunt current A/D value 3 storage (group A) (3-shunt) (AN102)
unsigned short	g_val_ad_gb_an103	Unit 1 group B A/D value storage (AN103)
unsigned short	g_val_ad_ga_an200	Unit 2 group A A/D value 1 storage (AN200)
unsigned short	g_val_ad_ga_an201	Unit 2 group A A/D value 2 storage (AN201)
unsigned short	g_val_ad_ga_an202	Unit 2 group A A/D value 3 storage (AN202)
unsigned short	g_val_ad_gb_an203	Unit 2 group B A/D value 1 storage (AN203)
unsigned short	g_val_ad_gb_an204	Unit 2 group B A/D value 2 storage (AN204)
unsigned short	g_val_ad_gb_an205	Unit 2 group B A/D value 3 storage (AN205)
unsigned short	g_val_ad_gc_an206	Unit 2 group C A/D value 1 storage (AN206)
unsigned short	g_val_ad_gc_an207	Unit 2 group C A/D value 2 storage (AN207)
unsigned short	g_val_ad_gc_an208	Unit 2 group C A/D value 3 storage (AN208)
unsigned short	g_val_ad_gc_an209	Unit 2 group C A/D value 4 storage (AN209)
unsigned short	g_val_ad_gc_an210	Unit 2 group C A/D value 5 storage (AN210)
unsigned short	g_val_ad_gc_an211	Unit 2 group C A/D value 6 storage (AN211)

4.6.5 Functions

Functions are listed below.

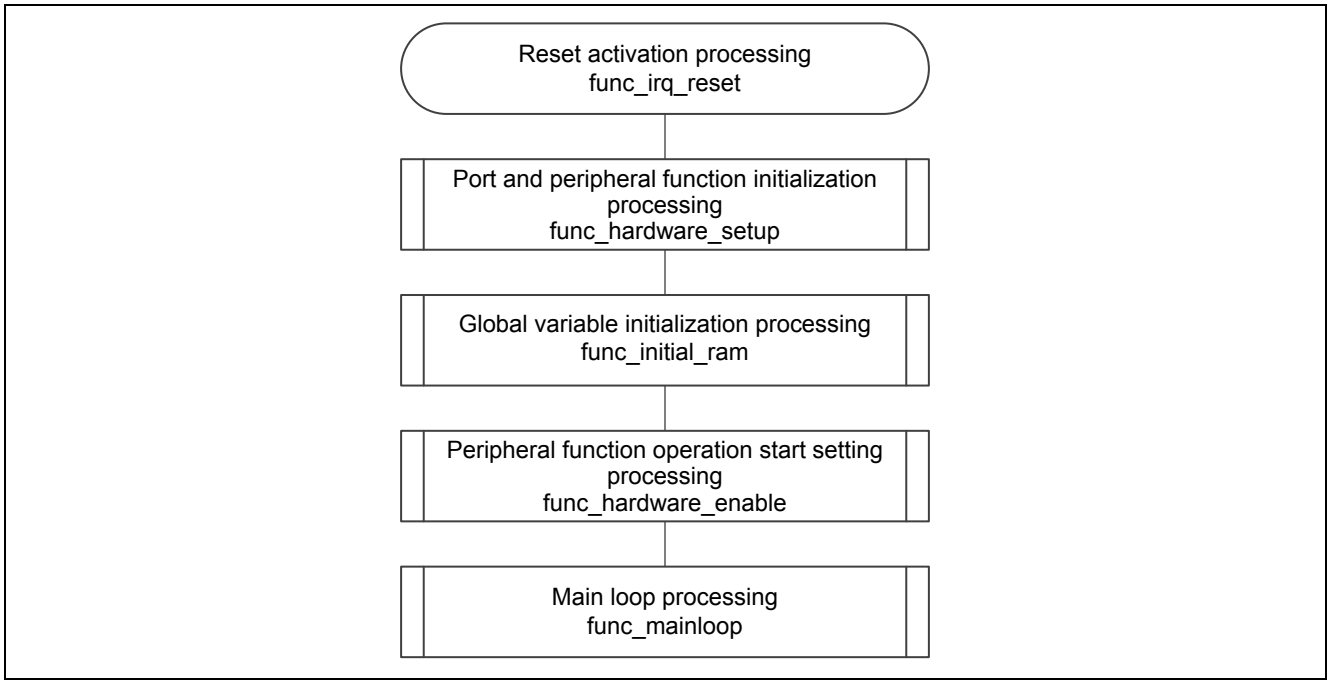
File	Function Name	Description
app.c	func_mainloop	Main loop processing
app.c	func_initial_ram	Global variable initialization processing
app.c	func_pwm_crest_1shunt	Motor 1 PWM output duty setting processing
app.c	func_pwm_crest_3shunt	Motor 2 PWM output duty setting processing
app.c	func_disable_pwm	MTU count stop processing
reg.c	func_hardware_setup	Port and peripheral function initialization processing
reg.c	func_hardware_enable	Peripheral function operation start setting processing
reg.c	func_irq_reset	Reset activation processing
reg.c	func_timercount_crest_isr	Motor 1 MTU3 TGIA3 interrupt handler (peak interrupt handler)
reg.c	func_ timercount_crest2_isr	Motor 2 MTU6 TGIA6 interrupt handler (peak interrupt handler)
reg.c	func_ ipm_fault_isr	POE OEI1 interrupt handler (POE0)
reg.c	func_ ipm_fault2_isr	POE OEI2 interrupt handler (POE4)
reg.c	func_ ad2_isr	AD converter unit 2 group C scan end interrupt handler
reg.c	func_set_ad_timing_2channel	Motor 1 A/D conversion timing setting processing
reg.c	func_set_pwm_to_io_port	MTU output disable processing
reg.c	func_set_io_port_to_pwm	MTU output enable processing
reg.c	func_set_pwm_duty_count_1	Motor 1 MTU buffer register setting processing
reg.c	func_set_pwm_duty_count_2	Motor 1 MTU double buffer register setting processing
reg.c	func_set_pwm_duty_count2_1	Motor 2 MTU buffer register setting processing
reg.c	func_reset_pwm_duty_count	Motor 1 MTU buffer register/double buffer register initial setting processing
reg.c	func_reset_pwm_duty_count2	Motor 2 MTU buffer register initial setting processing
reg.c	func_set_testport_on	Debug port 1 output on processing
reg.c	func_set_testport_off	Debug port 1 output off processing
reg.c	func_set_testport2_on	Debug port 2 output on processing
reg.c	func_set_testport2_off	Debug port 2 output off processing

4.7 Flowcharts

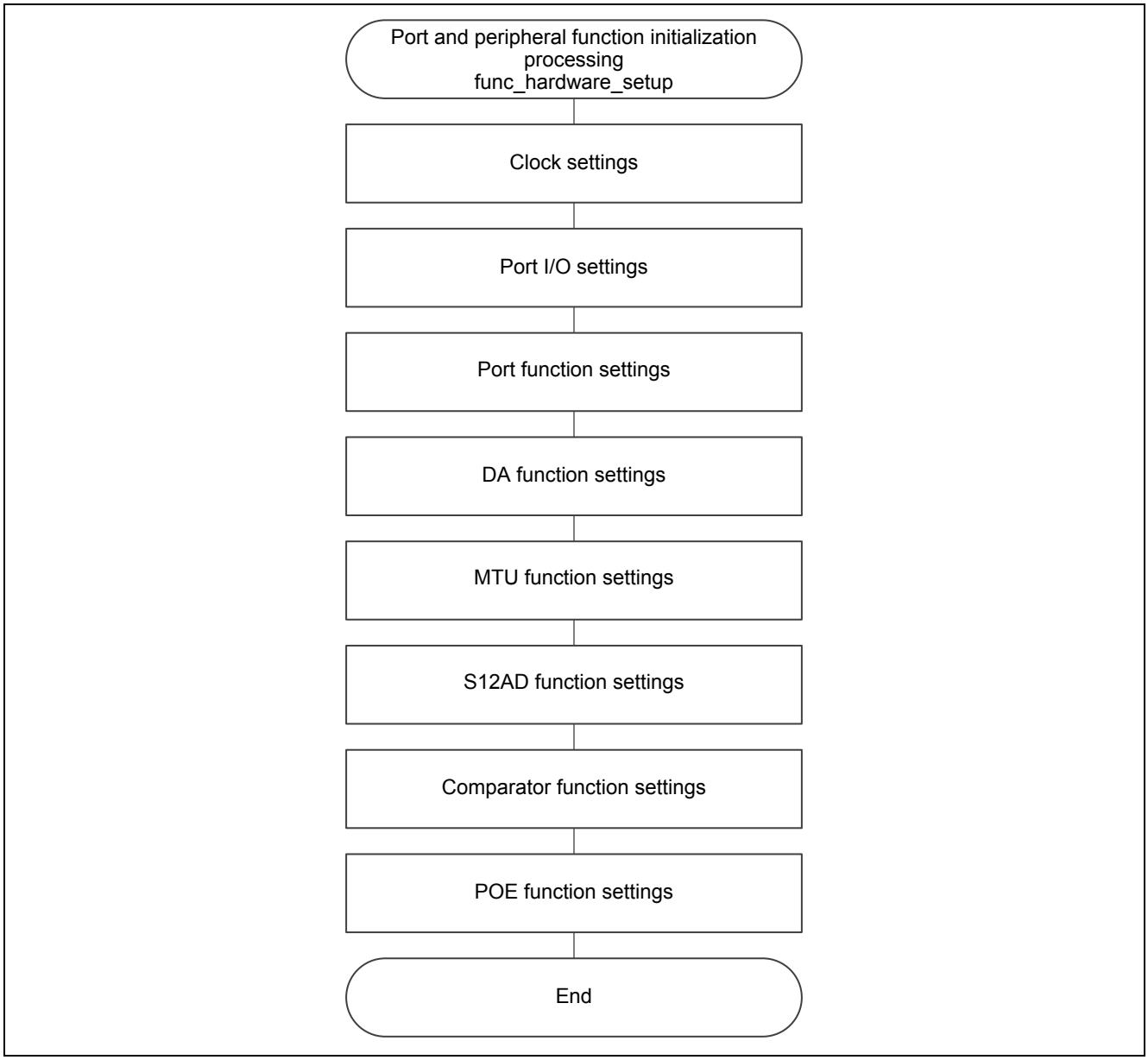
4.7.1 Activation Processing

Flowcharts of activation processing are shown below.

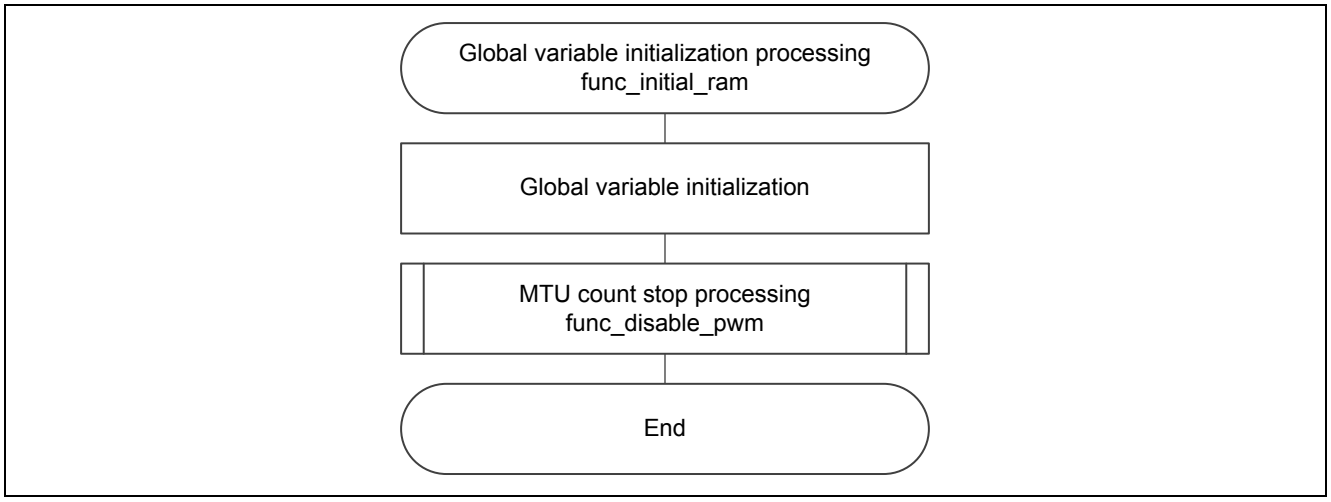
(1) Reset Activation Processing



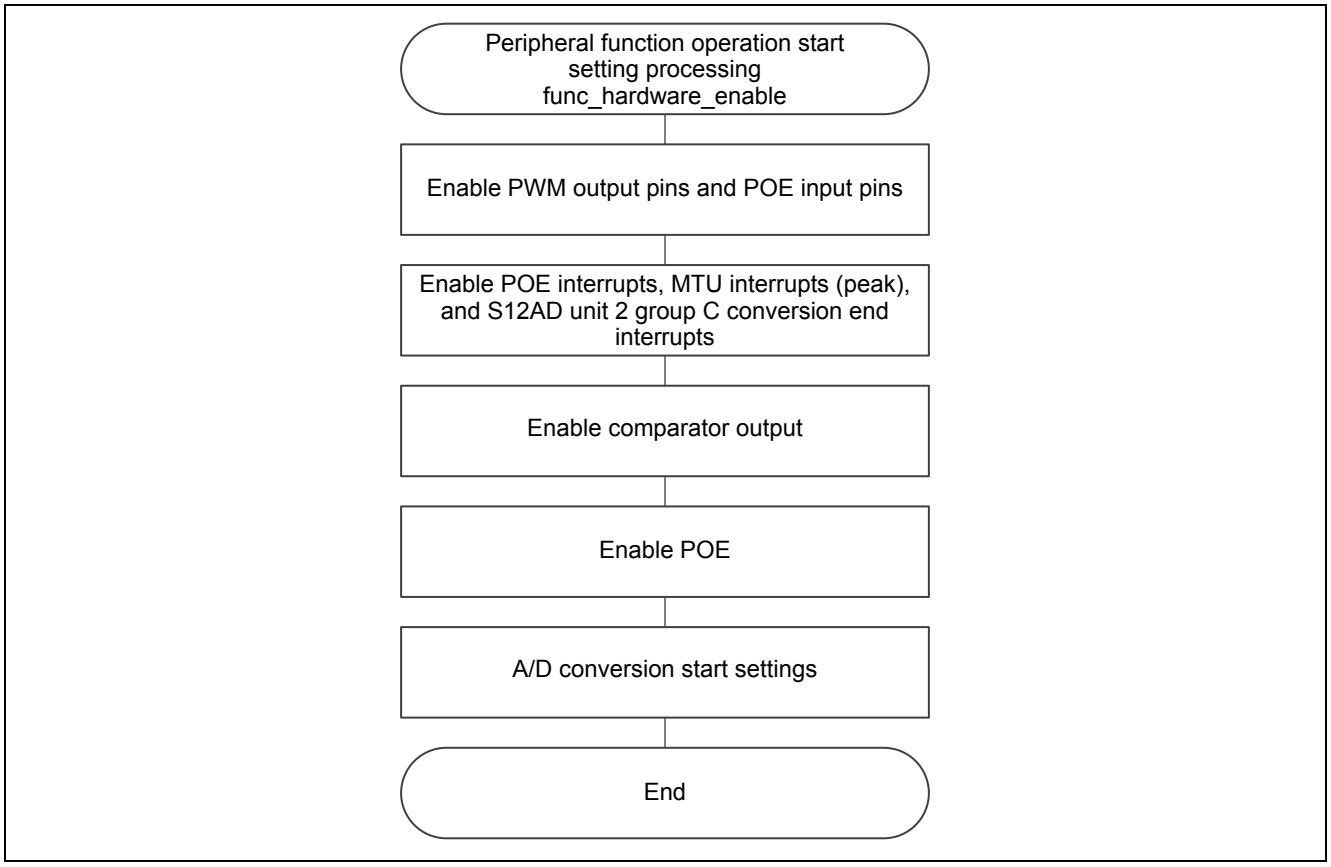
(2) Port and Peripheral Function Initialization Processing



(3) Global Variable Initialization Processing



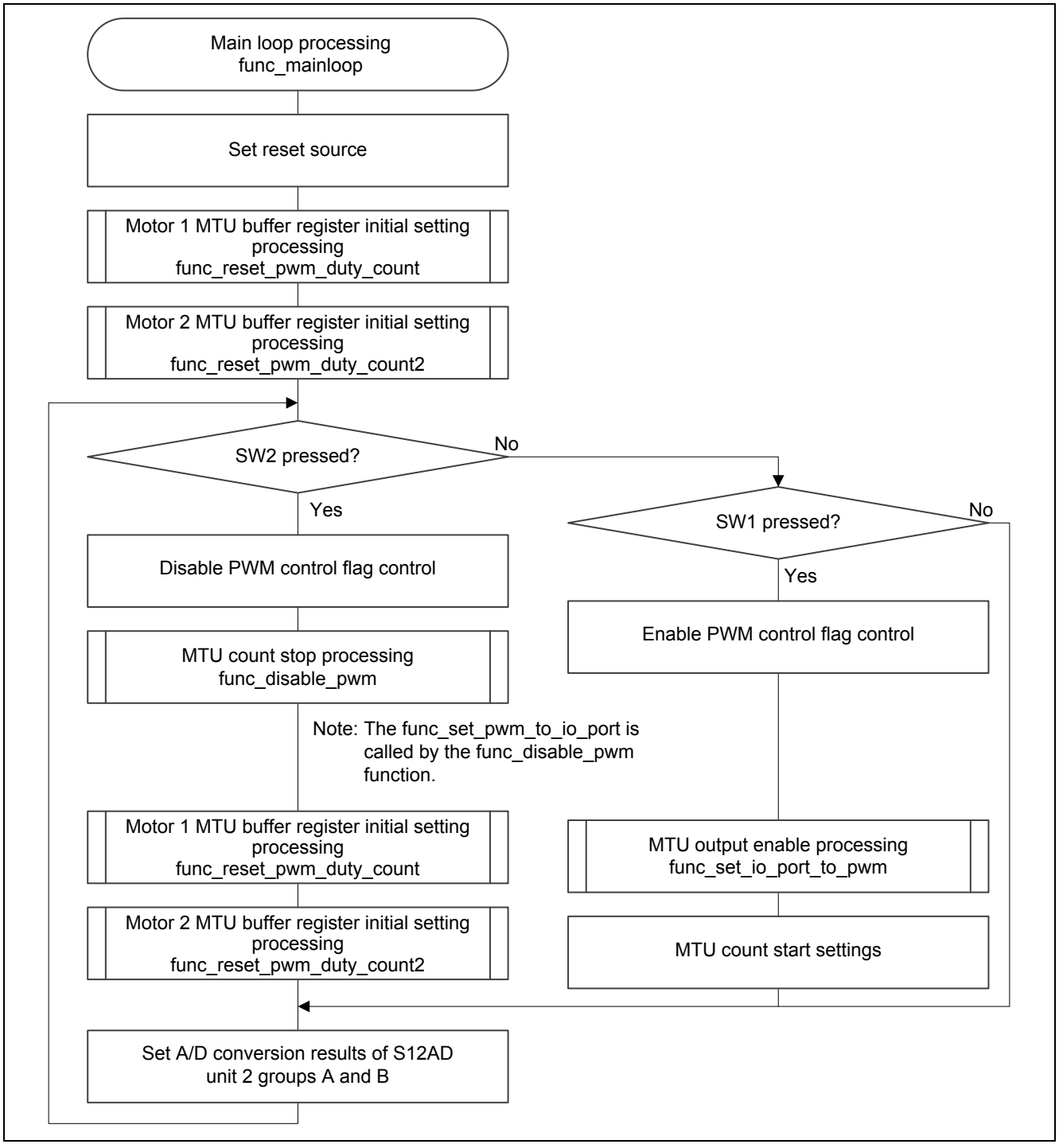
(4) Peripheral Function Operation Start Setting Processing



4.7.2 Main Processing Routine

A flowchart of the main processing routine is shown below.

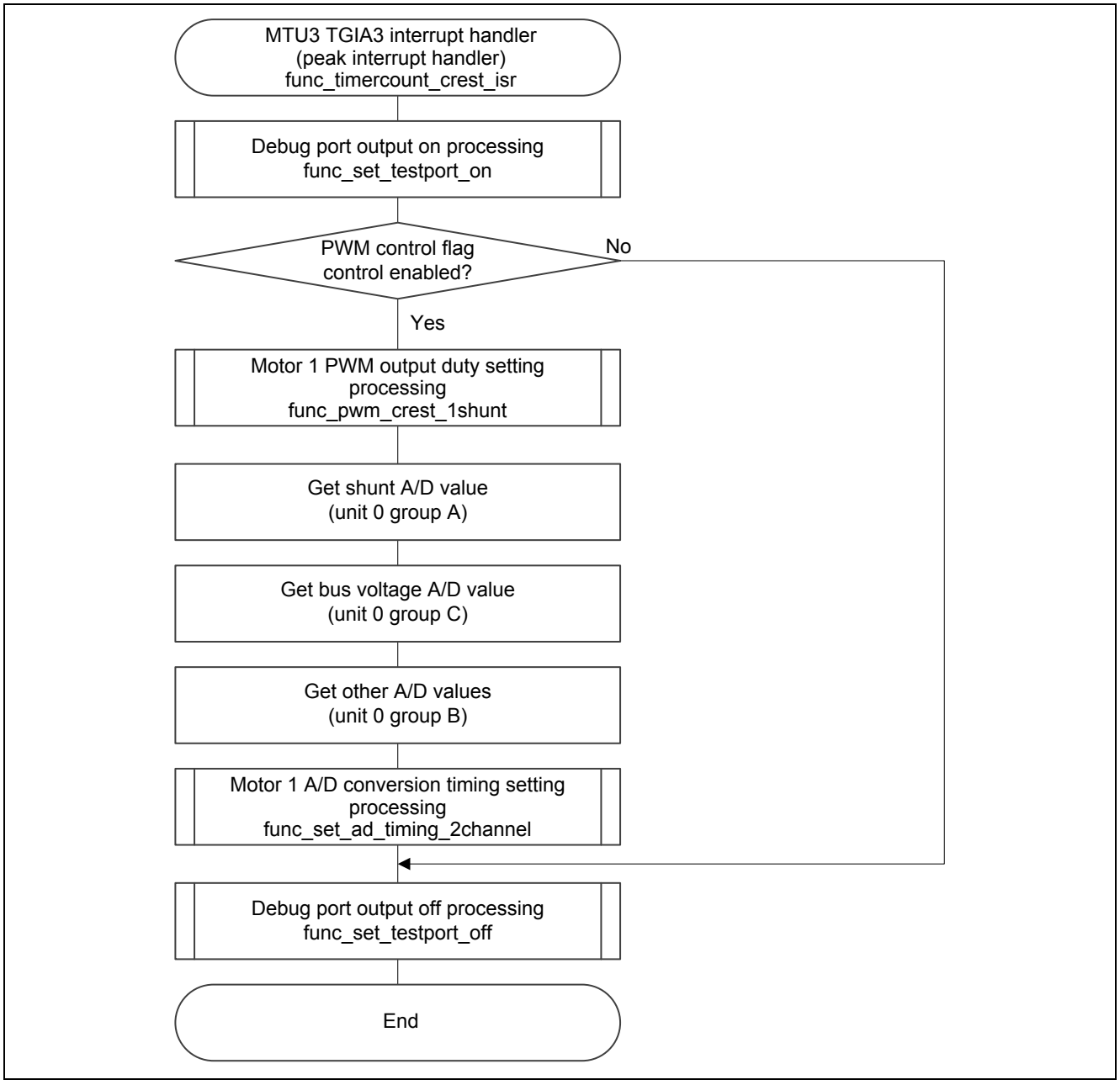
(1) Main Loop Processing



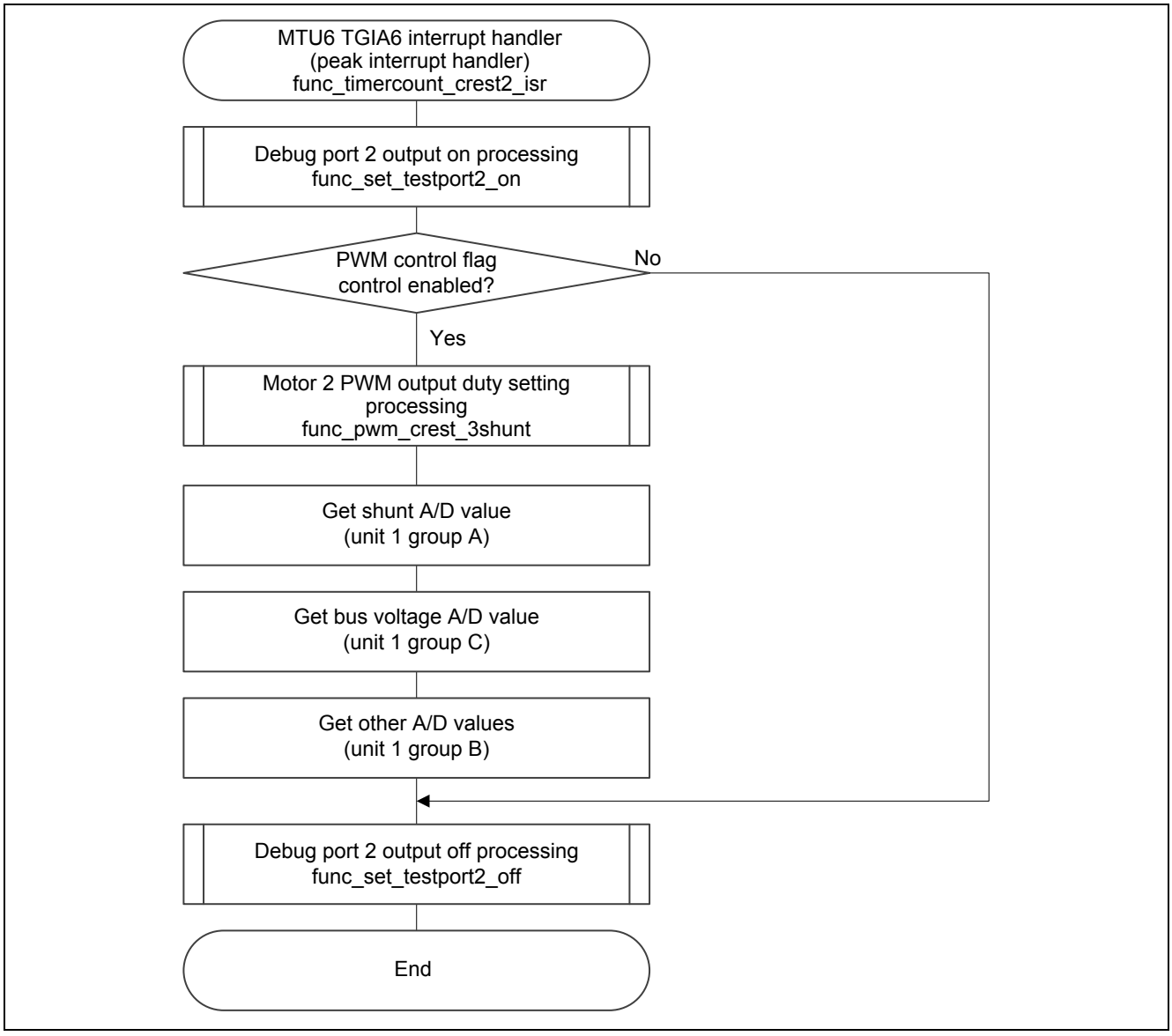
4.7.3 Interrupt Handlers

Flowcharts of the interrupt handlers are shown below.

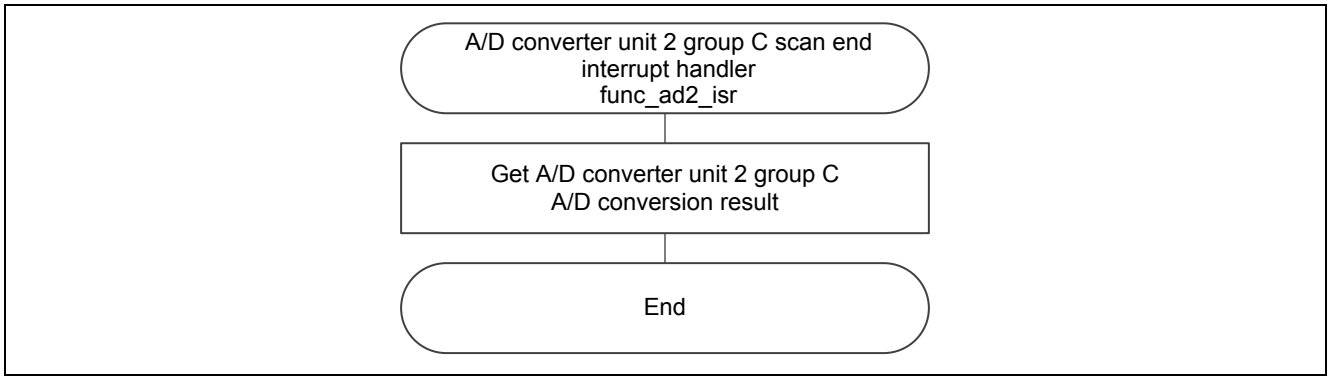
(1) Motor 1 MTU3 TGIA3 Interrupt Handler (Peak Interrupt Handler)



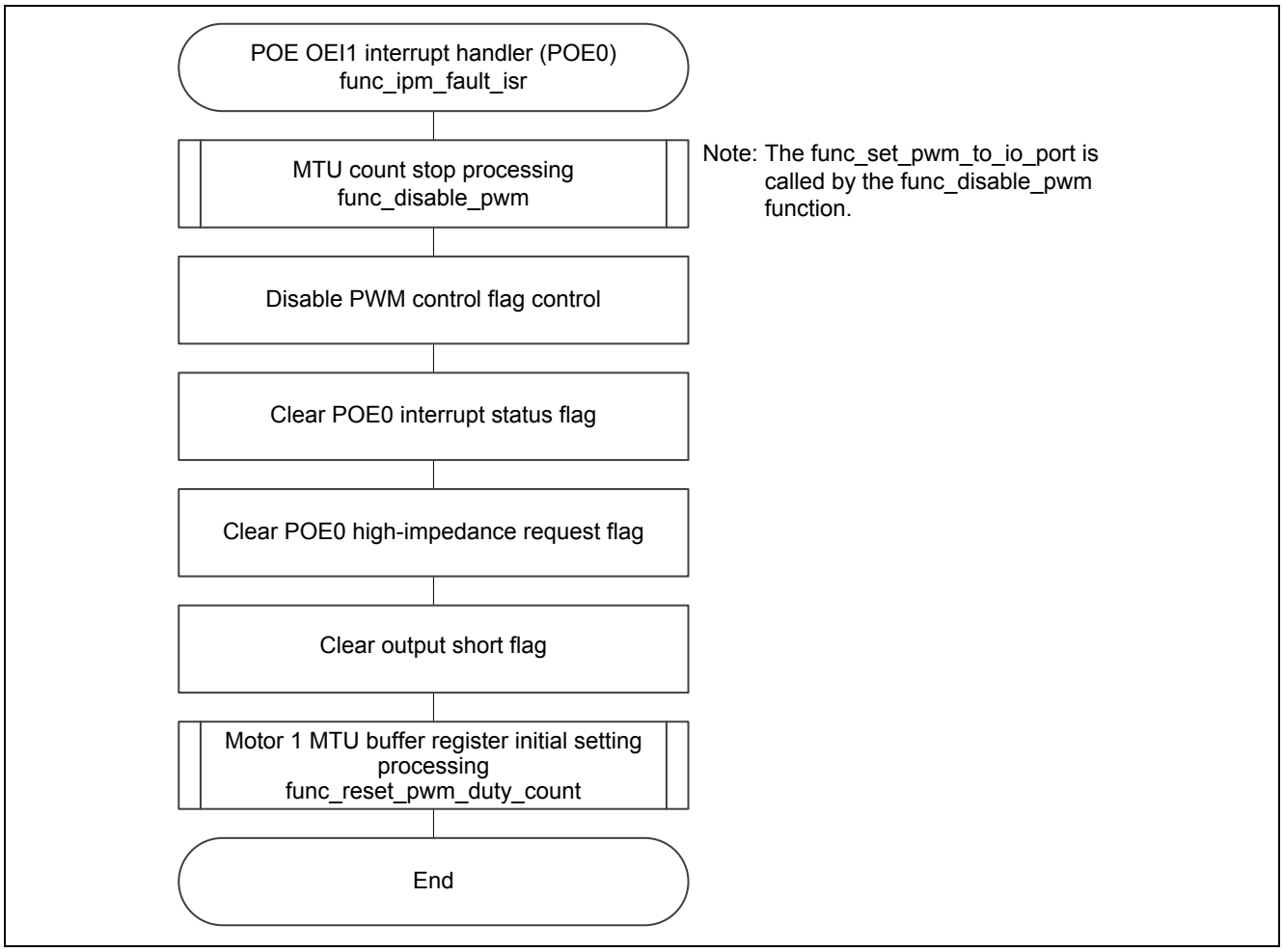
(2) Motor 2 MTU6 TGIA6 Interrupt Handler (Peak Interrupt Handler)



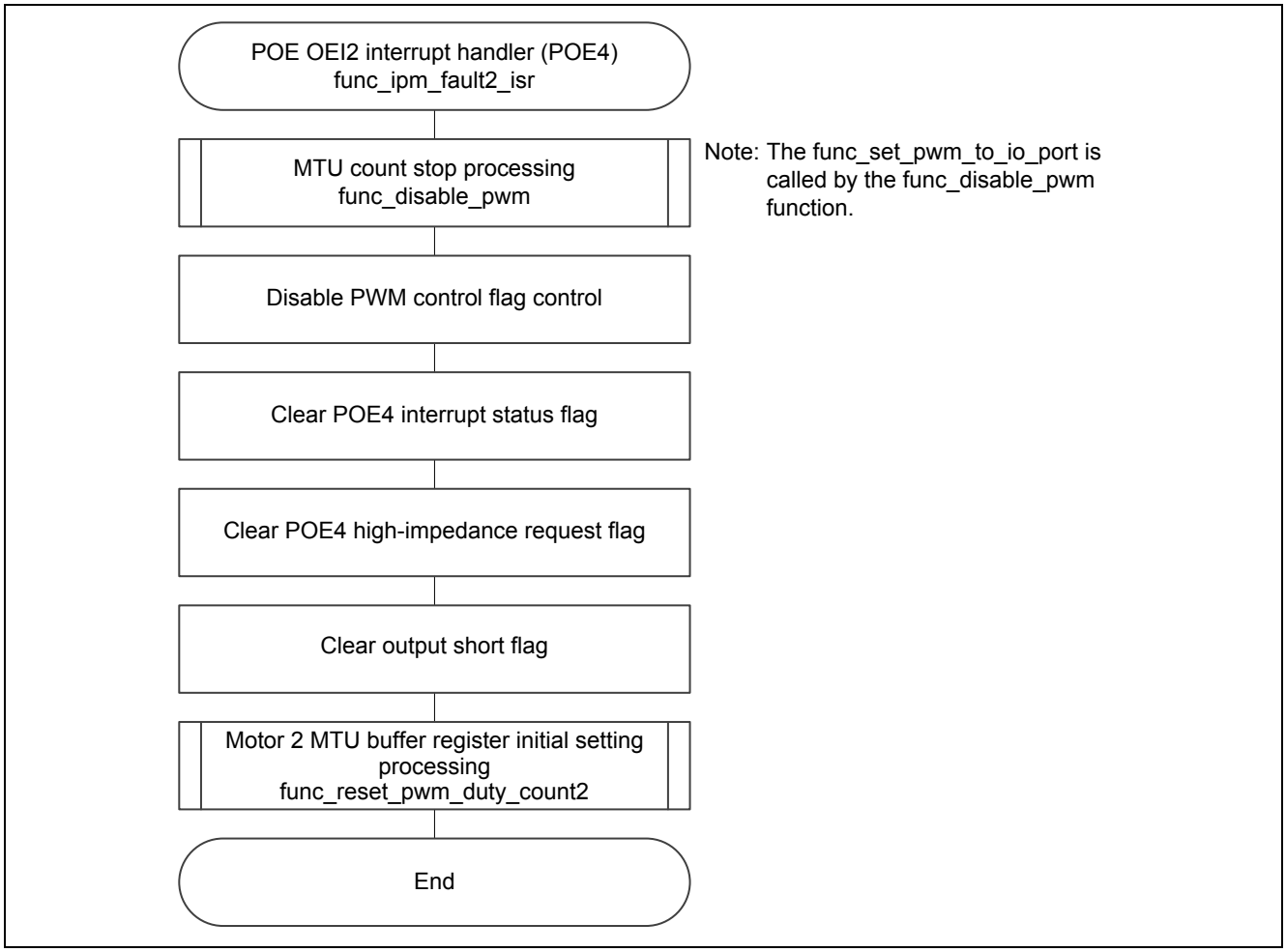
(3) A/D Converter Unit 2 Group C Scan End Interrupt Handler



(4) POE OEI1 Interrupt Handler (POE0)



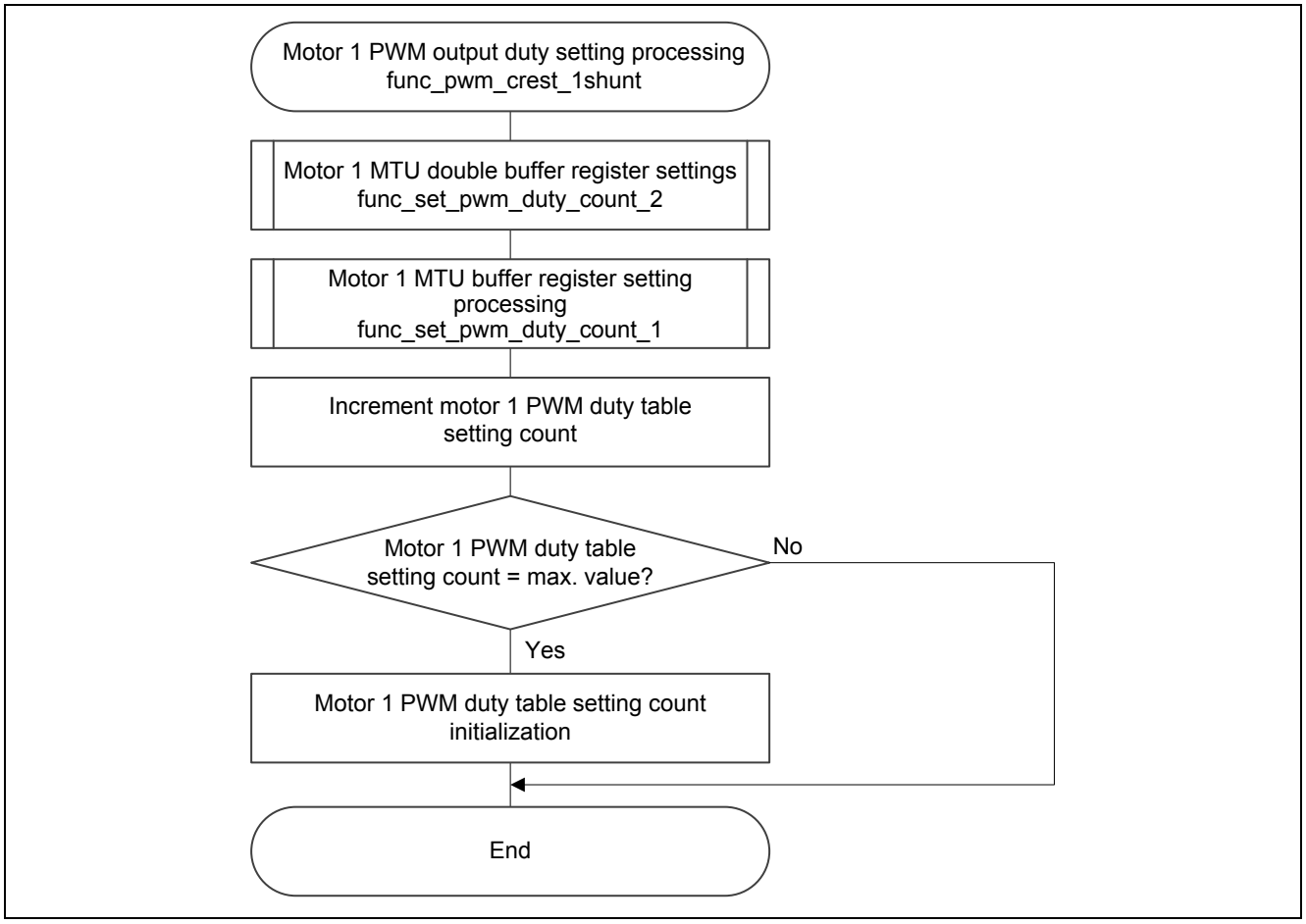
(5) POE OEI2 Interrupt Handler (POE4)



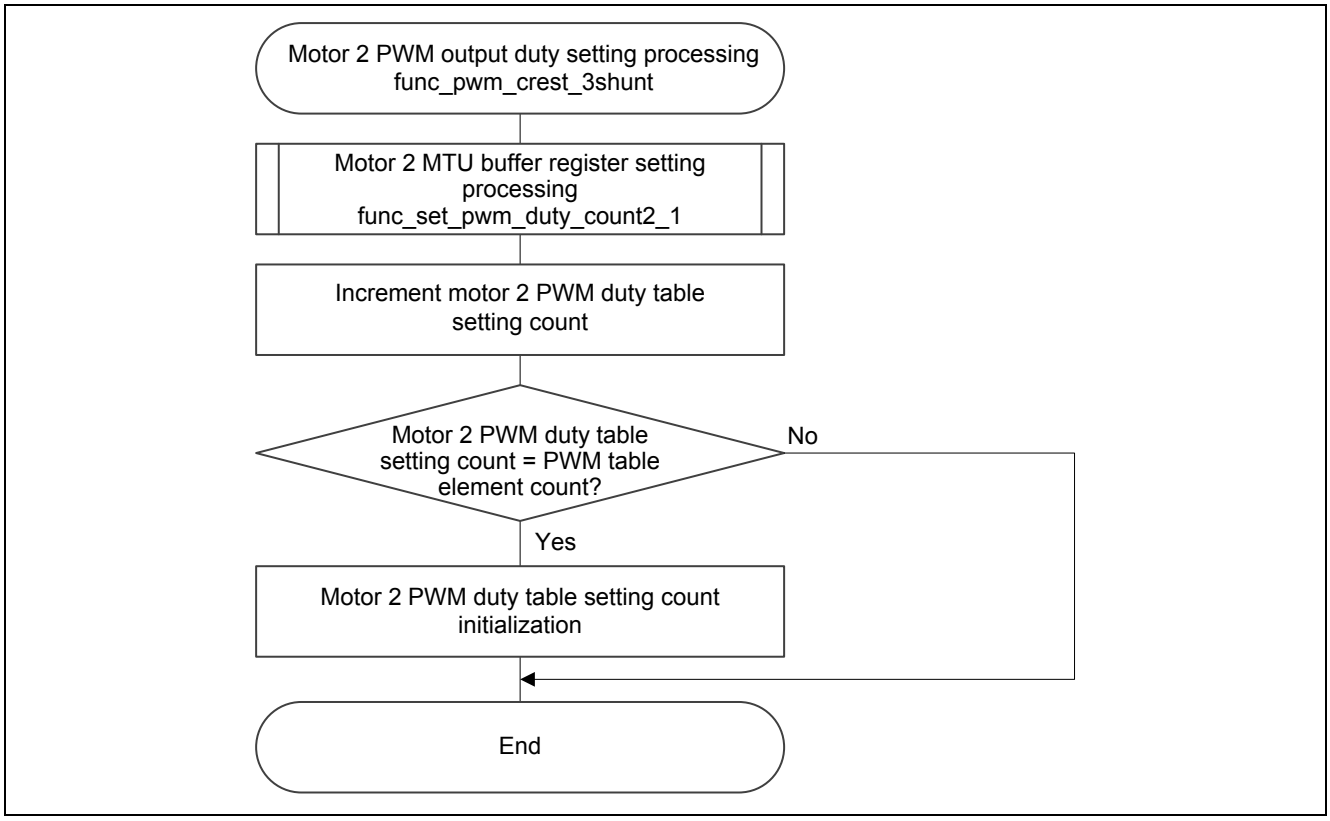
4.7.4 PWM Output Duty Setting Processing

Flowcharts of PWM output duty setting processing are shown below.

(1) Motor 1 PWM Output Duty Setting Processing



(2) Motor 2 PWM Output Duty Setting Processing



Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar. 03, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other disputes involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawing, chart, program, algorithm, application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics products.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (space and undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. When using the Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat radiation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions or failure or accident arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please ensure to implement safety measures to guard them against the possibility of bodily injury, injury or damage caused by fire, and social damage in the event of failure or malfunction of Renesas Electronics products, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures by your own responsibility as warranty for your products/system. Because the evaluation of microcomputer software alone is very difficult and not practical, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please investigate applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive carefully and sufficiently and use Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall not use Renesas Electronics products or technologies for (1) any purpose relating to the development, design, manufacture, use, stockpiling, etc., of weapons of mass destruction, such as nuclear weapons, chemical weapons, or biological weapons, or missiles (including unmanned aerial vehicles (UAVs)) for delivering such weapons, (2) any purpose relating to the development, design, manufacture, or use of conventional weapons, or (3) any other purpose of disturbing international peace and security, and you shall not sell, export, lease, transfer, or release Renesas Electronics products or technologies to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above. When exporting, selling, transferring, etc., Renesas Electronics products or technologies, you shall comply with any applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdiction over the parties or transactions.
10. Please acknowledge and agree that you shall bear all the losses and damages which are incurred from the misuse or violation of the terms and conditions described in this document, including this notice, and hold Renesas Electronics harmless, if such misuse or violation results from your resale or making Renesas Electronics products available any third party.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.3.0-1 November 2016)

RENESAS

Renesas Electronics Corporation

http://www.renesas.com

SALES OFFICES

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 6.0