RX Family, RL78 Family, 78K0R/Kx3-L

Micron Technology N25Q Serial NOR Flash Memory Control Software

R01AN1528EJ0104
Rev.1.04
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Introduction

This application note describes how to control N25Q SPI serial NOR flash memory, manufactured by Micron Technology, Inc., using an MCU manufactured by Renesas Electronics, and it explains the usage of the sample code provided for that purpose.

Note that the sample code is upper-layer software for controlling the serial NOR flash memory as a slave device.

Lower-layer software (clock synchronous single master control software) for controlling the SPI modes specific to individual MCU models is available separately, and should be obtained by the user, so please obtain this from the following URL as well. In addition, when a new microcontroller is added to the clock synchronous single-master control software, update of this application note may not be in time. Refer to 'Clock Synchronous Single Master Control Software (Lower-level layer of the software)' information in the following URL for the combination information on the latest supported microcontroller and its single-master control software.

- SPI/QSPI Serial Flash Memory, QSPI Serial Phase Change Memory Driver

  http://www.renesas.com/driver/spi_serial_flash

Target Devices

Serial NOR Flash Memory: N25Q SPI serial NOR flash memory, manufactured by Micron Technology, Inc.

MCUs on which operation has been confirmed:

RX600 series	: RX63N Group (using RSPI)
RX100 series	: RX111 (using the SCI)
	: RX111 (using the RSPI)
RL78/G1x	: RL78/G14, RL78/G1C group (using the SAU)
RL78/L1x	: RL78/L12, RL78/L12, RL78/L1C group (using the SAU)

See 3, Reference Application Notes, regarding MCU models other than those listed above.

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Note that the following abbreviations are used in this application note:

- Single-SPI (communication in single-SPI mode)
- Dual-SPI (communication in dual-SPI mode)
- Quad-SPI (communication in quad-SPI mode)

Contents

1. Specifications

A Renesas Electronics MCU is used to control N25Q serial NOR flash memory, manufactured by Micron Technology, Inc.

Separate MCU-specific clock synchronous single master control software is required.

Table 1-1 lists the peripheral functions used and their applications, and figure 1.1 shows a usage example.

Summaries of the functions are provided below:

- The software functions as a device driver, with a Renesas Electronics MCU operating as the master device and the Micron Technology, Inc., N25Q serial NOR flash memory operating as the slave device.
- The MCU's on-chip serial communication function (clock synchronous mode) is used in a single-SPI, dual-SPI, or quad-SPI configuration to control operation.
- One serial communication function channel can be specified by the user for use. It is not possible to use multiple channels.
- It is possible to control up to two serial NOR flash memory devices of the same type name.
- The communication speed can be specified by the user.
- Both big-endian and little-endian operation are supported. (The choice depends on the MCU used.)

Table 1-1 Peripheral Functions and Their Applications

Peripheral Function	Application
MCU's on-chip serial communication functionality (clock synchronous mode)	Communication with SPI slave device by means of serial communication function (clock synchronous mode) 1 channel (required)
Port	For SPI slave device select control signal Number of ports equal to number of devices (required)

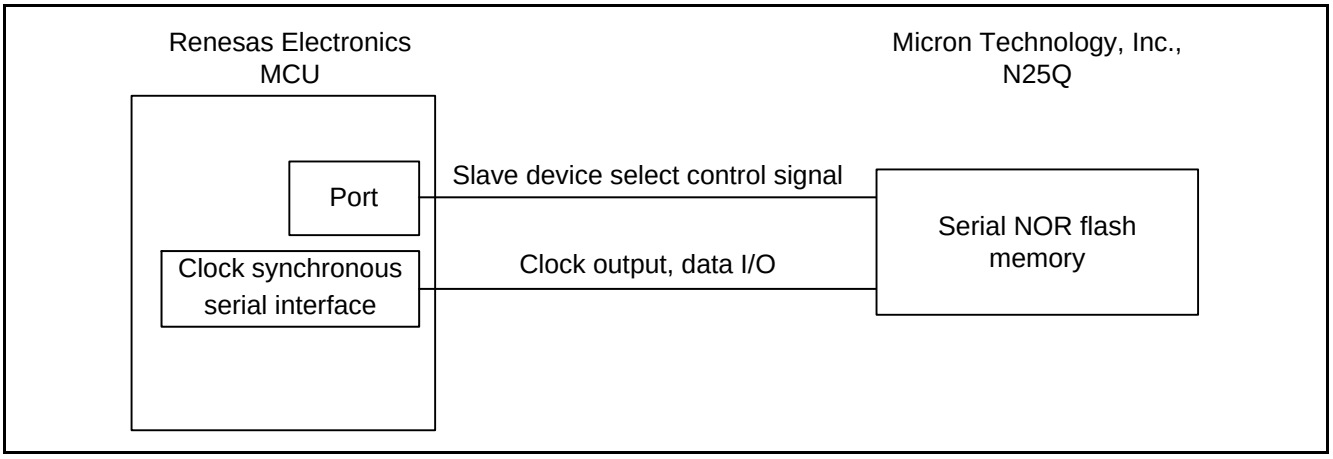


Figure 1.1 Usage Example

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

2.1 RX Family

(1) RX63N RSPI

Table 2-1 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RX63N Group (Program ROM: 1 MB/RAM: 128 KB)
Operating frequency	ICLK: 96 MHz, PCLK: 48 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance embedded Workshop Version 4.09.01.007
C compiler	Renesas Electronics Corporation RX Family C/C++ Compiler Package (Toolchain 1.2.1.0)
	Compiler options The integrated development environment default settings are used.
Endian order	Big endian / Little endian
Sample code version number	Ver. 2.20
Software	Clock synchronous single master control software using the RSPI, for RX63N, version 2.04
Board	Renesas Starter Kit for RX63N

(2) RX111 RSPI

Table 2-2 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RX111 Group (Program ROM: 128 KB, RAM: 16 KB)
Operating frequency	ICLK: 32 MHz, PCLK: 32 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics CubeSuite+ V2.01.00
C compiler	Renesas Electronics RX family C/C++ compiler package (Toolchain 2.01.00)
	Compiler options: The default settings (Optimize Level: 2, Optimize for size) for the integrated development environment are used.
Endian order	Big endian / Little endian
Sample code version number	Ver. 2.21.R01
Software	RX210, RX21A, RX220, RX63N, RX63T, RX111 Group Clock Synchronous Single Master Control Software Using the RSPI (R01AN1196EJ), Ver. 2.04.R04
Board	Renesas Starter Kit for RX111

(3) RX111 SCI

Table 2-3 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RX111 Group (Program ROM: 128 KB, RAM: 16 KB)
Operating frequency	ICLK: 32 MHz, PCLK: 32 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics CubeSuite+ V2.01.00
C compiler	Renesas Electronics RX family C/C++ compiler package (Toolchain 2.01.00)
	Compiler options: The default settings (Optimize Level: 2, Optimize for size) for the integrated development environment are used.
Endian order	Big endian / Little endian
Sample code version number	Ver. 2.21.R01
Software	RX210, RX21A, RX220, RX63N, RX63T,RX111 Group Clock Synchronous Single Master Control Software Using the SCI (R01AN1229EJ), Ver. 2.01.R05
Board	Renesas Starter Kit for RX111

2.2 RL78 Family, 78K0R/Kx3-L

(1) RL78/G14 Integrated Development Environment CubeSuite+ (Compiler:CA78K0R)

Table 2-4 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G14 Group (Program ROM: 256 MB/RAM: 24 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V1.03.00
C compiler	Renesas Electronics Corporation CubeSuite+ RL78,78K0R Compiler CA78K0R V1.60
	Compiler options The integrated development environment default settings ("-qx2") are used.
Endian order	Little endian
Sample code version number	Ver. 2.20
Software	Clock synchronous single master control software using CSI mode of serial array unit, version 2.02
Board	Renesas Starter Kit for RL78/G14

(2) RL78/G14 Integrated Development Environment CS+ for CC (Compiler:CC-RL)

Table 2-5 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G14 Group (Program ROM: 256 MB/RAM: 24 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CS+ for CC V3.02.00
C compiler	Renesas Electronics Corporation RL78 compiler CC-RL V1.02.00
	Compiler options The default settings (Perform the default optimization(None)) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.22
Software	RL78/G14, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0105), version 2.05)
Board	Renesas Starter Kit for RL78/G14

(3) RL78/G14 Integrated Development Environment IAR Embedded Workbench

Table 2-6 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G14 Group (Program ROM: 256 KB/RAM: 24 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	IAR Systems IAR Embedded Workbench for Renesas RL78 (Ver.1.30.2)
C compiler	IAR Systems IAR Assembler for Renesas RL78 (Ver.1.30.2.50666) IAR C/C++ Compiler for Renesas RL78 (Ver.1.30.2.50666)
	Compiler options: The default settings (Low) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.21
Software	Clock synchronous single master control software using CSI mode of serial array unit, version 2.03
Board	Renesas Starter Kit for RL78/G14

(4) RL78/G1C Integrated Development Environment CubeSuite+ (Compiler:CA78K0R)

Table 2-7 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G1C Group (Program ROM: 32 KB/RAM: 5.5 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 12 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V2.01.00
C compiler	Renesas Electronics Corporation CubeSuite+ RL78,78K0R Compiler CA78K0R V1.70
	Compiler options The integrated development environment default settings ("-qx2") are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas RL78/G1C Target Board QB-R5F10JGC-TB

(5) RL78/G1C Integrated Development Environment CS+ for CC (Compiler:CC-RL)

Table 2-8 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G1C Group (Program ROM: 32 KB/RAM: 5.5 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 12 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CS+ for CC V3.02.00
C compiler	Renesas Electronics Corporation RL78 compiler CC-RL V1.02.00
	Compiler options The default settings (Perform the default optimization(None)) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.22
Software	RL78/G14, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0105), version 2.05)
Board	Renesas RL78/G1C Target Board QB-R5F10JGC-TB

(6) RL78/G1C Integrated Development Environment IAR Embedded Workbench

Table 2-9 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/G1C Group (Program ROM: 256 KB/RAM: 24 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 12 MHz
Operating voltage	3.3 V
Integrated development environment	IAR Systems IAR Embedded Workbench for Renesas RL78 (Ver.1.30.5)
C compiler	IAR Systems IAR Assembler for Renesas RL78 (Ver.1.30.4.50715) IAR C/C++ Compiler for Renesas RL78 (Ver.1.30.5.50715)
	Compiler options: The default settings (Low) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas RL78/G1C Target Board QB-R5F10JGC-TB

(7) RL78/L12 Integrated Development Environment CubeSuite+

Table 2-10 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L12 Group (Program ROM: 32 KB, RAM:1.5 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V2.01.00
C compiler	Renesas Electronics Corporation CubeSuite+ RL78,78K0R Compiler CA78K0R V1.70
	Compiler options The integrated development environment default settings ("-qx2") are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L12

(8) RL78/L12 Integrated Development Environment IAR Embedded Workbench

Table 2-11 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L12 Group (Program ROM: 32 KB, RAM:1.5 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	IAR Systems IAR Embedded Workbench for Renesas RL78 (Ver.1.30.5)
C compiler	IAR Systems IAR Assembler for Renesas RL78 (Ver.1.30.4.50715) IAR C/C++ Compiler for Renesas RL78 (Ver.1.30.5.50715)
	Compiler options: The default settings (Low) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L12

(9) RL78/L13 Integrated Development Environment CubeSuite+

Table 2-12 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L13 Group (Program ROM: 128 KB/RAM: 8 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V2.01.00
C compiler	Renesas Electronics Corporation CubeSuite+ RL78,78K0R Compiler CA78K0R V1.70
	Compiler options The integrated development environment default settings ("-qx2") are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L13

(10) RL78/L13 Integrated Development Environment IAR Embedded Workbench

Table 2-13 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L13 Group (Program ROM: 128 KB/RAM: 8 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	IAR Systems IAR Embedded Workbench for Renesas RL78 (Ver.1.30.5)
C compiler	IAR Systems IAR Assembler for Renesas RL78 (Ver.1.30.4.50715) IAR C/C++ Compiler for Renesas RL78 (Ver.1.30.5.50715)
	Compiler options: The default settings (Low) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L13

(11) RL78/L1C Integrated Development Environment CubeSuite+

Table 2-14 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L1C Group (Program ROM: 256 KB/RAM: 16 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation CubeSuite+ V2.01.00
C compiler	Renesas Electronics Corporation CubeSuite+ RL78,78K0R Compiler CA78K0R V1.70
	Compiler options The integrated development environment default settings ("-qx2") are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L1C

(12) RL78/L1C Integrated Development Environment IAR Embedded Workbench

Table 2-15 Operation Confirmation Conditions

Item	Description
Memory	Micron Technology N25Q Serial NOR Flash Memory
Microcontroller used	RL78/L1C Group (Program ROM: 256 KB/RAM: 16 KB)
Operating frequency	Main system clock: 24 MHz CPU/peripheral hardware clock: 24 MHz Serial clock: 6 MHz
Operating voltage	3.3 V
Integrated development environment	IAR Systems IAR Embedded Workbench for Renesas RL78 (Ver.1.30.5)
C compiler	IAR Systems IAR Assembler for Renesas RL78 (Ver.1.30.4.50715) IAR C/C++ Compiler for Renesas RL78 (Ver.1.30.5.50715)
	Compiler options: The default settings (Low) for the integrated development environment are used.
Endian order	Little endian
Sample code version number	Ver. 2.21.R01
Software	RL78/G14,RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ0103), Ver. 2.03
Board	Renesas Starter Kit for RL78/L1C

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

In the related application notes listed below, refer to the “Target Device” item on the cover for a listing of MCU models on which operation has been confirmed.

3.1 RX Family: List of Related Application Notes

- RX610 Group Clock Synchronous Single Master Control Software Using the SCI (R01AN0534EJ)
- RX62N Group Clock Synchronous Single Master Control Software Using the RSPI (R01AN0323EJ)
- RX62N Group Clock Synchronous Single Master Control Software Using the SCI (R01AN1088EJ)
- RX210, RX21A, RX220, RX63N, RX63T, RX111 Group Clock Synchronous Single Master Control Software Using the RSPI (R01AN1196EJ)
- RX210, RX21A, RX220, RX63N, RX63T, RX111 Group Clock Synchronous Single Master Control Software Using the SCI (R01AN1229EJ)

3.2 RL78 Family, 78K0R Family: List of Related Application Notes

- 78K0R/Kx3-L Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN0708EJ)
- RL78/G14, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ)

4. Hardware

4.1 Hardware Configuration

An example hardware configuration is shown below.

4.1.1 Pin Assignments for Single-SPI Configuration

The following table lists the MCU pins used for single-SPI operation and their functions.

Table 4-1 Single-SPI Pins and Functions

MCU Pin Name	I/O	Description
CLK	Output	Clock output
DataOut	Output	Master data output
DataIn	Input	Master data input
Port (CS#)	Output	Slave device select output

4.1.2 Single-SPI Connection Example

A connection example for single-SPI operation is shown below:

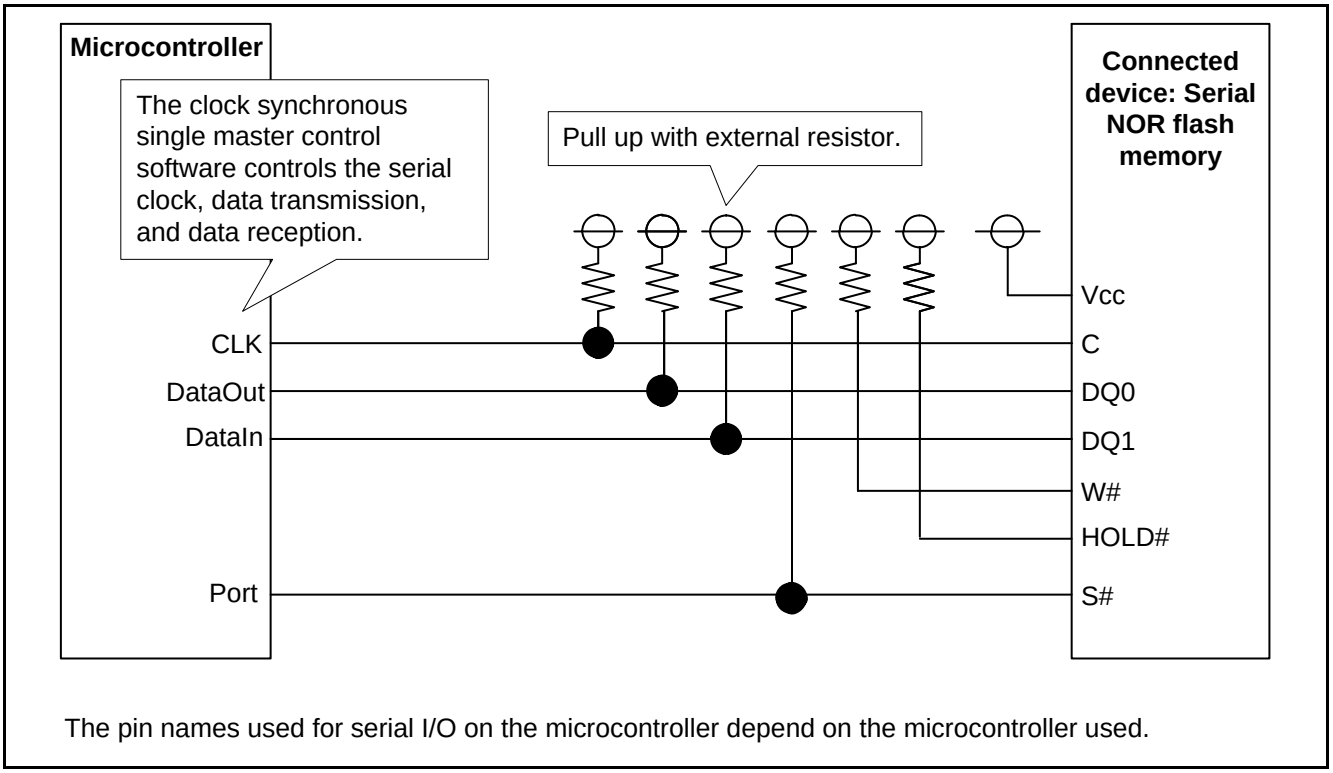


Figure 4.1 MCU and SPI Slave Device Connection Example for Single-SPI

4.1.3 Pin Assignments for Dual-SPI Configuration

The following table lists the MCU pins used for dual-SPI operation and their functions.

In order to use a dual-SPI configuration, the MCU must have a quad serial peripheral interface function.

Table 4-2 Dual-SPI Pins and Functions

MCU Pin Name	I/O	Description
CLK	Output	Clock output
DataIn/Out0	Input/output	Master data input/output 0
DataIn/Out1	Input/output	Master data input/output 1
Port(CS#)	Output	Slave device select output

4.1.4 Dual-SPI Connection Example

A connection example for dual-SPI operation is shown below:

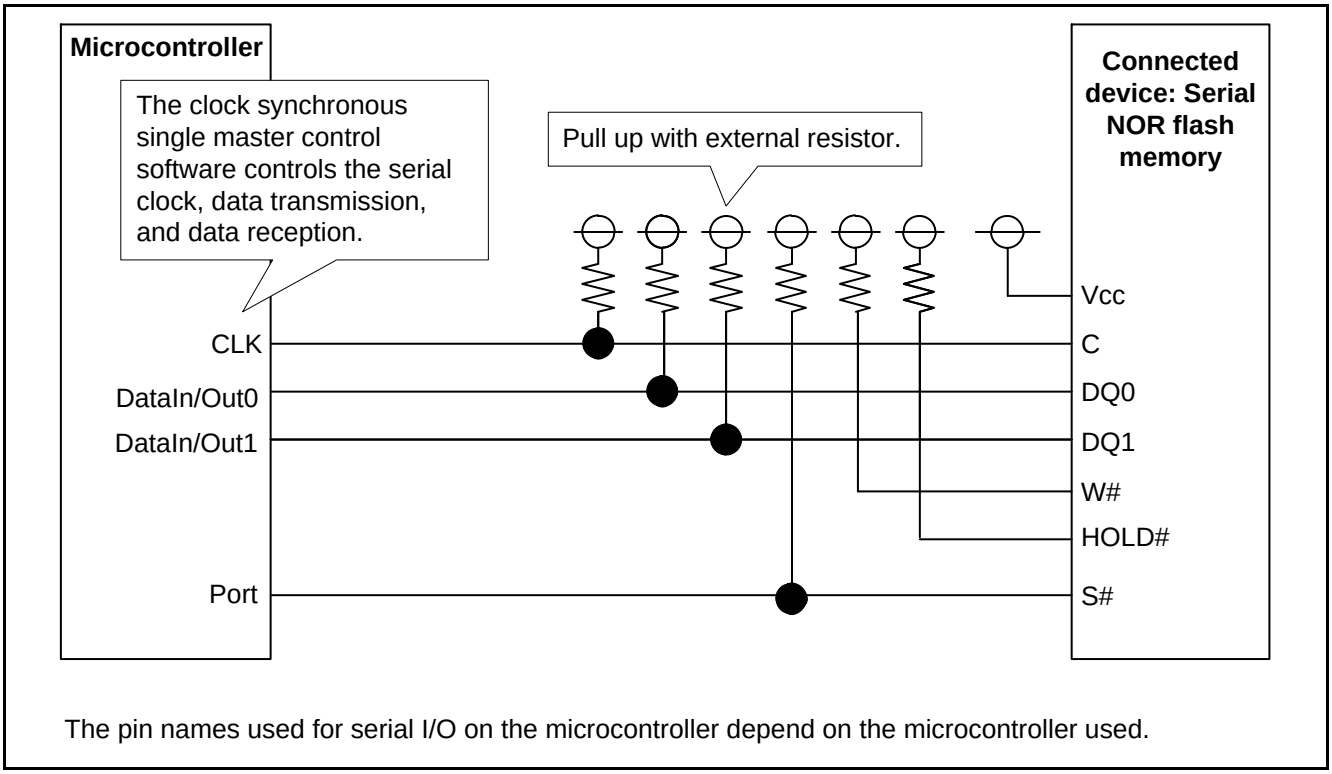


Figure 4.2 MCU and SPI Slave Device Connection Example for Dual-SPI

4.1.5 Pin Assignments for Quad-SPI Configuration

The following table lists the MCU pins used for quad-SPI operation and their functions.

In order to use a quad-SPI configuration, the MCU must have a quad serial peripheral interface function.

Table 4-3 Quad-SPI Pins and Functions

MCU Pin Name	I/O	Description
CLK	Output	Clock output
DataIn/Out0	Input/output	Master data input/output 0
DataIn/Out1	Input/output	Master data input/output 1
DataIn/Out2	Input/output	Master data input/output 2
DataIn/Out3	Input/output	Master data input/output 3
Port (CS#)	Output	Slave device select output

4.1.6 Quad-SPI Connection Example

A connection example for quad-SPI operation is shown below:

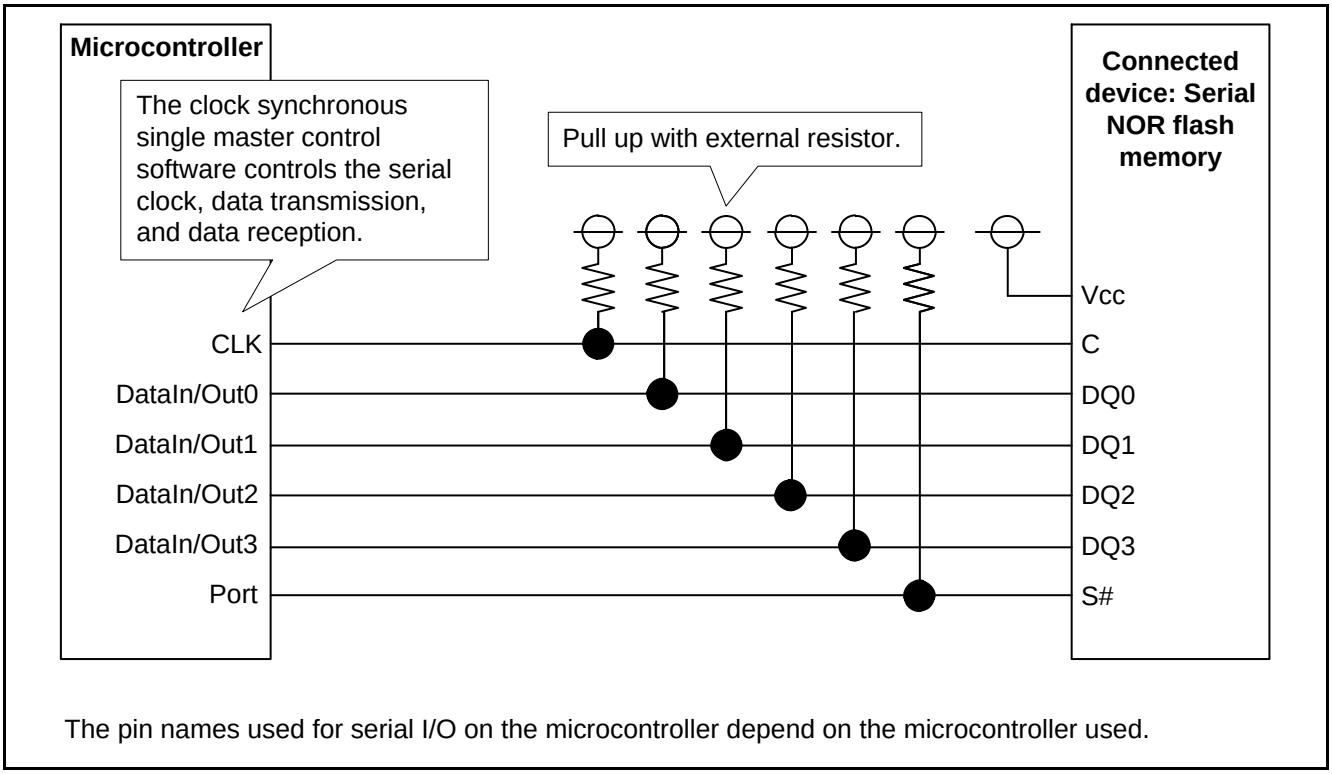


Figure 4.3 MCU and SPI Slave Device Connection Example for Quad-SPI

5. Software

5.1 Operation Overview

The MCU's clock synchronous serial communication function is used to control the serial NOR flash memory.

The sample code performs the following types of control:

- The S# pin of the SPI slave device is connected to the port of the MCU and is controlled by using MCU general port output. (This control is implemented by the sample code.)
- Data input and output is controlled in clock synchronous mode (using the internal clock of the MCU). (The sample code makes use of the MCU-specific clock synchronous single master control software.)

5.1.1 Relationship Between Data Buffers and Transmit/Receive Data

This sample code is a block type device driver and passes the transmit or receive data pointer as an argument. The relationship between the data ordering in the data buffer in RAM and the transmit/receive order is shown below and this sample code both transmits in the order data is stored in the transmit buffer and writes data to the receive data buffer in the order received regardless of the endian order or serial communication function used

Figure 5.1 illustrates the storage of transfer data.

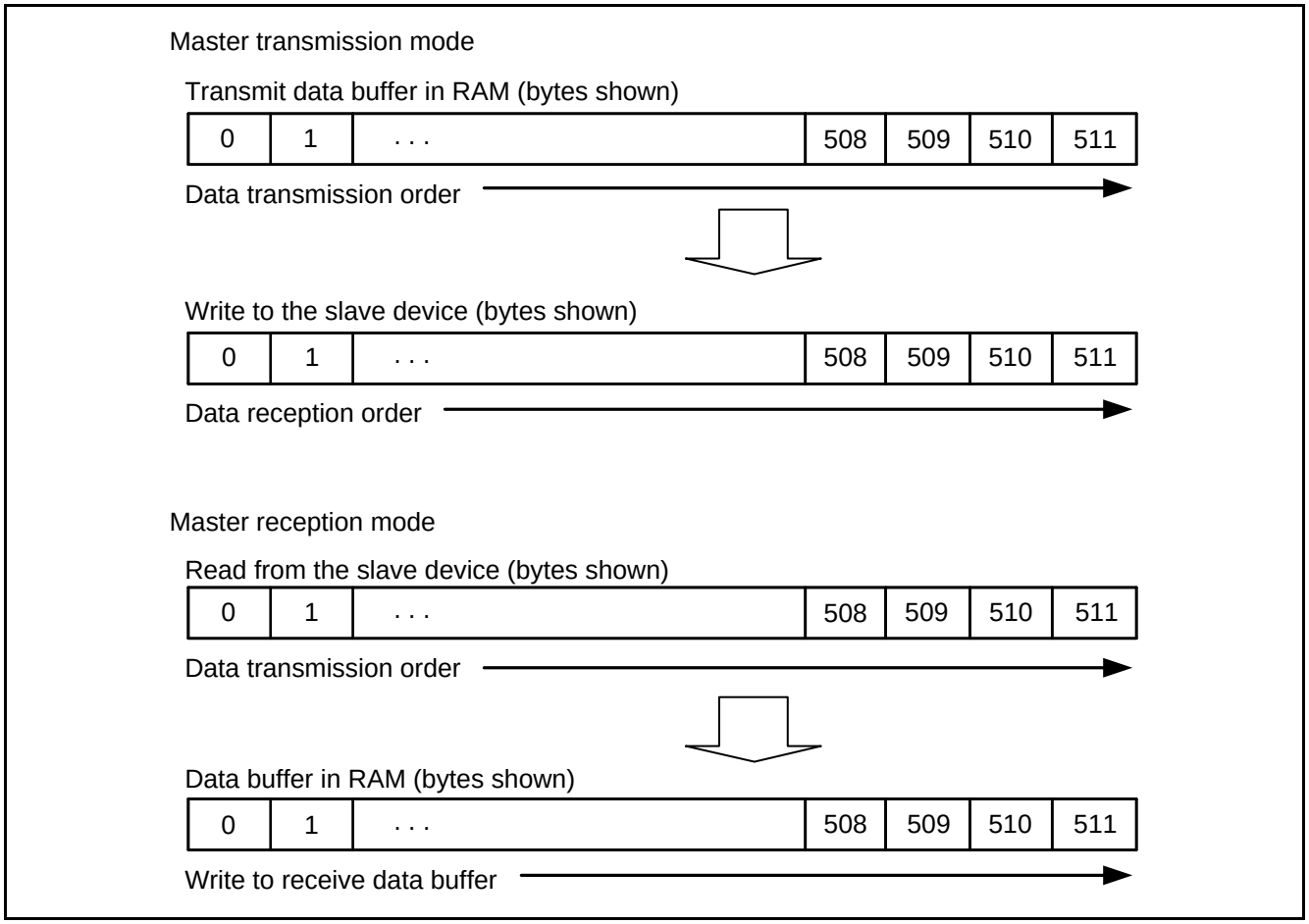


Figure 5.1 Storage of Transfer Data

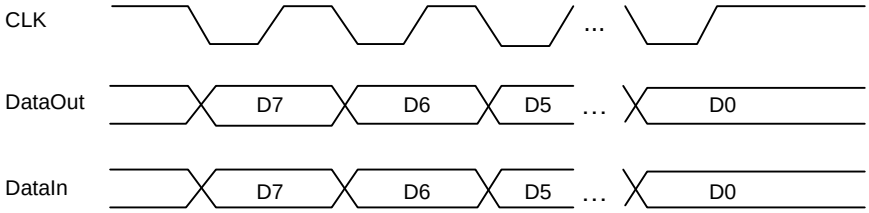
5.1.2 Timing Generation in Clock Synchronous Mode

The timings generated in clock synchronous mode are shown below.

Refer to the data sheets of the MCU and SPI device when determining the serial clock frequency to be used.

(1) Single-SPI Operation

To control serial NOR flash memory, the SPI mode 3 (CPOL = 1, CPHA = 1) shown in figure 5.2 is generated.



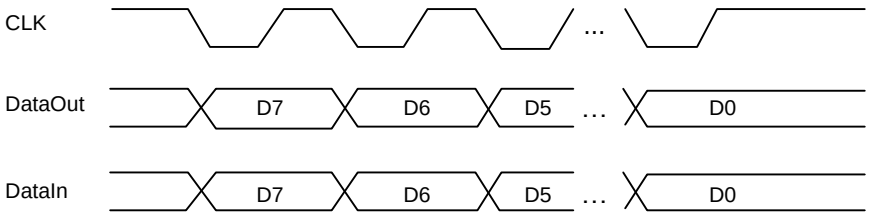
- Transmission from MCU to serial NOR flash memory:
  Output of transmit data starts at falling edge of transfer clock.
- Reception from serial NOR flash memory to MCU:
  Input of receive data starts at rising edge of transfer clock.
- MSB-first transfer

The CLK pin is high-level when no transfer is taking place.

Figure 5.2 Single-SPI Clock Synchronous Mode Timing Settings

(2) Dual-SPI Operation

To control serial NOR flash memory, the SPI mode 3 (CPOL = 1, CPHA = 1) shown in figure 5.3 is generated.



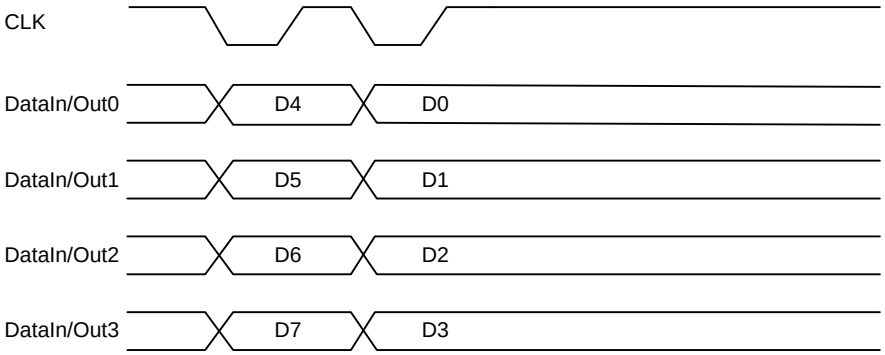
- Transmission from MCU to serial NOR flash memory:
  Output of transmit data starts at falling edge of transfer clock.
- Reception from serial NOR flash memory to MCU:
  Input of receive data starts at rising edge of transfer clock.
- MSB-first transfer

The CLK pin is high-level when no transfer is taking place.

Figure 5.3 Dual-SPI Clock Synchronous Mode Timing Settings

(3) Quad-SPI Operation

To control serial NOR flash memory, the SPI mode 3 (CPOL = 1, CPHA = 1) shown in figure 5.4 is generated.



- Transmission from MCU to serial NOR flash memory:
  Output of transmit data starts at falling edge of transfer clock.
- Reception from serial NOR flash memory to MCU:
  Input of receive data starts at rising edge of transfer clock.
- MSB-first transfer

The CLK pin is high-level when no transfer is taking place.

Figure 5.4 Quad-SPI Clock Synchronous Mode Timing Settings

5.1.3 Serial NOR Flash Memory S# Pin Control

The S# pin of the serial NOR flash memory is connected to the port of the MCU, and it is controlled by MCU general port output.

The duration from the falling edge of the S# (MCU port (CS#)) signal of the serial NOR flash memory to the falling edge of the C (MCU CLK) signal of the serial NOR flash memory is controlled by means of software wait to accommodate the S# setup time of the serial NOR flash memory.

The duration from the rising edge of the C (MCU CLK) signal of the serial NOR flash memory to the rising edge of the S# (MCU port (CS#)) signal of the serial NOR flash memory controlled by means of software wait to accommodate the S# hold time of the serial NOR flash memory.

Check the data sheet of the serial NOR flash memory and set the software wait time as appropriate for the system.

5.1.4 Serial NOR Flash Memory Instruction Codes

Instruction codes are used to control the serial NOR flash memory, and command control is implemented by using these codes.

Table 5-1 Instruction Set

Instruction	Description	Instruction Format
WREN	Write Enable	0000 0110 (06 h)
WRDI	Write Disable	0000 0100 (04 h)
RDSR	Read Status Register	0000 0101 (05 h)
WRSR	Write Status Register	0000 0001 (01 h)
RDFSR	Read Flag Status Register	0111 0000 (70 h)
CLFSR	Clear Flag Status Register	0101 0000 (50 h)
FAST_READ	Read Data at Higher Speed	0000 1011 (0b h)
DOFR	Dual Output Fast Read	0011 1011 (3b h)
QOFR	Quad Output Fast Read	0110 1011 (6b h)
PP	Page Program	0000 0010 (02 h)
DIFP	Dual Input Fast Program	1010 0010 (a2 h)
QIFP	Quad Input Fast Program	0011 0010 (32 h)
SE	Sector Erase	1101 1000 (d8 h)
SSE	Subsector Erase	0010 0000 (20 h)
BE	Bulk Erase	1100 0111 (c7 h)
DE	Die Erase	1100 0100 (c4 h)
RDID	Read Identification	1001 1111 (9f h)
ENTER4	Enter 4-Byte Address Mode	1011 0111 (b7 h)
EXIT4	Exit 4-Byte Address Mode	1110 1001 (e9 h)

5.2 Software Configuration

The sample code operates as upper-layer control software for controlling the SPI serial NOR flash memory (indicated as serial NOR flash memory control software in figure 5.5).

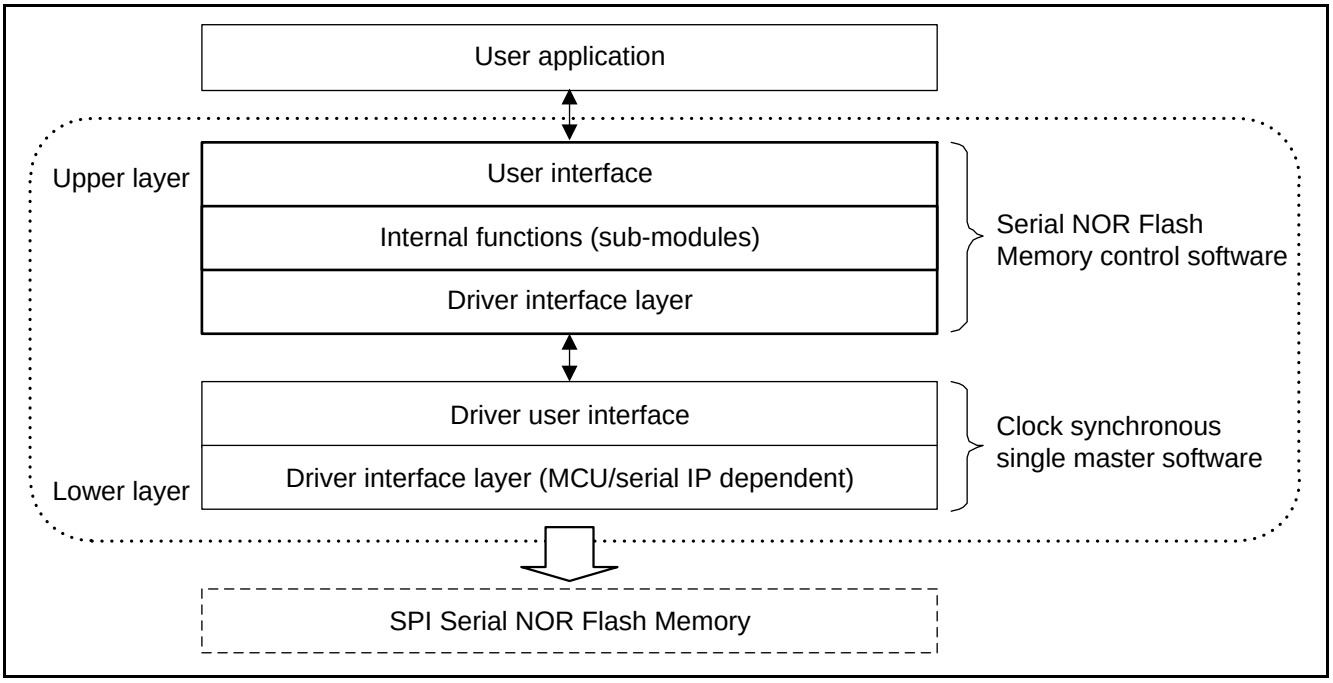


Figure 5.5 Software Configuration

The control procedure is as follows:

1. Port (CS#) signal falling edge
2. Software wait
3. Transmission and reception of commands and data using clock synchronous single master software
4. Software wait
5. Port (CS#) rising edge

5.3 Required Memory Size

The following table lists the required memory size.

5.3.1 RX Family

(1) RX63N

Table 5-2 Required Memory Size

Memory Used	Size	Remarks
ROM	3,760 bytes (little endian)	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c
RAM	6 bytes (little endian)	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c
Maximum user stack usage	140 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(2) RX111 RSPI

Table 5-3 Required Memory Size

Memory Used	Size	Remarks
ROM	3,792 bytes (little endian)	r_qspi_pcm_p5q_usr.c r_qspi_pcm_p5q_sub.c r_qspi_pcm_p5q_drvif.c
RAM	6 bytes (little endian)	r_qspi_pcm_p5q_usr.c r_qspi_pcm_p5q_sub.c r_qspi_pcm_p5q_drvif.c
Maximum user stack usage	160 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(3) RX111 SCI

Table 5-4 Required Memory Size

Memory Used	Size	Remarks
ROM	3,792 bytes (little endian)	r_qspi_pcm_p5q_usr.c r_qspi_pcm_p5q_sub.c r_qspi_pcm_p5q_drvif.c
RAM	6 bytes (little endian)	r_qspi_pcm_p5q_usr.c r_qspi_pcm_p5q_sub.c r_qspi_pcm_p5q_drvif.c
Maximum user stack usage	156 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

5.3.2 RL78 Family, 78K0R/Kx3-L

Show the memory size of the different MCU of the order. Check the order of the MCU and please refer to the following memory sizes.

(1) RL78/G14 Integrated Development Environment CubeSuite+ (Compiler:CA78K0R)

Table 5-5 Required Memory Size

Memory Used	Size	Remarks
ROM	6,211 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	102 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(2) RL78/G14 Integrated Development Environment CS+ for CC (Compiler:CC-RL)

Table 5.4 Required Memory Size

Memory Used	Size	Remarks
ROM	5,020 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	82 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(3) RL78/G14 Integrated Development Environment IAR Embedded Workbench

Table 5-6 Required Memory Size

Memory Used	Size	Remarks
ROM	6,907 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	154 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum user stack size is the stack size for the entire project. It includes the stack of the lower-layer clock synchronous single-master control software.

(4) RL78/L13 Integrated Development Environment CubeSuite+ (Compiler:CA78K0R)

Table 5-7 Required Memory Size

Memory Used	Size	Remarks
ROM	6,309 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	102 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(5) RL78/L13 Integrated Development Environment CS+ for CC (Compiler:CC-RL)

Table 5-8 Required Memory Size

Memory Used	Size	Remarks
ROM	5,024 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	82 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum usable user stack size includes the stack size of the lower-layer clock synchronous single master software.

(6) RL78/L13 Integrated Development Environment IAR Embedded Workbench

Table 5-9 Required Memory Size

Memory Used	Size	Remarks
ROM	5,398 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
RAM	6 bytes	r_qspi_flash_n25q_usr.c r_qspi_flash_n25q_sub.c r_qspi_flash_n25q_drvif.c r_qspi_flash_n25q_sfr_rl78.c
Maximum user stack usage	132 bytes	
Maximum interrupt stack usage	—	No interrupts used

Note: The required memory size varies depending on the C compiler version and compile options.
The indicated ROM and RAM sizes do not include the memory used by the lower-layer clock synchronous single master software.
The memory sizes listed above differ depending on the MCU type name.
The maximum user stack size is the stack size for the entire project. It includes the stack of the lower-layer clock synchronous single-master control software.

5.4 File Structure

The following table lists the files used by the sample code.

Table 5-10 File Structure

\an_r01an1528ej0104_mcu_serial		<DIR>	Sample code folder
	r01an1528ej0104_mcu.pdf		Application note
	\source	<DIR>	Program storage folder
		\r_qspi_flash_n25q <DIR>	Serial NOR Flash Memory control software folder
		r_qspi_flash_n25q.h	Header file
		r_qspi_flash_n25q_drvif.c	Driver interface source file
		r_qspi_flash_n25q_drvif.h	Driver interface header file
		r_qspi_flash_n25q_sfr.h.rl78g14	Common definition for registers (RL78/G14)
		r_qspi_flash_n25q_sfr.h.rl78g1c	Common definition for registers (RL78/G1C)
		r_qspi_flash_n25q_sfr.h.rl78l1c	Common definition for registers (RL78/L1C)
		r_qspi_flash_n25q_sfr.h.rl78l12	Common definition for registers (RL78/L12)
		r_qspi_flash_n25q_sfr.h.rl78l13	Common definition for registers (RL78/L13)
		r_qspi_flash_n25q_sfr.h.rx63n	Common definition for registers (RX63N)
		r_qspi_flash_n25q_sfr.h.rx111	Common definition for registers (RX111)
		r_qspi_flash_n25q_sfr_rl78g14.c	Common definition source file for registers (RL78/G14)
		r_qspi_flash_n25q_sfr_rl78g1c.c	Common definition source file for registers (RL78/G1C)
		r_qspi_flash_n25q_sfr_rl78l1c.c	Common definition source file for registers (RL78/L1C)
		r_qspi_flash_n25q_sfr_rl78l12.c	Common definition source file for registers (RL78/L12)
		r_qspi_flash_n25q_sfr_rl78l13.c	Common definition source file for registers (RL78/L13)
		r_qspi_flash_n25q_sub.c	Internal function source file
		r_qspi_flash_n25q_sub.h	Internal function header file
		r_qspi_flash_n25q_usr.c	User interface source file
		\sample <DIR>	Operation verification program storage folder
		testmain.c	Sample source file for operation verification

Note: In addition, separate MCU-specific clock synchronous single master control software is required.

5.5 Constants

5.5.1 Return Value

The following table lists the return value used in the sample code.

Table 5-11 Return Value (Refer to r_qspi_flash_n25q.h)

Constant Name	Setting Value	Contents
FLASH_OK	(error_t)(0)	Successful operation
FLASH_ERR_PARAM	(error_t)(-1)	Parameter error
FLASH_ERR_HARD	(error_t)(-2)	Hardware error
FLASH_ERR_WP	(error_t)(-4)	Write-protection error
FLASH_ERR_TIMEOUT	(error_t)(-6)	Time out error
FLASH_ERR_OTHER	(error_t)(-7)	Other error

5.5.2 Command Definitions

The following table lists the command definitions used in the sample code.

Table 5-12 Command Definitions (Refer to r_qspi_flash_n25q_sub.c)

Constant Name	Setting Value	Contents
FLASH_CMD_WREN	(uint8_t)(0x06)	Write Enable
FLASH_CMD_WRDI	(uint8_t)(0x04)	Write Disable
FLASH_CMD_RDSR	(uint8_t)(0x05)	Read Status Register
FLASH_CMD_WRSR	(uint8_t)(0x01)	Write Status Register
FLASH_CMD_RDFSR	(uint8_t)(0x70)	Read Flag Status Register
FLASH_CMD_CLFSR	(uint8_t)(0x50)	Clear Flag Status Register
FLASH_CMD_FREAD	(uint8_t)(0x0b)	Read Data at Higher Speed
FLASH_CMD_DOFR	(uint8_t)(0x3b)	Dual Output Fast Read
FLASH_CMD_QOFR	(uint8_t)(0x6b)	Quad Output Fast Read
FLASH_CMD_PP	(uint8_t)(0x02)	Page Program
FLASH_CMD_DIFP	(uint8_t)(0xa2)	Dual Input Fast Program
FLASH_CMD_QIFP	(uint8_t)(0x32)	Quad Input Fast Program
FLASH_CMD_SE	(uint8_t)(0xd8)	Sector Erase
FLASH_CMD_SSE	(uint8_t)(0x20)	Subsector Erase
FLASH_CMD_BE	(uint8_t)(0xc7)	Bulk Erase
FLASH_CMD_DE	(uint8_t)(0xc4)	Die Erase
FLASH_CMD_RDID	(uint8_t)(0x9f)	Read Identification
FLASH_CMD_ENTER4	(uint8_t)(0xb7)	Enter 4-Byte Address Mode
FLASH_CMD_EXIT4	(uint8_t)(0xe9)	Exit 4-Byte Address Mode

5.5.3 Other Definitions

The values of other definitions used in the sample code are listed below.

Table 5-13 Values Defined in r_qspi_flash_n25q.h

Constant Name	Setting Value	Contents
FLASH_DEV_NUM	(1)	Number of connected devices
FLASH_DEV0	(0)	Device number 0
FLASH_DEV1	(1)	Device number 1
FLASH_DELAY_TASK	(uint8_t)(1)	Wait time of delay task [unit: ms]*1
FLASH_LOG_ERR	(1)	Log Type: Error
FLASH_TRUE	(uint8_t)(0x01)	Flag "ON"
FLASH_FALSE	(uint8_t)(0x00)	Flag "OFF"
FLASH_MODE_B_ERASE	(uint8_t)(1)	Erase Mode: Bulk Erase
FLASH_MODE_S_ERASE	(uint8_t)(2)	Erase Mode: Sector Erase
FLASH_MODE_SS_ERASE	(uint8_t)(3)	Erase Mode: Subsector Erase
FLASH_MODE_D_ERASE	(uint8_t)(4)	Erase Mode: Dei Erase
FLASH_MODE_3BYTE	(uint8_t)(0)	Addressability Mode: 3-byte addressability Mode
FLASH_MODE_4BYTE	(uint8_t)(1)	Addressability Mode: 4-byte addressability Mode
FLASH_MODE_REG_WRITE	(uint8_t)(0)	Wait Mode: Register write mode
FLASH_MODE_PROG_ERASE	(uint8_t)(1)	Wait Mode: Page Program or Erase mode
FLASH_MEM_SIZE	(uint32_t)(33554432)	Memory size (byte units) Value at left corresponds to size of 256 Mbit.
FLASH_SECT_ADDR	(uint32_t)(0xffff0000)	Sector address mask value for sector erase Value at left corresponds to size of 256 Mbit.
FLASH_SSECT_ADDR	(uint32_t)(0xfffff000)	Sector address mask value for subsector erase Value at left corresponds to size of 256 Mbit.
FLASH_PAGE_SIZE	(uint32_t)(64)	Page size (byte units) Value at left corresponds to size of 256 Mbit.
FLASH_ADDR_SIZE	(uint8_t)(4)	Address size (byte units) Value at left corresponds to size of 256 Mbit.
FLASH_WP_WHOLE_MEM	(uint8_t)(0x1f)	Whole-chip write protect Value at left corresponds to size of 256 Mbit.
FLASH_FULL_CHIP_ERASE	FLASH_MODE_B_ERASE	Supported erase-all command Value at left corresponds to size of 256 Mbit.
FLASH_ADDR_MODE	FLASH_MODE_4BYTE	Addressability Mode Value at left corresponds to size of 256 Mbit.
FLASH_CMD_SIZE	(uint8_t)1	Command size (byte units)
FLASH_STSREG_SIZE	(uint16_t)1	Status register size (byte units)
FLASH_IDDATA_SIZE	(uint16_t)20	ID data size (byte units)

Note: 1. The delay task for OS control. The OS control used in the sample code assumes µITRON 4.0.

Table 5-14 Values Defined in r_qspi_flash_n25q_sfr.h.rx63n

Constant Name	Setting Value	Contents
FLASH_DR_CS0	PORTA.PODR.BIT.B0	Device number 0 port output data register SFR definition
FLASH_DDR_CS0	PORTA.PDR.BIT.B0	Device number 0 port direction register SFR definition
FLASH_DR_CS1	—	Device number 1 port output data register SFR definition (This setting is needed when controlling two devices.)
FLASH_DDR_CS1	—	Device number 1 port direction register SFR definition (This setting is needed when controlling two devices.)
FLASH_HI	(uint8_t)(0x01)	Port "H"
FLASH_LOW	(uint8_t)(0x00)	Port "L"
FLASH_OUT	(uint8_t)(0x01)	Port Output Setting
FLASH_IN	(uint8_t)(0x00)	Port Input Setting
FLASH_BR	(uint8_t)(0x01)	Transfer rate for command transmission*1
FLASH_BR_WRITE_DATA	(uint8_t)(0x01)	Transfer rate for data transmission*1
FLASH_BR_READ_DATA	(uint8_t)(0x01)	Transfer rate for data reception*1

Note: 1. This value is set in the RSPI bit rate register (SPBR) when using the clock synchronous single master control software with the RSPI. The value shown is for a peripheral module clock setting of 48 [MHz] and a transfer rate of 12 [MHz].
This value is set in the bit rate register (BRR) when using the clock synchronous single master control software with SCI. The value shown is for a peripheral module clock setting of 48 [MHz] and a transfer rate of 6 [MHz].

Table 5-15 Values Defined in r_qspi_flash_n25q_sfr.h.rl78

Constant Name	Setting Value	Contents
FLASH_DR_CS0	P4.2	Device number 0 port register SFR definition
FLASH_DDR_CS0	PM4.2	Device number 0 port mode register SFR definition
FLASH_DR_CS1	—	Device number 1 port output data register SFR definition (This setting is needed when controlling two devices.)
FLASH_DDR_CS1	—	Device number 1 port direction register SFR definition (This setting is needed when controlling two devices.)
FLASH_HI	(uint8_t)(0x01)	Port "H"
FLASH_LOW	(uint8_t)(0x00)	Port "L"
FLASH_OUT	(uint8_t)(0x00)	Port Output Setting
FLASH_IN	(uint8_t)(0x01)	Port Input Setting
FLASH_BR	(uint8_t)(0x01)	Transfer rate for command transmission*1
FLASH_BR_WRITE_DATA	(uint8_t)(0x01)	Transfer rate for data transmission*1
FLASH_BR_READ_DATA	(uint8_t)(0x01)	Transfer rate for data reception*1

Note: 1. This value is set in bits 15 to 9 of the serial data register (SDR) when using the clock synchronous single master control software in the serial array unit CSI mode. The sample code uses this value with an operation clock setting of 24 [MHz] and a transfer rate or 6 [MHz].

Table 5-16 Values Defined in r_qspi_flash_n25q_sub.c

Constant Name	Setting Value	Contents
FLASH_SHORT_SIZE	(uint32_t)(0x00008000)	Maximum transfer size setting for low-level functions (max.: 32 KB)

Table 5-17 Values Defined in r_qspi_flash_n25q_sub.h

Constant Name	Setting Value	Contents
FLASH_BE_BUSY_WAIT	(uint32_t)(480000)	Bulk Erase Busy Timeout 480000 × 1 ms = 480s
FLASH_SE_BUSY_WAIT	(uint32_t)(3000)	Sector Erase Busy Timeout 3000 × 1 ms = 3 s
FLASH_SSE_BUSY_WAIT	(uint32_t)(3000)	Subsector Erase Busy Timeout 3000 × 1 ms = 3 s
FLASH_DE_BUSY_WAIT	(uint32_t)(480000)	Dei Erase Busy Timeout 480000 × 1 ms = 480 s
FLASH_WBUSY_WAIT	(uint32_t)(8000)	Write Ready Timeout 8000 × 1 µs = 8 ms
FLASH_T_WBUSY_WAIT	(uint16_t)MTL_T_1US	Write Busy Polling Time
FLASH_T_EBUSY_WAIT	(uint16_t)MTL_T_1MS	Erase Busy Polling Time
FLASH_T_CS_HOLD	(uint16_t)MTL_T_1US	CS Stability Waiting Time
FLASH_T_R_ACCESS	(uint16_t)MTL_T_1US	Reading Start Waiting Time
FLASH_REG_SRWD	(uint8_t)(0x80)	Status Register Write Disable
FLASH_REG_BP3	(uint8_t)(0x40)	Block Protection Bit3
FLASH_REG_TB	(uint8_t)(0x20)	Top/Bottom Bit
FLASH_REG_BP2	(uint8_t)(0x10)	Block Protection Bit2
FLASH_REG_BP1	(uint8_t)(0x08)	Block Protection Bit1
FLASH_REG_BP0	(uint8_t)(0x04)	Block Protection Bit0
FLASH_REG_WEL	(uint8_t)(0x02)	Write Enable Latch Bit
FLASH_REG_WIP	(uint8_t)(0x01)	Write In Progress Bit
FLASH_REG_MASK	(uint8_t)(0xfc)	Write status fixed data
FLASH_FSTSREG_READY	(uint8_t)(0x80)	Program or erase controller
FLASH_FSTSREG_ERASE	(uint8_t)(0x20)	Erase (flag status register)
FLASH_FSTSREG_PROG	(uint8_t)(0x10)	Program (flag status register)
FLASH_FSTSREG_VPP	(uint8_t)(0x08)	V_{PP} (flag status register)
FLASH_FSTSREG_PROT	(uint8_t)(0x02)	Protection (flag status register)

5.6 Structure/Union List

Show the Structure/Union Used in the Sample Code.

```
typedef union {
    uint32_t    ul;
    uint8_t     uc[4];
} flash_exchg_long_t;                   /* total 4bytes                                    */
```

Figure 5.6 Union Used in the Sample Code (Refer to r_qspi_flash_n25q_sub.c)

```
typedef struct
{
    uint32_t            Addr;       /* Address to issue a command                          */
    uint32_t            Cnt;        /* Number of bytes to be read/written                  */
    uint16_t            DataCnt;    /* Temporary counter or Number of bytes to be written in a page */
    uint8_t             rsv[2];     /* Reserved                                            */
    uint8_t FAR*        pData;      /* Data storage buffer pointer                         */
} r_qspi_flash_info_t;
```

Figure 5.7 Structure Used in the Sample Code (Refer to r_qspi_flash_n25q.h)

Table 5-18 Description of Structure "r_qspi_flash_info_t"

Structure Member	Allowable Setting Range	Description
Addr	0000 0000h to FFFF FFFFh	Write/read start address
Cnt	0000 0000h to FFFF FFFFh	Write/read data counter (byte units)
DataCnt	(Setting prohibited.)	Write: Write data counter temp. (max. 1 page) Read: Read data counter temp. (max. 32 KB)
rsv[2]	(Setting has no effect.)	For alignment adjustment
pData	—	Data storage buffer pointer Write: Storage source of data to be written in serial NOR flash memory Read: Storage destination of data to be read from serial NOR flash memory

5.7 Variable

The following table lists the static variable.

Table 5-19 Static Variable (Refer to r_qspi_flash_n25q_sub.c)

Type	Variable Name	Contents	Function Used
STATIC uint8_t	g_flash_cmdbuf[6]	Command buffer	r_qspi_flash_send_cmd r_qspi_flash_set_cmd

5.8 Functions

The following table lists the functions.

Table 5-20 Functions

Function Name	Outline
R_QSPI_FLASH_Init_Driver()	Driver initialization processing
R_QSPI_FLASH_Read_Status()	Status register read processing
R_QSPI_FLASH_Read_Flag_Status()	Flag status register read processing
R_QSPI_FLASH_Set_Write_Protect()	Write protect setting processing
R_QSPI_FLASH_Clear_Status()	Clear flag status processing
R_QSPI_FLASH_Write_Di	WRDI command issue processing
R_QSPI_FLASH_Read_Data()	Data read processing
R_QSPI_FLASH_Write_Data()	Data write processing
R_QSPI_FLASH_Write_Data_Page()	Data write processing (for single-page write)
R_QSPI_FLASH_Erase()	Erase processing
R_QSPI_FLASH_Read_ID()	ID read processing
R_QSPI_FLASH_Wait()	Busy wait processing
R_QSPI_FLASH_Set_Addressability_Mode()	Address mode setting processing

On cache-equipped MCUs, specify a non-cached area as the location of the read/write data storage buffer.

The read/write data storage buffer address is dependent on the lower-layer MCU-specific clock synchronous single master control software, and in some cases it is necessary to specify an address on a 4-byte boundary. For details, refer to the application note for the MCU-specific clock synchronous single master control software.

5.9 Function Specifications

The following tables list the sample code function specifications.

5.9.1 Driver Initialization Processing

R_QSPI_FLASH_Init_Driver

Outline	Driver initialization processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Init_Driver(void)
Description	• Calls the r_qspi_flash_init_port() function to initialize the CS# pin. • Calls the initialization function of the clock synchronous single master control software to initialize the I/O ports. • Call this function once at system startup
Arguments	None
Return Value	The initialization result is returned. FLASH_OK ; Successful operation FLASH_ERR_OTHER ; Other error The return value of r_qspi_flash_drvif_init_driver() is returned.

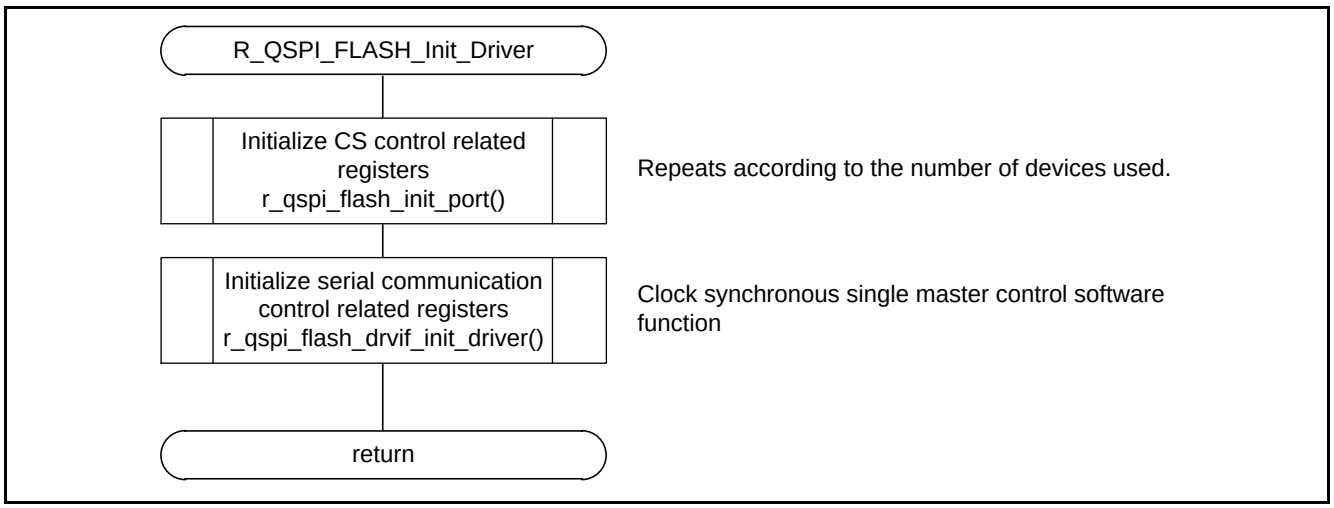


Figure 5.8 Overview of Driver Initialization Processing

5.9.2 Status Register Read Processing

R_QSPI_FLASH_Read_Status

Outline	Status register read processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Read_Status(uint8_t DevNo, uint8_t FAR* pStatus)
Description	• Reads the status register and stores the result in pStatus. Set 1 byte as a read buffer. • Stores the following information in the read status storage buffer (pStatus): Bit 7:SRWD 1: TB, BP3, BP2, BP1, BP0 are read-only bits 0: TB, BP3, BP2, BP1, BP0 are read/writable Bits 6 to 2: BP3, TB, BP2, BP1, BP0 Bit 1:WEL 1: Internal Write Enable Latch is set 0: Internal Write Enable Latch is reset Bit 0:WIP 1: Program or Erase cycle is in progress 0: No Program or Erase cycle is in progress • Refer to the data sheet of the serial NOR flash memory for the relationship between protect areas and protect bits. It is possible that the BP bits may not be allocated.
Arguments	uint8_t DevNo ; Device number uint8_t FAR* pStatus ; Read status storage buffer pointer
Return Value	The status register fetch result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

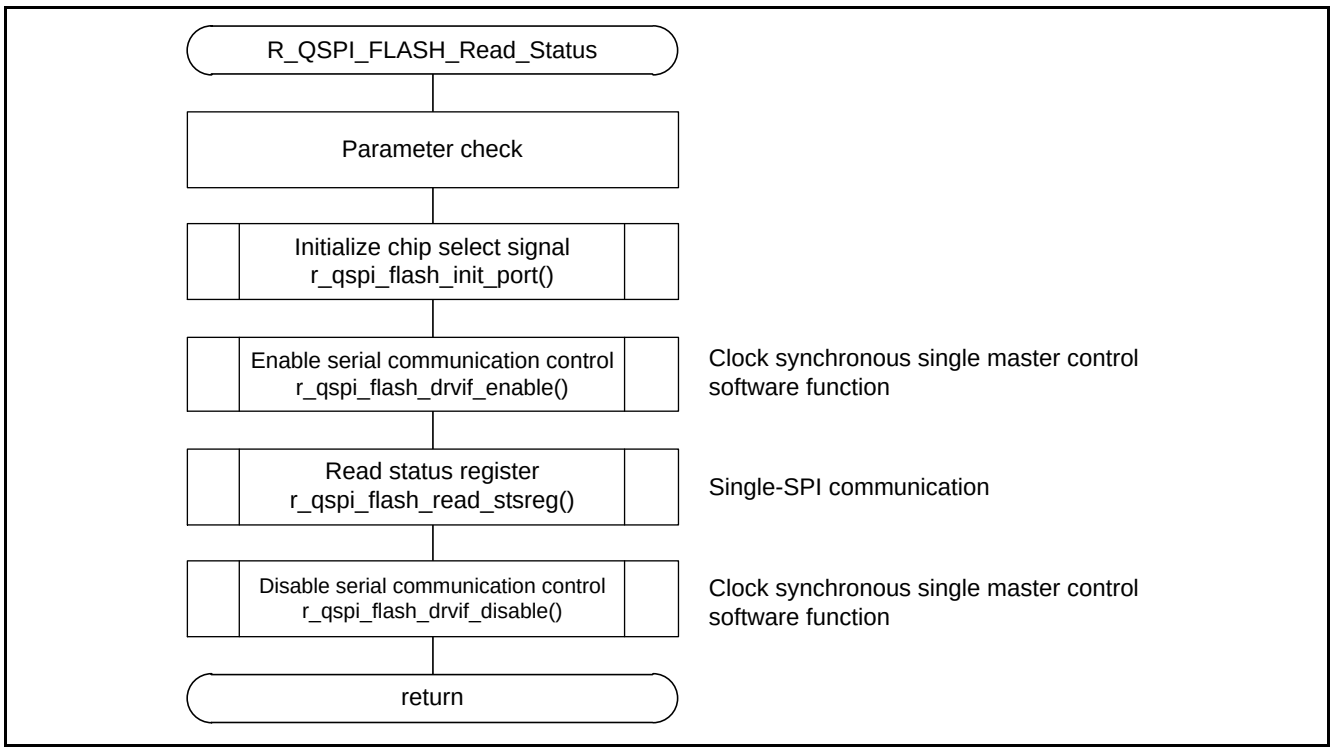


Figure 5.9 Overview of Status Register Read Processing

5.9.3 Flag Status Register Read Processing

R_QSPI_FLASH_Read_Flag_Status

Outline	Flag status register read processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Read_Flag_Status(uint8_t DevNo, uint8_t FAR* pFStatus)
Description	• Reads the flag status register and stores the result in pFStatus. Set 1 byte as a read buffer. • Stores the following information in the read flag status storage buffer (pFStatus): Bit 7: Program or erase controller 1: Ready 0: Busy Bits 6: Erase suspend 1: In effect 0: Not in effect Bits 5: Erase 1: Failure or protection error 0: Clear Bits 4: Program 1: Failure or protection error 0: Clear Bits 3: V_{PP} 1: Disable 0: Enabled Bits 2: Program suspend 1: In effect 0: Not in effect Bit 1: Protection 1: Failure or protection error 0: Clear Bit 0: Reserved
Arguments	uint8_t DevNo ; Device number uint8_t FAR* pFStatus ; Read flag status storage buffer pointer
Return Value	The flag status register fetch result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

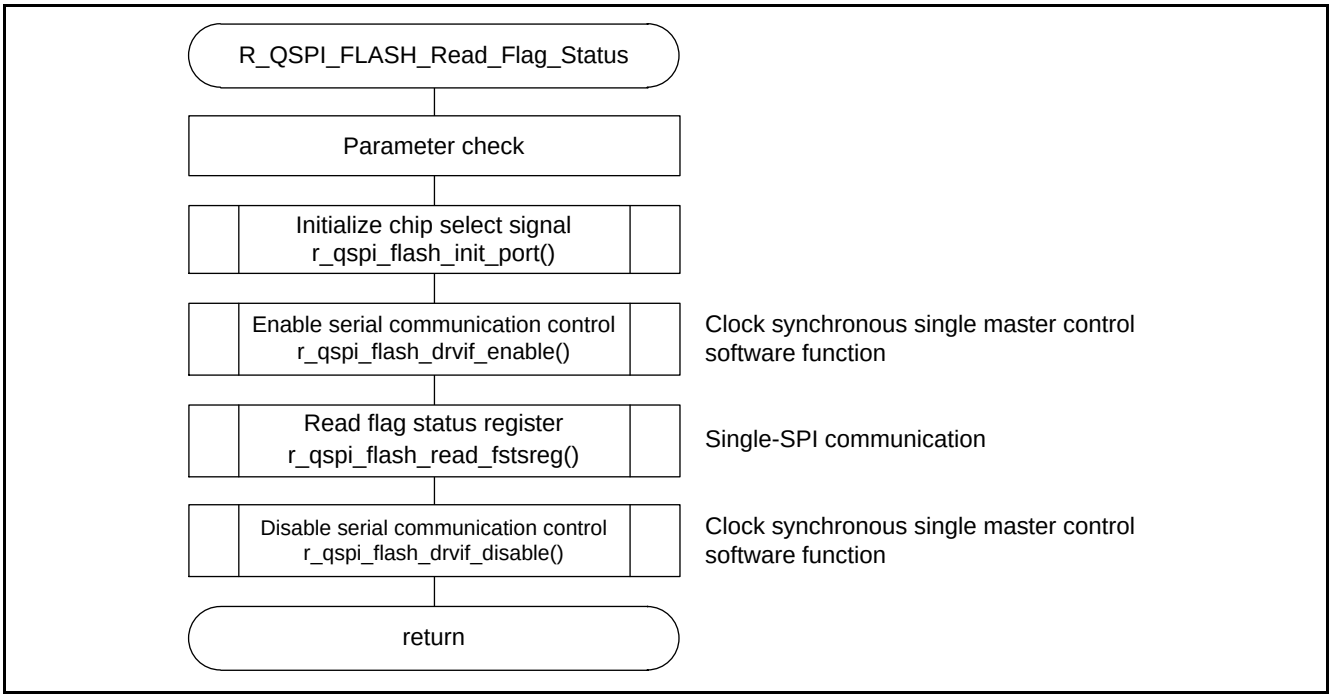


Figure5.10 Overview of Flag Status Register Read Processing

5.9.4 Write Protect Setting Processing

R_QSPI_FLASH_Set_Write_Protect

Outline Write protect setting processing

Header r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h

Declaration error_t R_QSPI_FLASH_Set_Write_Protect(uint8_t DevNo, uint8_t WpSts)

Description

- Makes write protect settings
- Make settings using the following write protect setting data (WpSts):

WpSts	BP3	TB1	BP2	BP1	BP0	Protected Area
0x00	0	0	0	0	0	None
0x01	0	0	0	0	1	Sector 2047
0x02	0	0	0	1	0	Sectors (2046 to 2047)
0x03	0	0	0	1	1	Sectors (2044 to 2047)
0x04	0	0	1	0	0	Sectors (2040 to 2047)
0x05	0	0	1	0	1	Sectors (2032 to 2047)
0x06	0	0	1	1	0	Sectors (2016 to 2047)
0x07	0	0	1	1	1	Sectors (1984 to 2047)
0x10	1	0	0	0	0	Sectors (1920 to 2047)
0x11	1	0	0	0	1	Sectors (1792 to 2047)
0x12	1	0	0	1	0	Sectors (1536 to 2047)
0x13	1	0	0	1	1	Sectors (1024 to 2047)
0x14 – 0x17	1	0	1	0/1	0/1	All sectors
0x08	0	1	0	0	0	None
0x09	0	1	0	0	1	Sector 0
0x0a	0	1	0	1	0	Sectors (0 to 1)
0x0b	0	1	0	1	1	Sectors (0 to 3)
0x0c	0	1	1	0	0	Sectors (0 to 7)
0x0d	0	1	1	0	1	Sectors (0 to 15)
0x0e	0	1	1	1	0	Sectors (0 to 31)
0x0f	0	1	1	1	1	Sectors (0 to 63)
0x18	1	1	0	0	0	Sectors (0 to 127)
0x19	1	1	0	0	1	Sectors (0 to 255)
0x1a	1	1	0	1	0	Sectors (0 to 511)
0x1b	1	1	0	1	1	Sectors (0 to 1023)
0x1c – 0x1f	1	1	1	0/1	0/1	All sectors

- Clears SRWD to 0.
- Refer to the data sheet of the serial NOR flash memory for the relationship between protect areas and protect bits. It is possible that the BP bits may not be allocated.
- There are two ways to wait for write completion. These are described below. Note that the next processing task (write, read, erase, etc.) should be executed after confirming write completion.
- To use the user API to wait for write completion, enable FLASH_WAIT_READY in r_qspi_flash_n25q.h.
- To wait for write completion without using the user API, disable FLASH_WAIT_READY in r_qspi_flash_n25q.h and call R_QSPI_FLASH_Wait() after processing by the user API finishes. This processing method allows the use of a user-defined duration when waiting for write completion. Refer to figure 5.12 for the usage method.

- To confirm whether or not protect was applied successfully, read the status register. In addition, if the WEL bit has be set to 1, execute the WRDI command issue processing function (R_QSPI_FLASH_Write_Di()).

Arguments

```
uint8_t     DevNo     ; Device number
uint8_t     WpSts     ; Write protect setting data
```

Return Value

The write protect setting result is returned.

```
FLASH_OK            ; Successful operation
FLASH_ERR_PARAM     ; Parameter error
FLASH_ERR_HARD      ; Hardware error
FLASH_ERR_TIMEOUT   ; Time out error (FLASH_WAIT_READY enabled)
FLASH_ERR_OTHER     ; Other error
```

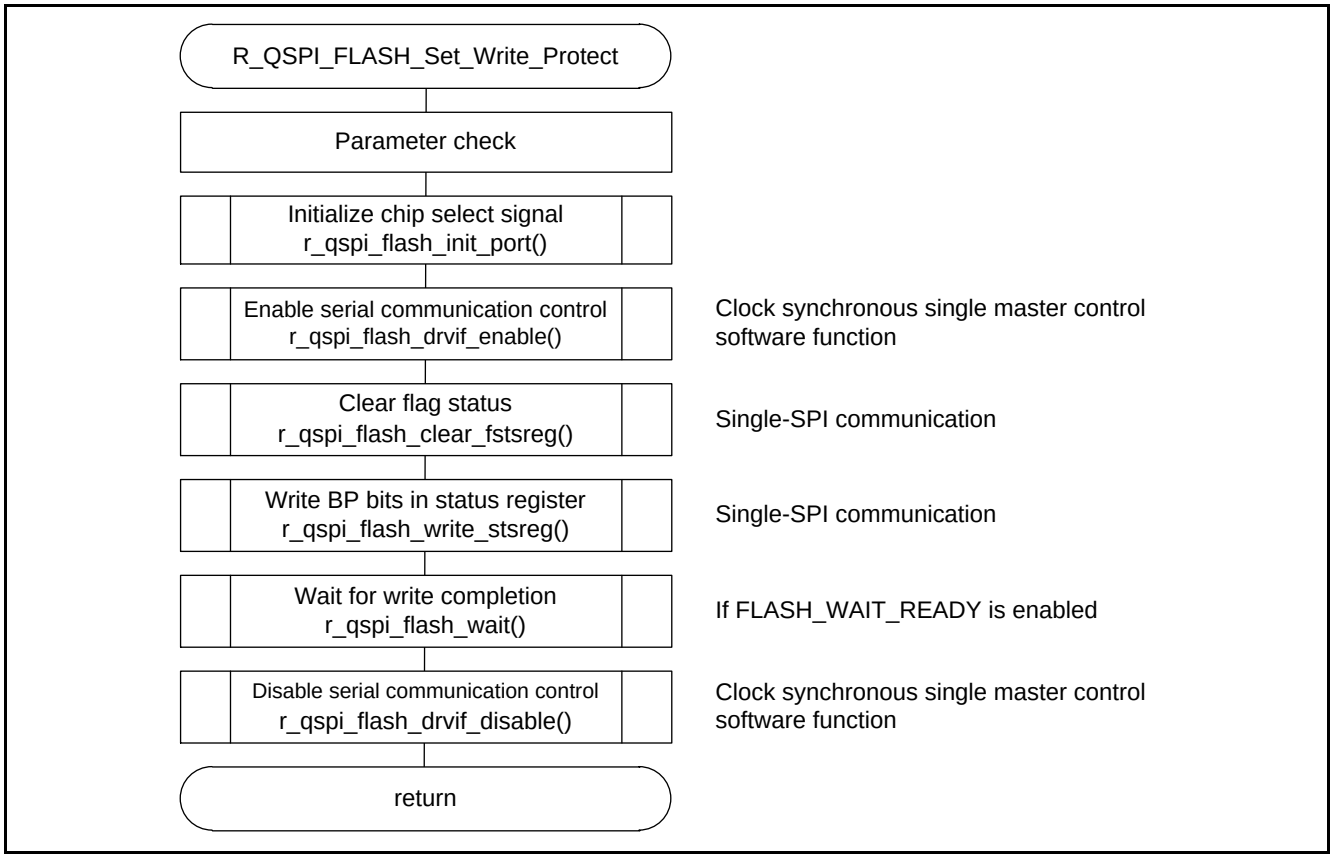


Figure 5.11 Overview of Write Protect Setting Processing

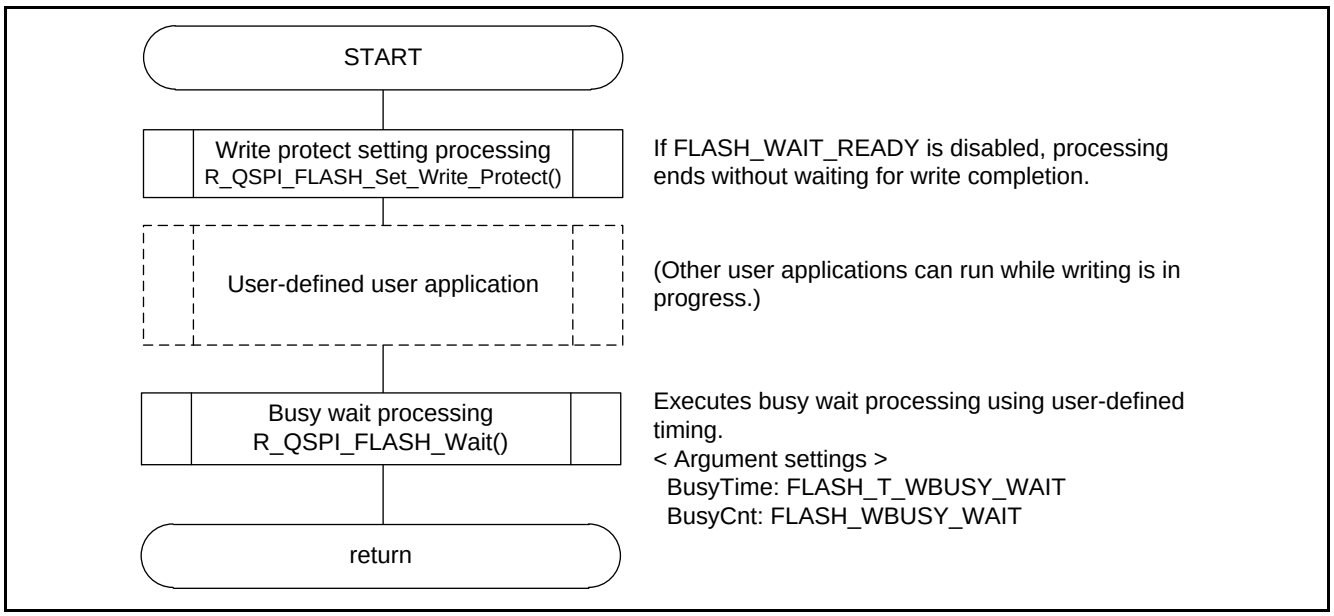


Figure 5.12 Using R_QSPI_FLASH_Wait() to Wait for Write Protect Setting Completion

5.9.5 Clear Flag Status Processing

R_QSPI_FLASH_Clear_Status

Outline	Clear flag status processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Clear_Status(uint8_t DevNo)
Description	• Clears the error bits in the flag status register. • When a programming error, erase error, or write protect error occurs, this function must be called to clear the error bits.
Arguments	uint8_t DevNo ; Device number
Return Value	The clearing result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

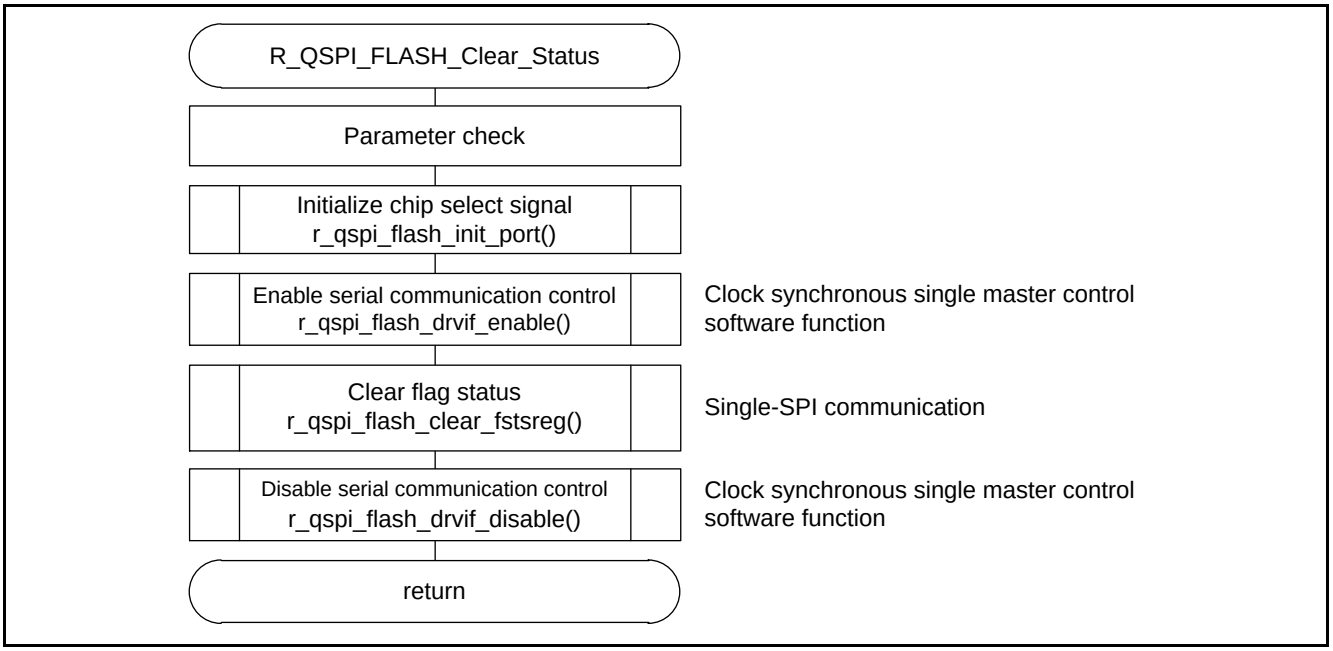


Figure 5.13 Overview of Clear Flag Status Processing

5.9.6 WRDI Command Issue Processing

R_QSPI_FLASH_Write_Di

Outline	WRDI command issue processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Write_Di(uint8_t DevNo)
Description	• Clears the WEL bit in the status register. • When a programming error, erase error, or write protect error occurs, this function must be called to clear the WEL bit.
Arguments	uint8_t DevNo ; Device number
Return Value	The clearing result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

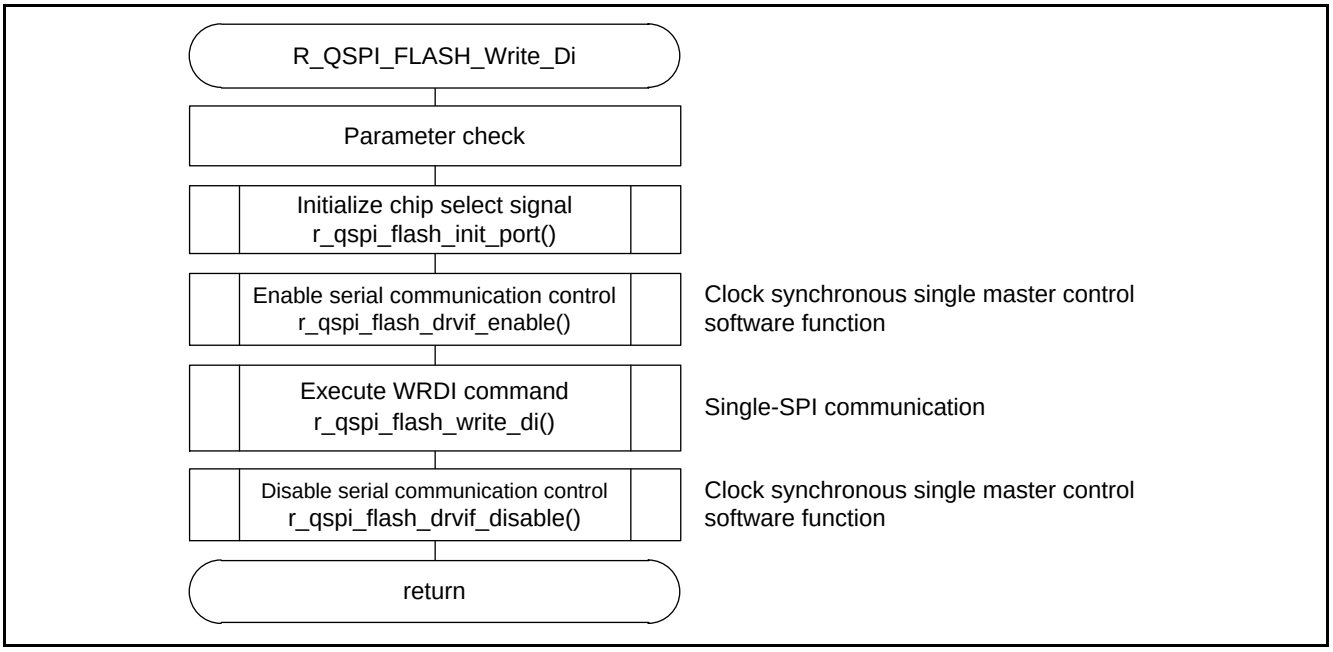


Figure 5.14 Overview of WRDI Command Issue Processing

5.9.7 Data Read Processing

R_QSPI_FLASH_Read_Data

Outline	Data read processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Read_Data(uint8_t DevNo, r_qspi_flash_info_t FAR* pFlash_Info)
Description	• Reads the specified number of bytes of data from the specified address in the serial NOR flash memory, and stores it in pData. • The final read address is equal to the serial NOR flash memory capacity – 1. • It is not possible to continue reading by means of a rollover. After reading the final address, end processing once and then call the user API again after specifying a new address.
Arguments	uint8_t DevNo ; Device number r_qspi_flash_info_t FAR* pFlash_Info ; FLASH communication information structure uint32_t Addr ; Read start address uint32_t Cnt ; Read byte count uint16_t DataCnt ; Read byte temp. (setting prohibited) uint8_t FAR* pData ; Read data storage buffer pointer
Return Value	The read result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

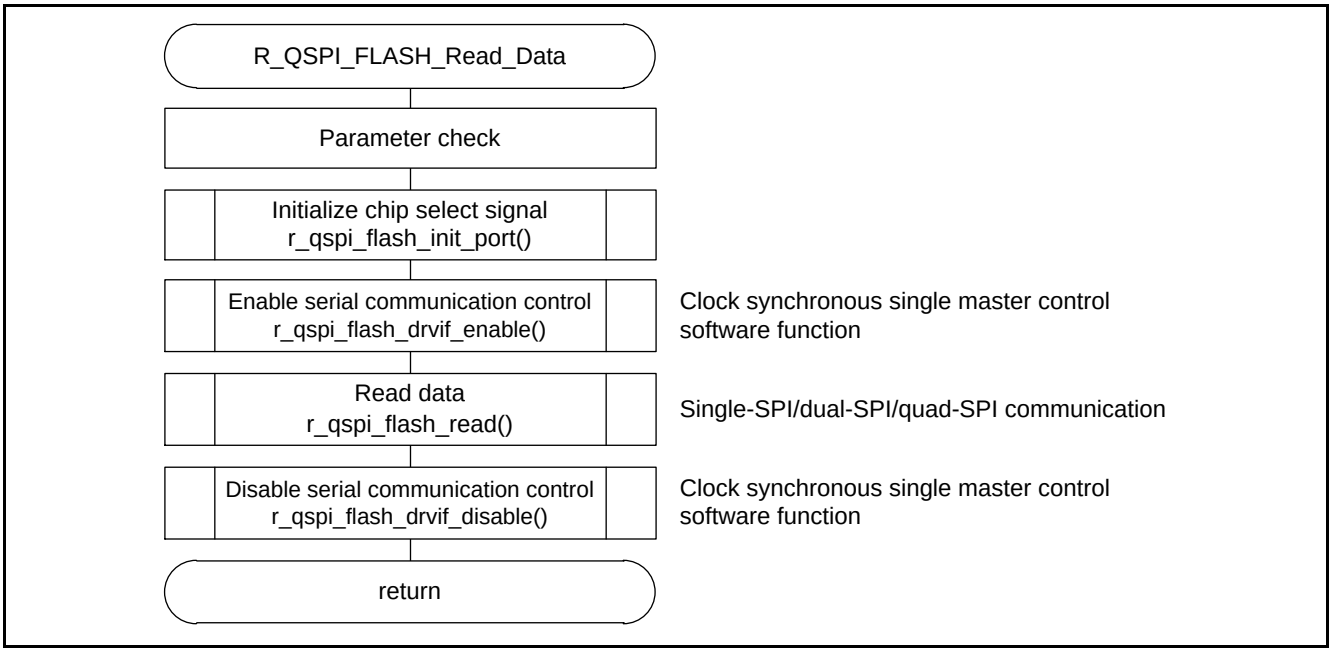


Figure 5.15 Overview of Data Read Processing

5.9.8 Data Write Processing

R_QSPI_FLASH_Write_Data

Outline	Data write processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Write_Data(uint8_t DevNo, r_qspi_flash_info_t FAR* pFlash_Info)
Description	• Writes the specified number of bytes of the data in pData to the specified address in the serial NOR flash memory. • Writing to the serial NOR flash memory can only be performed to areas with write protect disabled. It is not possible to write to areas where protect is enabled. FLASH_ERR_WP is returned when a write is attempted. • The final write address is equal to the serial NOR flash memory capacity – 1. • The maximum value that can be set for the write byte count (Cnt) is equal to the serial NOR flash memory capacity. • The user API performs a wait for write completion regardless of the setting of FLASH_WAIT_READY in r_qspi_flash_n25q.h. • When the return value is FLASH_ERR_WP or FLASH_ERR_OTHER, an error bit has been set in the flag status register and clear flag status processing should be performed. To clear the WEL bit in the status register, perform WRDI command issue processing.
Arguments	uint8_t DevNo ; Device number r_qspi_flash_info_t FAR* pFlash_Info ; Flash communication information structure uint32_t Addr ; Write start address uint32_t Cnt ; Write byte count uint16_t DataCnt ; Write byte temp. (setting prohibited) uint8_t FAR* pData ; Write data storage buffer pointer
Return Value	The read result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_WP ; Write-protection error FLASH_ERR_TIMEOUT ; Time out error FLASH_ERR_OTHER ; Other error

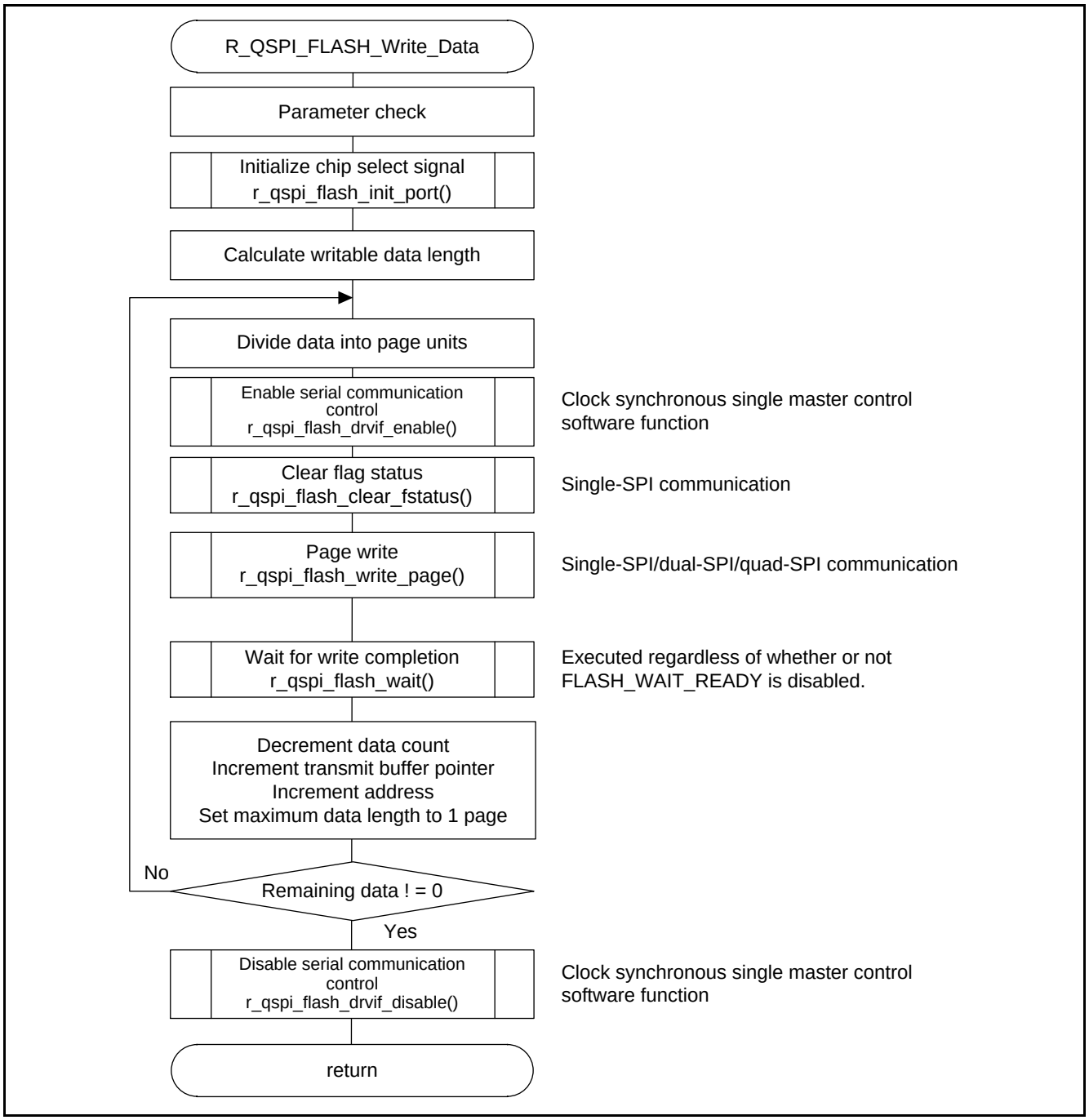


Figure 5.16 Overview of Data Write Processing

5.9.9 Data Write Processing (for single-page write)

R_QSPI_FLASH_Write_Data_Page

Outline Data write processing (for single-page write)

Header r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h

Declaration error_t R_QSPI_FLASH_Write_Data_Page(uint8_t DevNo, r_qspi_flash_info_t FAR* pFlash_Info)

Description

- Writes the specified number of bytes (maximum: 1 page) of the data in pData to the specified address in the serial NOR flash memory.
- Writing to the serial NOR flash memory can only be performed to areas with write protect disabled. It is not possible to write to areas where protect is enabled. FLASH_ERR_WP is returned when a write is attempted.
- It is not possible to write to areas where protect is enabled. When a write is attempted, an error is returned.
- The final write address is equal to the serial NOR flash memory capacity – 1.
- The maximum value that can be set for the write byte count (Cnt) is equal to the serial NOR flash memory capacity.
- Even if a byte count that exceeds one page is specified, the remaining byte count and the next address information remains in the FLASH communication information structure (pFlash_Info) after write processing of one page finishes. It is possible to write the remaining byte count by setting pFlash_Info once again without modification.
- There are two ways to wait for write completion. These are described below. Note that the next processing task (write, read, erase, etc.) should be executed after confirming write completion.
- To use the user API to wait for write completion, enable FLASH_WAIT_READY in r_qspi_flash_n25q.h.
- To wait for write completion without using the user API, disable FLASH_WAIT_READY in r_qspi_flash_n25q.h and call R_QSPI_FLASH_Wait() after processing by the user API finishes. This processing method allows the use of a user-defined duration when waiting for write completion. Refer to figure 5.18 for the usage method.
- When the return value is FLASH_ERR_WP or FLASH_ERR_OTHER, an error bit has been set in the flag status register and clear flag status processing should be performed. To clear the WEL bit in the status register, perform WRDI command issue processing.

Arguments

```
uint8_t              DevNo          ; Device number
r_qspi_flash_info_t FAR* pFlash_Info ; FLASH communication information structure
        uint32_t     Addr           ; Write start address
        uint32_t     Cnt            ; Write byte count
        uint16_t     DataCnt        ; Write byte temp. (setting prohibited)
        uint8_t FAR* pData          ; Write data storage buffer pointer
```

Return Value The read result is returned.

```
FLASH_OK          ; Successful operation
FLASH_ERR_PARAM   ; Parameter error
FLASH_ERR_HARD    ; Hardware error
FLASH_ERR_WP      ; Write-protection error (FLASH_WAIT_READY enabled)
FLASH_ERR_TIMEOUT; Time out error (FLASH_WAIT_READY enabled)
FLASH_ERR_OTHER   ; Other error
```

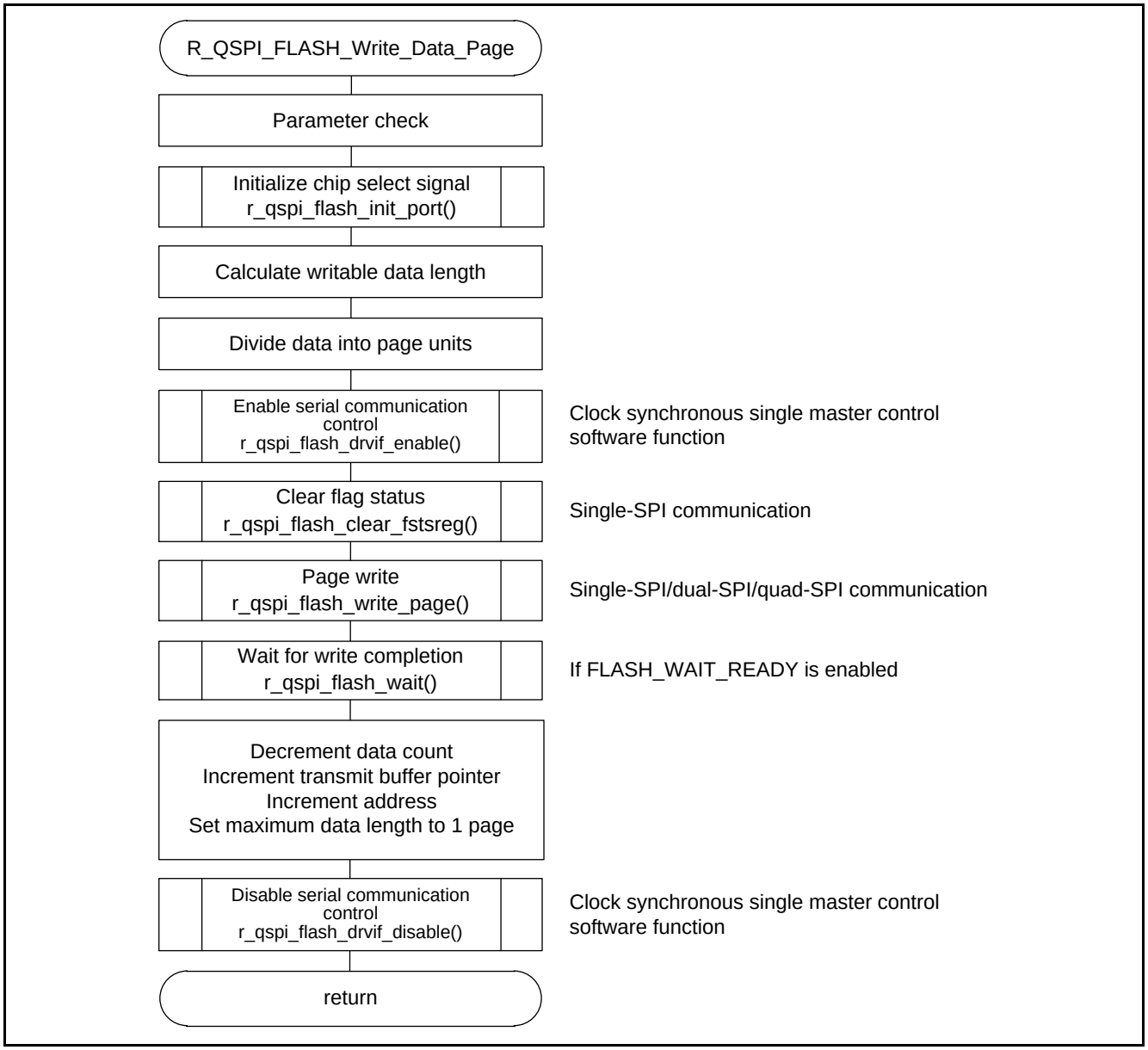


Figure 5.17 Overview of Data Write Processing (for single-page write)

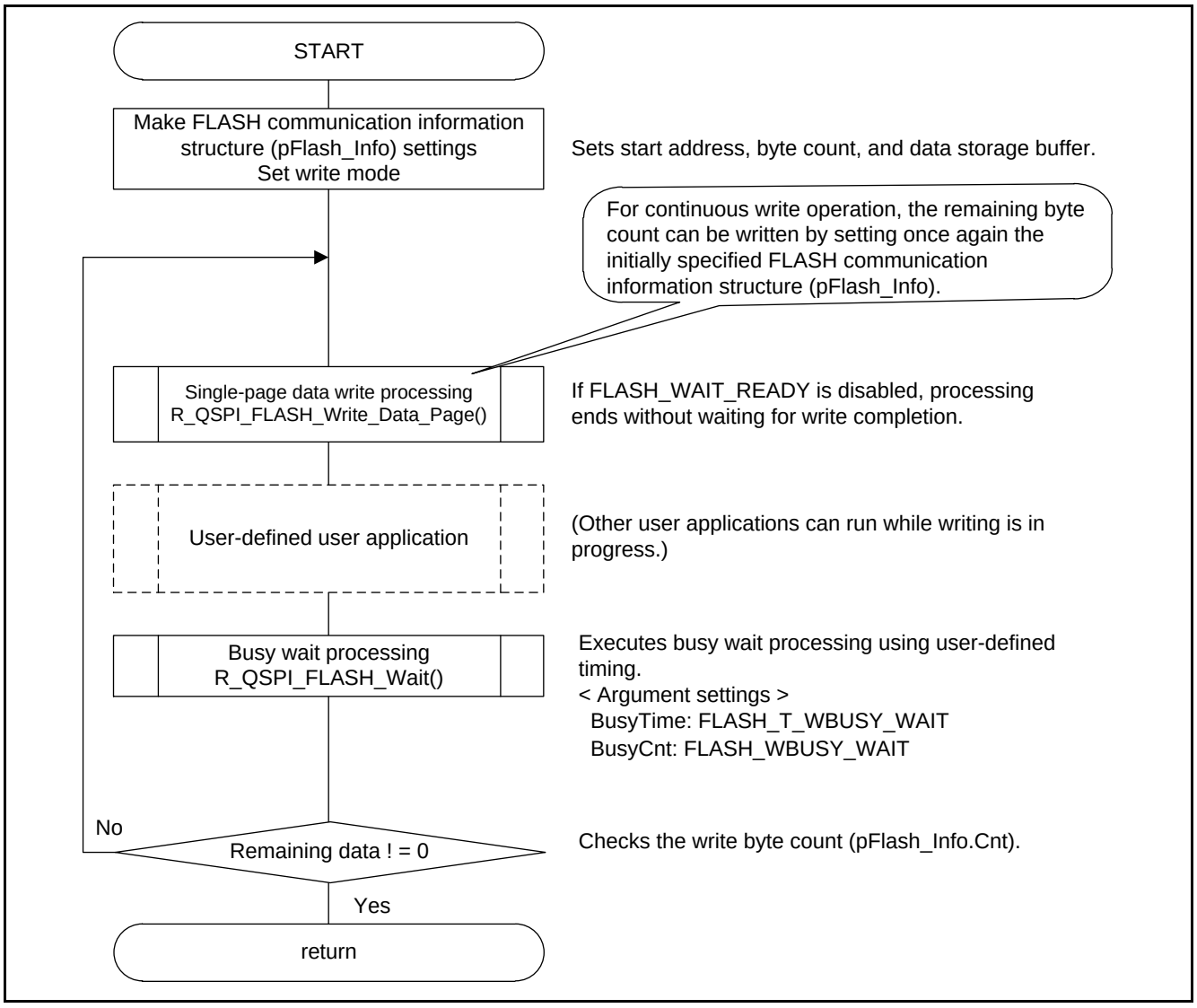


Figure 5.18 Using R_QSPI_FLASH_Wait() to Wait for Data Write Processing (for Single-Page Write) Completion

5.9.10 Erase Processing

R_QSPI_FLASH_Erase

Outline Erase processing

Header r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h

Declaration error_t R_QSPI_FLASH_Erase(uint8_t DevNo, uint32_t Addr, uint8_t Mode)

Description

- Erases all the data in the memory (bulk erase), all the data in a specified sector (sector erase), all the data in a specified subsector (subsector erase), or all the data in a specified die (die erase) by using the Mode setting.
- For bulk erase, set Addr to 0x00000000.
- For die erase, set Addr to the start address of the specific die.
- Erasing the serial NOR flash memory can only be performed on areas with write protect disabled.
- It is not possible to erase areas where protect is enabled. Executing a wait for erase completion causes FLASH_ERR_WP to be returned.
- There are two ways to wait for erase completion. These are described below. Note that the next processing task (write, read, erase, etc.) should be executed after confirming erase completion.
- To use the user API to wait for completion, enable FLASH_WAIT_READY in r_qspi_flash_n25q.h.
- To wait for completion without using the user API, disable FLASH_WAIT_READY in r_qspi_flash_n25q.h and call R_QSPI_FLASH_Wait() after processing by the user API finishes. This processing method allows the use of a user-defined duration when waiting for completion. Refer to figure 5.20 for the usage method.
- The argument setting (BusyCnt) when calling R_QSPI_FLASH_Wait() differs depending on the erase mode.

  Bulk Erase; BusyCnt = FLASH_BE_BUSY_WAIT
  Sector Erase; BusyCnt = FLASH_SE_BUSY_WAIT
  Subsector Erase; BusyCnt = FLASH_SSE_BUSY_WAIT
  Die Erase; BusyCnt = FLASH_DE_BUSY_WAIT
- When the return value is FLASH_ERR_WP or FLASH_ERR_OTHER, an error bit has been set in the flag status register and clear flag status processing should be performed. To clear the WEL bit in the status register, perform WRDI command issue processing.

Arguments

```
uint8_t     DevNo   ; Device number
uint32_t    Addr    ; Erase address
uint8_t     Mode    ; Erase mode (selectable from the following):
                        FLASH_MODE_B_ERASE
                        FLASH_MODE_S_ERASE
                        FLASH_MODE_SS_ERASE
                        FLASH_MODE_D_ERASE
```

Return Value The erase result is returned.

```
FLASH_OK            ; Successful operation
FLASH_ERR_PARAM     ; Parameter error
FLASH_ERR_HARD      ; Hardware error
FLASH_ERR_WP        ; Write-protection error (FLASH_WAIT_READY enabled)
FLASH_ERR_TIMEOUT; Time out error (FLASH_WAIT_READY enabled)
FLASH_ERR_OTHER     ; Other error
```

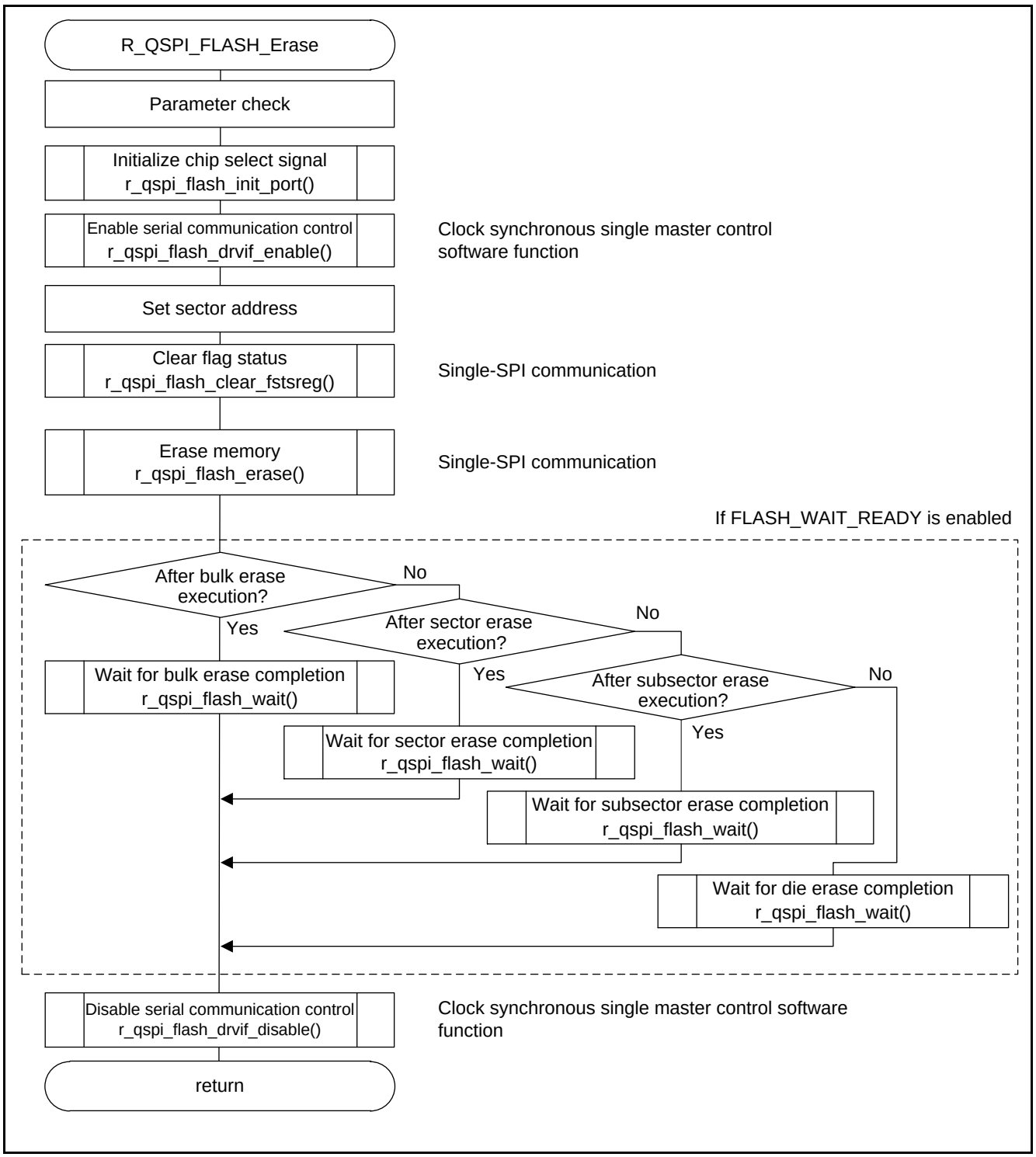


Figure 5.19 Overview of Erase Processing

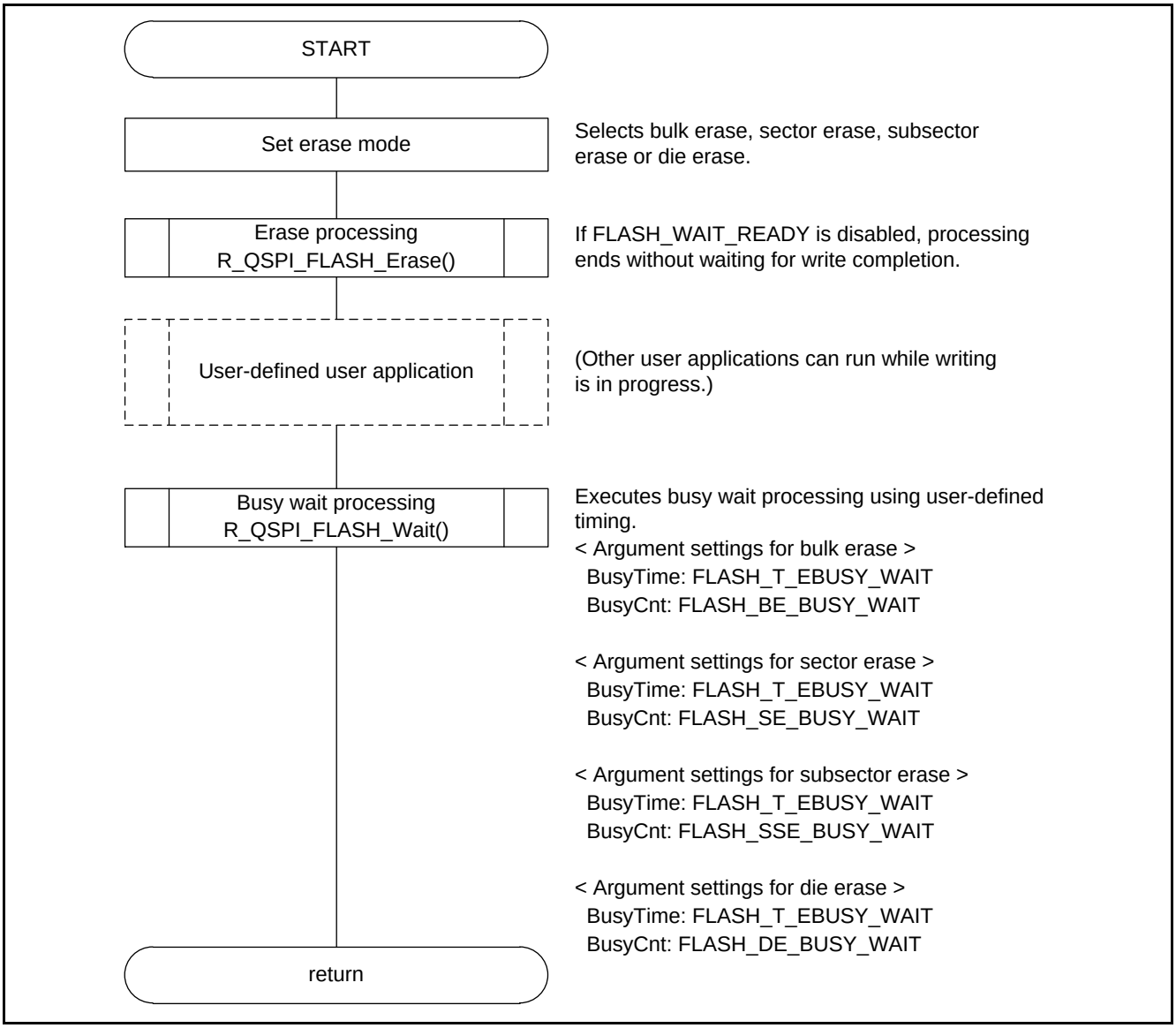


Figure 5.20 Using R_QSPI_FLASH_Wait() to Wait for Erase Processing Completion

5.9.11 ID Read Processing

R_QSPI_FLASH_ReadID

Outline	ID read processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Read_ID(uint8_t DevNo, uint8_t FAR* pData)
Description	• Reads the manufacturer ID and device ID, and stores them in pData. Set 20 bytes as a read buffer. • Stores the following information in the read status storage buffer (pData): (1) Manufacturer ID (2) Memory Type (3) Memory Capacity (4) Length of data to follow (5) Extended device ID and device configuration information (6 - 20) Customized factory data
Arguments	uint8_t DevNo ; Device number uint8_t FAR* pData ; Read data storage buffer pointer
Return Value	The read result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

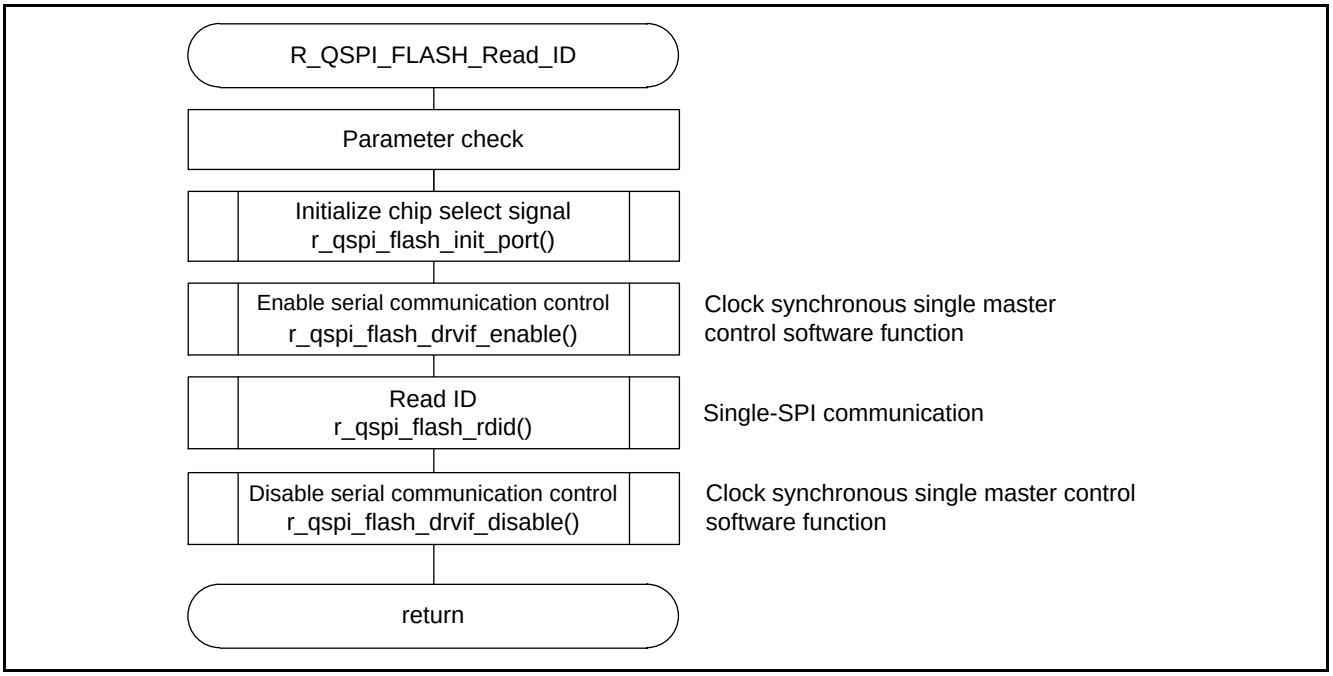


Figure 5.21 Overview of ID Read Processing

5.9.12 Busy Wait Processing

R_QSPI_FLASH_Wait

Outline Busy wait processing

Header r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h

Declaration error_t R_QSPI_FLASH_Wait(uint8_t DevNo, uint16_t BusyTime, uint32_t BusyCnt, uint8_t Mode)

Description

- Use this function to confirm completion of write or erase when FLASH_WAIT_READY is disabled.
- When BusyCnt = 0, a wait is performed for a busy period equal to the BusyTime interval.
- When BusyCnt ≠ 0, a wait is performed for a busy period equal to the BusyTime interval multiplied by BusyCnt. If the busy state exceeds the BusyCnt, FLASH_ERR_TIMEOUT is returned.
- Performs wait for register write, data write, or erase, according to the Mode setting.
  FLASH_MODE_REG_WRITE: Register write mode
  FLASH_MODE_PROG_ERASE: Data write and erase mode
- In register write mode (small-capacity products of 256 Mbits or less), the function issues the RDSR command and determines the ready/busy state by means of the WIP bit.
- In register write mode (512 Mbit and 1 Gbit products), the function issues the RDFSR command and determines the ready/busy state by means of the program or erase controller bit. The device is determined to be in the ready state when the read value of the program or erase controller is 1 (ready) twice in succession for 512 Mbit products, or four times in succession for 1 Gbit products.
- In data write and erase mode, the function first determines the ready/busy state by means of the WIP bit. If the WIP bit indicates the ready state, the function issues the RDFSR command and determines the ready/busy state by means of the program or erase controller bit.
- When the value of the protection error bit is 1, FLASH_ERR_WP is returned.
- When the value of the protection error bit is 0, and the value of the erase, programming, or V_{PP} error bit is 1, FLASH_ERR_OTHER is returned.
- The BusyCnt and BusyTime setting values are different for writing and erasing. A timeout error may occur if busy wait takes place using other than the expected settings. Make settings according to the following table:

State	BusyTime	BusyCnt
Status register write in progress (write protect bit set)	FLASH_T_WBUSY_WAIT	FLASH_WBUSY_WAIT
Data write in progress	FLASH_T_WBUSY_WAIT	FLASH_WBUSY_WAIT
Erase in progress (bulk erase)	FLASH_T_EBUSY_WAIT	FLASH_BE_BUSY_WAIT
Erase in progress (sector erase)	FLASH_T_EBUSY_WAIT	FLASH_SE_BUSY_WAIT
Erase in progress (subsector erase)	FLASH_T_EBUSY_WAIT	FLASH_SSE_BUSY_WAIT
Erase in progress (die erase)	FLASH_T_EBUSY_WAIT	FLASH_DE_BUSY_WAIT

Arguments

```
uint8_t   DevNo      ; Device number
uint16_t  BusyTime   ; Wait duration (selectable from the following):
                       FLASH_T_WBUSY_WAIT: Write
                       FLASH_T_EBUSY_WAIT: Erase
uint32_t  BusyCnt    ; Counter (selectable from the following):
                       FLASH_WBUSY_WAIT: Write
                       FLASH_BE_BUSY_WAIT: Erase (Bulk Erase)
                       FLASH_SE_BUSY_WAIT: Erase (Sector Erase)
                       FLASH_SSE_BUSY_WAIT: Erase (Subsector Erase)
                       FLASH_DE_BUSY_WAIT: Erase (Die Erase)
uint8_t   Mode       ; Wait mode (selectable from the following):
                       FLASH_MODE_REG_WRITE: Register write
                       FLASH_MODE_PROG_ERASE: Data write and erase
```

Return Value

The wait result is returned.

```
FLASH_OK           ; Successful operation
FLASH_ERR_PARAM    ; Parameter error
FLASH_ERR_HARD     ; Hardware error
FLASH_ERR_WP       ; Write-protection error
FLASH_ERR_TIMEOUT  ; Time out error (when BusyCnt ≠ 0)
FLASH_ERR_OTHER    ; Other error
```

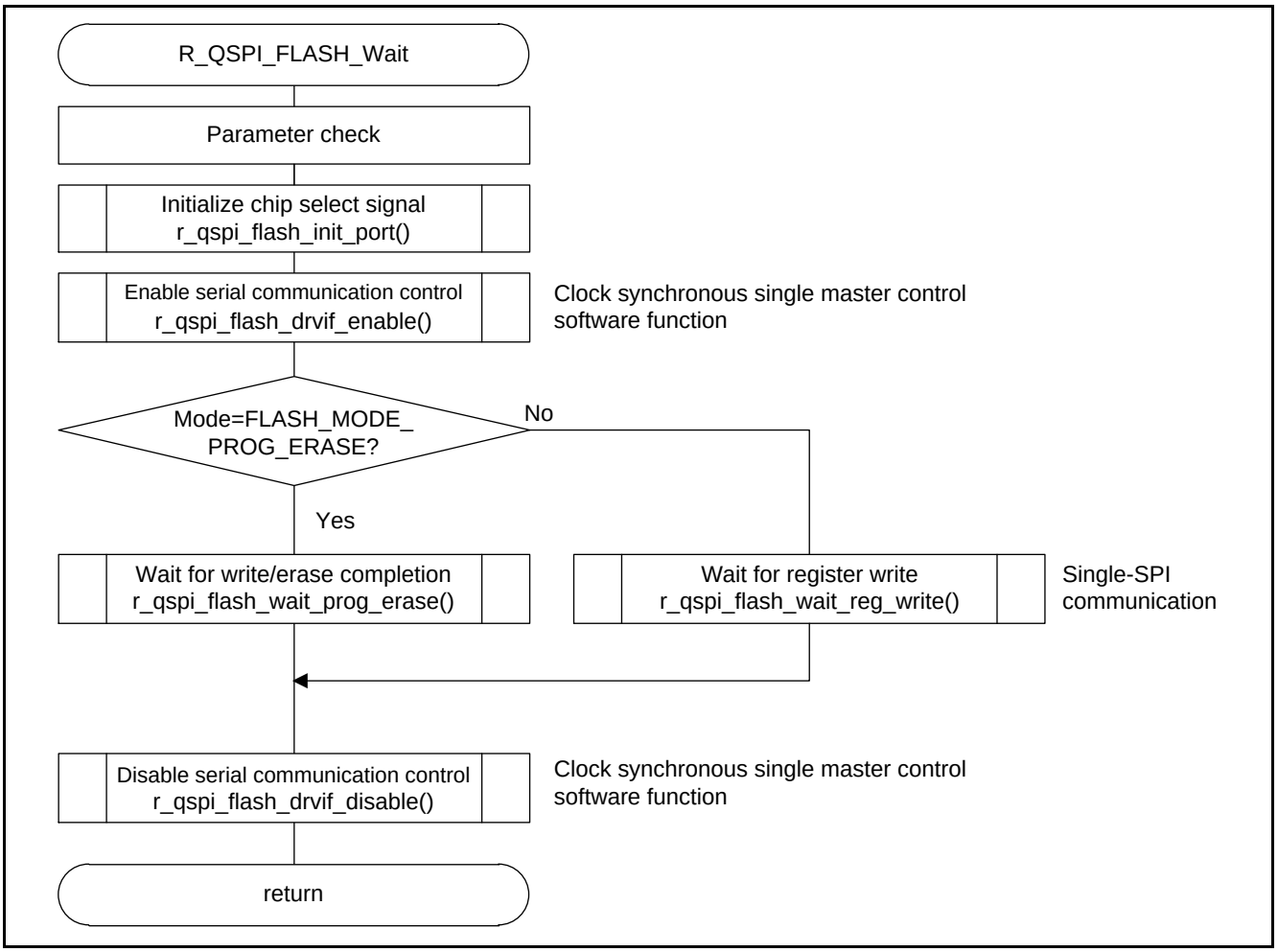


Figure 5.20 Overview of Busy Wait Processing

5.9.13 Address Mode Setting Processing

R_QSPI_FLASH_Set_Addressability_Mode

Outline	Address mode setting processing
Header	r_qspi_flash_n25q.h, r_qspi_flash_n25q_sub.h, r_qspi_flash_n25q_sfr.h, r_qspi_flash_n25q_drvif.h
Declaration	error_t R_QSPI_FLASH_Set_Addressability_Mode (uint8_t DevNo)
Description	• Calls the r_qspi_flash_enter_4addr() function to enable 4-byte address mode. • At system startup, call this function once after calling the R_QSPI_FLASH_Init_Driver() function.
Arguments	uint8_t DevNo ; Device number
Return Value	The address mode setting result is returned. FLASH_OK ; Successful operation FLASH_ERR_PARAM ; Parameter error FLASH_ERR_HARD ; Hardware error FLASH_ERR_OTHER ; Other error

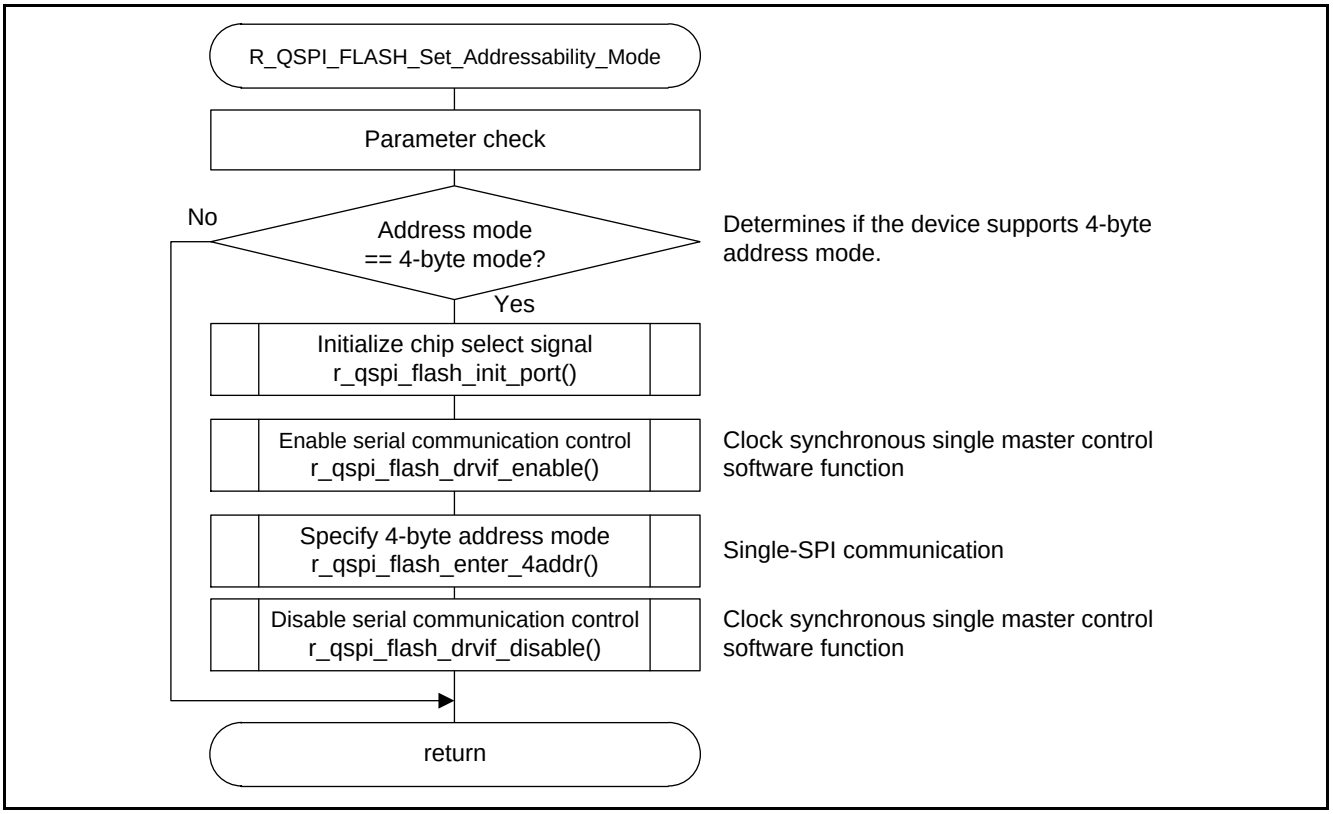


Figure 5.23 Overview of Address Mode Setting Processing

6. Application Example

Example settings for the serial NOR flash memory control portion are shown below. (The serial I/O control portion is not covered.)

Refer to the MCU-specific application note on the clock synchronous single master control software for details of the serial I/O control portion.

Note that the communication speed requires settings for each individual slave device, and these setting are included in the sample code.

The setting locations are designated in each file by the comment /** SET **/.

In addition, for functions used in common (mtl_wait_lp(), etc.), make sure to use the versions included in the MCU-specific clock synchronous single master control software.

6.1 Serial NOR Flash Memory Control Software Settings

The setting locations are designated in each file by the comment /** SET **/.

6.1.1 r_qspi_flash_n25q.h

This is the definition file for the serial NOR flash memory.

The setting locations are designated in each file by the comment /** SET **/.

(1) Definition of Number of Devices Used and Device Numbers

Specify the number of devices to be used, and allocate a number to each device.

In the example below, one device is used, and it is allocated the device number 0.

Up to two devices can be controlled.

```
/*------------------------------------------------------------------------- */
/* Define number of required serial FLASH devices.(1~N devices)             */
/* Define the device number in accordance with the number of serial FLASH   */
/* devices to be connected.                                                 */
/*------------------------------------------------------------------------- */
/* Define no. of devices */
#define FLASH_DEV_NUM           (1)                 /* 1device          */

/* Define no. of slots */
#define FLASH_DEV0              (0)                 /* Device 0         */
#define FLASH_DEV1              (1)                 /* Device 1         */
```

(2) Definition of Capacity of Device Used

Specify the capacity of the device(s) used.

In the example below, a device with a capacity of 256 Mbit is used.

```
/*------------------------------------------------------------------------- */
/*  Define the serial FLASH device.                                         */
/*------------------------------------------------------------------------- */

//#define N25Q32M                               /*  32Mbit  (  4MByte)      */
//#define N25Q64M                               /*  64Mbit  (  8MByte)      */
//#define N25Q128M                              /* 128Mbit  ( 16MByte)      */
#define N25Q256M                                /* 256Mbit  ( 32MByte)      */
//#define N25Q512M                              /* 512Mbit  ( 64MByte)      */
//#define N25Q1G                                /*   1Gbit  (128MByte)      */
```

(3) Delay Task Wait Time Setting (Valid when OS Control is Used)

This setting specifies the OS control* delay task wait time. The unit is ms.

In the example below, a setting of 1 ms is used.

```
/*-------- Definitions of delay task wait time ---------*/
#define FLASH_DELAY_TASK  (uint8_t)(1) /* OS delay task wait time (Uint:ms)  */
```

Note: * The OS control used in the sample code assumes µITRON 4.0.

(4) Write/Erase Completion Wait Processing Integration Setting

The functions listed below support a setting designating waiting for completion following execution of a command. To designate waiting for completion, enable the setting.

Affected functions:

- Write protect setting processing (R_QSPI_FLASH_Set_Write_Protect())
- Data write processing (for single-page write) (R_QSPI_FLASH_Write_Data_Page())
- Erase processing (R_QSPI_FLASH_Erase())

In the example below, waiting for completion is enabled.

```
/*-------- Definitions of using wait ---------*/
/* When you wait completion a Flash memory writing or erasing, please define it.*/
#define FLASH_WAIT_READY
```

6.1.2 r_qspi_flash_n25q_sfr.h

A separate version of r_qspi_flash_n25q_sfr.h.XXX is provided for each MCU model. Rename the version appropriate for the system to r_qspi_flash_n25q_sfr.h in order to use it. If there is no available version corresponding to the MCU to be used, refer to the information below and create an appropriate version of r_qspi_flash_n25q_sfr.h.

The setting locations are designated in each file by the comment /** SET **/.

(1) Chip Select Signal Setting

Define the port SFR of the chip select signal to be used.

When connecting two devices, two ports must be defined.

In the example below, port A0 is used on the RX63N.

```
/*------------------------------------------------------------------------- */
/*   Define the CS port.                                                    */
/*------------------------------------------------------------------------- */
#define FLASH_DR_CS0    PORTA.PODR.BIT.B0 /* FLASH CS0(Negative-true logic)  */
#define FLASH_DDR_CS0   PORTA.PDR.BIT.B0  /* FLASH CS0(Negative-true logic)  */

#if (FLASH_DEV_NUM > 1)
#define FLASH_DR_CS1                      /* FLASH CS1(Negative-true logic)  */
#define FLASH_DDR_CS1                     /* FLASH CS1(Negative-true logic)  */
#endif  /* #if (FLASH_DEV_NUM > 1) */
```

In the example below, port 80 is used on the RL78/G14.

```
/*------------------------------------------------------------------------- */
/*   Define the CS port.                                                    */
/*------------------------------------------------------------------------- */
#ifdef __CA78K0R__                      /* Renesas RL78 Compiler            */
    #define FLASH_DR_CS0    P8.0        /* FLASH CS0    (Negative-true logic)*/
    #define FLASH_DDR_CS0   PM8.0       /* FLASH CS0    (Negative-true logic)*/

    #if (FLASH_DEV_NUM > 1)
    #define FLASH_DR_CS1                /* FLASH CS1    (Negative-true logic)*/
    #define FLASH_DDR_CS1               /* FLASH CS1    (Negative-true logic)*/
    #endif  /* #if (FLASH_DEV_NUM > 1) */
#endif  /* __CA78K0R__ */
#ifdef __CCRL__                         /* Renesas CC-RL Compiler           */
    #define FLASH_DR_CS0    P8_bit.no0  /* FLASH CS0    (Negative-true logic)*/
    #define FLASH_DDR_CS0   PM8_bit.no0 /* FLASH CS0    (Negative-true logic)*/

    #if (FLASH_DEV_NUM > 1)
    #define FLASH_DR_CS1                /* FLASH CS1    (Negative-true logic)*/
    #define FLASH_DDR_CS1               /* FLASH CS1    (Negative-true logic)*/
    #endif  /* #if (FLASH_DEV_NUM > 1) */
#endif  /* __CCRL__ */
#ifdef __ICCRL78__                      /* IAR RL78 Compiler                */
    #define FLASH_DR_CS0    P8_bit.no0  /* FLASH CS0    (Negative-true logic)*/
    #define FLASH_DDR_CS0   PM8_bit.no0 /* FLASH CS0    (Negative-true logic)*/

    #if (FLASH_DEV_NUM > 1)
    #define FLASH_DR_CS1                /* FLASH CS1    (Negative-true logic)*/
    #define FLASH_DDR_CS1               /* FLASH CS1    (Negative-true logic)*/
    #endif  /* #if (FLASH_DEV_NUM > 1) */
#endif  /* __ICCRL78__ */
```

(2) Communication Speed Settings

These settings define the communication speed. The unit is bits per second.

The appropriate setting values depend on the MCU and serial I/O interface used. Separate settings are provided for different communication applications. See table 6.1 for details.

Table 6-1 Communication Speed Settings

#define Definition	Application
FLASH_BR	Communication processing for other than the following two items (command transmission, etc.)
FLASH_BR_WRITE_DATA	Data write processing
FLASH_BR_READ_DATA	Data read processing

In the example below, the RSPI of the RX63N is used.

```
    /* PCLK = 48MHz, n=0 for RX63N RSPI */
#define FLASH_BR            (uint8_t)(0x01)  /* SPBR initial setting        */
                    /*       ++---------------- 12.00MHz                   */

    /* PCLK = 48MHz, n=0 for RX63N RSPI Write Data */
#define FLASH_BR_WRITE_DATA (uint8_t)(0x02)  /* SPBR initial setting        */
                    /*       ++---------------- 12.00MHz                   */

    /* PCLK = 48MHz, n=0 for RX63N RSPI Read Data */
#define FLASH_BR_READ_DATA  (uint8_t)(0x01)  /* SPBR initial setting        */
                    /*       ++---------------- 12.00MHz                   */
```

In the example below, the CSI of the RL78/G14 is used.

```
    /* fMCK = 24MHz for RL78 CSI */
#define FLASH_BR              (uint8_t)(0x01)   /* SDR[15:9] initial setting*/
                    /*       ++---------------- 6.00MHz                    */

    /* fMCK = 24MHz for RL78 CSI Write Data */
#define FLASH_BR_WRITE_DATA   (uint8_t)(0x01)   /* SDR[15:9] initial setting*/
                    /*       ++---------------- 6.00MHz                    */

    /* fMCK = 24MHz for RL78 CSI Read Data */
#define FLASH_BR_READ_DATA    (uint8_t)(0x01)   /* SDR[15:9] initial setting*/
                    /*       ++---------------- 6.00MHz                    */
```

Refer to the hardware manual of the MCU when determining the setting values.

6.1.3 r_qspi_flash_n25q_sub.h

The setting locations are designated in each file by the comment /** SET **/.

(1) Erase Timeout Duration Settings

These settings specify the timeout duration when erasing all the data in the memory (bulk erase), all the data in a specified sector (sector erase), all the data in a specified subsector (subsector erase), and all the data in a specified die (die erase).

The settings below should be reevaluated if the erase duration differs according to the device.

In the example below, the bulk erase and die erase timeout duration is set to 480 seconds, and the sector erase and subsector erase timeout duration is set to 3 seconds.

```
/*------------------------------------------------------------------------*/
/*   Define the software timer value of erase or page program busy waiting. */
/*------------------------------------------------------------------------*/

/*------- Definitions of software timer value --------*/
/* Bulk Erase              : 480s                                          */
/* Sector Erase            : 3s                                            */
/* Subsector Erase         : 3s                                            */
/* Die Erase               : 480s                                          */
/* Page (256 bytes) Program: 8ms                                           */
#define FLASH_BE_BUSY_WAIT  (uint32_t)(480000)
                           /* Bulk Erase busy timeout    480,000*1ms = 480s  */
#define FLASH_SE_BUSY_WAIT  (uint32_t)(3000)
                           /* Sector Erase busy timeout   3,000*1ms = 3s     */
#define FLASH_SSE_BUSY_WAIT (uint32_t)(3000)
                           /* Subsector Erase busy timeout   3,000*1ms = 3s  */
#define FLASH_DE_BUSY_WAIT  (uint32_t)(480000)
                           /* Die Erase busy timeout     480,000*1ms = 480s  */
```

(2) Write Timeout Duration Setting

The settings below should be reevaluated if the write duration differs according to the device.

In the example below, the write timeout duration is set 8 ms.

```
#define FLASH_WBUSY_WAIT     (uint32_t)(8000)
                           /* Write ready timeout          8,000*1us = 8ms  */
```

6.1.4 r_qspi_flash_n25q_sub.c

This is the source file for internal functions of the serial NOR flash memory.

The setting locations are designated in each file by the comment /** SET **/.

(1) Macro Function R_QSPI_FLASH_CMD_READ() Definition

This specifies the operation command for read processing. Define one item from the table below.

Table 6-2 Macro Function R_QSPI_FLASH_CMD_READ() Definition

No.	#define Definition	Instruction Code on Data Sheet	Processing Details
1	r_qspi_flash_send_cmd(**FLASH_CMD_FREAD**,(uint32_t) Addr,FLASH_CMD_SIZE+FLASH_ADDR_SIZE+1)	FAST READ	Single-SPI read (high-speed)
2	r_qspi_flash_send_cmd(**FLASH_CMD_DOFR**,(uint32_t) Addr,FLASH_CMD_SIZE+FLASH_ADDR_SIZE+1)	DUAL OUTPUT FAST READ	Dual-SPI read (high-speed)
4	r_qspi_flash_send_cmd(**FLASH_CMD_QOFR**,(uint32_t) Addr,FLASH_CMD_SIZE+FLASH_ADDR_SIZE+1)	QUAD OUTPUT FAST READ	Quad-SPI read (high-speed)

(2) Macro Function R_QSPI_FLASH_CMD_PP() Setting

This specifies the operation command for write processing. Define one item from the table below.

Table 6-3 Macro Function R_QSPI_FLASH_CMD_PP() Definition

No.	#define Definition	Instruction Code on Data Sheet	Processing Details
1	r_qspi_flash_send_cmd(**FLASH_CMD_PP**,(uint32_t)Addr, FLASH_CMD_SIZE+FLASH_ADDR_SIZE)	PAGE PROGRAM	Single-SPI write
2	r_qspi_flash_send_cmd(**FLASH_CMD_DIPP**,(uint32_t) Addr,FLASH_CMD_SIZE+FLASH_ADDR_SIZE)	DUAL INPUT FAST PROGRAM	Dual-SPI write
3	r_qspi_flash_send_cmd(**FLASH_CMD_QIPP**,(uint32_t) Addr,FLASH_CMD_SIZE+FLASH_ADDR_SIZE)	QUAD INPUT FAST PROGRAM	Quad-SPI write

6.1.5 r_qspi_flash_n25q_drvif.c

This is the source file for the clock synchronous single control software interface of the serial NOR flash memory.

The setting locations are designated in each file by the comment /** SET **/.

(1) r_qspi_flash_drvif_init_driver() Setting

This specifies the driver initialization processing of the clock synchronous single master control software used.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_init_driver(void)
{
    return R_SIO_Init_Driver();
}
```

(2) r_qspi_flash_drvif_disable() Setting

This specifies the serial I/O disable setting processing of the clock synchronous single master control software used.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_disable(void)
{
    return R_SIO_Disable();
}
```

(3) r_qspi_flash_drvif_enable() Setting

This specifies the serial IO enable setting processing used by the clock-synchronous single master control software.

The value of the BrgData argument is set in the bit rate register.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_enable(uint8_t BrgData)
{
    return R_SIO_Enable(BrgData);
}
```

(4) r_qspi_flash_drvif_enable_tx_data() Setting

This specifies the data write-only serial IO enable setting processing of the clock synchronous single master control software used.

The value of the BrgData argument is set in the bit rate register.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_enable_tx_data(uint8_t BrgData)
{
    return R_SIO_Enable(BrgData);
}
```

(5) r_qspi_flash_drvif_enable_rx_data() Setting

This specifies the data read-only serial IO enable setting processing of the clock synchronous single master control software used.

The value of the BrgData argument is set in the bit rate register.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_enable_rx_data(uint8_t BrgData)
{
    return R_SIO_Enable(BrgData);
}
```

(6) r_qspi_flash_drvif_open_port() Setting

This specifies the serial IO open setting processing of the clock synchronous single master control software used.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_open_port(void)
{
    return R_SIO_Open_Port();
}
```

(7) r_qspi_flash_drvif_tx() Setting

This specifies the serial IO data transmit processing used by the clock-synchronous single master control software. It is mainly used for command transmission and writing to the status register.

The TxCnt argument specifies the transmit data size (bytes), and the pData argument specifies the transmit data storage destination buffer address.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_tx(uint16_t TxCnt, uint8_t FAR * pData)
{
    return R_SIO_Tx_Data(TxCnt, pData);
}
```

(8) r_qspi_flash_drvif_tx_data() Setting

This specifies the serial IO data transmit processing exclusively for data writes used by the clock-synchronous single master control software. It is mainly used for writing data.

The TxCnt argument specifies the transmit data size (bytes), and the pData argument specifies the transmit data storage destination buffer address.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_tx_data(uint16_t TxCnt, uint8_t FAR * pData)
{
    return R_SIO_Tx_Data(TxCnt, pData);
}
```

(9) r_qspi_flash_drvif_rx() Setting

This specifies the serial IO data receive processing used by the clock-synchronous single master control software. It is mainly used for reading the status register.

The RxCnt argument specifies the receive data size (bytes), and the pData argument specifies the receive data storage destination buffer address.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_rx(uint16_t RxCnt, uint8_t FAR * pData)
{
    return R_SIO_Rx_Data(RxCnt, pData);
}
```

(10) r_qspi_flash_drvif_rx_data() Settings

This specifies the serial IO data transmit processing exclusively for data reads used by the clock-synchronous single master control software.

The RxCnt argument specifies the receive data size (bytes), and the pData argument specifies the receive data storage destination buffer address.

If there is no corresponding item, add one as necessary.

```
error_t r_qspi_flash_drvif_rx_data(uint16_t RxCnt, uint8_t FAR * pData)
{
    return R_SIO_Rx_Data(RxCnt, pData);
}
```

6.1.6 r_qspi_flash_n25q_sfr_rl78.c

This is an I/O module file for this Serial Flash memory.

The settings to be made are identified by the comments header "/** SET **/" in the file.

1. Setting the definition of SFR

When an RL78 family or 78K0R family microcontroller is used, there will be predefined preprocessor symbols in the C compiler used. The program is coded using these predefined preprocessor symbols.

Also, when the microcontroller used is an RL78 family or 78K0R family product and furthermore, the IAR Systems integrated development environment is used, it will be necessary to set the header file in which the SFRs for the microcontroller used are defined.

See the clock synchronous single master control software for the individual microcontroller.

These settings are used for the SPI slave device select control signals.

Table 6-4 Microcontroller and SFR Area Define Settings

Integrated development environment	Microcontroller	SFR setting required?	Method
CubeSuite+	RL78	Not required	Not required
CS+	78K0R	Not required	Not required
	RX	Not required	Not required
IAR Embedded Workbench	RL78	Required	#ifdef __ICCRL78__ #include <ior5f104pj.h> ← Change to match the microcontroller used. #include <ior5f104pj_ext.h> ← Change to match the microcontroller used. #endif
	78K0R	Required	#ifdef __ICC78K__ #include <io78f1009_64.h> ← Change to match the microcontroller used. #include <io78f1009_64_ext.h> ← Change to match the microcontroller used. #endif
	RX	(Not supported by this software)	(Not supported by this software)

The example below is for the 100-pin RL78/G14 microcontroller.

```
#ifdef __ICCRL78__                      /* IAR RL78 Compiler                */
   #include <ior5f104pj.h>              /* for RL78/G14 100pin (R5F104PJ)   */
   #include <ior5f104pj_ext.h>          /* for RL78/G14 100pin (R5F104PJ)   */
#endif   /* __ICCRL78__ */
```

7. Usage Notes

7.1 Notes on Integrating Sample Code

To integrate the sample code, include the following header files:

r_qspi_flash_n25q.h
r_qspi_flash_n25q_sub.h
r_qspi_flash_n25q_sfr.h
r_qspi_flash_n25q_drvif.h

7.2 Using an MCU with On-Chip Cache

Specify a non-cached area for the read/write data storage buffer.

7.3 Support for Other Capacities

To support other capacities, the following definitions must be reevaluated:

FLASH_MEM_SIZE
FLASH_SECT_ADDR
FLASH_SSECT_ADDR
FLASH_PAGE_SIZE
FLASH_ADDR_SIZE
FLASH_WP_WHOLE_MEM
FLASH_FULL_CHIP_ERASE
FLASH_ADDR_MODE

It may be necessary to reevaluate definitions other than those listed above as well. Obtain the data sheet of the memory, and reevaluate the definitions as appropriate.

7.4 Using Other Slave Devices

It is possible to control other slave devices connected to the same SPI bus.

Refer to the sample code when creating slave device control software.

Note that the communication speed may be set individually for each slave device control software program.

7.5 Voltage Stabilization Time After Power-On

Make sure to allow sufficient time for the voltage to stabilize after power-on before calling the initialization function.

Check the data sheet of the slave device regarding the voltage stabilization wait time after power-on.

Note that in the case of serial NOR flash memory, the write in progress bit (WIP) of the status register is set to 1 after the S# pin reaches the specified voltage of $V_{CC\ min}$. or above following power-on. After this, WIP is reset to 0 after the ^{t}VTW ($V_{CC,\ min}$. to device fully accessible) time elapses. During the period from when WIP is set to 1 and when it reverts to 0, no commands are accepted, except for READ STATUS REGISTER and READ FLAG STATUS REGISTER. The WRITE, PROGRAM, and ERASE commands should only be issued when the value of WIP is 0.

7.6 Unsupported N25Q256A83ESF40x and N25Q256A83E1240x Commands (ENTER QUAD and EXIT QUAD Commands)

To change to and from 4-byte address mode on the N25Q256A83ESF40x and N25Q256A83E1240x, it is necessary to issue the ENTER and EXIT QUAD commands. However, these commands are not supported by the sample code. It is therefore necessary for the user to provide suitable code for processing the issuing of these commands.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RX Family, RL78 Family, 78K0R/Kx3-L Application Note Micron Technology N25Q Serial NOR Flash Memory Control Software

Rev.	Date	Description	
		Page	Summary
1.01	Sep. 26, 2013	—	First edition issued
1.03	Apr. 30, 2014	1	Modified Introduction to add short address.
		1	Added RX63N, RX63T, RX210, RX21A, RX220, RX111 RL78/G1C, RL78/L12, RL78/L13, RL78/L1C and RL78/G14 as supported devices.
		5, 7	Added 2.1 RX Family and 2.2 RL78 Family, 78K0R/Kx3-L.
		6	Added the following conditions to section 2.1. (2) RX111 RSPI (3) RX111 SCI
		7 to 11	Added the following conditions to section 2.1. (2) RL78/G14 SAU Integrated Development Environment IAR Embedded Workbench (3) RL78/G1C SAU Integrated Development Environment CubeSuite+ (4) RL78/G1C SAU Integrated Development Environment IAR Embedded Workbench (5) RL78/L12 SAU Integrated Development Environment CubeSuite+ (6) RL78/L12 SAU Integrated Development Environment IAR Embedded Workbench (7) RL78/L13 SAU Integrated Development Environment CubeSuite+ (8) RL78/L13 SAU Integrated Development Environment IAR Embedded Workbench (9) RL78/L1C SAU Integrated Development Environment CubeSuite+ (10) RL78/L1C SAU Integrated Development Environment IAR Embedded Workbench
		12	Updated application note title in section 3, Related Application Notes. -RX210, RX21A, RX220, RX63N, RX63T, RX111 Group Clock Synchronous Single Master Control Software Using the RSPI (R01AN1196EJ) -RX210, RX21A, RX220, RX63N, RX63T, RX111 Group Clock Synchronous Single Master Control Software Using the SCI (R01AN1229EJ) -RL78/G14, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C Group Clock Synchronous Single Master Control Software Using CSI Mode of Serial Array Unit (R01AN1195EJ)
		22, 24	Added 5.3.1 RX Family and 5.3.2 RL78 Family, 78K0R/Kx3-L.
		23	Added the following to section 5.3.1, Sizes of Required Memory. (2) RX111 RSPI (3) RX111 SCI
		24 to 25	Added the following to section 5.3.2, Sizes of Required Memory. (2) RL78/G14 SAU Integrated Development Environment IAR Embedded Workbench (3) RL78/L13 SAU Integrated Development Environment CubeSuite+ (4) RL78/L13 SAU Integrated Development Environment IAR Embedded Workbench
		26	5.4 File Structure

			Changed name for folder for the sample code. Changed application note number. Added new device register common definitions.
		65	Added 6.1.6 r_qspi_flash_n25q_sfr_rl78.c.
		-	Changed “Table No” format.
1.04	Mar. 31, 2016	-	Support CC-RL compiler.
		7 to 9	Added the following conditions to section 2.2. (2) RL78/G14 Integrated Development Environment CS+ for CC (Compiler:CC-RL) (5) RL78/G1C Integrated Development Environment CS+ for CC (Compiler:CC-RL)
		25 to 27	Added the following to section 5.3.2, Required Memory Size. (2) RL78/G14 Integrated Development Environment CS+ for CC (Compiler:CC-RL) (5) RL78/L13 Integrated Development Environment CS+ for CC (Compiler:CC-RL)
		26 to 27	Modified the following to Remarks of table. (3) RL78/G14 Integrated Development Environment IAR Embedded Workbench (4) RL78/L13 Integrated Development Environment CubeSuite+ (Compiler:CA78K0R) (6) RL78/L13 Integrated Development Environment IAR Embedded Workbench
		28	Updated the software version in Table 5.10 File Structure.
		62	Updated example in 6.1.2 (1) Chip Select Signal Setting.
		69	Updated Table 6.4 Microcontrollers and Settings for Defining SFR Area.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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