

RX Family

How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

Introduction

This application note describes methods of starting transmission immediately after writing transmit data in asynchronous mode of the serial communication interface (SCI).

Target Devices

RX Family

Target Tools

- Smart Configurator V2.19.0 or earlier
- e2 studio Version 2023-10 or earlier

Please use the Smart Configurator implemented in e2 studio 2024-01 and Smart Configurator V2.20.0 or later version because equivalent functions have been implemented in Smart Configurator.

Confirmed Devices

RX660 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.



Contents

1.	Wait Time in the SCI	4
1.1	Overview of the Wait Time	4
1.2	Instant Transmission Function	4
1.3	Overview of the Code Generation Function of Smart Configurator	4
2.	Operation Confirmation Conditions	5
3.	Description of Software	6
3.1	Control Example by Using the Transmit Data Empty Interrupt	6
3.1.1	Overview	6
3.1.2	Code Generation Procedure Example	8
3.1.3	Modifying the Program	. 11
R_C	onfig_SCI12_Start ()	. 11
R_C	onfig_SCI12_Serial_Send ()	. 12
r_Co	nfig_SCI12_transmit_interrupt ()	. 13
r_Co	nfig_SCI12_transmitend_interrupt ()	. 14
3.1.4	Sample Program	. 15
3.1.5	Operation After Modification	. 16
3.2	Control Example Using the DMAC	. 18
3.2.1	Overview	. 18
3.2.2	Code Generation Procedure Example	. 19
3.2.3	Modifying the Program	. 22
R_C	onfig_SCI12_Start ()	. 22
R_C	onfig_SCI12_Serial_Send ()	. 23
R_C	onfig_DMAC0_Create ()	24
R_S	/steminit()	. 26
3.2.4	Sample Program	. 28
3.2.5	Operation of the Sample Program	. 31
3.3	Control Example Using the DTC	. 32
3.3.1	Overview	. 32
3.3.2	Code Generation Procedure Example	. 33
3.3.3	Modifying the Program	. 36
R_C	onfig_SCI12_Start ()	. 36
R_C	onfig_SCI12_Serial_Send ()	. 37
R_C	onfig_DTC_Create ()	. 38
R_S	/steminit()	. 40
3.3.4	Sample Program	. 42
3.3.5	Operation of the Sample Program	. 45
4.	Disabling Automatic Code Regeneration at Build Time	.46



RX	Family	How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode
5.	Importing a	Project
5.1		Project into e ² studio
5.2	Importing a	Project into CS+
6.	Reference	Documents
Re	vision History	<i>.</i>



1. Wait Time in the SCI

1.1 Overview of the Wait Time

In asynchronous mode, data transmission starts when transmit data is written to the TDR register after the SCR.TE bit is set to 1.

However, after the SCR.TE bit is set to 1, an internal wait time that is equal to the time required to transmit one frame of data is generated before data transmission starts, and this internal wait time occurs each time the SCR.TE bit is set to 1.



Figure 1.1 Internal Wait Time in Data Transmission

1.2 Instant Transmission Function

In some products that support the SEMR.ITE bit, the SCI can be used without generating internal wait times by controlling this bit.

1.3 Overview of the Code Generation Function of Smart Configurator

The SCI components generated by the code generation function support processing equivalent to the flowchart example for serial transmission in asynchronous mode described in the user's manual.

In the serial transmission flowchart example, the transmission process is controlled by the TE bit, so an internal wait time occurs when the SCI components are used.

In this application note, the SCI components generated by the code generation function are used for a sample program, so the processing has been modified not to generate internal wait times. Sections 3 and 4 describe modification procedures.



2. Operation Confirmation Conditions

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	R5F56609HDFB (RX660N Group)
Operating frequency	Main clock: 24 MHz
	PLL: 240 MHz (Main clock, divided by 1, multiplied by 10)
	 System clock (ICLK): 120 MHz (PLL divided by 2)
	Peripheral module clock B (PCLKB): 60 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development	Renesas Electronics
environment	e ² studio Version 2023-01 (23.1.0)
C compiler	Renesas Electronics
	C/C++ Compiler Package for RX Family V.3.05.00
	Compile options
	-lang = c99
iodefine.h version	Version 1.00
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample program version	Version 1.00
Board used	Renesas Starter Kit for RX660 (Product No.: RTK556609xxxxxxxx)



3. Description of Software

This section describes how to start transmission immediately after writing transmit data. This sample program uses SCI components (SCIh module (SCI12)) that do not have an instant transmission function.

3.1 Control Example by Using the Transmit Data Empty Interrupt

3.1.1 Overview

An internal wait time is generated when the TE bit changes from 0 to 1 for the reason described in section 1.1. The modified method described in this section controls interrupts by using a 0-to-1 state change of the IEN bit as the trigger while maintaining the state of TE = 1, and writes transmit data within the interrupt process so that no internal wait time is generated in the second and subsequent transmissions.

Figure 3.1 is a timing chart before modification, and Figure 3.2 is a timing chart after modification.





Figure 3.1 Timing Chart Before Modification



Figure 3.2 Timing Chart After Modification



3.1.2 Code Generation Procedure Example

This section describes a code generation procedure example in Smart Configurator.

1. Open the [Components] tab and click on the [Add component] icon.

			\times
🌼 *interrupt_sample_for_sci.scfg 🗡		G	
Software component configuration	🛐 Generate Code	e Generate Re	port
Components 🚵 🛃 🎘 🕞 🕀 🌞 Configure			^
type filter text Add component			
			>
Overview Board Clocks System Components Pins Interrupts			

2. In the [Software Component Selection] window, select [SCI (SCIF) Asynchronous Mode], and then click on [Next].

💽 New Co	mponent					\times
Software	Component	Selection				
Select com	nponent from	those available in list				
Category	All					~
Function	All					×
Filter						
Titter						
Compon	ents	`	Short Name	Туре	Version	^
🖶 Remo	te Control Sig	nal Receiver		Code Generator	1.2.0	
🖶 RSCI 🛙	Driver		r_rsci_rx	Firmware Integra	2.10	
🖶 RSPI D	Driver		r_rspi_rx	Firmware Integra	3.04	
🖶 SCI Di	river		r_sci_rx	Firmware Integra	4.40	
🖶 SCI/SC	CIF Asynchron	ous Mode		Code Generator	1.12.0	
BCI/SC	CIF Clock Sync	hronous Mode		Code Generator	1.12.0	
🖶 SD Me	ode SD Memo	ory Card Driver	r_sdc_sdmem_rx	Firmware Integra	3.00	
	- IIC D			Planetter Internet	250	~
		duplicated functional	ity			
	ware compone nous mode.	ent provides configura	ations for SCI(SCIF, RS	CI) single(multi-processor)		^
	l the latest FIT general settin	drivers and middlewa Igs	ire			~
?		< <u>B</u> ack	<u>N</u> ext >	<u>F</u> inish	Cancel	



3. Specify an appropriate configuration name, work mode, and resource, and then click on [Finish]. In this sample, the configuration name is "Config_SCI12", the work mode is "Transmission", and the resource is "SCI12".

New Component		—	×
dd new configuratio	on for selected component	ŧ	
SCI/SCIF Asynchronou			
Configuration name:	Config_SCI12		
Work mode:	Transmission		~
Resource:	SCI12		\sim
?	< <u>B</u> ack <u>N</u> ext >	<u>Einish</u> Cancel	



4. Configure software component settings for SCI12, and then click on the [Generate Code] icon. The required settings for this sample are listed below.

Transmit data handling: Data handled by the interrupt service routine Callback function setting: "Transmission end" selected

*interrupt_sample_for_sci.scfg	×				-
Software component c				Generate Code	🁜 Generate Rep
Compone 🚵 🛃 🎘 🗎 🕀	Configure			-	
10 T	Data length setting				
type filter text	0 9 bits	8 bits 8	○7 bits		
✓ 🗁 Startup	e_for_sciscifg × ponent configuration Generate Code Gener Configure Data length setting O bits Parity setting None Even Odd Stop bit length setting O 1 bit O 2 bits				
V 🧁 Generic	None	O Even	Odd		Generate Repo
r_bsp Crivers	Stop bit length setting				
V 🗁 Communications		🔾 2 bits			
Config_SCI12	Transfer direction setting				
		◯ MSB-first			
	Data inversion setting				
		◯ Inverted			
	Transfer rate setting				
	Transfer clock	Internal clock	~		
	Base clock	16 cycles for 1-bit period	~		
	Bit rate	9600	 (bps) (Actual 	value: 9615.385, Er	ror: 0.16%)
	Enable modulation duty correction		-		Generate Re
		SCK12 is not used	~		
	Hardware flow control setting				Generate Rep
	None	○ CTS12#			
	Data handling setting				
	Transmit data handling	Data handled in interrupt service routine	~		
	Interrupt setting				
	TXI12 priority	Level 15 (highest)	✓		
	TEI12 priority (Group BL0)	Level 15 (highest)	~		
	Callback function setting				
	✓ Transmission end				

5. A message box for code generation appears. Click on [Proceed].

👩 Code Generating		×
Configuration must be saved before generating code.		
Proceed with save and generate?		
Always save and generate without asking?	Proceed	Cancel



3.1.3 Modifying the Program

Table 3.1 lists the functions to be modified.

 Table 3.1
 Functions to Be Modified

Function Name
R_Config_SCI12_Start
R_Config_SCI12_Serial_Send
r_Config_SCI12_transmit_interrupt
r_Config_SCI12_transmitend_interrupt

R_Config_SCI12_Start ()

Before modification:

```
void R_Config_SCI12_Start(void)
{
    /* Clear interrupt flag */
    IR(SCI12, TXI12) = 0U;
    /* Enable SCI interrupt */
    IEN(SCI12, TXI12) = 1U;
    ICU.GENBL0.BIT.EN16 = 1U;
}
To be deleted because IEN is set to 1 at the start of
    transmission by the R_Config_SCI12_Serial_Send function
}
```





RX Family

R_Config_SCI12_Serial_Send ()

Before modification:







r_Config_SCI12_transmit_interrupt ()

Before modification:







r_Config_SCI12_transmittend_interrupt ()

Before modification:



```
void r_Config_SCI12_transmitend_interrupt(void)
{
    SCI12.SCR.BIT.TEIE = 0U;
    r_Config_SCI12_callback_transmitend();
}
```



3.1.4 Sample Program

The following shows how the sample program works.

[Main function]

(1) Call the R_Config_SCI12_Start function to configure transmission.

(2) Set g_flag = 0.

(3) Call the R_Config_SCI12_Serial_Send function to transmit 3-byte data {0x11, 0x22, 0x33}.

(4) Wait until transmission is completed. (Wait until g_flag = 1 is set by the transmission end interrupt.)

(5) Insert 300-µs wait time.

(6) Repeat steps (2) to (5) twice.

(7) After transmission is completed, call the R_Config_SCI12_Stop function to disable the transmission setting.

Note: Since the R_Config_SCI12_Create function is called in the R_Systeminit function before reaching the main function, it does not need to be called in the main function.

```
Global variables
volatile uint8 t g flag;
Private (static) variables and functions
g data[] = \{0x11, 0x22, 0x33\};
uint8 t
void main(void);
* Function Name: main
* Description : This function uses the modified program to send data without a wait time.
* Arguments : None
* Return Value : None
void main(void)
{
  uint8 t i
                = 0;
  uint8 t send count = 2;
  R_Config_SCI12_Start();
  for (i = 0; i < send count; i++)
   {
     g flag = 0;
     R Config SCI12 Serial Send(g data, 3);
     while (0 == g flag)
     {
        nop();
     }
     R BSP SoftwareDelay((uint32 t)300, BSP DELAY MICROSECS);
  }
  R Config SCI12 Stop();
  while (1)
   {
     nop();
   }
```

Figure 3.3 "main" Function of the Sample Program



[SCI12 transmission end callback function]

(1) Set the transmission end flag ($g_flag = 1$).

```
static void r_Config_SCI12_callback_transmitend(void)
{
    /* Start user code for r_Config_SCI12_callback_transmitend. Do not edit comment
generated here */
    g_flag = 1;
    /* End user code. Do not edit comment generated here */
}
```

Figure 3.4 "r_Config_SCI12_callback_transmittend" Function in the Sample Program

3.1.5 Operation After Modification

Figure 3.5 and Figure 3.6 show the operation waveforms before and after modification when 3-byte data $\{0x11, 0x22, 0x33\}$ is transmitted.





Figure 3.5 Waveform Before Modification

Before the modification, it can be confirmed that an internal wait time occurs when TE changes from 0 to 1.





Operation after modification:



It can be confirmed that during the first transmission, an internal wait time occurs when TE changes from 0 to 1, but during the second transmission, the TE bit is not controlled, so the transmission starts without generating an internal wait time. For the first transmission, no internal wait time occurs either if the R_Config_SCI12_Serial_Send function is executed at least one frame after the R_Config_SCI12_Start function is called.



3.2 Control Example Using the DMAC

3.2.1 Overview

As in section 3.1, Control Example by Using the Transmit Data Empty Interrupt, this section describes the case where the TE = 1 state is maintained and transmit data is written by DMAC transfer.

Figure 3.7 is a timing chart after modification (writing transmit data by DMAC transfer).

(Timings before modification are equivalent to those in Figure 3.1 except for DMAC operation.)



Figure 3.7 Timing Chart After Modification (Writing Transmit Data by DMAC Transfer)



3.2.2 Code Generation Procedure Example

Code generation is performed using Smart Configurator in the same way as in the code generation procedure example in section 3.1, Control Example by Using the Transmit Data Empty Interrupt.

- 1. Perform the same procedure as steps 1 through 3 in section 3.1.2, Code Generation Procedure Example.
- 2. Configure software component settings for SCI12, and then click on the [Generate Code] icon. The required settings for this sample are listed below.

Transmit data handling: Data handled by DMAC TXI12 priority: Level 0 (disabled) Callback function setting: "Transmission end" selected

dmac_sample_for_sci.scfg \times				-
oftware component configuration	n			🕤 🤷 Generate Code Generate Rep
Components 🛛 🖄 🛃 🎘 🕀 🕀 莽 🔻	Configure			
1 U	Data length setting			
type filter text	◯ 9 bits	8 bits		○ 7 bits
✓ 🗁 Startup	Parity setting			
	None	O Even		Odd
✓ ➢ Drivers	Stop bit length setting			
Image: Startup Data length setting Image: Startup Image: Startup Image: Startup Image: Startup Image: Startup Image: Startup <td></td> <td></td>				
	Transfer direction setting			
	 LSB-first 	O MSB-first		
	Data inversion setting			
		○ Inverted		
	Transfer rate setting			
	Transfer clock	Internal clock	~	
	Base clock	16 cycles for 1-bit period	~	
	Bit rate	9600	~	(bps) (Actual value: 9615.385, Error: 0.1
	Enable modulation duty correction			
	SCK12 pin function	SCK12 is not used	~	
	Hardware flow control setting			
	None	○ CTS12#		
	Data handling setting			
	Transmit data handling	Data handled by DMAC	~	(Please ensure DMAC config is added)
Sype filter text Specifier text Startup Parity setting Startup Startup Startup Parity setting Startup Startup Parity setting Startup Startup Parity setting Startup Startup Startup Parity setting Startup Startup Startup Startup Parity setting Startup				
	TXI12 priority	Level 0 (disabled)	~	
	TEI12 priority (Group BL0)	Level 15 (highest)	~	
	Callback function setting			
	Transmission end			



3. Go to the [Software Component Selection] window again. Select [DMA Controller], and then click on [Next].

📴 New Com	nponent				\times
	Component Selection ponent from those available in list				
Category	All				\sim
Function	All				~
Filter					_
Compone	nts	Short Name	Туре	Version	~
🖶 Data Tr	ansfer Controller		Code Generator	1.11.0	
			Code Generator	1.11.0	-
🖶 DMA C	ontroller		Code Generator	1.8.0	
		r_dmaca_rx	Firmware Integra	2.90	_
		r_dtc_rx	Firmware Integra	4.10	
🖶 Event L	ink Controller		Code Generator	1.9.0	
Function All Filter Components Data Transfer Controller Code Generator Data Transfer Controller Code Generator DMA Controller Code Generator DMAC driver r_dmaca_rx Firmware Integra 2.90 DTC driver r_dtc_rx					
Show or	nly latest version				
✓ Hide iter	ms that have duplicated functionality	v l			
The DMAC	C is a module to transfer data withou	it the CPU.			~
					~
Download	the latest FIT drivers and middleware	9			
		-			
configure e	general sectings				
?	< Back	Next >	Finish	Cance	el

4. Specify an appropriate configuration name and resource, and then click on [Finish]. In this sample, the configuration name is "Config_DMAC0" and the resource is "DMAC0".





5. Configure software component settings for DMAC0, and then click on the [Generate Code] icon. The required settings for this sample are listed below.

Activation source: SCI12 (TXI12) Activation source flag control: Clear interrupt flag of the activation source Transfer mode: Normal mode Transfer data size: 8 bits Source address: Incremented Destination address: Fixed Enable interrupt on transfer end: Selected Priority: Level 15 (highest)

oftware component config	guration	Generate Co	de Generat
omponents 🚵 🛃 📲 🚍 🚔	▼ Configure		
10 1	Transfer setting		\neg
type filter text	Activation source	SCI12(TXI12)	~
🗸 🗁 Startup	Activation source flag control	Clear interrupt flag of the activation source	~
✓ Generic eneric eneric	Transfer mode	Normal mode	~
✓ 🧁 Drivers	Transfer data size	8 bits	~
✓ 🗁 DMA	Transfer count / Repeat size / Block size	1	7
Config_DMAC0	Repeat count / Transfer-block count	1	- I
Config_SCI12	Total transfer size	1	byte(s)
	Block / Repeat area setting		
	Transfer destination	◯ Transfer source	
	Source address setting		
	Source address	0x00000000 Incremented	~
	Specify the transfer source as extended	repeat area	
	Extended repeat area	Lower 1 bit of the address (2 bytes)	~
	Start address of the extended repeat area		
	End address of the extended repeat area		
	Destination address setting		_
	Destination address	0x00000000 Fixed	~
	Specify the transfer destination as exten	ded repeat area	_
	Extended repeat area	Lower 1 bit of the address (2 bytes)	с.
	Start address of the extended repeat area		
	End address of the extended repeat area		
	Address offset setting		
	Amount of offset	+ ~ 0x0000000	
	Interrupt setting (DMAC0I)		
	Enable interrupt on transfer end		
	Enable interrupt on 1 repeat / block size		
	Enable interrupt on source address exter		
	Enable interrupt on destination address Priority		

Note: The transfer count, source address, and destination address are to be changed by software, so here they are left at their default values.



3.2.3 Modifying the Program

Table 3.2 lists the functions to be modified.

 Table 3.2
 Functions to Be Modified

Function Name
R_Config_SCI12_Start
R_Config_SCI12_Serial_Send
R_Config_DMAC0_Create
R_Systeminit

R_Config_SCI12_Start ()

Before modification:

```
void R_Config_SCI12_Start (void)
{
    /* Clear interrupt flag */
    IR(SCI12, TXI12) = 0U;
    /* Enable SCI interrupt */
    IEN(SCI12, TXI12) = 1U;
    ICU.GENBL0.BIT.EN16 = 1U;
}
To be deleted because IEN is set to 1 at the start of
transmission by the R_Config_SCI12_Serial_Send function
}
```





R_Config_SCI12_Serial_Send ()

Before modification:

MD_	STATUS R_CONTIG_SCII2_Seri	al_Send(uint8_t * const tx_buf, uint16_t tx_num)	
{	<pre>SCI12.SCR.BYTE = 0xA0U; /* Set TXD12 pin */ PORTA.PMR.BYTE = 0x10U;</pre>	To be deleted because SCI12.SCR.BYTE and the TXD12 pin are set by the R_Config_SCI12_Start function	
}	return MD_OK;		





RX Family

R_Config_DMAC0_Create ()

Before modification:

```
void R Config DMAC0 Create (void) 🔶
                                                     To be changed so that the transfer
{
                                                     source address and the transfer
    /* Cancel DMAC/DTC module stop state in LPC */ count can be set as arguments.
   MSTP(DMAC) = OU;
    /* Disable DMAC interrupts */
    IEN(DMAC, DMACOI) = OU;
    /* Disable DMAC0 transfer */
    DMAC0.DMCNT.BIT.DTE = OU;
    /* Set DMAC0 activation source */
    ICU.DMRSR0 = 75 DMAC0 ACTIVATION SOURCE;
    /* Set DMAC0 transfer address update and extended repeat setting */
    DMAC0.DMAMD.WORD = 8000 DMAC SRC ADDR UPDATE INCREMENT |
                      _0000_DMAC_DST_ADDR_UPDATE FIXED |
                           0000 DMACO SRC EXT RPT AREA |
0000 DMACO DST EXT RPT AREA;
    /* Set DMAC0 transfer mode, data size and repeat area */
    DMAC0.DMTMD.WORD = 0000 DMAC TRANS MODE NORMAL |
_2000_DMAC_REPEAT AREA NONE |
                      0000 DMAC TRANS DATA SIZE 8 |
                          0001 DMAC TRANS REQ SOURCE INT;
    /* Set DMAC0 interrupt flag control */
    DMACO.DMCSL.BYTE = 00 DMAC INT TRIGGER FLAG CLEAR;
    /* Set DMAC0 source address */
                                                             The transfer source
    DMAC0.DMSAR = (void *) 00000000 DMAC0 SRC ADDR;
                                                             address and the transfer
                                                             count are to be set from
    /* Set DMAC0 destination address */
                                                             arguments.
    DMAC0.DMDAR = (void *) 00000000 DMAC0 DST ADDR;
                                                             The transfer destination
                                                             address is to be changed
    /* Set DMAC0 transfer count */
                                                             to SCI12.TDR.
    DMAC0.DMCRA = _00000001_DMAC0 DMCRA COUNT;
    /* Set DMAC0 interrupt settings */
    DMAC0.DMINT.BIT.DTIE = 1U;
    /* Set DMAC0 priority level */
    IPR(DMAC, DMACOI) = OF DMAC PRIORITY LEVEL15;
    /* Enable DMAC activation */
    DMAC.DMAST.BIT.DMST = 1U;
    R Config DMAC0 Create UserInit();
```



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

After modification:

```
void R Config DMAC0 Create(void *sar, uint16 t count)
    /* Cancel DMAC/DTC module stop state in LPC */
   MSTP(DMAC) = OU;
                                                      Changed so that the transfer
    /* Disable DMAC interrupts */
                                                      source address and the transfer
    IEN(DMAC, DMACOI) = OU;
                                                      count can be set as arguments.
    /* Disable DMAC0 transfer */
    DMAC0.DMCNT.BIT.DTE = 0U;
    /* Set DMAC0 activation source */
    ICU.DMRSR0 = 75 DMAC0_ACTIVATION_SOURCE;
    /* Set DMAC0 transfer address update and extended repeat setting */
    DMAC0.DMAMD.WORD = 8000 DMAC SRC ADDR UPDATE INCREMENT |
                      _0000_DMAC_DST ADDR UPDATE FIXED |
                           0000 DMACO SRC EXT RPT AREA |
0000 DMACO DST EXT RPT AREA;
    /* Set DMAC0 transfer mode, data size and repeat area */
    DMAC0.DMTMD.WORD = _0000_DMAC_TRANS_MODE_NORMAL |
2000 DMAC REPEAT AREA NONE |
                     0000 DMAC TRANS DATA SIZE 8 |
                         0001 DMAC TRANS REQ SOURCE INT;
    /* Set DMAC0 interrupt flag control */
    DMAC0.DMCSL.BYTE = 00 DMAC INT TRIGGER FLAG CLEAR;
    /* Set DMAC0 source address */
    DMAC0.DMSAR = sar;
                                                              The transfer source
                                                              address and the transfer
    /* Set DMAC0 destination address */
                                                              count are set from
    DMAC0.DMDAR = (void *) (& (SCI12.TDR));
                                                              arguments.
                                                              The transfer destination
    /* Set DMAC0 transfer count */
                                                              address is changed to
    DMAC0.DMCRA = count;
                                                              SCI12.TDR.
    /* Set DMAC0 interrupt settings */
    DMAC0.DMINT.BIT.DTIE = 1U;
    /* Set DMAC0 priority level */
    IPR(DMAC, DMACOI) = OF DMAC PRIORITY LEVEL15;
    /* Enable DMAC activation */
    DMAC.DMAST.BIT.DMST = 1U;
    R Config DMACO Create UserInit();
```

Modifying the prototype declaration in the Config_DMAC0.h file:



RX Family

R_Systeminit()

Before modification:

```
void R Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
    SYSTEM.PRCR.WORD = 0xA50BU;
    /* Enable writing to MPC pin function control registers */
    MPC.PWPR.BIT.BOWI = OU;
    MPC.PWPR.BIT.PFSWE = 1U;
    /* Write 0 to the target bits in the POECR2 registers */
    POE3.POECR2.WORD = 0 \times 0000U;
    /* Initialize clocks settings */
    R CGC Create();
    /* Set peripheral settings */
                                        The initial settings are to be deleted because DMAC
    R Config SCI12 Create();
                                     _____ settings will be changed to such a specification that
   R_Config_DMAC0_Create();
                                        the transmit buffer and the transfer count are set
                                        before transmission from the SCI.
    /* Set interrupt settings */
    R Interrupt Create();
    /* Register undefined interrupt */
    R_BSP_InterruptWrite(BSP_INT_SRC_UNDEFINED_INTERRUPT,
     (bsp int cb t)r undefined exception);
    /* Register group BL0 interrupt TEI12 (SCI12) */
    R BSP InterruptWrite(BSP INT SRC BL0 SCI12 TEI12,
     (bsp int cb t)r Config SCI12 transmitend interrupt);
    /* Disable writing to MPC pin function control registers */
    MPC.PWPR.BIT.PFSWE = OU;
    MPC.PWPR.BIT.BOWI = 1U;
    /* Enable protection */
    SYSTEM.PRCR.WORD = 0xA500U;
```



```
void R Systeminit(void)
   /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
   SYSTEM.PRCR.WORD = 0xA50BU;
   /* Enable writing to MPC pin function control registers */
   MPC.PWPR.BIT.BOWI = OU;
   MPC.PWPR.BIT.PFSWE = 1U;
   /* Write 0 to the target bits in the POECR2 registers */
   POE3.POECR2.WORD = 0x0000U;
    /* Initialize clocks settings */
   R CGC Create();
   /* Set peripheral settings */
   R Config SCI12 Create();
   /* Set interrupt settings */
   R Interrupt Create();
   /* Register undefined interrupt */
   R BSP InterruptWrite (BSP INT SRC UNDEFINED INTERRUPT,
    (bsp int cb t)r undefined exception);
    /* Register group BL0 interrupt TEI12 (SCI12) */
   R BSP InterruptWrite(BSP INT SRC BL0 SCI12 TEI12,
     (bsp int cb t)r Config SCI12 transmitend interrupt);
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = OU;
   MPC.PWPR.BIT.BOWI = 1U;
    /* Enable protection */
    SYSTEM. PRCR. WORD = 0 \times A500U;
```



3.2.4 Sample Program

The following shows how the sample program works.

[Main function]

- (1) Call the R_Config_SCI12_Start function to configure transmission.
- (2) Call the R_Config_DMAC_Create function to set transmit data for the DMAC transfer source, the SCI transmit buffer for the transfer destination, and the transfer count.
- (3) Set g_flag = 0, and set g_flag = 1 only after transmission is complete to prevent further processing until transmission is complete.
- (4) Execute the R_Config_DMAC_Start function to put the DMAC in a state waiting for transfer.
- (5) Call the R_Config_SCI12_Serial_Send function to enable the TXI interrupt that works as an activation source for the DMAC. DMAC transfer occurs at the timing of the TXI interrupt and transmit data is written to the transmit buffer.
- (6) Wait until transmission is completed.
- (7) Insert 300-µs wait time.
- (8) Repeat steps (2) to (7) twice.
- (9) After transmission is completed, call the R_Config_DMAC_Stop function and the R_Config_SCI12_Stop function to disable the transmission setting.
- Note: Since the R_Config_SCI12_Create function is called in the R_Systeminit function before reaching the main function, it does not need to be called in the main function.



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

```
Global variables
volatile uint8 t g flag;
Private (static) variables and functions
            uint8 t
       g_data[] = \{0x11, 0x22, 0x33\};
void main(void);
* Function Name: main
* Description : This function uses the modified program to send data without a wait time.
* Arguments : None
* Return Value : None
void main(void)
{
  uint8_t i
                = 0;
  uint8 t send count = 2;
  R Config SCI12 Start();
  for (i = 0; i < send count; i++)
   {
     g flag = 0;
     R Config DMAC0 Create((void *)g data, 3);
     R Config DMAC0 Start();
     R Config SCI12 Serial Send(NULL, 0);
     while (0 == g flag)
     {
        nop();
     }
     R_BSP_SoftwareDelay((uint32_t)300, BSP_DELAY_MICROSECS);
  }
  R Config DMAC0 Stop();
  R Config SCI12 Stop();
  while (1)
   {
     nop();
  }
```





[DMAC0 transfer end callback function]

- (1) The DMAC0 transfer end callback function (r_dmac0_callback_transfer_end) is called when all transmit data has been transferred to the SCI's transmit buffer.
- (2) The function disables the TXI interrupt request and enables the transmission end interrupt (TEIE = 1).



[SCI12 transmission end callback function]

(1) The function disables the transmission end interrupt and sets the transmission end flag (g_flag = 1). Note: Since the r_Config_SCI12_callback_transmittend function is also called during the TXI12 interrupt, it should only be processed when the transmission end interrupt is enabled.

```
* Function Name: r Config SCI12 callback transmitend
* Description : This function is a callback function when SCI12 finishes
transmission
* Arguments
           : None
* Return Value : None
static void r_Config_SCI12_callback_transmittend(void)
{
 /* Start user code for r Config SCI12 callback transmitend. Do not edit
comment generated here */
 if(1 == SCI12.SCR.BIT.TEIE)
  /* Interrupt processing when SCI12 transmit end */
  SCI12.SCR.BIT.TEIE = OU;
  g_flag = 1;
 }
 /* End user code. Do not edit comment generated here */
```

Figure 3.10 "r_dmac0_callback_transfer_end" Function in the Sample Program



3.2.5 Operation of the Sample Program

Figure 3.11 shows the waveforms when the control example using the DMAC is operated.



Figure 3.11 Waveforms of the Sample Program

It can be confirmed that during the first transmission, an internal wait time occurs when TE changes from 0 to 1, but during the second transmission, the TE bit is not controlled, so the transmission starts without generating an internal wait time. For the first transmission, no internal wait time occurs either if the R_Config_SCI12_Serial_Send function is executed at least one frame after the R_Config_SCI12_Start function is called.



3.3 Control Example Using the DTC

3.3.1 Overview

As in section 3.1, Control Example by Using the Transmit Data Empty Interrupt, this section describes the case where the TE = 1 state is maintained and transmit data is written by DTC transfer.

Figure 3.12 is a timing chart after modification (writing transmit data by DTC transfer).

(Timings before modification are equivalent to those in Figure 3.1 except for DTC operation.)



Figure 3.12 Timing Chart After Modification (Writing Transmit Data by DTC Transfer)



3.3.2 Code Generation Procedure Example

Code generation is performed using Smart Configurator in the same way as in the code generation procedure example in section 3.1, Control Example by Using the Transmit Data Empty Interrupt.

- 1. Perform the same procedure as steps 1 through 3 in section 3.1.2, Code Generation Procedure Example.
- 2. Configure software component settings for SCI12, and then click on the [Generate Code] icon. The required settings for this sample are listed below.

Transmit data handling: Data handled by DTC TXI12 priority: Level 15 (highest) Callback function setting: "Transmission end" selected

8				- 🗆 X	
$^{\oplus}$ dtc_sample_for_sci.scfg \times				- 6	3
Software component co	onfiguration			Generate Code Generate Report	
Compon 🚵 🛃 📲 🗄 🗄	Configure			(ī
2.2	Data length setting				
type filter text	○ 9 bits	8 bits	C	7 bits	
✓ 🥭 Startup ✓ 🍋 Generic	Parity setting None 	O Even	C	bpo(
 ✓ → Drivers ✓ → DMA 	Stop bit length setting	◯ 2 bits			
Config_DTC Communications Config_SCI12	Transfer direction setting	◯ MSB-first			
	Data inversion setting Normal	◯ Inverted			
	Transfer rate setting Transfer clock	Internal clock	*		
	Base clock	16 cycles for 1-bit period	~		
	Bit rate	9600	~	(bps) (Actual value: 9615.385, Error: 0.16%)	
	Enable modulation duty correction				
	SCK12 pin function	SCK12 is not used	~		
	Hardware flow control setting None	⊖ CTS12#			
	Data handling setting Transmit data handling	Data handled by DTC	~	(Please ensure DTC config is added)	
	Interrupt setting				
	TXI12 priority	Level 15 (highest)	~		
	TEI12 priority (Group BL0)	Level 15 (highest)	~		
	Callback function setting				
	<			>	
Overview Board Clocks System	Components Pins Interrupts				Î



3. Go to the [Software Component Selection] window again. Select [Data Transfer Controller], and then click on [Next].

S New Component ×					×	
Software (Software Component Selection					
Select com	ponent from those available in list					
Category	Category All					
Function	All				\sim	
Filter						
Compone	ents	Short Name	Туре	Version	^	
- Contro	l Low Power States.	r_lpc_rx	Firmware Integra	2.04		
CRC C	alculator		Code Generator	1.11.0		
🖶 D/A C	onverter		Code Generator	1.11.0		
Bata C	Deration Circuit		Code Generator	1110		
🖶 Data T	ransfer Controller		Code Generator	1.11.0		
	time Compensation Counter		Code Generator	1.11.0		
	Controller		Code Generator	1.8.0		
			Etano tata ana	2.00	•	
	only latest version					
✓ Hide ite	ems that have duplicated functionality	у				
Description	n					
This softv	vare component provides configurat	ions for DTC to perio	orm data transfers.		^	
		/				
					\sim	
Download	the latest FIT drivers and middleward					
Configure general settings						
Configure	general settings					
		1				
		1				
		¥				
0		N	Finish	Cancel		
	< Back	Next >	Finish	Cancel		

4. Specify an appropriate configuration name and resource, and then click on [Finish]. In this sample, the configuration name is "Config_DTC" and the resource is "DTC".

New Component					×
Add new configurat	ion for selected co	omponent			
Data Transfer Control	ler				
Configuration name:	Config_DTC				
Resource:	DTC				~
?	< Back	Next >	Finish	Can	cel



5. Configure software component settings for the DTC, and then click on the [Generate Code] icon. The required settings for this sample are listed below.

Activation source: SCI12 (TXI12) Transfer mode: Normal mode Transfer data size: 8 bits Interrupt setting: An interrupt request to the CPU is generated when specified data transfer is completed Source address: Address incremented Destination address: Address fixed

dtc_sample_for_sci.scfg \times				
oftware component conf	iguration			Generate Code Generate Repo
Compone 🚵 🛃 🎘 🗔 🏵 茸	Configure			(
10 T	Base setting DTC0			
type filter text	Activation source setting	g		
✓	Activation source	SCI12(TXI12)	~	
♂ r_bsp	Chain transfer			
✓ Drivers	Chain transfer setting			
✓ DMA Config_DTC	Continuous	Only when transfer	counter is changed from 1	1 to 0 or 1 to CRAH
✓ 🧁 Communications	Transfer mode setting			
Config_SCI12	Normal mode	O Repeat mode	O Block mode	
	Transfer data size setting	-	100	
	8 bits	16 bits	◯ 32 bits	
	Interrunt setting			
	Interrupt setting An interrupt request 	to the CPU is generated v	vhen specified data transfe	r is completed
	An interrupt request		when specified data transfe each time DTC data transfe	
	An interrupt request	to the CPU is generated e		
	 An interrupt request An interrupt request 	to the CPU is generated e		
	An interrupt request An interrupt request Block/Repeat area settin	to the CPU is generated e		
	 An interrupt request An interrupt request Block/Repeat area settin Transfer destination 	to the CPU is generated e		
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting Enable	to the CPU is generated of generated of Transfer source		
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting	to the CPU is generated of g Transfer source Disable		r is performed
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting Enable Transfer address and con Source address	to the CPU is generated of g Transfer source Disable unt setting N00000000	each time DTC data transfer	r is performed
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting Enable Transfer address and con Source address Destination address	to the CPU is generated of g Transfer source Disable Unit setting Ox0000000 Ox0000000	ach time DTC data transfer	ris performed
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting Enable Transfer address and con Source address Destination address Count	to the CPU is generated of g Transfer source Disable unt setting N00000000	each time DTC data transfer	ris performed
	An interrupt request An interrupt request Block/Repeat area settin Transfer destination Write back setting Enable Transfer address and con Source address Destination address	to the CPU is generated of g Transfer source Disable Unit setting Ox0000000 Ox0000000	each time DTC data transfer	ris performed

Note: The transfer count, source address, and destination address are to be changed by software, so here they are left at their default values.



3.3.3 Modifying the Program

Table 3.2 lists the functions to be modified.

 Table 3.3
 Functions to Be Modified

Function Name
R_Config_SCI12_Start
R_Config_SCI12_Serial_Send
R_Config_DTC_Create
R_Systeminit

R_Config_SCI12_Start ()

Before modification:

```
void R_Config_SCI12_Start (void)
{
    /* Clear interrupt flag */
    IR(SCI12, TXI12) = 0U;
    /* Enable SCI interrupt */
    IEN(SCI12, TXI12) = 1U;
    To be deleted because IEN is set to 1 at the start of
    IEN(SCI12, TXI12) = 1U;
    To be deleted because IEN is set to 1 at the start of
    IEN(SCI12, TXI12) = 1U;
}
```

```
void R Config SCI12 Start(void)
{
    /* Clear interrupt flag */
    IR(SCI12, TXI12) = 0U;
                                        To prevent a 0-to-1 TE state change from working as a
                                        trigger, set TE = 1 by this function to inhibit control by the
    /* Enable SCI interrupt */
                                        R_Config_SCI12_Serial_Send function.
    ICU.GENBLO.BIT.EN16 = 1U;
                                        Although TE = 1 sets IR of TXI12 to 1, no DTC transfer
    SCI12.SCR.BYTE |= 0xA0U;
                                        request is generated because IEN = 0. The request is held
                                        pending.
    /* Set TXD12 pin */
                                        Also, set the TXD12 pin when setting TE = 1.
    PORTA.PMR.BYTE |= 0x10U;
```


R_Config_SCI12_Serial_Send ()

Before modification:

MD_{{	<pre>MD_STATUS R_Config_SCI12_Serial_Send(uint8_t * const tx_buf, uint16_t tx_num) {</pre>					
	<pre>SCI12.SCR.BYTE = 0xA0U; /* Set TXD12 pin */ PORTA.PMR.BYTE = 0x10U;</pre>	←	To be deleted because SCI12.SCR.BYTE and the TXD12 pin are set by the R_Config_SCI12_Start function			
}	return MD_OK;	-				

After modification:





RX Family

How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

R_Config_DTC_Create ()

Before modification:

```
void R Config DTC Create void
                                                  To be changed so that the transfer
{
                                                  source address and the transfer
    /* Cancel DTC module stop state */
                                                  count can be set as arguments.
    MSTP(DTC) = OU;
    /* Disable transfer data read skip to clear the flag */
    DTC.DTCCR.BYTE = _08_DTC_TRANSFER_READSKIP_DISABLE;
    /* Set DTC0 transfer data */
    dtc_transferdata_vector117.mra_mrb = ((uint32_t)(_00_DTC_WRITE_BACK_ENABLE
_08_DTC_SRC_ADDRESS INCREMENTED |
                                           _00_DTC_TRANSFER_SIZE_8BIT |
                                           00 DTC TRANSFER MODE NORMAL) <<24U) |
((uint32 t) ( 00 DTC DST ADDRESS FIXED |
                                           00_DTC_INTERRUPT_COMPLETED) <<16U);
                                          = _00000000_DTC0_SRC_ADDRESS;
    dtc_transferdata_vector117.sar
                                          = _00000000_DTC0_DST_ADDRESS;
    dtc_transferdata_vector117.dar
    dtc_transferdata_vector117.cra_crb = (uint32 t)
                                          ( 0001 DTCO TRANSFER COUNT CRA) << 16U;
    /* Set transfer data start address in DTC vector table */
    dtc vector117 = (uint32 t) &dtc transferdata vector117;
                                                           The transfer source
    /* Set address mode */
                                                           address and the transfer
    DTC.DTCADMOD.BYTE = _00_DTC_ADDRESS_MODE_FULL;
                                                           count are to be set from
                                                           arguments.
    /* Set base address */
    DTC.DTCVBR = (void *) 0x0001FC00UL;
                                                           The transfer destination
                                                           address is to be changed
    /* Enable DTC module start */
                                                           to SCI12.TDR.
    DTC.DTCST.BYTE = 01 DTC MODULE START;
    R Config DTC Create UserInit();
```



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

After modification:

```
void R Config DTC Create(uint32 t sar, uint16 t count)
                                                      Changed so that the transfer source
    /* Cancel DTC module stop state */
                                                      address and the transfer count can
    MSTP(DTC) = OU;
                                                      be set as arguments.
    /* Disable transfer data read skip to clear the flag */
    DTC.DTCCR.BYTE = 08 DTC TRANSFER READSKIP DISABLE;
    /* Set DTC0 transfer data */
    dtc transferdata vector117.mra mrb = ((uint32 t)( 00 DTC WRITE BACK ENABLE
08 DTC SRC ADDRESS INCREMENTED |
                                            00 DTC TRANSFER SIZE 8BIT |
                                           00 DTC TRANSFER MODE NORMAL) <<24U) |
((uint32 t) ( 00 DTC DST ADDRESS FIXED |
                                           00 DTC INTERRUPT COMPLETED) <<16U);
                                          = sar;
    dtc transferdata vector117.sar
    dtc transferdata vector117.dar
                                          = (uint32 t) (&(SCI12.TDR));
    dtc_transferdata_vector117.cra_crb = (uint32 t)count << 16U;</pre>
    /* Set transfer data start address in DTC vector table */
    dtc vector117 = (uint32 t) &dtc transferdata vector117;
    /* Set address mode */
                                                          The transfer source
    DTC.DTCADMOD.BYTE = 00 DTC ADDRESS MODE FULL;
                                                          address and the transfer
                                                          count are set from
                                                          arguments.
    /* Set base address */
    DTC.DTCVBR = (void *) 0x0001FC00UL;
                                                          The transfer destination
                                                          address is changed to
    /* Enable DTC module start */
                                                          SCI12.TDR.
    DTC.DTCST.BYTE = _01_DTC MODULE START;
    R Config DTC Create UserInit();
```

Modifying the prototype declaration in the Config_DTC.h file:



RX Family

R_Systeminit()

Before modification:

```
void R Systeminit(void)
{
    /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
    SYSTEM.PRCR.WORD = 0xA50BU;
    /* Enable writing to MPC pin function control registers */
    MPC.PWPR.BIT.BOWI = OU;
    MPC.PWPR.BIT.PFSWE = 1U;
    /* Write 0 to the target bits in the POECR2 registers */
    POE3.POECR2.WORD = 0 \times 0000U;
    /* Initialize clocks settings */
    R CGC Create();
    /* Set peripheral settings */
                                          The initial settings are to be deleted because DTC
    R Config SCI12 Create();
                                          settings will be changed to such a specification that
   R_Config_DTC_Create();
                                          the transmit buffer and the transfer count are set
                                          before transmission from the SCI.
    /* Set interrupt settings */
    R Interrupt Create();
    /* Register undefined interrupt */
    R_BSP_InterruptWrite(BSP_INT_SRC_UNDEFINED_INTERRUPT,
     (bsp int cb t)r undefined exception);
    /* Register group BL0 interrupt TEI12 (SCI12) */
    R BSP InterruptWrite(BSP INT SRC BL0 SCI12 TEI12,
     (bsp int cb t)r Config SCI12 transmitend interrupt);
    /* Disable writing to MPC pin function control registers */
    MPC.PWPR.BIT.PFSWE = OU;
    MPC.PWPR.BIT.BOWI = 1U;
    /* Enable protection */
    SYSTEM.PRCR.WORD = 0xA500U;
```



After modification:

```
void R Systeminit(void)
   /* Enable writing to registers related to operating modes, LPC, CGC and
software reset */
   SYSTEM.PRCR.WORD = 0xA50BU;
   /* Enable writing to MPC pin function control registers */
   MPC.PWPR.BIT.BOWI = OU;
   MPC.PWPR.BIT.PFSWE = 1U;
   /* Write 0 to the target bits in the POECR2 registers */
   POE3.POECR2.WORD = 0x0000U;
    /* Initialize clocks settings */
   R CGC Create();
   /* Set peripheral settings */
   R Config SCI12 Create();
   /* Set interrupt settings */
   R Interrupt Create();
   /* Register undefined interrupt */
   R BSP InterruptWrite (BSP INT SRC UNDEFINED INTERRUPT,
    (bsp int cb t)r undefined exception);
    /* Register group BL0 interrupt TEI12 (SCI12) */
   R BSP InterruptWrite(BSP INT SRC BL0 SCI12 TEI12,
     (bsp int cb t)r Config SCI12 transmitend interrupt);
   /* Disable writing to MPC pin function control registers */
   MPC.PWPR.BIT.PFSWE = OU;
   MPC.PWPR.BIT.BOWI = 1U;
    /* Enable protection */
    SYSTEM. PRCR. WORD = 0 \times A500U;
```



3.3.4 Sample Program

The following shows how the sample program works.

[Main function]

- (1) Call the R_Config_SCI12_Start function to configure transmission.
- (2) Call the R_Config_DTC_Create function to set transmit data for the DTC transfer source, the SCI transmit buffer for the transfer destination, and the transfer count.
- (3) Set g_flag = 0, and set g_flag = 1 only after transmission is complete to prevent further processing until transmission is complete.
- (4) Execute the R_Config_DTC_Start function to put the DTC in a state waiting for transfer.
- (5) Call the R_Config_SCI12_Serial_Send function to enable the TXI interrupt that works as an activation source for the DTC. DTC transfer occurs at the timing of the TXI interrupt, and transmit data is written to the transmit buffer.
- (6) Wait until transmission is completed.
- (7) Insert 300-µs wait time.
- (8) Repeat steps (2) to (7) twice.
- (9) After transmission is completed, call the R_Config_DTC_Stop function and the R_Config_SCI12_Stop function to disable the transmission setting.
- Note: Since the R_Config_SCI12_Create function is called in the R_Systeminit function before reaching the main function, it does not need to be called in the main function.



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

```
Global variables
volatile uint8 t g flag;
Private (static) variables and functions
            uint8 t
       g_data[] = \{0x11, 0x22, 0x33\};
void main(void);
* Function Name: main
* Description : This function uses the modified program to send data without a wait time.
* Arguments : None
* Return Value : None
void main(void)
{
  uint8_t i
                = 0;
  uint8 t send count = 2;
  R Config SCI12 Start();
  for (i = 0; i < send count; i++)
   {
     g flag = 0;
     R Config DTC Create((uint32 t)g data, 3 );
     R Config DTC Start();
     R Config SCI12 Serial Send(NULL, 0);
     while (0 == g flag)
     {
        nop();
     }
     R_BSP_SoftwareDelay((uint32_t)300, BSP_DELAY_MICROSECS);
  }
  R Config DTC Stop();
  R Config SCI12 Stop();
  while (1)
  {
     nop();
  }
```

Figure 3.13 "main" Function of the Sample Program



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

[SCI12 transmission end callback function]

- (1) The SCI12 transmit end callback function (r_Config_SCI12_callback_transmitend) is called upon completion of DTC transfer and upon completion of SCI transfer.
- (2) When the transmission end interrupt is disabled (TEIE = 0), the function judges that it is called because DTC transfer is completed, so it disables the TXI interrupt request and enables the transmission end interrupt (TEIE = 1).
- (3) When the transmission end interrupt is enabled (TEIE = 1), the function judges that it is called because transmission is completed, so it disables the transmission end interrupt and sets the transmission end flag (g_flag = 1).

```
* Function Name: r_Config_SCI12_callback_transmitend
* Description : This function is a callback function when SCI12 finishes
transmission
* Arguments
           : None
* Return Value : None
static void r_Config_SCI12_callback_transmitend(void)
{
   /* Start user code for r_Config_SCI12_callback_transmitend. Do not edit
comment generated here */
 if(0 == SCI12.SCR.BIT.TEIE)
 {
  /* Interrupt processing when DTC transfer is completed */
  IEN(SCI12, TXI12) = 0U;
   SCI12.SCR.BIT.TEIE = 1U;
 }
 else
 {
  /* Interrupt processing when SCI12 transmit end */
  SCI12.SCR.BIT.TEIE = OU;
  g_flag = 1;
 }
 /* End user code. Do not edit comment generated here */
```

Figure 3.14 "r_Config_SCI12_callback_transmittend" Function in the Sample Program



3.3.5 Operation of the Sample Program

Figure 3.15 shows the waveforms when the control example using the DTC is operated.



Figure 3.15 Waveforms of the Sample Program

It can be confirmed that during the first transmission, an internal wait time occurs when TE changes from 0 to 1, but during the second transmission, the TE bit is not controlled, so the transmission starts without generating an internal wait time. For the first transmission, no internal wait time occurs either if the R_Config_SCI12_Serial_Send function is executed at least one frame after the R_Config_SCI12_Start function is called.



4. Disabling Automatic Code Regeneration at Build Time

Smart Configurator is provided with a function that automatically regenerates code at build time.

In this sample program, this function is disabled because code-generated components are modified for use.

Note that if you regenerate the code manually, the components will be overwritten.

If you generate the code manually, salvage the components from the trash folder or make a backup beforehand.

Figure 4.1 shows how to disable code regeneration when building with e² studio.



Figure 4.1 Disabling Automatic Code Regeneration at Build Time



5. Importing a Project

The sample programs are distributed in e^2 studio project format. This section shows how to import a project into e^2 studio or CS+. After importing the sample project, make sure to confirm build and debugger setting.

5.1 Importing a Project into e² studio

To use sample programs in e² studio, follow the steps below to import them into e² studio.

In projects managed by e² studio, do not use space codes, multibyte characters, and symbols such as "\$", "#", "%" in folder names or paths to them.

(Note that depending on the version of e² studio you are using, the interface may appear somewhat different from the screenshots below.)

	🥶 work - e' studio	
	File Edit Source Refactor Navigate Search Project Renesas Views Rui New Alt+Shift+N > h Configurations	
	Open File	
	Open Projects from File System [™] : Ø : @ ▼ 63	🛢 Import — 🗆 🗙
	Recent Files	import – L X
	Close Editor Ctrl+W	Select
	Class All F	Create new projects from an archive file or directory.
	Start the e ² studio and select the	
	File >> [Import 1	Select an import wizard:
		type filter text
	Save All Ctrl+Shift+S	Seneral
	Revert	Archive File
	Move	Existing Projects into Workspace
	Rename F2	Preferences
	E Refresh F5	[©] Projects from Pold
	Convert Line Delimiters To >	
	Print Ctrl+P	☐ Renesas CCRX pro ☐ Renesas CS+ Projection
	🔄 Import	🚘 Renesas CS+ Project for CC-RX and CC-RL
	🗠 Export	Renesas GitHub FreeRTOS (with IoT libraries) Project
	Properties Alt+Enter	Sample Projects on Renesas Website > >> C/C++
		> > Code Generator
	Switch Workspace > Restart	N Cas Install
	Exit	
	LAIL	
	Select a directory to search for existing Eclipse projects. Select root directory: C*application_note¥sample_project Select root directory:	Select [Select roo <u>t</u> directory:].
	○ Select <u>a</u> rchive file:	se
	Projects:	
	sample_project (C:¥application_note¥sample_project)	
	Deselection of the second	directory which stored the project to import.
[Options Search for no ted projects Copy projects into workspace Copy projects into workspace Copy constrained projects upon completion Hide projects that already exist in the workspace Working sets Add project to working sets	Select [Copy projects into workspace(C)] when to copy project to workspace.
	oject to working sets] e working sets.	
	(?) < <u>Back</u> Next > Einish Canc	el

Figure 5.1 Importing a Project into e² studio



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

5.2 Importing a Project into CS+

To use sample programs in CS+, follow the steps below to import them into CS+.

In projects managed by CS+, do not use space codes, multibyte characters, and symbols such as "\$", "#", "%" in folder names or paths to them.

(Note that depending on the version of CS+ you are using, the interface may appear somewhat different from the screenshots below.)



Figure 5.2 Importing a Project into CS+



6. Reference Documents

- RX660 Group User's Manual: Hardware (R01UH0937)
- Renesas e² studio Smart Configurator User's Guide (R20AN0451)
- Renesas Starter Kit for RX660 User's Manual (R20UT5017)
- Renesas Starter Kit for RX660 CPU Board Circuit Diagram (R20UT5016)



RX Family How to Start Transmission Immediately After Writing Transmit Data in SCI Asynchronous Mode

Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Mar.20.23	-	First edition issued
1.01	Mar.21.24	1	Added Target Tools



General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.)

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
- 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
- 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- 4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
- 5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
- Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

- 7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
- 8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
- 9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
- 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
- 12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.