RX Family

How to Prevent the On-Chip Flash Memory from Being Accessed by Third Parties or Being Accidentally Programmed by Developers

Summary

This application note describes methods of prohibiting access by third parties to the on-chip flash memory of Renesas MCUs for each connection configuration and methods of protecting the on-chip flash memory during self-programming initiated by developers.

As used in this application note, the terms “developer” and “third party” are defined as follows.

Developer: The program developer. The person enabling protection of the on-chip flash memory.

Third party: A person other than the developer.

Target Devices

RX Family

Contents

1. Protection from Third-Party Access

An overview of the structure of this chapter is shown in Figure 1-1. This chapter explains the available protection features for each user connection type. The RX groups include functional enhancements and improvements, even for the same protection features like ID Code Protect. This application note classifies the functions into types by appending the letters A through D to the end of the function names for identification purposes.

1.1 Protection functions for each connection type

Connection type	Protection Functions	Description
1.1.1 Serial Programmer Connection	1.1.1.1 ID Code Protection	Protection Type: 1.1.1.1.1 ID Code Protection A — Protection Setting Patterns: Description of four protection patterns in (1)–(4) Protection Type: 1.1.1.1.2 ID Code Protection B — Protection Setting Patterns: Description of four protection patterns in (1)–(4) Protection Type: 1.1.1.1.3 ID Code Protection C — Protection Setting Patterns: Description of four protection patterns in (1)–(4) Protection Type: 1.1.1.1.4 ID Code Protection D — Protection Setting Patterns: Description of five protection patterns in (1)–(5)
	1.1.1.2 Access Window	Description of three access window function
1.1.2 On-Chip Debugger Connection	1.1.2.1 On-Chip Debugger ID Code Protection	Protection Type: 1.1.2.1.1 On-Chip Debugger ID Code Protection A — Protection Setting Patterns: Description of three protection patterns in (1)–(3) Protection Type: 1.1.2.1.2 On-Chip Debugger ID Code Protection B — Protection Setting Patterns: Description of two protection patterns in (1)–(2) Protection Type: 1.1.2.1.3 On-Chip Debugger ID Code Protection C — Protection Setting Patterns: Description of three protection patterns in (1)–(3)
	1.1.2.2 Access Window	
1.1.3 Parallel Programmer Connection	1.1.3.1 ROM Code Protection	Description of three protection patterns

1.2 Other Protection Function

Protection Functions
1.2.1 Trusted Memory

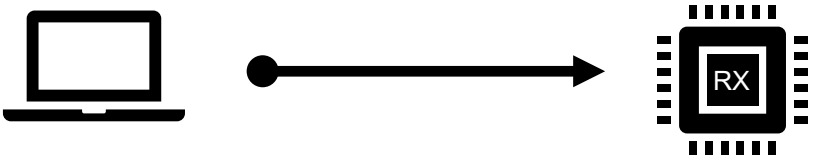
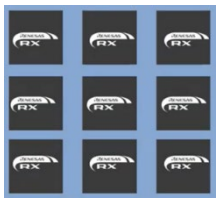
Legend: Function name

Figure 1-1 Structure of Chapter 1

The types of third-party connections include serial programmer, on-chip debugger, and parallel programmer connections. This chapter describes protection methods against third-party access for each of these connection types.

Connection images for each connection type are shown in Table 1-1.

Table 1-1 Connection images for each connection type

Connection type	Connection images
Serial Programmer Connection On-Chip Debugger Connection	 **On-Board Programming**
Parallel Programmer Connection	 **Off-Board Programming**

1.1 Protection functions for each connection type

An overview of the protection functions available for each connection type is shown in Table 1-2.

Table 1-2 Overview of Protection Functions by Connection Type

Connection type	Protection Functions	Overview of Protection Functions
Serial Programmer Connection	ID Code Protection	After the MCU starts up in boot mode, ID authentication is performed when a host such as a PC is connected, prohibiting connection by third parties and preventing reading, programming, or erasing of the on-chip flash memory.
	Access Window	If the access window is set, the area set outside the access window is prevented programming or erasing. The access window is a function to prevent erroneous rewriting in case a program runs out of control during self-programming.
On-Chip Debugger Connection	On-Chip Debugger ID Code Protection	After the MCU starts up in single-chip mode or user boot mode, ID authentication is performed when an on-chip debugger is connected, prohibiting connection by third parties and preventing reading, programming, or erasing of the on-chip flash memory.
	Access Window	If the access window is set, the area set outside the access window is prevented programming or erasing. The access window is a function to prevent erroneous rewriting in case a program runs out of control during self-programming.
Parallel Programmer Connection	ROM Code Protection	When a parallel programmer is used, reading, programming, or erasing of the on-chip flash memory by third parties is prevented.

The protection functions available for each connection type on each device are listed in Table 1-3. For details of each protection function, refer to the User's Manual: Hardware of the device.

Table 1-3 List of Device Protection Functions

Connection type	Serial Programmer Connection	On-Chip Debugger Connection	Parallel Programmer Connection	Serial Programmer Connection or On-Chip Debugger Connection
	Protection Function (✓: Supported, —: Not Supported, A-D: Supported(Category symbol within the function)*)			
Devices	ID Code Protection	On-Chip Debugger Connection	ROM Code Protection	Access Window
• RX110	A	A	—	A
• RX111	A	A	—	A
• RX113	A	A	—	A
• RX130	A	A	—	A
• RX13T	A	A	—	A
• RX140	A	A	—	B
• RX14T	A	A	—	B
• RX210	A	A	✓	—
• RX21A	A	A	—	—
• RX220	A	A	—	—
• RX230	A	A	✓	A
• RX231	A	A	✓	A
• RX23E-A	A	A	—	A
• RX23E-B	A	A	—	A
• RX23T	A	A	—	A
• RX23W	A	A	—	A
• RX24T	A	A	✓	A
• RX24U	A	A	✓	A
• RX260	A	A	—	B
• RX261	A	A	—	B
• RX26T	D	C	—	C
• RX610	A	A	✓	—
• RX621	A	A	✓	—
• RX62G	A	A	✓	—
• RX62N	A	A	✓	—
• RX62T	A	A	✓	—
• RX630	A	A	✓	—
• RX631	A	A	✓	—
• RX634	A	A	✓	—
• RX63N	A	A	✓	—
• RX63T	A	A	✓	—
• RX64M	B	B	✓	—
• RX651	C	B	✓	C
• RX65N	C	B	✓	C
• RX65W	C	B	✓	C

• RX660	D	C	✓	—
• RX66N	C	B	✓	C
• RX66T	D	B	✓	—
• RX671	C	C	✓	C
• RX71M	B	B	✓	—
• RX72M	C	B	✓	C
• RX72N	C	B	✓	C
• RX72T	D	B	✓	—

Note: * A-D : The ID Code Protection and On-Chip Debugger ID Code Protection are referred to by the same name in the User's Manual: Hardware of the device for all RX groups. Since each RX group includes functional enhancements or improvements, this application note classifies the functions into types by appending the letters A through D to the end of the function names for identification purposes.

1.1.1 Serial Programmer Connection

This section explains the protection functions in the Serial Programmer Connection.

Depending on the boot mode, the RX microcontroller is connected via a serial interface such as UART or USB.

1.1.1.1 ID Code Protection

The ID Code Protection is a protection feature that, after the MCU starts up in boot mode, ID authentication is performed when a host such as a PC is connected, prohibiting connection by third parties, thereby preventing reading, programming, or erasing of the on-chip flash memory.
Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to D to the end of each function name.

This chapter explains these four types separately.

Table 1-4 shows the setting details of each type.

Table 1-4 Types and Setting Details of ID Code Protection

Types	Characteristics
ID Code Protection A	The control code (1 byte) and ID codes 1 to 15 (15 bytes) are set at addresses 0xFFFFFFA0 to 0xFFFFFFAF (16 bytes) on the on-chip flash memory.
ID Code Protection B	Set the OSIS register (ID code) and the SPE, IDE, PDPR, WRPR, and SEPR bits in the SPCC register.
ID Code Protection C	Set the OSIS register (the control code and ID Codes 1 through 15) and the OCDE bit in the SPCC register.
ID Code Protection D	Set the OSIS register (the control code and ID Codes 1 through 15) and the SPE, IDE, PDPR, WRPR, and SEPR bits in the SPCC register.

1.1.1.1.1 ID Code Protection A

This section provides an explanation for devices classified as Type A in the ID Code Protection of **Table 1-3**.

1.1.1.1.1.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.1.1.1.2(1) to 1.1.1.1.1.2(4).

- Protection setting pattern A1
  This protection prevents memory readout without distinction between third parties and developers. When connected in boot mode, the entire internal flash memory is erased.
- Protection setting pattern A2
  This protection setting pattern prevents reading by third parties. When a connection is made in boot mode, ID authentication takes place. If multiple consecutive mismatches of the ID code occur, the on-chip flash memory is erased completely, without distinction between third parties and developers.
- Protection setting pattern A3
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern A4
  This protection setting pattern prohibits connections by both developers and third parties. Once this protection setting pattern is applied, **the protection cannot be removed, so caution is necessary**.

Table 1-5 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase			
		Developer		Third party	
		R	P/E	R	P/E
A1	Reading is prevented by complete erasure of the on-chip flash memory.*1	—	✓	—	✓
A2	Reading, programming, and erasing are enabled when the ID code matches. The on-chip flash memory is erased completely*1 if repeated ID code mismatches occur.	✓	✓	—*2	—
A3	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	—	—
A4	Reading, programming, and erasing are prevented always.	—	—	—	—

R : Read P/E : Program/Erase
✓: Allowed, —: Not allowed

Note 1. For details of the scope of “complete erasure,” refer to the User’s Manual: Hardware of the device.
Note 2. The on-chip flash memory is erased completely if repeated ID code mismatches occur.

When a USB connection in boot mode is established for the following devices, no ID authentication takes place but the user area and data area are erased, thereby preventing third parties from reading from the on-chip flash memory.

- RX621, RX62N, RX630, RX631, RX63N, RX63T

1.1.1.1.1.2 Description of Protection Setting Patterns

The settings are made in a 16-byte area from address 0xFFFFFFA0 to 0xFFFFFFAF on the internal flash memory.

The control code (1 byte) and the ID code (15 bytes) are set.

The Serial Programmer Connection is permitted when the ID code matches and denied when it does not.

(1) Protection Setting Pattern A1

In this pattern, the on-chip flash memory is erased when connected in boot mode.

The setting details of protection setting pattern A1 are shown in **Table 1-6**.

Table 1-6 Protection Setting Pattern A1 Setting Details

ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
Other than (45h, 52h)	Any value

For the setting method, refer to 1.1.1.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A1 is outlined in **Table 1-7**.

Table 1-7 Operation of Protection Setting Pattern A1

Devices	**Operation**	**Prevented Items**
・RX110 ・RX111 ・RX113	If a connection occurs in boot mode and there is no data in the on-chip flash memory, no ID authentication occurs and the device transitions to a state in which reading, programming, and erasing are possible. If a connection occurs in boot mode and there is data in the on-chip flash memory, no ID authentication occurs and the device transitions to the erase-ready state. After all blocks in the user area and data area have been erased, the device transitions to a state in which reading, programming, and erasing are possible.	Reading of the contents of the on-chip flash memory by third parties is prevented by transitioning to the erase-ready state and preventing reading and programming until all blocks in the user area and data area have been erased.
Other	When a connection is made in boot mode, no ID authentication occurs and the on-chip flash memory is erased completely. The device then transitions to a state in which reading, programming, and erasing are possible.	Reading the contents of the on-chip flash memory by a third party is prevented by complete erasure of the on-chip flash memory.

(2) Protection Setting Pattern A2

This pattern provides protection by means of ID authentication. However, if ID authentication fails three times in succession, the on-chip flash memory is erased completely.

The setting details of protection setting pattern A2 are shown in **Table 1-8**.

Table 1-8 Protection Setting Pattern A2 Setting Details

ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
45h	Any value

For the setting method, refer to 1.1.1.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A2 is outlined in **Table 1-9**.

Table 1-9 Operation of Protection Setting Pattern A2

Devices	**Operation**	**Prevented Items**
・RX110 ・RX111 ・RX113	Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again. However, if ID authentication fails three times in succession, the device transitions to the erase-ready state. After all blocks in the user area and data area have been erased, the device transitions to a state in which reading, programming, and erasing are possible.	Reading of the on-chip flash memory by third parties is prevented by transitioning to the erase-ready state and preventing reading and programming until all blocks in the user area and data area have been erased. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.
Other	Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again. However, if ID authentication fails three times in succession, the on-chip flash memory is erased completely.	Reading the contents of the on-chip flash memory by a third party is prevented by complete erasure of the on-chip flash memory. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(3) Protection Setting Pattern A3

This pattern provides protection by means of ID authentication.

The setting details of protection setting pattern A3 are shown in **Table 1-10**.

Table 1-10 Protection Setting Pattern A3 Setting Details

ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
52h	Other than 50h,72h,6Fh,74h,65h,63h,74h,FFh,…,FFh

For the setting method, refer to 1.1.1.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A3 is outlined in **Table 1-11**.

Table 1-11 Operation of Protection Setting Pattern A3

Operation	**Prevented Items**
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(4) Protection Setting Pattern A4

This pattern prevents reading, programming, or erasing of the on-chip flash memory when a connection is made in boot mode.

Note: After this setting is made and the device is reset, **the protection cannot be removed by any method, so caution is necessary**.

The setting details of protection setting pattern A4 are shown in **Table 1-12**.

Table 1-12 Protection Setting Pattern A4 Setting Details

ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
52h	50h,72h,6Fh,74h,65h,63h,74h,FFh,…,FFh

For the setting method, refer to 1.1.1.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A4 is outlined in **Table 1-13**.

Table 1-13 Operation of Protection Setting Pattern A4

Operation	**Prevented Items**
ID authentication is performed when a connection is made in boot mode, but the ID code is always processed as not matching, and ID authentication is performed again.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.1.1.1.3 Protection Setting Examples

Each protection function is enabled by setting a control code and ID code to addresses in the on-chip flash memory. The control code and ID code should be set to 0xFFFFFFA0.

Protection setting examples are shown in **Figure 1-2** and **Figure 1-3** .

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE[4] = {0x45010203, 0x04050607, 0x08090A0B, 0x0C0D0E0F};
```

In this example, the control code is 45h, and the ID code is 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

Figure 1-2 Protect Setting Pattern A2 Setting Example

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE[4] = {0x5250726F, 0x74656374, 0xFFFFFFFF, 0xFFFFFFFF};
```

In this example, the control code is 52h, and the ID code is 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh.

Figure 1-3 Protect Setting Pattern A4 Setting Example

1.1.1.1.2 ID Code Protection B

This section provides an explanation for devices classified as Type B in the ID Code Protection of **Table 1-3**.

1.1.1.1.2.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.1.1.2.2(1) to 1.1.1.1.2.2(4).

- Protection setting pattern B1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern B2
  This protection setting pattern individually enables/disables reading, programming, or erasing of the on-chip flash memory by third parties and developers, without distinction.
- Protection setting pattern B3
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern B4
  This protection setting pattern prohibits connections by both developers and third parties.

Table 1-14 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase					
		Developer			Third party		
		R	P	E	R	P	E
B1	Disabled	✓	✓	✓	✓	✓	✓
B2	Individually enables/disables reading, programming, or erasing.	✓/—*1	✓/—*1	✓/—*1	✓/—*1	✓/—*1	✓/—*1
B3	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	✓	—	—	—
B4	Reading, programming, and erasing are prevented always.	—	—	—	—	—	—

R : Read P/E : Program/Erase
✓: Allowed, —: Not allowed

Note 1. The serial programmer command control register (SPCC) is used to individually enable or disable reading, programming, or erasing. For details of the serial programmer command control register (SPCC), refer to the User's Manual: Hardware of the device.

1.1.1.1.2.2 Description of Protection Setting Patterns

The configuration is applied to the Serial Programmer Command Control Register(SPCC) and the OCD/Serial Programmer ID Setting Register(OSIS).

Serial Programmer Connection is basically permitted when the Serial Programmer Enable bit(SPCC.SPE) is set to 1, and prohibited when it is set to 0.

In addition, by configuring the Serial Programmer Command Control settings — specifically the Read Command Protect bit(SPCC.RDPR), Programming Command Protect bit(SPCC.WRPR), and Block Erasure Command Protect bit(SPCC.SEPR) — read, program, and erase operations can be individually permitted or prohibited.

(1) Protection Setting Pattern B1

This pattern disables all protection.

The setting details of protection setting pattern 1 are shown in **Table 1-15** and **Table 1-16**.

Table 1-15 Protection Setting Pattern B1 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 bytes)				
ID Code Protection Enable bit (IDE) (bit: b24)	**ID Code Protection Enable bit (IDE) (bit: b24)**	**ID Code Protection Enable bit (IDE) (bit: b24)**	**ID Code Protection Enable bit (IDE) (bit: b24)**	**ID Code Protection Enable bit (IDE) (bit: b24)**
1	1	1	1	1

Table 1-16 Protection Setting Pattern B1 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
All FFh

For the setting method, refer to 1.1.1.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B1 is outlined in **Table 1-17**.

Table 1-17 Operation of Protection Setting Pattern B1

Operation	**Prevented Items**
If a connection occurs in boot mode, no ID authentication occurs and the device transitions to a state in which reading, programming, and erasing are possible.	None

(2) Protection Setting Pattern B2

This pattern does not perform ID code verification; however, reading, programming, or erasing of the on-chip flash memory can be enabled/disabled individually.

The setting details of protection setting pattern B2 are shown in **Table 1-18** and **Table 1-19**.

Table 1-18 Protection Setting Pattern B2 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
Serial Programmer Connection Enable bit (SPE) (bit: b27)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**
1	1	0/1*1	0/1*2	0/1*3

Note 1. When the SEPR bit is set to 1 erasing is enabled, and erasing is disabled when it is cleared to 0.
Note 2. When the WRPR bit is set to 1 programming is enabled, and programming is disabled when it is cleared to 0.
Note 3. When the RDPR bit is set to 1 reading is enabled, and reading is disabled when it is cleared to 0.

Table 1-19 Protection Setting Pattern B2 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.1.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B2 is outlined in **Table 1-20**.

Table 1-20 Operation of Protection Setting Pattern B2

Operation	**Prevented Items**
No ID authentication occurs when a connection is made in boot mode. Enables/disables reading, programming, and erasing individually after the connection is established.	Individually disables enables/disables reading, programming, and erasing, without distinction between third parties and developers.

(3) Protection Setting Pattern B3

In this pattern, protection based on ID authentication is performed when a connection is made in boot mode.

The setting details of protection setting pattern B3 are shown in **Table 1-21** and **Table 1-22**.

Table 1-21 Protection Setting Pattern B3 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
Serial Programmer Connection Enable bit (SPE) (bit: b27)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**
0	1	0	0	0

Table 1-22 Protection Setting Pattern B3 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.1.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B3 is outlined in **Table 1-23**.

Table 1-23 Operation of Protection Setting Pattern B3

Operation	**Prevented Items**
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(4) Protection Setting Pattern B4

In this pattern, connections to a host are prohibited in boot mode.

The setting details of protection setting pattern B4 are shown in **Table 1-24** and **Table 1-25**.

Note that both setting number 1 and setting number 2 prohibit connections to a host in boot mode.

Table 1-24 Protection Setting Pattern B4 Setting Details 1

	Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
	Serial Programmer Command Control Register (SPCC) (4 Bytes)				
Setting No.	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**
1	0	0	0	0	0
2	1	0	Don’t care	Don’t care	Don’t care

Table 1-25 Protection Setting Pattern B4 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.1.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B4 is outlined in **Table 1-26**.

Table 1-26 Operation of Protection Setting Pattern B4

Operation	**Prevented Items**
Connections to a host are prohibited when connecting in boot mode.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.1.1.2.3 Protection Setting Examples

Each protection function is enabled by setting serial programmer connection enable/disable, serial programmer command control, and an ID code to addresses in the option-setting memory to an address in the on-chip flash memory. Serial programmer connection enable/disable and serial programmer command control should be setting to 0x00120040 and the ID code to 0x00120050.

Also, for instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Protection setting examples are shown in **Figure 1-4** and **Figure 1-5**.

```
/* Setup the Serial programmer command control register */
#pragma address SPCC_REG = 0x00120040
const unsigned long SPCC_REG = 0x1EFFFFFF

/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0x00120050
const unsigned long ID_CODE[4] = {0x04030201, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the ID code is 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-4 Protect Setting Pattern B3 Setting Example

```
/* Setup the Serial programmer command control register */
#pragma address SPCC_REG = 0x00120040
const unsigned long SPCC_REG = 0x16FFFFFF

/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0x00120050
const unsigned long ID_CODE[4] = {0x04030201, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the ID code is 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-5 Protect Setting Pattern B4 Setting Example

1.1.1.1.3 ID Code Protection C

This section provides an explanation for devices classified as Type C in the ID Code Protection of **Table 1-3**.

1.1.1.1.3.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.1.1.3.2(1) to 1.1.1.1.3.2(4).

- Protection setting pattern C1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern C2
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern C3
  This protection setting pattern prevents reading, programming, or erasing by third parties. If ID authentication fails three times in succession, the on-chip flash memory is erased completely.
- Protection setting pattern C4
  This protection setting pattern prohibits connections by both developers and third parties.

Table 1-27 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Connection in Boot Mode (ID Code Protection, Serial Programmer Connection Enable/Disable)			
		Developer		Third party	
		R	P/E	R	P/E
C1	Disabled	✓	✓	✓	✓
C2	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	—	—
C3	Reading, programming, and erasing are enabled when the ID code matches. If ID authentication fails three times in succession, the on-chip flash memory is erased completely.	✓	✓	—*1	—
C4	Reading, programming, and erasing are prevented always.	—	—	—	—

R: Read, P/E: Program/Erase
✓: Allowed, —: Not allowed

Note 1. The on-chip flash memory is erased completely if repeated ID code mismatches occur.

1.1.1.1.3.2 Description of Protection Setting Patterns

The configuration is applied to the Serial Programmer Command Control Register(SPCC) and the OCD/Serial Programmer ID Setting Register(OSIS).

The OSIS is configured with the control code (1 byte) and the ID code (15 bytes).

Serial Programmer Connection is basically permitted when the Serial Programmer Enable bit(SPCC.SPE) is set to 1, and prohibited when it is set to 0.

(1) Protection Setting Pattern C1

This pattern disables all protection.

The setting details of protection setting pattern C1 are shown in **Table 1-28**.

Table 1-28 Protection Setting Pattern C1 Setting Details

ID Code Protection Settings	Serial Programmer Connection Enable/Disable
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 Bytes)**
All FFh	FFFF FFFFh

For the setting method, refer to 1.1.1.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C1 is outlined in **Table 1-29**.

Table 1-29 Operation of Protection Setting Pattern C1

Operation	Prevented Items
If a connection occurs in boot mode, the device transitions to a state in which reading, programming, and erasing are possible by transmitting the ID code all set to FFh.	None

(2) Protection Setting Pattern C2

In this pattern, protection based on ID authentication is performed when a connection is made in boot mode.

The setting details of protection setting pattern C2 are shown in **Table 1-30**.

Table 1-30 Protection Setting Pattern C2 Setting Details

ID Code Protection Settings	Serial Programmer Connection Enable/Disable
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 Bytes)**
Control code / ID code 1: Other than 45h ID code 2 to ID code 16: Any value	FFFF FFFFh

For the setting method, refer to 1.1.1.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C2 is outlined in **Table 1-31**.

Table 1-31 Operation of Protection Setting Pattern C2

Operation	Prevented Items
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(3) Protection Setting Pattern C3

In this pattern, protection based on ID authentication is performed when a connection is made in boot mode. If ID authentication fails three times in succession, the on-chip flash memory is erased completely in boot mode.

The setting details of protection setting pattern C3 are shown in Table 1-32.

Table 1-32 Protection Setting Pattern C3 Setting Details

ID Code Protection Settings	Serial Programmer Connection Enable/Disable
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 Bytes)**
Control code / ID code 1: 45h ID code 2 to ID code 16: Any value	FFFF FFFFh

For the setting method, refer to 1.1.1.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C3 is outlined in Table 1-33.

Table 1-33 Operation of Protection Setting Pattern C3

Operation	Prevented Items
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again. If ID authentication fails three times in succession, the on-chip flash memory is erased completely in boot mode.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. If ID authentication fails three times in succession, the on-chip flash memory is erased completely. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(4) Protection Setting Pattern C4

In this pattern, connection to the host is prohibited during boot mode.

The setting details of protection setting pattern C4 are shown in **Table 1-34**.

Table 1-34 Protection Setting Pattern C4 Setting Details

ID Code Protection Settings	Serial Programmer Connection Enable/Disable
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 Bytes)**
16 bytes are Other than FFh	F7FFFFFFh (SPE bit = 0)

For the setting method, refer to 1.1.1.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C4 is outlined in **Table 1-35**.

Table 1-35 Operation of Protection Setting Pattern C4

Operation	Prevented Items
Connections to a host are prohibited when connecting in boot mode.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.1.1.3.3 Protection Setting Examples

Each protection function is enabled by setting serial programmer connection enable/disable and the ID code to addresses in the option-setting memory. Serial programmer connection enable/disable should be set to 0xFE7F5D40 and the ID code to 0xFE7F5D50.

Also, for instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Protection setting examples are shown in **Figure 1-6** and **Figure 1-7**.

```
/* Setup the Serial programmer command control Register */
#pragma address SPCC_REG = 0xFE7F5D40
const unsigned long SPCC_REG = 0xFFFFFFFF;

/* Setup the OCD/Serial Programmer ID Setting Register */
#pragma address OSIS_REG = 0xFE7F5D50
const unsigned long OSIS_REG[4] = {0x04030245, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the Control code / ID code 1 is 45h, from ID code 2 to ID code 16 are 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-6 Protect Setting Pattern C3 Setting Example

```
/* Setup the Serial programmer command control Register */
#pragma address SPCC_REG = 0xFE7F5D40
const unsigned long SPCC_REG = 0xF7FFFFFF;

/* Setup the OCD/Serial Programmer ID Setting Register */
#pragma address OSIS_REG = 0xFE7F5D50
const unsigned long OSIS_REG[4] = {0x04030201, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the Control code / ID code 1 is 01h, from ID code 2 to ID code 16 are 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-7 Protect Setting Pattern C4 Setting Example

1.1.1.1.4 ID Code Protection D

This section provides an explanation for devices classified as Type D in the ID Code Protection of **Table 1-3**.

1.1.1.1.4.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.1.1.4.2(1) to 1.1.1.1.4.2(5).

- Protection setting pattern D1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern D2
  This protection setting pattern individually enables/disables reading, programming, or erasing of the on-chip flash memory by third parties and developers, without distinction.
- Protection setting pattern D3
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern D4
- This protection setting pattern prevents reading, programming, or erasing by third parties. If ID authentication fails three times in succession, the on-chip flash memory is erased completely.
- Protection setting pattern D5
  This protection setting pattern prohibits connections for developers and third parties.

Table 1-36 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Connection in Boot Mode (ID Code Protection, Serial Programmer Connection Enable/Disable, Serial Programmer Command Control)					
		Developer			Third party		
		R	P	E	R	P	E
D1	Disabled	✓	✓	✓	✓	✓	✓
D2	Individually enables/disables reading, programming, or erasing.	✓/× *1	✓/× *1	✓/× *1	✓/× *1	✓/× *1	✓/× *1
D3	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	✓	—	—	—
D4	Reading, programming, and erasing are enabled when the ID code matches. If ID authentication fails three times in succession, the on-chip flash memory is erased completely.	✓	✓	✓	—*2	—	—
D5	Reading, programming, and erasing are prevented always.	—	—	—	—	—	—

R: Read, P: Program, E: Erase
✓: Allowed, —: Not allowed

Note 1. The serial programmer command control register (SPCC) is used to individually enable or disable reading, programming, or erasing. For details of the serial programmer command control register (SPCC), refer to the User's Manual: Hardware of the device.

Note 2. The on-chip flash memory is erased completely if repeated ID code mismatches occur.

1.1.1.1.4.2 Description of Protection Setting Patterns

The configuration is applied to the Serial Programmer Command Control Register(SPCC) and the OCD/Serial Programmer ID Setting Register(OSIS).

The OSIS is configured with the control code (1 byte) and the ID code (15 bytes).

Serial Programmer Connection is basically permitted when the Serial Programmer Enable bit(SPCC.SPE) is set to 1, and prohibited when it is set to 0.

In addition, by configuring the Serial Programmer Command Control settings — specifically the Read Command Protect bit(SPCC.RDPR), Programming Command Protect bit(SPCC.WRPR), and Block Erasure Command Protect bit(SPCC.SEPR) — read, program, and erase operations can be individually permitted or prohibited.

(1) Protection Setting Pattern D1

This pattern disables all protection.

The setting details of protection setting pattern D1 are shown in **Table 1-37** and **Table 1-38**.

Table 1-37 Protection Setting Pattern D1 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
ID Code Protection Enable bit (IDE) (bit: b24)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Block Erasure Command Protect bit (SEPR) (bit: b29)**	**Programming Command Protect bit (WRPR) (bit: b30)**	**Read Command Protect bit (RDPR) (bit: b31)**
1	1	1	1	1

Table 1-38 Protection Setting Pattern D1 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
All FFh

For the setting method, refer to 1.1.1.1.4.3 Protection Setting Examples

The operation of protection setting pattern D1 is outlined in **Table 1-39**.

Table 1-39 Operation of Protection Setting Pattern D1

Operation	**Prevented Items**
If a connection occurs in boot mode, no ID authentication occurs and the device transitions to a state in which reading, programming, and erasing are possible.	None

(2) Protection Setting Pattern D2

This pattern does not perform ID code verification; however, reading, programming, or erasing of the on-chip flash memory can be enabled/disabled individually.

The setting details of protection setting pattern D2 are shown in **Table 1-40** and **Table 1-41**.

Table 1-40 Protection Setting Pattern D2 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
ID Code Protection Enable bit (IDE) (bit: b24)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Block Erasure Command Protect bit (SEPR) (bit: b29)**	**Programming Command Protect bit (WRPR) (bit: b30)**	**Read Command Protect bit (RDPR) (bit: b31)**
1	1	0/1*1,*4	0/1*2,*4	0/1*3,*4

Note 1. When the SEPR bit is set to 1 erasing is enabled, and erasing is disabled when it is cleared to 0.

Note 2. When the WRPR bit is set to 1 programming is enabled, and programming is disabled when it is cleared to 0.

Note 3. When the RDPR bit is set to 1 reading is enabled, and reading is disabled when it is cleared to 0.

Note 4. The following devices require that when the IDE bit is set to 1, the SEPR bit, WRPR bit, and RDPR bit must each be set to 1 as well. Therefore, it is not possible to individually disable read/program/erase operations for the internal flash memory.

- RX26T

Table 1-41 Protection Setting Pattern D2 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.1.1.4.3 Protection Setting Examples

The operation of protection setting pattern D2 is outlined in **Table 1-42**.

Table 1-42 Operation of Protection Setting Pattern D2

Operation	**Prevented Items**
No ID authentication occurs when a connection is made in boot mode. Enables/disables reading, programming, and erasing individually after the connection is established.	Individually disables enables/disables reading, programming, and erasing, without distinction between third parties and developers.

(3) Protection Setting Pattern D3

In this pattern, protection based on ID authentication is performed when a connection is made in boot mode.

The setting details of protection setting pattern D3 are shown in **Table 1-43** and **Table 1-44**.

Table 1-43 Protection Setting Pattern D3 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
ID Code Protection Enable bit (IDE) (bit: b24)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Block Erasure Command Protect bit (SEPR) (bit: b29)**	**Programming Command Protect bit (WRPR) (bit: b30)**	**Read Command Protect bit (RDPR) (bit: b31)**
0	1	0	0	0

Table 1-44 Protection Setting Pattern D3 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Control code / ID code 1: Other than 45h ID code 2 to ID code 16: Any value

For the setting method, refer to 1.1.1.1.4.3 Protection Setting Examples

The operation of protection setting pattern D3 is outlined in **Table 1-45**.

Table 1-45 Operation of Protection Setting Pattern D3

Operation	**Prevented Items**
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(4) Protection Setting Pattern D4

In this pattern, protection based on ID authentication is performed when a connection is made in boot mode. If ID authentication fails three times in succession, the on-chip flash memory is erased completely in boot mode.

The setting details of protection setting pattern D4 are shown in **Table 1-46** and **Table 1-47**.

Table 1-46 Protection Setting Pattern D4 Setting Details 1

Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
Serial Programmer Command Control Register (SPCC) (4 Bytes)				
ID Code Protection Enable bit (IDE) (bit: b24)	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Block Erasure Command Protect bit (SEPR) (bit: b29)**	**Programming Command Protect bit (WRPR) (bit: b30)**	**Read Command Protect bit (RDPR) (bit: b31)**
0	1	0	0	0

Table 1-47 Protection Setting Pattern D4 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Control code / ID code 1: 45h ID code 2 to ID code 16: Any value

For the setting method, refer to 1.1.1.1.4.3 Protection Setting Examples.

The operation of protection setting pattern D4 is outlined in **Table 1-48**.

Table 1-48 Operation of Protection Setting Pattern D4

Operation	**Prevented Items**
Protection is provided by ID authentication when a connection is made in boot mode. If the ID code matches, the device transitions to a state in which reading, programming, and erasing are possible. If the ID code does not match, ID authentication is performed again. If ID authentication fails three times in succession, the on-chip flash memory is erased completely in boot mode.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. If ID authentication fails three times in succession, the on-chip flash memory is erased completely. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(5) Protection Setting Pattern D5

In this pattern, connection to the host is prohibited during boot mode.

The setting details of protection setting pattern D5 are shown in **Table 1-49** and **Table 1-50**. Note that both setting number 1 and setting number 2 prohibit connections to a host in boot mode.

Table 1-49 Protection Setting Pattern D5 Setting Details 1

	Serial Programmer Connection Enable/Disable and Serial Programmer Command Control Settings				
	Serial Programmer Command Control Register (SPCC) (4 Bytes)				
Setting No.	**ID Code Protection Enable bit (IDE) (bit: b24)**	**Serial Programmer Connection Enable bit (SPE) (bit: b27)**	**Block Erasure Command Protect bit (SEPR) (bit: b29)**	**Programming Command Protect bit (WRPR) (bit: b30)**	**Read Command Protect bit (RDPR) (bit: b31)**
1	0	0	0	0	0
2	1	0	Don’t care	Don’t care	Don’t care

Table 1-50 Protection Setting Pattern D5 Setting Details 2

ID Code Protection Settings
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.1.1.4.3 Protection Setting Examples.

The operation of protection setting pattern D5 is outlined in **Table 1-51**.

Table 1-51 Operation of Protection Setting Pattern D5

Operation	**Prevented Items**
Connections to a host are prohibited when connecting in boot mode.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.1.1.4.3 Protection Setting Examples

Each protection function is enabled by setting serial programmer connection enable/disable, serial programmer command control, and an ID code to addresses in the option-setting memory to an address in the on-chip flash memory. Serial programmer connection enable/disable and serial programmer command control should be setting to 0x00120040 and the ID code to 0x00120050.

Also, for instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Protection setting examples are shown in **Figure 1-8** and **Figure 1-9**.

```
/* Setup the Serial programmer command control register */
#pragma address SPCC_REG = 0x00120040
const unsigned long SPCC_REG = 0x1EFFFFFF

/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0x00120050
const unsigned long ID_CODE[4] = {0x04030245, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the Control code / ID code 1 is 45h,
from ID code 2 to ID code 16 are 02h, 03h, 04h, 05h,
06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-8 Protect Setting Pattern D4 Setting Example

```
/* Setup the Serial programmer command control register */
#pragma address SPCC_REG = 0x00120040
const unsigned long SPCC_REG = 0x16FFFFFF

/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0x00120050
const unsigned long ID_CODE[4] = {0x04030201, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the Control code / ID code 1 is 01h,
from ID code 2 to ID code 16 are 02h, 03h, 04h, 05h,
06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-9 Protect Setting Pattern D5 Setting Example

1.1.1.2 Access Window

The Access Window is a protection feature that prevents programming and erasing outside the access window area.
For details on the Access Window, see 2.1.3 Area Protection
Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to C to the end of each function name.

1.1.1.2.1 Access Window A

This device has the Access Window.

Setting the Access Window prevents unintended programming and erasing on areas outside the access window in case a program runs out of control during self-programming.
This function does not prevent accesses from third parties.

1.1.1.2.2 Access Window B

This device has the Access Window and the Access Window Protection.

Executing the Access Window Protect command prevents the Access Window from being reset. Once protected, the protection cannot be removed.
By setting the Access Window and the Access Window Protection at the same time, the area outside the Access Window cannot be programmed or erased again by both developers and third parties.

The Access Window is enabled only during self-programming in the single-chip mode. The user area can be programed or erased in the boot mode because the Access Window is disabled.

1.1.1.2.3 Access Window C

This device has the Access Window and the Access Window Protection.

Setting the FSPR bit prevents the Access Window from being reset. Once protected, the protection cannot be removed.
By setting the Access Window and the FSPR bit at the same time, the area outside the Access Window can never be programmed or erased again by both developers and third parties.

The Access Window is enabled during self-programming in the single-chip mode or serial programming in the boot mode. Exercise extra caution when handling the FSPR bit.

1.1.2 On-Chip Debugger Connection

This section explains the protection functions in the On-Chip Debugger Connection.

1.1.2.1 On-Chip Debugger ID Code Protection

The On-Chip Debugger ID Code Protection is a security feature that, after the MCU starts up in single-chip mode or user boot mode, performs ID authentication when an on-chip debugger is connected, prohibiting connection by third parties and preventing reading, programming, or erasing of the on-chip flash memory.

Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to C to the end of each function name.

This chapter explains these three types separately.

Table 1-52 shows the setting details of each type.

Table 1-52 Types and Setting Details of On-Chip Debugger ID Code Protection

Types	Characteristics
On-Chip Debugger ID Code Protection A	The control code (1 byte) and ID codes 1 to 15 (15 bytes) are set at addresses 0xFFFFFFA0 to 0xFFFFFFAF (16 bytes) on the on-chip flash memory.
On-Chip Debugger ID Code Protection B	Set the ID code in the OSIS register (16 bytes).
On-Chip Debugger ID Code Protection C	Set the OSIS register (16 bytes) and the OCDE bit in the SPCC register.

1.1.2.1.1 On-Chip Debugger ID Code Protection A

This section provides an explanation for devices classified as Type A in the On-Chip Debugger ID Code Protection of **Table 1-3**.

1.1.2.1.1.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.2.1.1.2(1)～1.1.2.1.1.2(3).

- Protection setting pattern A1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern A2
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern A3
  This protection setting pattern prohibits connections by both developers and third parties.

Table 1-53 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase			
		Developer		Third party	
		R	P/E	R	P/E
A1	Disabled	✓	✓	✓	✓
A2	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	—	—
A3	Reading, programming, and erasing are prevented always.	—	—	—	—

R: Read, P/E: Program/Erase
✓: Allowed, —: Not allowed

1.1.2.1.1.2 Description of Protection Setting Patterns

The configuration is applied to the 16-byte area in ROM from address 0xFFFFFFA0 to 0xFFFFFFAF.

The configuration is applied to the control code (1 byte) and the ID code (15 bytes).

The On-Chip Debugger Connection is allowed when the ID code matches and is denied when the ID code does not match.

(1) Protection Setting Pattern A1

This pattern disables all protection.

The setting details of protection setting pattern A1 are shown in **Table 1-54**.

Table 1-54 Protection Setting Pattern A1 Setting Details

On-Chip Debugger ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
FFh	All FFh

For the setting method, refer to 1.1.2.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A1 is outlined in **Table 1-55**.

Table 1-55 Operation of Protection Setting Pattern A1

Operation	Prevented Items
When an on-chip debugger is connected, no ID authentication occurs and the connection with the on-chip debugger is established.	None

(2) Protection Setting Pattern A2

This pattern provides protection by ID code verification.

The setting details of protection setting pattern A2 are shown in **Table 1-56**.

Table 1-56 Protection Setting Pattern A2 Setting Details

On-Chip Debugger ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
Other than the following (1) Control code is FFh and ID code is All FFh (2) Control code is 52h and ID code is 50h,72h,6Fh,74h,65h,63h,74h + any 8 bytes	

For the setting method, refer to 1.1.2.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A2 is outlined in Table 1-57.

Table 1-57 Operation of Protection Setting Pattern A2

Operation	Prevented Items
When a connection is made by an on-chip debugger, ID authentication is performed. If the ID code matches, a connection is established with the on-chip debugger. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(3) Protection Setting Pattern A3

This pattern prevents reading, programming, or erasing of the on-chip flash memory.

Note: After this setting is made and the device is reset, **the protection cannot be removed by any method, so caution is necessary**.

The setting details of protection setting pattern A3 are shown in **Table 1-58**.

Table 1-58 Protection Setting Pattern A3 Setting Details

On-Chip Debugger ID Code Protection Settings	
Control code (1 byte)	**ID code (15 bytes)**
52h	50h,72h,6Fh,74h,65h,63h,74h + any 8 bytes

For the setting method, refer to 1.1.2.1.1.3 Protection Setting Examples.

The operation of protection setting pattern A3 is outlined in **Table 1-59**.

Table 1-59 Operation of Protection Setting Pattern A3

Operation	Prevented Items
ID authentication is performed when an on-chip debugger is connected, but the ID code is always processed as not matching, and ID authentication is performed again.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.2.1.1.3 Protection Setting Examples

Each protection function is enabled by setting a control code and ID code to an address in the on-chip flash memory. The control code and ID code should be set to 0xFFFFFFA0.

Protection setting examples are shown in **Figure 1-10** and **Figure 1-11**.

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE[4] = {0x52010203, 0x04050607, 0x08090A0B, 0x0C0D0E0F};
```

In this example, the control code is 52h, and the ID code is 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

Figure 1-10 Protect Setting Pattern A2 Setting Example

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE[4] = {0x5250726F, 0x74656374, 0xFFFFFFFF, 0xFFFFFFFF};
```

In this example, the control code is 52h, and the ID code is 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh.

Figure 1-11 Protect Setting Pattern A3 Setting Example

1.1.2.1.2 On-Chip Debugger ID Code Protection B

This section provides an explanation for devices classified as Type B in the On-Chip Debugger ID Code Protection of **Table 1-3**.

1.1.2.1.2.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.2.1.2.2(1)～1.1.2.1.2.2(2).

- Protection setting pattern B1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern B2
  This protection setting pattern prevents reading, programming, or erasing by third parties.

Table 1-60 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase			
		Developer		Third party	
		R	P/E	R	P/E
B1	Disabled	✓	✓	✓	✓
B2	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	—	—

R: Read, P/E: Program/Erase
✓: Allowed, —: Not allowed

1.1.2.1.2.2 Description of Protection Setting Patterns

The ID code is set in the OSIS register (16 bytes).

The On-Chip Debugger Connection is allowed when the ID code matches and is denied when the ID code does not match.

(1) Protection Setting Pattern B1

This pattern disables all protection.

The setting detail of protection setting pattern B1 is shown in Table 1-61.

Table 1-61 Protection Setting Pattern B1 Setting Details

On-Chip Debugger ID Code Protection Setting
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
All FFh

For the setting method, refer to 1.1.2.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B1 is outlined in **Table 1-62**.

Table 1-62 Operation of Protection Setting Pattern B1

Operation	**Prevented Items**
If a connection occurs in On-Chip Debugger Connection, the device transitions to a state in which reading, programming, and erasing are possible by transmitting the ID code all set to FFh.	None

(2) Protection Setting Pattern B2

This pattern provides protection by ID code verification.

The setting detail of protection setting pattern B2 is shown in **Table 1-63**.

Table 1-63 Protection Setting Pattern B2 Setting Details

On-Chip Debugger ID Code Protection Setting
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)
Other than (All FFh)

For the setting method, refer to 1.1.2.1.2.3 Protection Setting Examples.

The operation of protection setting pattern B2 is outlined in **Table 1-64**.

Table 1-64 Operation of Protection Setting Pattern B2

Operation	**Prevented Items**
When a connection is made by an on-chip debugger, ID authentication is performed. If the ID code matches, a connection is established with the on-chip debugger. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

1.1.2.1.2.3 Protection Setting Examples

Each protection function is enabled by setting an ID code in the option-setting memory. As the ID code setting addresses differ by device, please refer to the User's Manual: Hardware of the device.

Also, for instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Protection setting examples are shown in **Figure 1-12** and **Figure 1-13**.

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0x00120050
const unsigned long ID_CODE[4] = {0xFFFFFFFF, 0xFFFFFFFF, 0xFFFFFFFF, 0xFFFFFFFF};
```

In this example, the ID code is FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh, FFh.

Figure 1-12 Protect Setting Pattern B1 Setting Example (in the case of devices configured with 0x00120050)

```
/* Setup the ID Code Protection and the ID Code Protection on Connection of the On-Chip Debugger */
#pragma address ID_CODE = 0xFE7F5D50
const unsigned long ID_CODE[4] = {0x04030201, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the ID code is 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-13 Protect Setting Pattern B2 Setting Example (in the case of devices configured with 0xFE7F5D50)

1.1.2.1.3 On-Chip Debugger ID Code Protection C

This section provides an explanation for devices classified as Type C in the On-Chip Debugger ID Code Protection of **Table 1-3**.

1.1.2.1.3.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.2.1.3.2(1)～1.1.2.1.3.2(3).

- Protection setting pattern C1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern C2
  This protection setting pattern prevents reading, programming, or erasing by third parties.
- Protection setting pattern C3
  This protection setting pattern prohibits connections by both developers and third parties. This protection setting pattern prohibits connections by both developers and third parties. Once this protection setting pattern is applied, **the protection cannot be removed, so caution is necessary**.

Table 1-65 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase			
		Developer		Third party	
		R	P/E	R	P/E
C1	Disabled	✓	✓	✓	✓
C2	Reading, programming, and erasing are enabled when the ID code matches.	✓	✓	—	—
C3	Reading, programming, and erasing are prevented always.	—	—	—	—

R: Read, P/E: Program/Erase
✓: Allowed, —: Not allowed

1.1.2.1.3.2 Description of Protection Setting Patterns

The ID code is set in the OSIS register (16 bytes), and the permission to connect to the on-chip debugger is controlled by the OCDE bit in the SPCC register. Setting the OCDE bit to 0 prohibits connection to the on-chip debugger (setting it to 1 permits connection).

(1) Protection Setting Pattern C1

This pattern disables all protection.

The setting details of protection setting pattern C1 are shown in Table 1-66.

Table 1-66 Protection Setting Pattern C1 Setting Details

On-Chip Debugger ID Code Protection Setting	On-chip debugger Connection Enable/Disable Setting
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 bytes)**
All FFh	FFFF FFFFh

For the setting method, refer to 1.1.2.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C1 is outlined in **Table 1-67**.

Table 1-67 Operation of Protection Setting Pattern C1

Operation	Prevented Items
If a connection occurs in On-Chip Debugger Connection, the device transitions to a state in which reading, programming, and erasing are possible by transmitting the ID code all set to FFh.	None

(2) Protection Setting Pattern C2

This pattern provides protection by ID code verification.

The setting details of protection setting pattern C2 are shown in **Table 1-68**.

Table 1-68 Protection Setting Pattern C2 Setting Details

On-Chip Debugger ID Code Protection Setting	On-chip debugger Connection Enable/Disable Setting
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	Serial Programmer Command Control Register (SPCC) (4 bytes)
Other than (All FFh)	FFFF FFFFh

For the setting method, refer to 1.1.2.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C2 is outlined in **Table 1-69**.

Table 1-69 Operation of Protection Setting Pattern C2

Operation	Prevented Items
When a connection is made by an on-chip debugger, ID authentication is performed. If the ID code matches, a connection is established with the on-chip debugger. If the ID code does not match, ID authentication is performed again.	Third parties are prevented from reading, programming, or erasing the on-chip flash memory by means of ID authentication. Developers can read, program, or erase the on-chip flash memory by providing the matching ID code.

(3) Protection Setting Pattern C3

This pattern prevents reading, programming, or erasing of the on-chip flash memory.

Note: After this setting is made and the device is reset, **the protection cannot be removed by any method, so caution is necessary**.

The setting details of protection setting pattern C3 are shown in **Table 1-70**.

Table 1-70 Protection Setting Pattern C3 Setting Details

On-Chip Debugger ID Code Protection Settings	On-chip debugger Connection Enable/Disable Setting
OCD/Serial Programmer ID Setting Register (OSIS) (16 bytes)	**Serial Programmer Command Control Register (SPCC) (4 bytes)**
All FFh	FFFD FFFFh(SPCC.OCDE is set to 0 only)

For the setting method, refer to 1.1.2.1.3.3 Protection Setting Examples.

The operation of protection setting pattern C3 is outlined in **Table 1-71**.

Table 1-71 Operation of Protection Setting Pattern C3

Operation	Prevented Items
The connection to the on-chip debugger is prohibited.	Connections are prohibited, preventing both third parties and developers, without distinction, from reading, programming, and erasing.

1.1.2.1.3.3 Protection Setting Examples

The option-setting memory is enabled by configuring the OCDE bit in the SPCC register to On-chip debugger Connection Enable/Disable, and by setting the control code and ID code in the OSIS register.

As the setting addresses differ by device, please refer the User's Manual: Hardware of the device.

Also, for instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Protection setting examples are shown in **Figure 1-14** and **Figure 1-15**.

```
/* Setup the Serial programmer command control Register */
#pragma address SPCC_REG = 0xFE7F5D40
const unsigned long SPCC_REG = 0xFFFFFFFF;

/* Setup the OCD/Serial Programmer ID Setting Register */
#pragma address OSIS_REG = 0xFE7F5D50
const unsigned long OSIS_REG[4] = {0x04030245, 0x08070605, 0x0C0B0A09, 0x100F0E0D};
```

In this example, the Control code / ID code 1 is 45h, from ID code 2 to ID code 16 are 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h.

Figure 1-14 Protect Setting Pattern C2 Stting Example (for RX671)

```
/* Setup the Serial programmer command control Register */
#pragma address SPCC_REG = 0x00120040
const unsigned long SPCC_REG = 0xFFFDFFFF;

/* Setup the OCD/Serial Programmer ID Setting Register */
#pragma address OSIS_REG = 0x00120050
const unsigned long OSIS_REG[4] = {0xFFFFFFFF, 0xFFFFFFFF, 0xFFFFFFFF, 0xFFFFFFFF};
```

In this example, the Control code / ID code 1, from ID code 2 to ID code 16 are all FFh.

Figure 1-15 Protect Setting Pattern C3 Setting Example (for RX26T or RX660)

1.1.2.2 Access Window

Refer to 1.1.1.2 Access Window.

1.1.3 Parallel Programmer Connection

This section explains the protection functions in the Parallel Programmer Connection.

1.1.3.1 ROM Code Protection

The ROM Code Protection is a protection feature that prevents reading, programming, and erasing of the on-chip flash memory when using a Parallel Programmer.

1.1.3.1.1 Selecting Protection Settings

Choose the most suitable protection setting pattern from the following according to the protection purpose.

For details on each protection setting pattern, refer to 1.1.3.1.2 Description of Each Protection Setting..

- Protection setting pattern 1
  All protection against access by developers and third parties is disabled.
- Protection setting pattern 2
  This protection prevents reading operations regardless of whether they are performed by a developer or a third party.
- Protection setting pattern 3
  This protection prevents reading, programming, and erasing operations regardless of whether they are performed by a developer or a third party.

Table 1-72 Comparison of Protection Setting Patterns

Protection Setting Pattern	Functional Description	Read/Program/Erase			
		Developer		Third party	
		R	P/E	R	P/E
1	Disabled	✓	✓	✓	✓
2	Reading are prevented always.	—	✓	—	✓
3	Reading, programming, and erasing are prevented always.	—	—	—	—

R: Read, P/E: Program/Erase
✓: Allowed, —: Not allowed

1.1.3.1.2 Description of Each Protection Setting

Settings and Operation for ROM Code Protection are shown in **Table 1-73**.

Table 1-73 Settings and Operation for ROM Code Protection

Protection Setting Pattern	Settings of ROM Code Protection	Operation
1	Other than (0000 0000h, 0000 0001h)	Reading, programming, and erasing are prevented.
2	0000 0001h	Reading is prevented.
3	0000 0000h	Reading, programming, and erasing are prevented.

For the setting method, refer to 1.1.3.1.3 Protection Setting Examples.

The location for setting ROM Code Protection varies depending on the device; some devices use the address FFFFFF9C, while others use the ROM Code Protection Register (ROMCODE).

The correspondence between devices and their setting locations is shown Table 1-74.

Table 1-74 Setting Location for ROM Code Protection

Devices	Setting Location
RX210, RX230, RX231, RX24T, RX24U, RX610, RX621, RX62G, RX62N, RX62T, RX630, RX631, RX634, RX63N, RX63T, RX64M, RX71M	FFFF FF9Ch
Devices that include ROM Code Protection other than those listed above	ROM Code Protection Register*(ROMCODE)

Note * ROM Code Protection Register:

The addresses differ depending on the device. Refer to the User's Manual: Hardware of the device.

1.1.3.1.3 Protection Setting Examples

Protection setting examples are shown in **Figure 1-16** and **Figure 1-17**.

```
/* Setup the ROM Code Protection */
#pragma address ROM_CODE = 0x0012007C
const unsigned long ROM_CODE = 0x00000001;
```

Figure 1-16 Protect Setting Pattern 2 Stting Example(for RX660 and others)

```
/* Setup the ROM Code Protection */
#pragma address ROM_CODE = 0xFFFFFF9C
const unsigned long ROM_CODE = 0x00000000;
```

Figure 1-17 Protect Setting Pattern 3 Stting Example(for RX230 and others)

1.2 Other Protection Function

1.2.1 Trusted Memory

Reading of the trusted memory area in the on-chip flash memory is prevented.

For instructions on using the trusted memory function, refer to the application note “RX Family: Using the Trusted Memory Function” (R01AN2618).

2. Protection during Self-Programming Initiated by Developers

2.1 Device Protection Features

Table 2-1 shows the device classification. For details of each protection function, refer to the User's Manual: Hardware of the device.

Table 2-1 List of Device Protection Functions

Device	Protection Function((✓: Supported, —: Not Supported , A to D: Correspondence (Classification symbols within the function)*)									
	Lock Bits	Area Protection	FENTRYR Register	FLWE bit	RPDIS bit	DBWE bit	DBRE bit	DFLEN bit	Start-Up Program Protection	Dual Bank Function
● RX110	—	A	A	—	✓	—	—	—	A	—
● RX111	—	A	A	—	✓	—	—	✓	A	—
● RX113	—	A	A	—	✓	—	—	✓	A	—
● RX130	—	A	A	—	✓	—	—	✓	A	—
● RX13T	—	A	A	—	✓	—	—	✓	A	—
● RX140	—	B	B	—	✓	—	—	✓	A	—
● RX14T	—	B	B	—	✓	—	—	✓	A	—
● RX210	A	—	C	✓	—	✓	✓	—	—	—
● RX21A	A	—	C	✓	—	✓	✓	—	—	—
● RX220	A	—	C	✓	—	✓	✓	—	—	—
● RX230	—	B	A	—	✓	—	—	✓	A	—
● RX231	—	B	A	—	✓	—	—	✓	A	—
● RX23T	—	B	A	—	✓	—	—	—	A	—
● RX23E-A	—	B	A	—	✓	—	—	✓	A	—
● RX23E-B	—	B	A	—	✓	—	—	✓	A	—
● RX23W	—	B	A	—	✓	—	—	✓	A	—
● RX24T	—	B	A	—	✓	—	—	✓	A	—
● RX24U	—	B	A	—	✓	—	—	✓	A	—
● RX260	—	B	B	—	✓	—	—	✓	A	—
● RX261	—	B	B	—	✓	—	—	✓	A	—
● RX26T	—	C	D	✓	—	—	—	—	B	✓
● RX610	A	—	C	✓	—	✓	✓	—	—	—
● RX621	A	—	C	✓	—	✓	✓	—	—	—
● RX62N	A	—	C	✓	—	✓	✓	—	—	—
● RX62T	A	—	C	✓	—	✓	✓	—	—	—
● RX62G	A	—	C	✓	—	✓	✓	—	—	—
● RX630	A	—	C	✓	—	✓	✓	—	—	—
● RX631	A	—	C	✓	—	✓	✓	—	—	—
● RX634	A	—	C	✓	—	✓	✓	—	—	—
● RX63N	A	—	C	✓	—	✓	✓	—	—	—
● RX63T	A	—	C	✓	—	✓	✓	—	—	—
● RX64M	B	—	D	✓	—	—	—	—	—	—
● RX651	—	C	D	✓	—	—	—	—	B	✓
● RX65N	—	C	D	✓	—	—	—	—	B	✓
● RX65W	—	C	D	✓	—	—	—	—	B	✓
● RX660	B	—	D	✓	—	—	—	—	—	—
● RX66N	—	C	D	✓	—	—	—	—	B	✓
● RX66T	B	—	D	✓	—	—	—	—	—	—
● RX671	–	C	D	✓	—	—	—	—	B	✓
● RX71M	B	—	D	✓	—	—	—	—	—	—
● RX72N	—	C	D	✓	—	—	—	—	B	✓
● RX72M	—	C	D	✓	—	—	—	—	B	✓
● RX72T	B	—	D	✓	—	—	—	—	—	—

Note: * A-D : Each protection function are referred to by the same name in the User's Manual: Hardware of the device for all RX groups. Since each RX group includes functional enhancements or improvements, this application note classifies the functions into types by appending the letters A through D to the end of the function names for identification purposes.

2.1.1 Protection during Self-Programming

Eight protection functions are provided for protection during self-programming: the lock bits, area protection, FENTRYR register, FLWE bit, RPDIS bit, DBWE bit, DBRE bit and DFLEN bit.

An overview of these protection functions is shown in **Table 2-2**.

Table 2-3 indicates the areas to which the protection can be configured. Configure the area for which rewriting is to be prohibited during self-programming.

Table 2-2 Overview of Protection Functions

Protection Type	Purpose	Overview of Function
Lock Bits	Prohibits programming/erasure of the user area in block units.	Each block in the user area includes a lock bit. If you enable lock bit protection, programming/erasure of the block whose lock bit is set to "0".
Area Protection	Prohibits programming/erasure of the selected blocks in the user area.	Rewriting of the user area other than the selected blocks (access window) is prohibited during self-programming.
FENTRYR Register	Prohibits programming/erasure of the user area and data area by setting the flash memory to read mode.	When the FENTRYR register is set to "0000h", the flash memory is in read mode. In read mode, programming/erasure of the flash memory is prohibited.
FLWE bit	Prohibits programming/erasure of an area where the P/E mode is set by the FENTRYR register.	If you set the FLWE bit, programming/erasure of the flash memory and lock bits, reading of the lock bits, and blank check are prohibited.
RPDIS bit	Prohibits programming/erasure of the user area.	If you set the RPDIS bit, programming/erasure of the user area is prohibited.
DBWE bit	Prohibits programming/erasure of the data area in units of multiple blocks.	If you set the DBWE bit, programming/erasure of the specified data area blocks are prohibited.
DBRE bit	Prohibits reading of the data area in units of multiple blocks.	If you set the DBRE bit, reading of the specified data area blocks are prohibited. Programming/erasure cannot be prohibited.
DFLEN bit	Prohibits access to the data area.	If you set the DFLEN bit, access to the data area (i.e. reading/programming/erasure) is prohibited, and access to the extra area in P/E mode (i.e. start-up area information program, access window protection*3, and access window information program) is prohibited.

.

Table 2-3 Area to Which Protection Can be Configured

Protection Function	Flash Memory Reading/Programming/Erasure Prohibition			
	User Area		Data Area	
	Reading	Programming/Erasure	Reading	Programming/Erasure
Lock Bits	—	✓	—	—
Area Protection	—	✓	—	—
FENTRYR Register	—	✓	—	✓
FLWE bit	—	✓	—	✓
RPDIS bit	—	✓	—	—
DBWE bit	—	—	—	✓
DBRE bit	—	—	✓	—
DFLEN bit	—	—	✓	✓

✓: Can be configured, —: Cannot be configured

2.1.2 Lock Bits

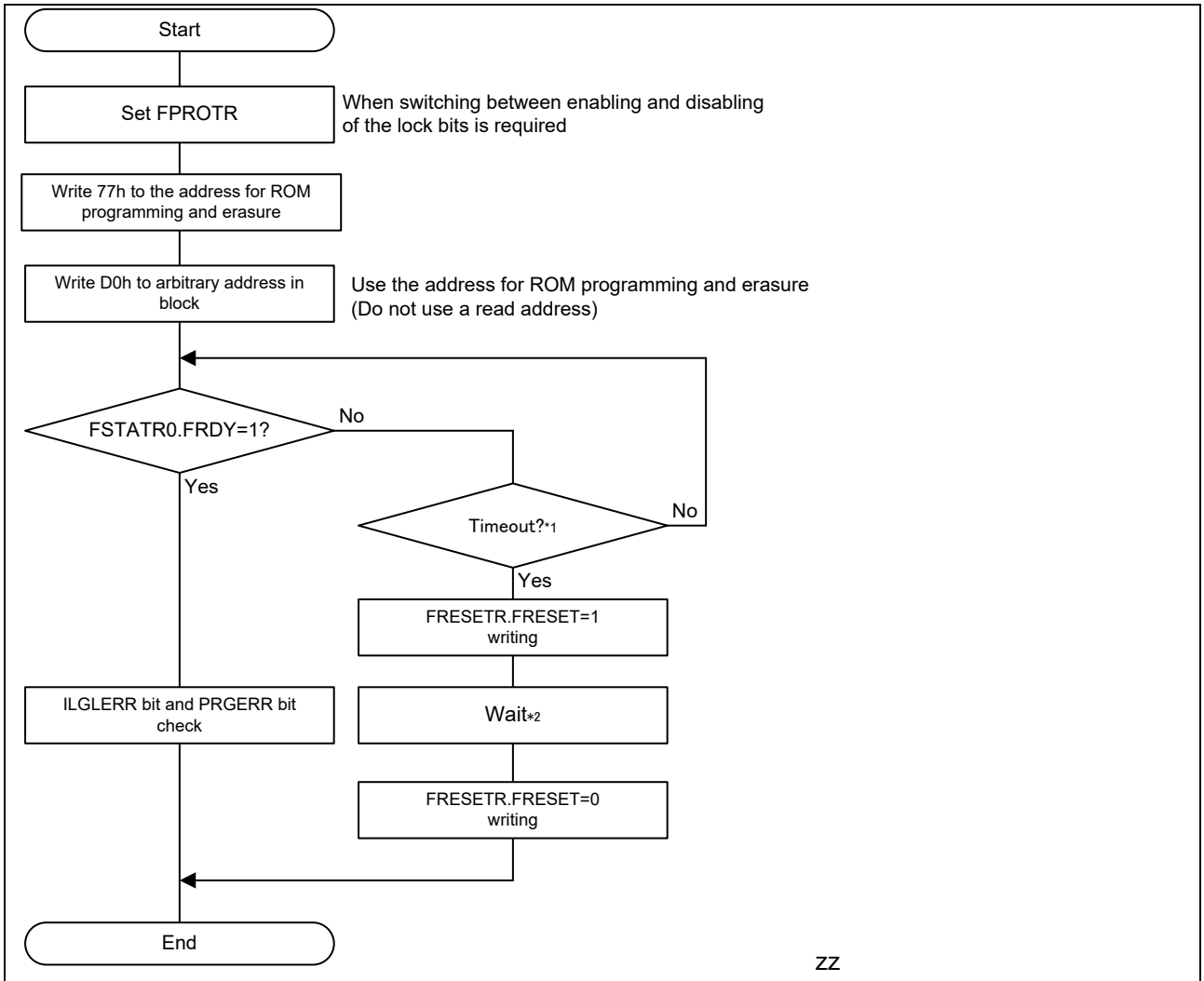
You can prohibit programming/erasure of the user area in block units.

Each block in the user area includes a lock bit. If the FPROTCN bit of the FPROTR register is set to “0”, programming/erasure of the block whose lock bit is set to “0” is prohibited. The lock bit is set by using the lock bit programming command.

Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to B to the end of each function name.

2.1.2.1 Lock Bits A

Figure 2-1 shows the flow for issuing the lock bit programming command.



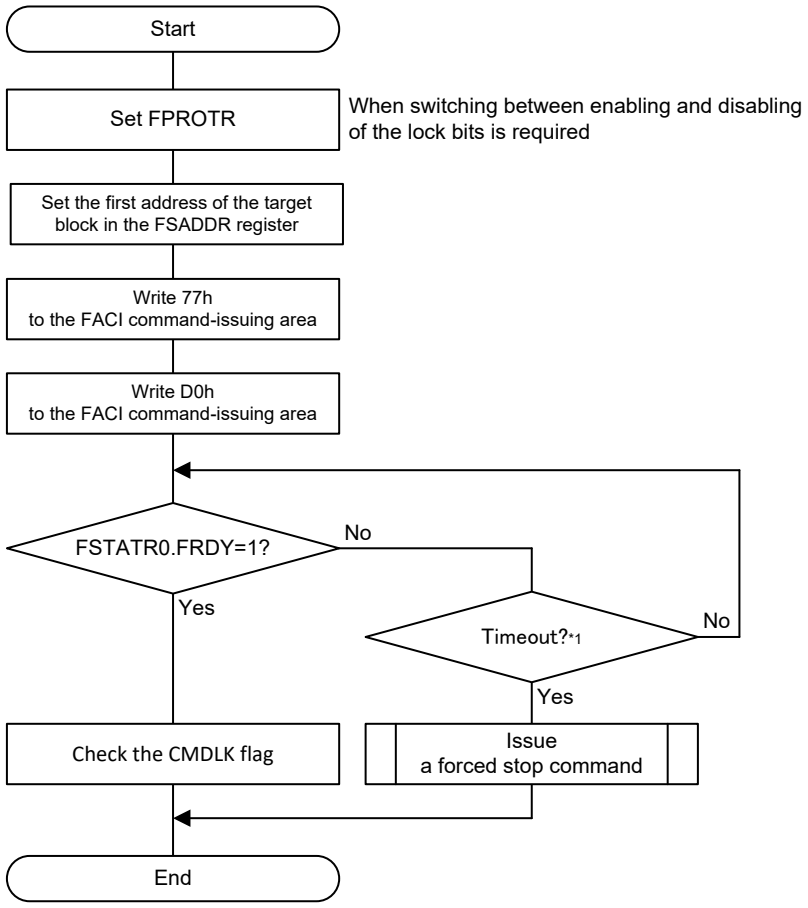
Note 1. For the timeout time (time required for programming data), refer to the “Electrical Characteristics” of your device.

Note 2. For the wait time (reset pulse width during programming/erasure), refer to the “Electrical Characteristics” of your device.

Figure 2-1 Flow for Issuing the Lock Bit Programming Command

2.1.2.2 Lock Bits B

Figure 2-2 shows the flow for issuing the lock bit programming command.



Note 1. Judgment is based on 25ms (when 20MHz ≤ FCLK ≤ 60MHz) or 50ms (when FCLK = 4MHz).

Figure 2-2 Flow for Issuing the Lock Bit Programming Command

2.1.3 Area Protection

You can prohibit programming/erasure of the selected blocks in the user area.

Rewriting of the user area other than the selected blocks (access window) is prohibited during self-programming.

Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to C to the end of each function name.

2.1.3.1 Area Protection A

The settings are configured using the Access Window Information Programming command.

Table 2-4 shows the settings of the access window.

Table 2-4 Access window settings

Register Name	**Flash write buffer register H (FWBH)**	**Flash write buffer register L (FWBL)**
Setting Value	From b19 to b10 of the access window start address	From b19 to b10 of the address that follows the access window end address

For how to issue the access window information program command, refer to 2.2.4 .

2.1.3.2 Area Protection B

The settings are configured using the Access Window Information Programming command.

Table2-5 shows the settings of the access window.

Table2-5 Access window settings

Register Name	**Flash write buffer 0 register (FWB0)**）	**Flash write buffer 1 register (FWB1)**
Setting Value	From b21 to b11 of the access window start address	From b21 to b11 of the address that follows the access window end address

For how to issue the access window information program command, refer to 2.2.4 .

2.1.3.3 Area Protection C

The settings are configured using the FAW register.

If the FSPR bit is set, the access window never be set again. Once the FSPR bit set to “0”, this bit cannot be restored to “1”. Exercise extra caution when handling the FSPR bit.

For details of FAW Register, refer to the User’s Manual: Hardware of the device.

Table 2-6 shows the access window settings.

Table 2-6 FAW Register Setting

Register Name	**Flash access window setting register (FAW)**			
Bit Name	**Flash access window start address bit (FAWS)**	**Access Window protection bit (FSPR)**	**Flash access window end address bit (FAWE)**	**Start-up area select bit (BTFLG)**
Setting Value	The access window start address	“0” when protection is enabled	The address that follows the access window end address	Don’t care

For how to set the FAW register, refer to 2.2.5, Option-Setting Memory Setting Example

2.1.4 FENTRYR Register

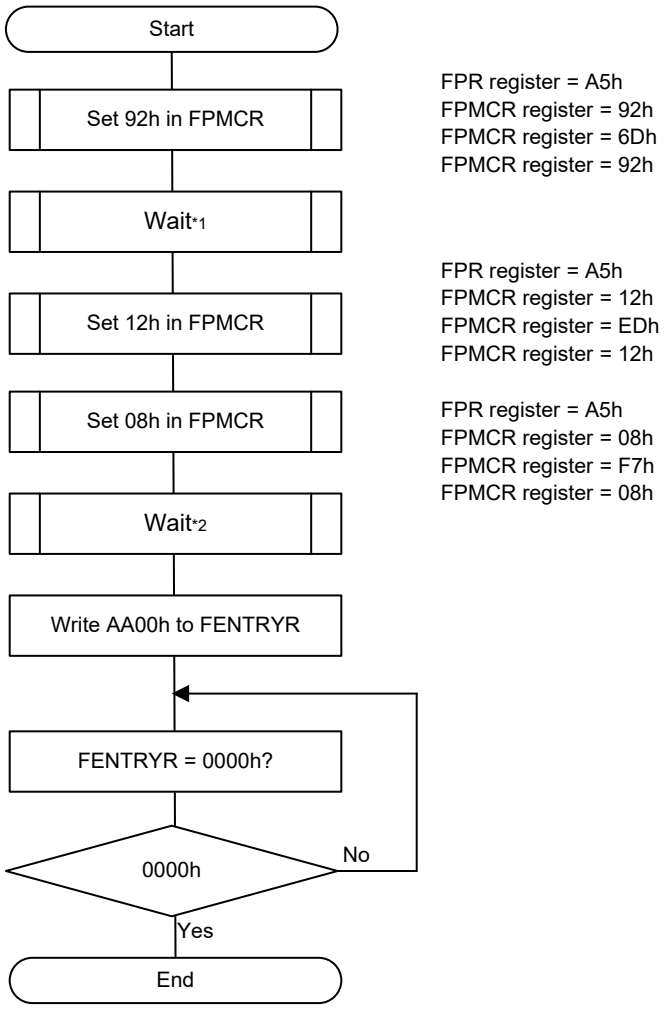
You can prohibit programming/erasure of the user area and data area by setting the flash memory to read mode.

When the FENTRYR register is set to “0000h”, the flash memory is in read mode. In read mode, programming/erasure of the flash memory is prohibited.

Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A to D to the end of each function name.

2.1.4.1 FENTRYR Register A

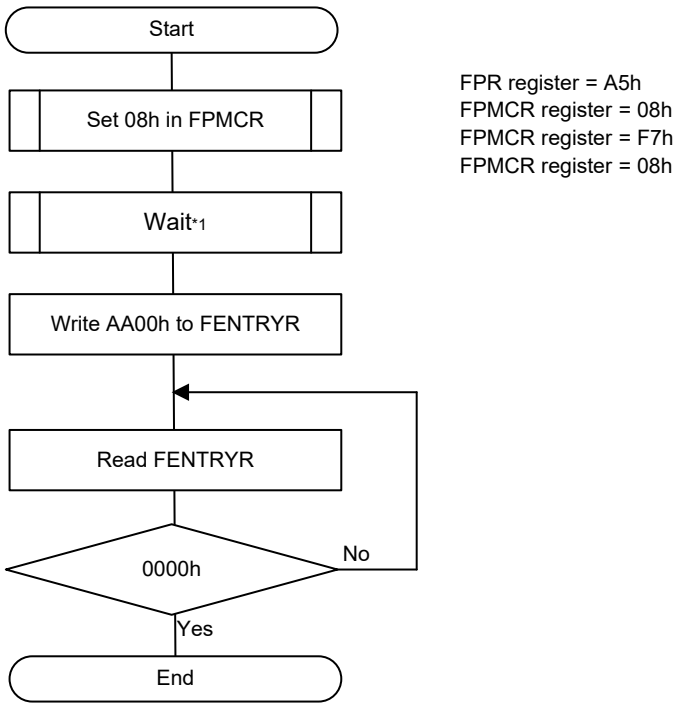
Figure 2-3 and Figure 2-4 show the transition flow to read mode.



Note 1. For the wait time (ROM mode transition wait time 1), refer to the “Electrical Characteristics” of your device.

Note 2. For the wait time (ROM mode transition wait time 2), refer to the “Electrical Characteristics” of your device.

Figure 2-3 Flow for Transition from ROM P/E Mode to Read Mode

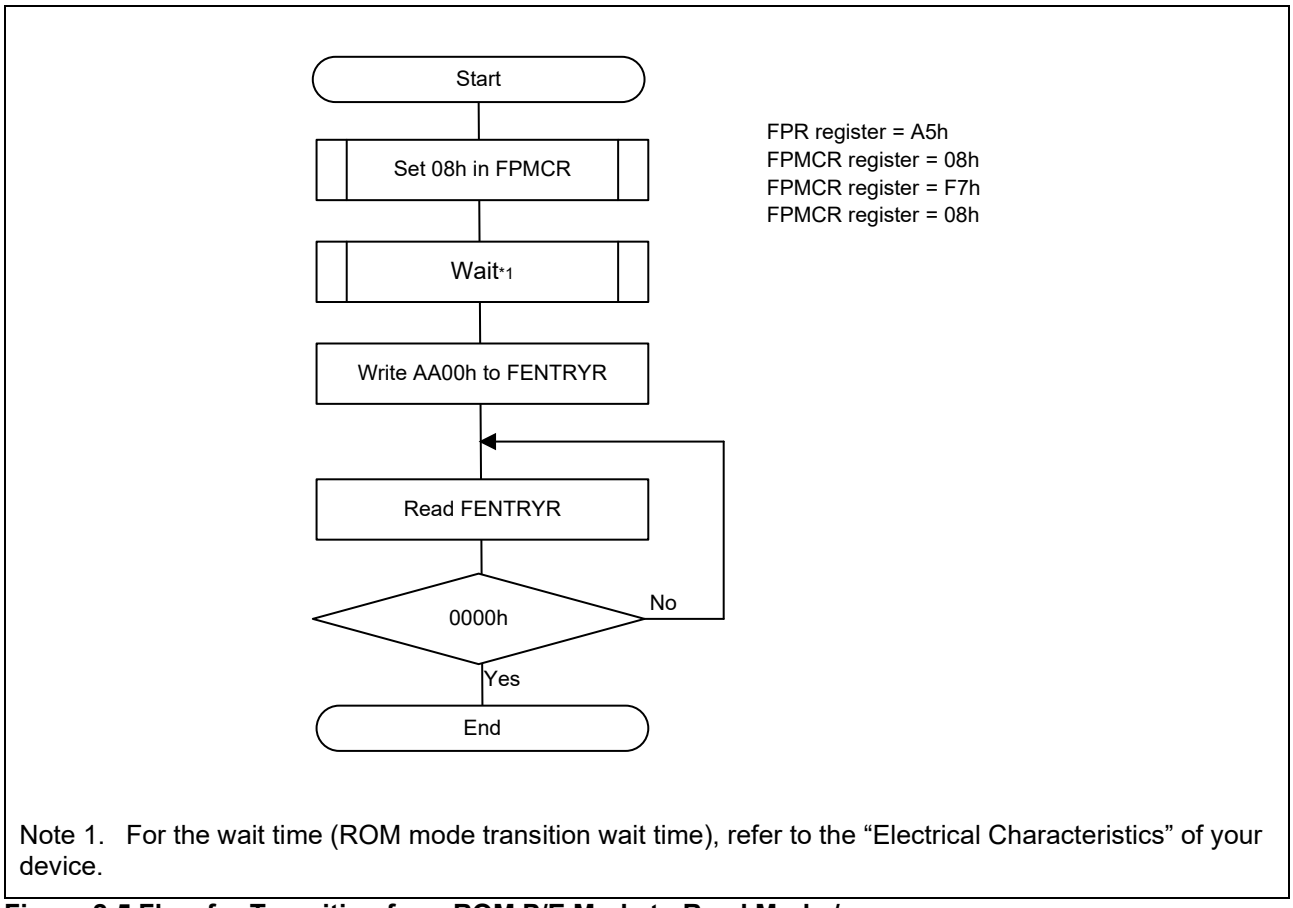


Note 1. For the wait time (ROM mode transition wait time 2), refer to the “Electrical Characteristics” of your device.

Figure 2-4 Flow for Transition from E2 DataFlash P/E Mode to Read Mode

2.1.4.2 FENTRYR Register B

Figure 2-5 show the transition flow to read mode.



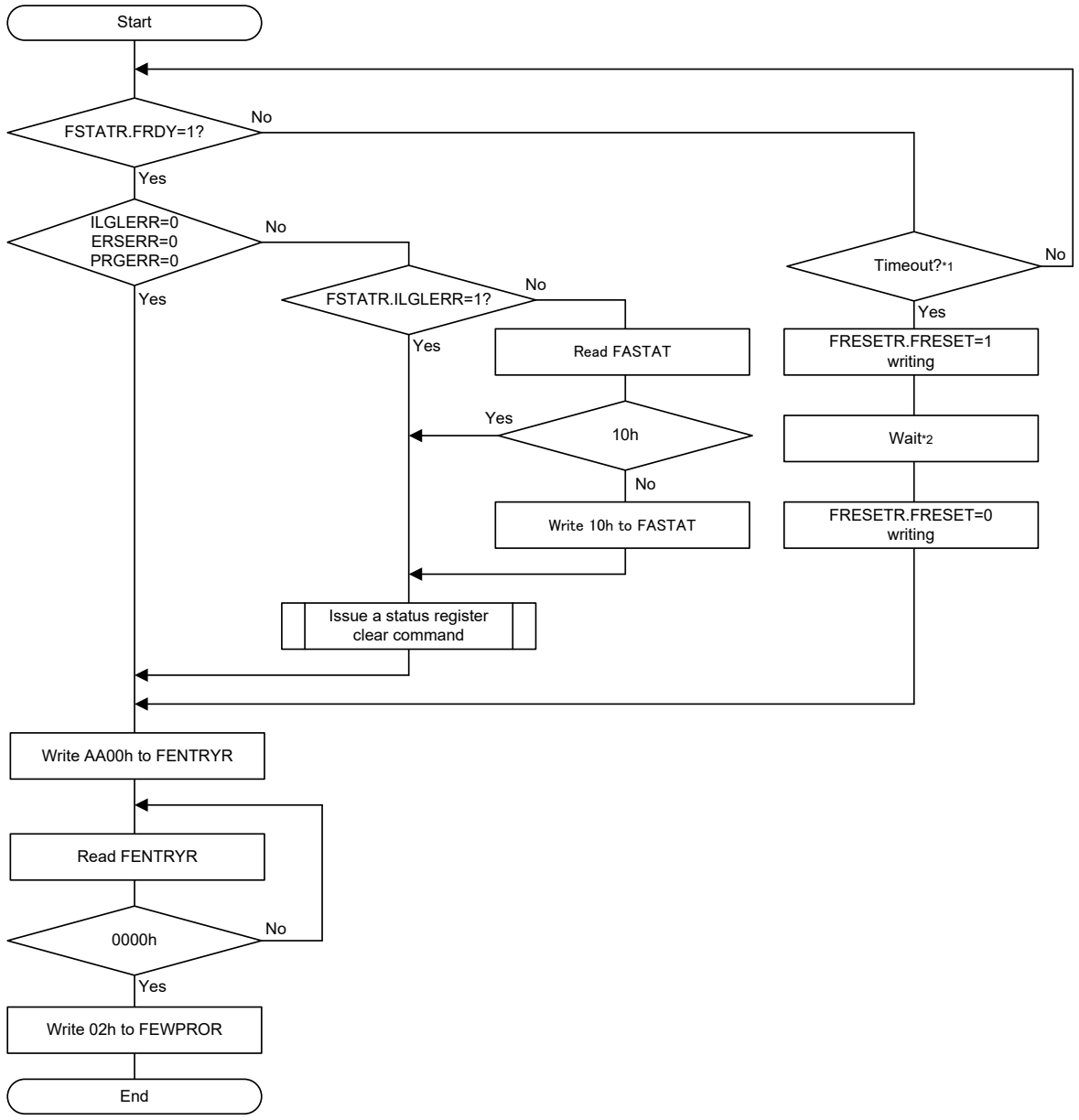
Note 1. For the wait time (ROM mode transition wait time), refer to the “Electrical Characteristics” of your device.

Figure 2-5 Flow for Transition from ROM P/E Mode to Read Mode /

Flow for Transition from E2 DataFlash P/E Mode to Read Mode

2.1.4.3 FENTRYR Register C

Figure 2-6 shows the transition flow to read mode.

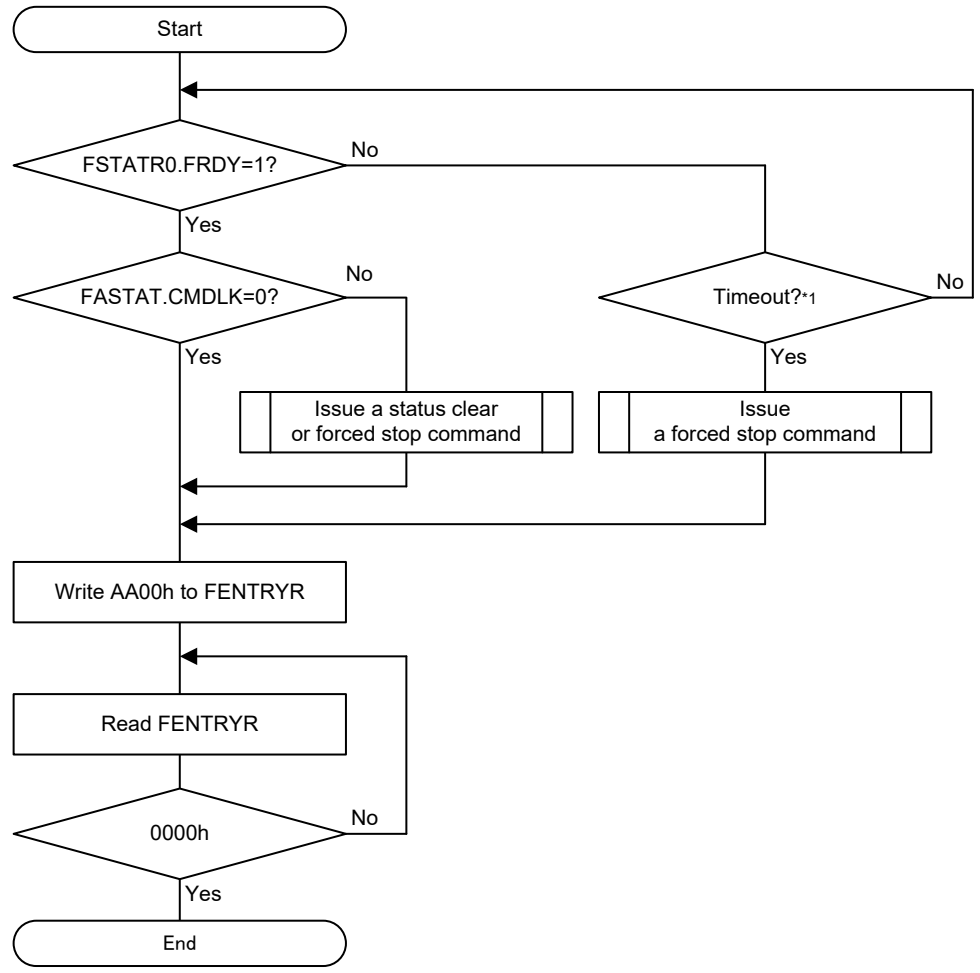


Note 1. For the timeout time (data erasure time), refer to the “Electrical Characteristics” of your device.
Note 2. For the wait time (reset pulse width during programming/erasure), refer to the “Electrical Characteristics” of your device.

Figure 2-6 Flow for Transition to Read Mode

2.1.4.4 FENTRYR Register C

Figure 2-7 shows the transition flow to read mode.



Note 1. For the timeout time (the maximum time for processing of the FACI command that is in progress), refer to the “Electrical Characteristics” of your device.)

Figure 2-7 Flow for Transition to Read Mode

2.1.5 FLWE bit

You can prohibit programming/erasure of an area where the P/E mode is set by the FENTRYR register.

If you set the FLWE bit of the FWEPROR register, programming/erasure of the flash memory and lock bits, reading of the lock bits, and blank check are prohibited by software.

Table 2-7 shows the setting of the FWEPROR register.

Table 2-7 FWEPROR Register Setting

Register Name	**Flash P/E protect register (FWEPROR)*1**
Bit Name	**Flash P/E bit (FLWE) (Bit: b0-b1)**
Setting Value	00h, 10h (default value), or 11h

Note 1. The FWEPROR register is called with a different name in RX210, RX21A, RX220, RX610, RX621, RX62G, RX62N, and RX62T.

2.1.6 RPDIS bit

You can prohibit programming/erasure of the user area.

If you set the RPDIS bit of the FPMCR register, programming/erasure of the user area is prohibited.

Table 2-8 shows the setting of the FPMCR register.

Table 2-8 FPMCR Register Setting

Register Name	**Flash P/E mode control register (FPMCR)**
Bit Name	**ROM P/E disable bit (RPDIS) (Bit: b3)**
Setting Value	1

2.1.7 DBWE bit

You can prohibit programming/erasure of the data area in units of multiple blocks.

If you set the DBWE bit of the DFLWE register, programming/erasure of the respective data area blocks is prohibited.

Table 2-9 shows the setting of the DFLWE register.

Table 2-9 DFLWE Register Setting

Register Name	**E2 DataFlash P/E enable register (DFLWE)*1**	
Bit Name	**Block P/E enable bit (DBWEj) (j = Varies by device) (Bit: b0-b7)**	**Key code (KEY) (Bit: b8-b15)**
Setting Value	Set the enable bit corresponding to the block for which programming/erasure is to be prohibited to “0”.	To modify the DFLWE0 register, write 1Eh To modify the DFLWE1 register, write E1h

Note 1. The DFLWE register is called with a different name in RX210, RX21A, RX220, RX610, RX621, RX62G, RX62N, and RX62T.

2.1.8 DBRE bit

If you set the DBRE bit, reading of the specified data area blocks are prohibited. Programming/erasure cannot be prohibited.

For setting details, refer to the User's Manual: Hardware of the device.

Figure 2-10 shows the setting of the DFLRE register.

Table 2-10 DFLRE Register Setting

Register Name	**E2 DataFlash Read Enable Register (DFLRE)*1**	
Bit Name	**Block read enable bit (DBREj)** **(j = Varies by device)** **(Bit: b0-b7)**	**Key code (KEY)** **(Bit: b8-b15)**）
Setting Value	Set the enable bit corresponding to the block for which read is to be prohibited to "0".	To modify the DFLRE 0 register, write 2Dh To modify the DFLRE 1 register, write D2h

Note 1. The DFLRE register is called with a different name in RX210, RX21A, RX220, RX610, RX621, RX62G, RX62N, and RX62T.

2.1.9 DFLEN bit

If you set the DFLEN bit of the DFLCTL register, access to the data area (i.e. reading/programming/erasure) is prohibited, and access to the extra area in P/E mode (i.e. start-up area information program, access window protection, and access window information program) is prohibited.

Table 2-11 shows the setting of the DFLCTL register.

Table 2-11 Register Setting

Register Name	**E2 DataFlash control register (DFLCTL)**
Bit Name	**E2 DataFlash access enable bit (DFLEN)** **(Bit: b0)**
Setting Value	0

2.2.1 Protection during Update

Two protection functions are provided for protection during update: the start-up program protection and dual bank function.

An overview of these protection functions is shown in **Table 2-12**.

Table 2-12 Overview of Protection Functions

Protection Type	Overview of Function
Start-Up Program Protection	When you update the start-up program, this function allows you to update to a new program without erasing the current start-up program. If the update operation is disrupted for any reason including a reset, the program is still safely updated.
Dual Bank Function	You can use the bank mode switching function and selecting the startup bank to update a program in another bank while user programs continue to run. If the update operation is disrupted for any reason including a reset, the program is still safely updated.

For a sample program for the start-up program protection, refer to “RX100/RX200 Series Updating Firmware Using Start-Up Program Protection and Serial Communication (R01AN3740)”.

For a sample program for the dual bank function, refer to “RX Family Firmware Update Module Using Firmware Integration Technology (R01AN5824)”.

2.2.2 Start-up Program Protection

When you update the start-up program, this function allows you to update to a new program without erasing the current start-up program. If the update operation is disrupted for any reason including a reset, the program is still safely updated.

Since each device has functional enhancements or improvements, resulting in differences in details, this application note categorizes them for convenience by appending letters A or B to the end of each function name.

2.2.2.1 Start-Up Program Protection A

When updating the start-up program, the default area (where the current start-up program is stored) is swapped with the alternate area (where the new start-up program is stored) so that the start-up program can be updated without erasing the current start-up program. If the update operation is disrupted for any reason including a reset, the program is still safely updated. The start-up area is swapped by using the start-up area information program command.

Figure 2-8 gives an overview of the start-up program protection.

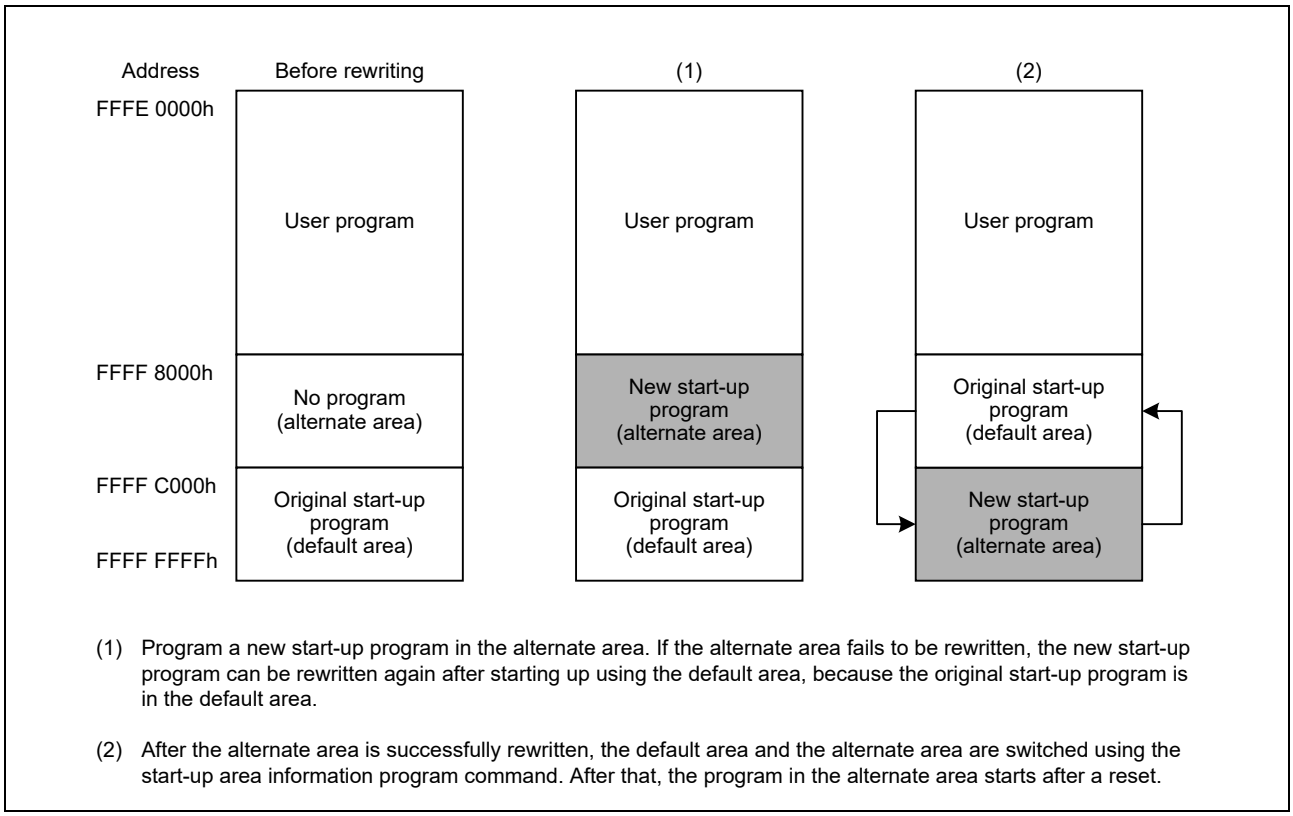


Figure 2-8 Overview of the Start-Up Program Protection (for RX140)

For how to issue the start-up area program command, refer to 2.2.4 How to Issue the Start-Up Area Information Program Command / Access Window Information Program Command.

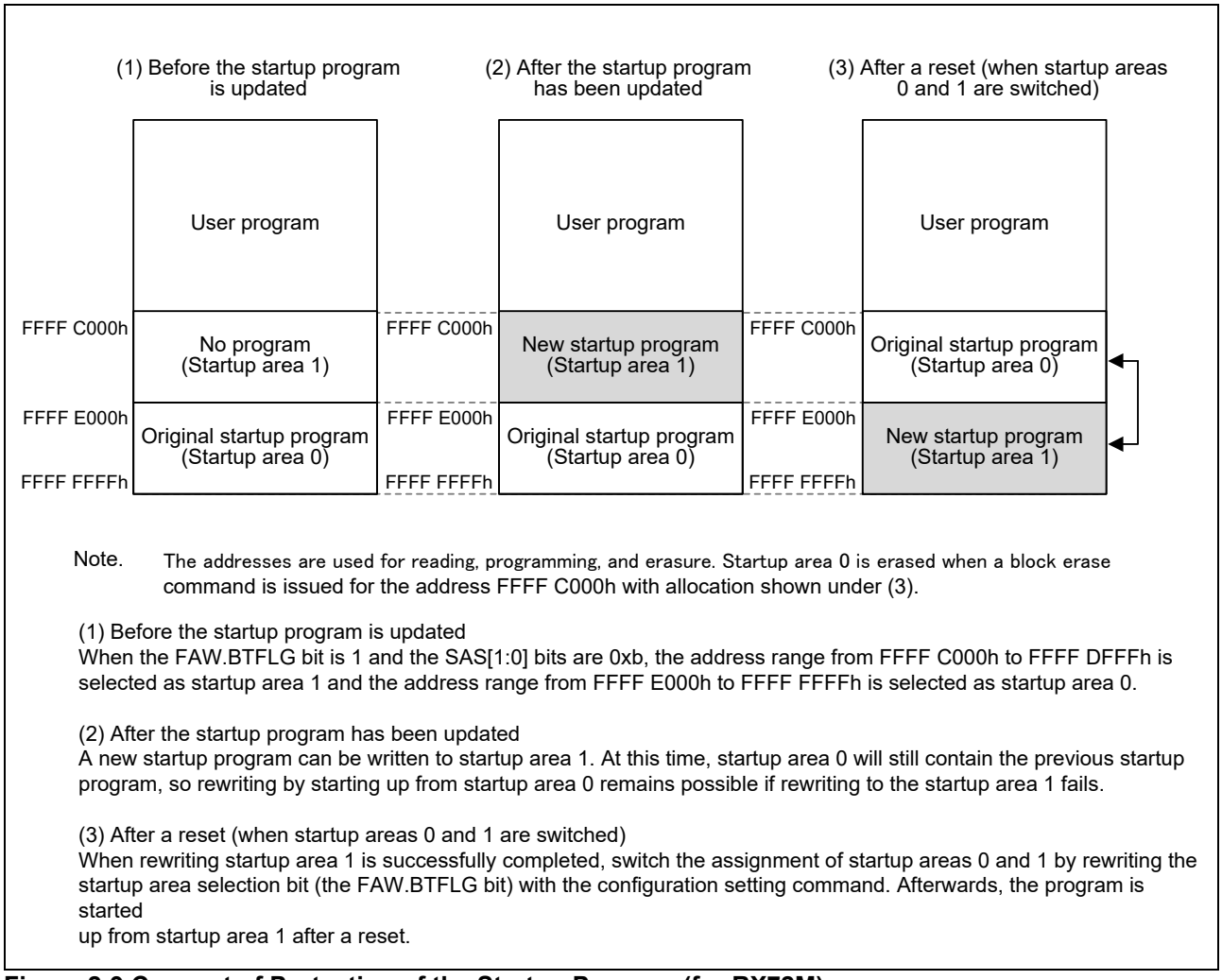
2.2.2.2 Start-Up Program Protection B

When updating the start-up program, an area (where the current start-up program is stored) is swapped with another area (where the new start-up program is stored) so that the start-up program can be updated without erasing the current start-up program. If the update operation is disrupted for any reason including a reset, the program is still safely updated.

The FSPR bit of the FAW register can be used to fix the start-up area selection status. Once the FSPR bit set to “0”, this bit cannot be restored to “1”. Exercise extra caution when handling the FSPR bit.

Note that the start-up program protection cannot be used when dual mode is selected by the bank mode switching function of the dual bank function.

Figure 2-9 gives an overview of the start-up program protection. Figure 2-10 shows the flow for swapping the start-up area.



Note. The addresses are used for reading, programming, and erasure. Startup area 0 is erased when a block erase command is issued for the address FFFF C000h with allocation shown under (3).

(1) Before the startup program is updated
When the FAW.BTFLG bit is 1 and the SAS[1:0] bits are 0xb, the address range from FFFF C000h to FFFF DFFFh is selected as startup area 1 and the address range from FFFF E000h to FFFF FFFFh is selected as startup area 0.

(2) After the startup program has been updated
A new startup program can be written to startup area 1. At this time, startup area 0 will still contain the previous startup program, so rewriting by starting up from startup area 0 remains possible if rewriting to the startup area 1 fails.

(3) After a reset (when startup areas 0 and 1 are switched)
When rewriting startup area 1 is successfully completed, switch the assignment of startup areas 0 and 1 by rewriting the startup area selection bit (the FAW.BTFLG bit) with the configuration setting command. Afterwards, the program is started
up from startup area 1 after a reset.

Figure 2-9 Concept of Protection of the Startup Program (for RX72M)

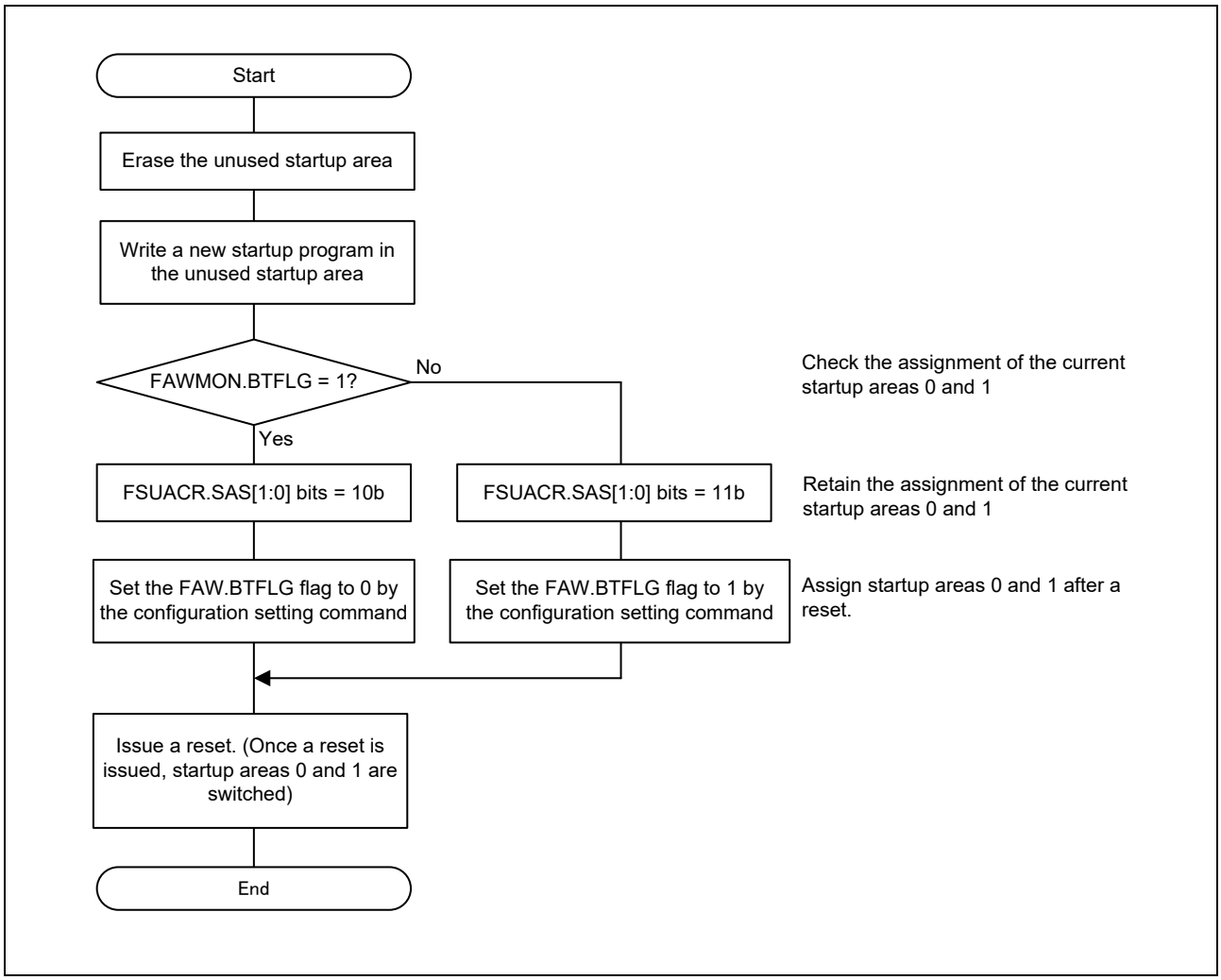


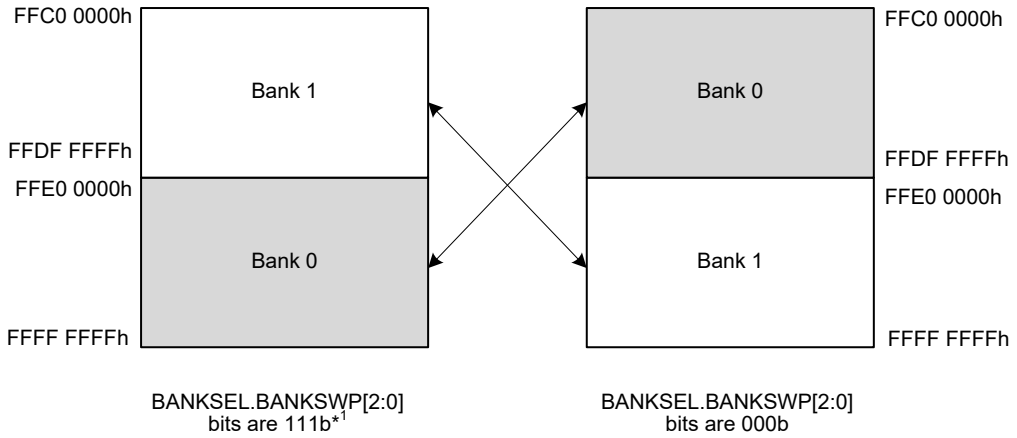
Figure 2-10 Flow for Swapping the Start-Up Area

For how to set the FAW register, refer to 2.2.5 Option-Setting Memory Setting Example.

2.2.3 Dual Bank Function

You can use the bank mode switching function and selecting the startup bank to switch the bank address so that a program can be updated in another bank while user programs continue to run. If the update operation is disrupted for any reason including a reset, the program is still safely updated.

Figure 2-11 gives an example start-up bank selection. Figure 2-12 shows the flow for switching the start-up bank.



Note: The addresses of the reset vector are fixed to FFFF FFFCh to FFFF FFFFh.

Note 1. For products without setting of the option-setting memory, the BANKSEL.BANKSWP[2:0] bits are 111b.

Figure 2-11 Example of Start-Up Bank Selection (for RX72M)

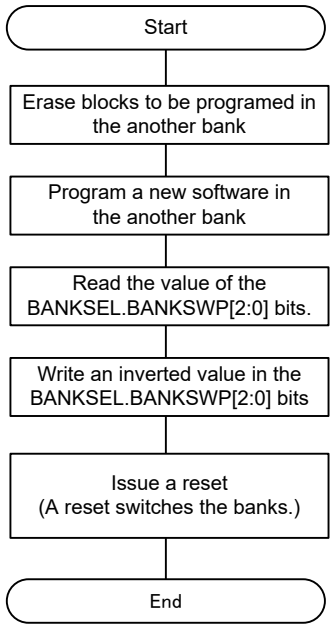


Figure 2-12 Flow for Switching the Start-Up Bank

2.2.4 How to Issue the Start-Up Area Information Program Command / Access Window Information Program Command

Figure 2-13 shows the flow for issuing the start-up area information program command and access window information program command.

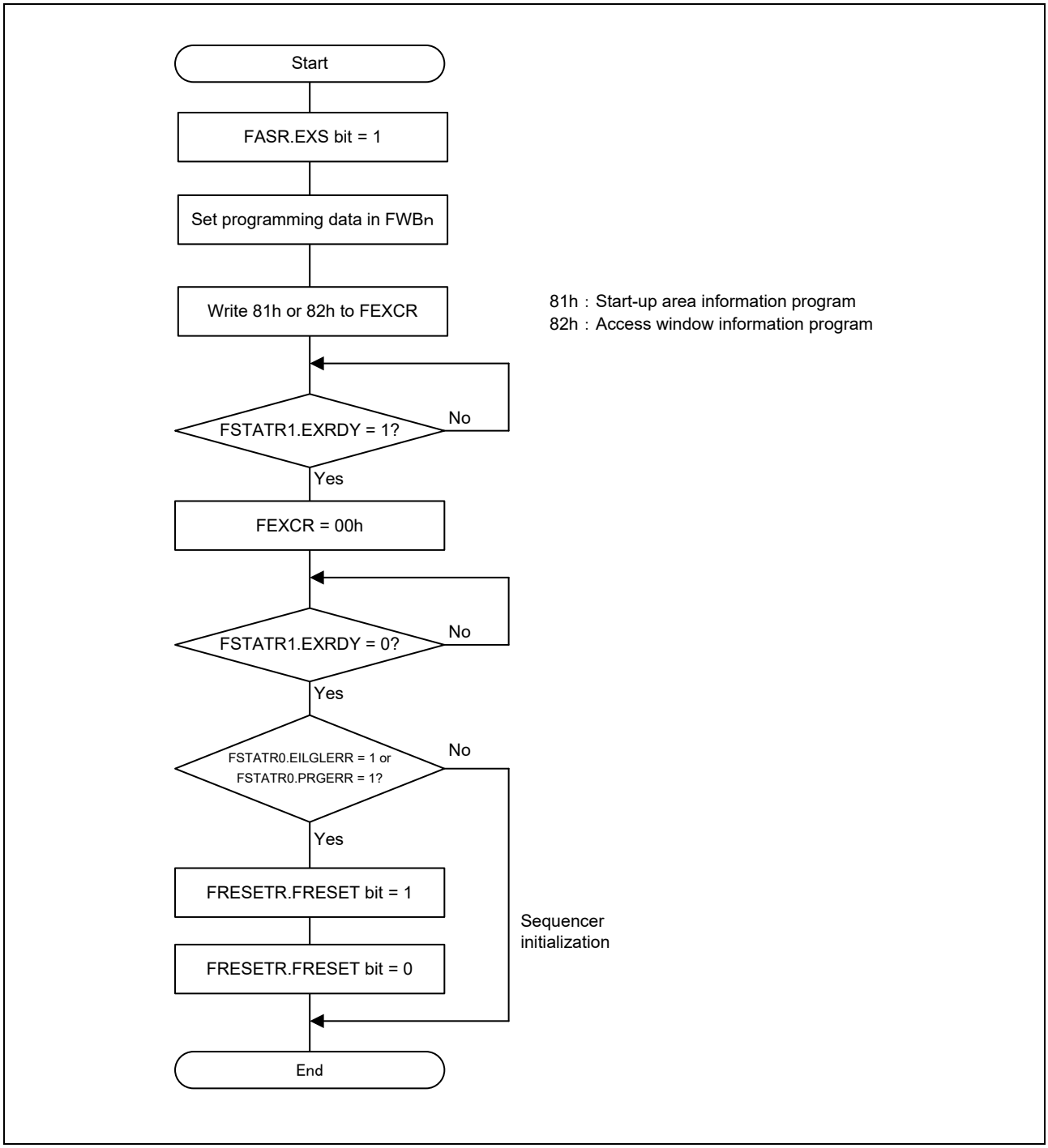


Figure 2-13 Flow for Issuing the Start-Up Area Information Program Command / Access Window Information Program Command

2.2.5 Option-Setting Memory Setting Example

The access window and Startup Program Protection settings are enabled by writing to the FAW register in the option-setting memory.

Also, the FAW register addresses vary depending on the device. For instructions on writing data to the option-setting memory, refer to the User's Manual: Hardware of the device.

Figure 2-14 and Figure 2-15 gives a setting example for each protection.

```
/* Setup the Flash access window setting Register */
#pragma address FAW_REG = 0xFE7F5D64
const unsigned long FAW_REG = 0x07FB07F9;
```

In this example,
the access window start address is FFFF 2000h (the FAWS bit is set to 7F9h (b23 to b13 of FFFF 2000h)), the access window end address is set to FFFF 7FFFh (the FAWE bit is set to 7FBh (b23 to b13 of FFFF 7FFFh)), and protection provided by the FSPR bit is enabled.

Figure 2-14 Setting the Access Window

```
/* Setup the Flash access window setting Register */
#pragma address FAW_REG = 0xFE7F5D64
const unsigned long FAW_REG = 0x80000000;
```

In this example, the start-up area is set to use the addresses from FFFF E000h to FFFF FFFFh.

Figure 2-15 Setting the Start-Up Program Protection

3. Reference Documents

RX110 Group User's Manual: Hardware (R01UH0421)
RX111 Group User's Manual: Hardware (R01UH0365)
RX113 Group User's Manual: Hardware (R01UH0448)
RX130 Group User's Manual: Hardware (R01UH0560)
RX13T Group User's Manual: Hardware (R01UH0822)
RX140 Group User's Manual: Hardware (R01UH0905)
RX14T Group User's Manual: Hardware (R01UH1126)
RX210 Group User's Manual: Hardware (R01UH0037)
RX21A Group User's Manual: Hardware (R01UH0251)
RX220 Group User's Manual: Hardware (R01UH0292)
RX230 Group, RX231 Group User's Manual: Hardware (R01UH0496)
RX23E- A Group User's Manual: Hardware (R01UH0801)
RX23E- B Group User's Manual: Hardware(R01UH0972)
RX23T Group User's Manual: Hardware (R01UH0520)
RX23W Group User's Manual: Hardware (R01UH0823)
RX24T Group User's Manual: Hardware (R01UH0576)
RX24U Group User's Manual: Hardware (R01UH0658)
RX260 Group, RX261 Group User's Manual: Hardware (R01UH1045)
RX26T Group User's Manual: Hardware (R01UH0979)
RX610 Group User's Manual: Hardware (R01UH0032)
RX62N Group, RX621 Group User's Manual: Hardware (R01UH0033)
RX62T Group, RX62G Group User's Manual: Hardware (R01UH0034)
RX630 Group User's Manual: Hardware (R01UH0040)
RX634 Group User's Manual: Hardware (R01UH0495)
RX63N Group, RX631 Group User's Manual: Hardware (R01UH0041)
RX63T Group User's Manual: Hardware (R01UH0238)
RX64M Group User's Manual: Hardware (R01UH0377)
RX65N Group, RX651 Group User's Manual: Hardware (R01UH0590)
RX65W-A Group User's Manual: Hardware (R01UH0993)
RX660 Group User's Manual: Hardware (R01UH0937)
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RX72T Group User's Manual: Hardware (R01UH0803)
RX72M Group User's Manual: Hardware (R01UH0804)
RX72N Group User's Manual: Hardware (R01UH0824)
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C compiler manual
C/C++ Compiler Package for RX Family
(Get the latest version from the Renesas Electronics website.)

RX100/RX200 Series Updating Firmware Using Start-Up Program Protection and Serial Communication (R01AN3740)

RX Family Firmware Update Module Using Firmware Integration Technology (R01AN5824)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.28.12	—	First edition issued
2.00	Sep.30.16	All	Added the following target devices: • RX110 Group • RX111 Group • RX113 Group • RX130 Group • RX210 Group • RX21A Group • RX220 Group • RX231, RX230 Group • RX23T Group • RX24T Group • RX62G Group • RX62T Group • RX634 Group • RX63T Group • RX64M Group • RX71M Group Added “1. Device Categories”. Changed the arrangement of the sections according to the target device categories.
3.00	Jun.01.17	All	Added the following target devices: RX65N, RX651 Group
4.00	May.13.19	All	Added the following target devices: • RX24U, RX66T, RX72T Group Corrected RX21A Group and RX220 Group from device group A to device group B in Table 1. Corrected Table 4, Table 17 and Table 30. Add descriptions of the access window.
5.00	Nov.07.19	All	Added the following target devices: • RX23E-A Group • RX23W Group • RX13T Group • RX72M Group • RX72N Group RX66N Group
6.00	Sep.10.21	All	Changed Target Device to RX Family. Added RX140 Group and RX671 Group to "Device” in “1. Device Categories". Added On-Chip Debugger Connection Enable/Disable and Access Window Protection Command to "Protection Function" in "1. Device Categories". Added “8. Device Group G Protection Methods”.

			Changed the description of the specifications of the device group that supports the access window.
7.00	Nov.11.21	All	Changed the title to “How to Prevent the On-Chip Flash Memory from Being Accessed by Third Parties or Being Accidentally Programmed by Developers”. Reordered the device names in “1. Device Categories". Changed the Note 3 in “1. Device Categories". Corrected RX23W Group from device group A to device group B. Added “2. Protection during Self-Programming Initiated By Developers”. Changed the arrangement of the sections to add “Protection during Self-Programming Initiated By Developers”. Changed reference to a figure or a table from “below” to the Figure or Table number.
8.00	Mar.25.25	All	Added the following target devices: • RX660 Group • RX23E-B Group • RX260, RX261 Group • RX26T Group • RX65W Group
9.00	Mar.2.26	All	The device group classification has been eliminated, and the document has been restructured based on individual protection functions. Added the following target devices: • RX14T Group

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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