RX Family

Hardware Design Guide

Introduction

This application note presents notes on board design and layout examples when using RX Family MCUs.

Target Device

RX Family

Contents

1. Board Configuration

1.1 Block Diagram

Figure 1.1 shows a block diagram of the board configuration used in the design example.

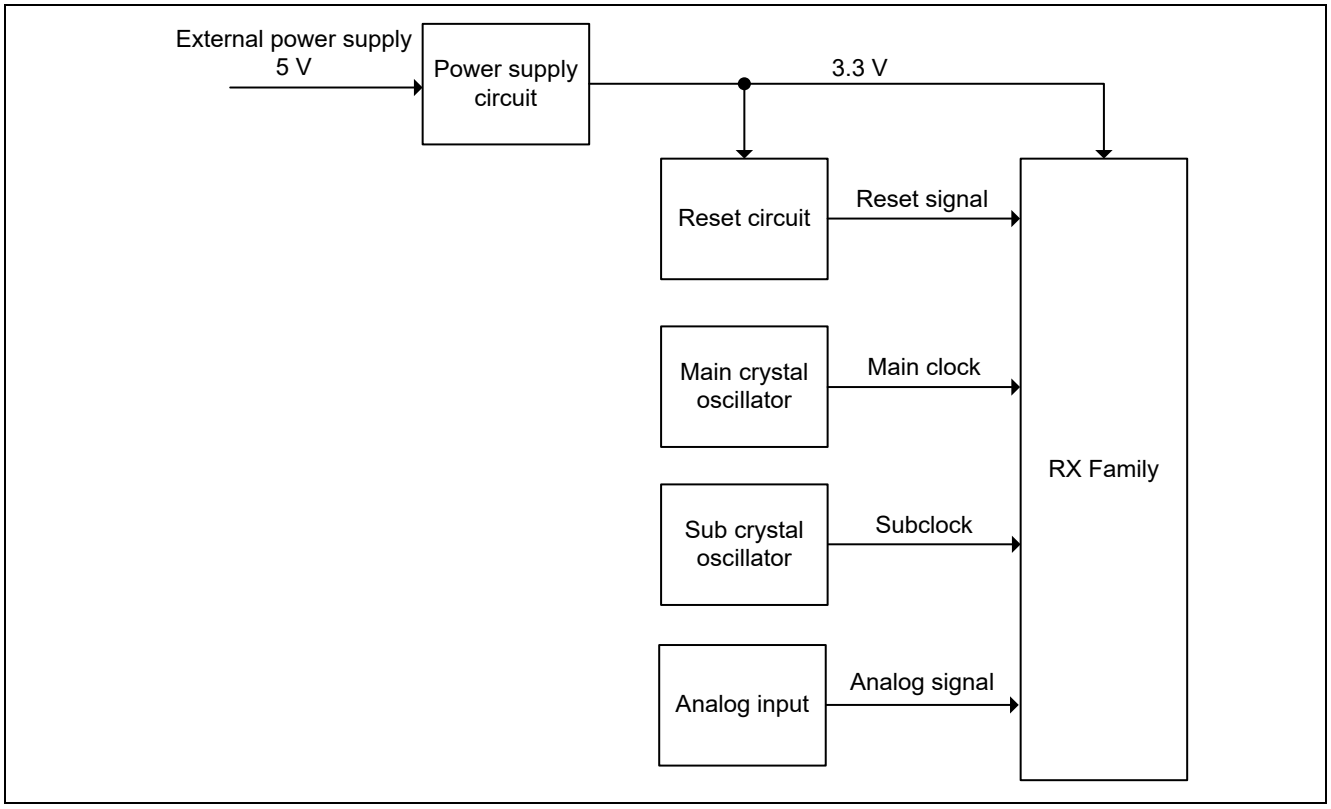


Figure 1.1 Block Diagram

1.2 Component Layout

Figure 1.2 and Figure 1.3 show component layout examples. Note that the board thickness is typically 1.6 mm.

The feedback resistor (R2) and damping resistors (R3 and R5) are usually unnecessary. (In Figure 1.2 no feedback resistors are mounted.) If the oscillator manufacturer stipulates that external feedback resistors or damping resistors should be added, mount them according to the manufacturer's specification.

In some cases 0 Ω damping resistors (R3 and R5) or wiring pattern connection can be used.

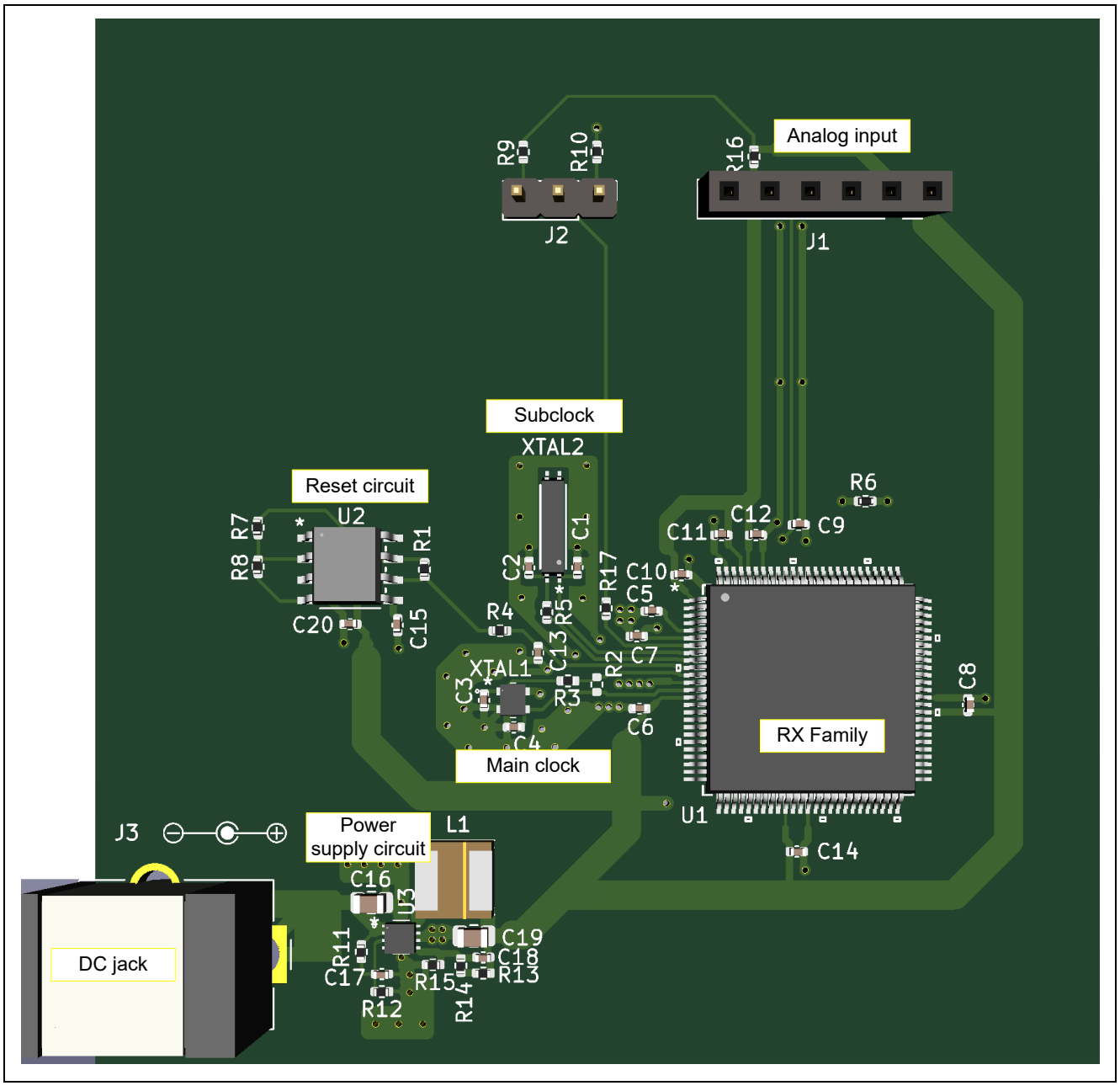


Figure 1.2 Component Layout (Front Side)

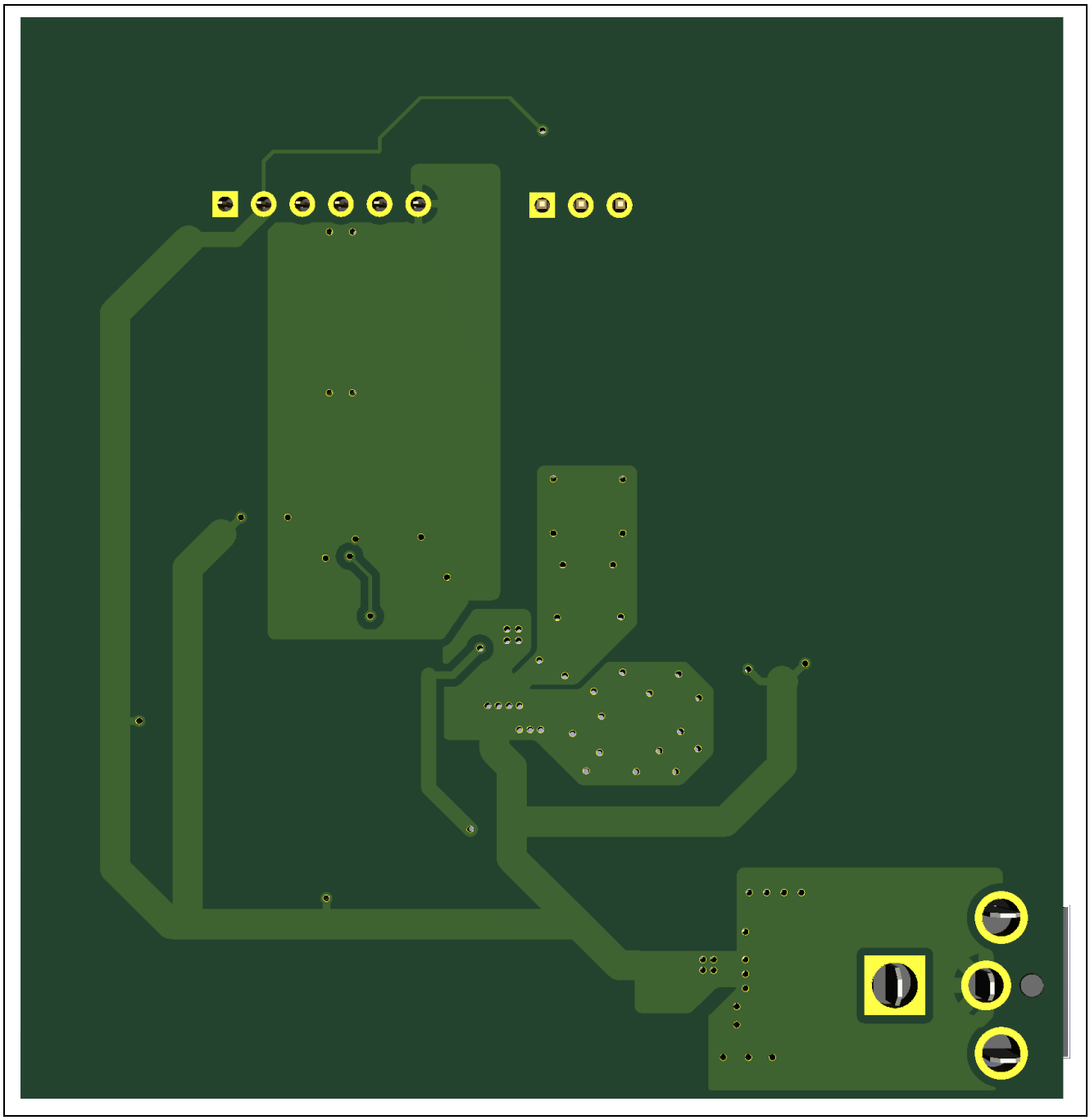


Figure 1.3 Component Layout (Back Side)

1.3 Layer Structure

Figure 1.4 shows layer structure examples.

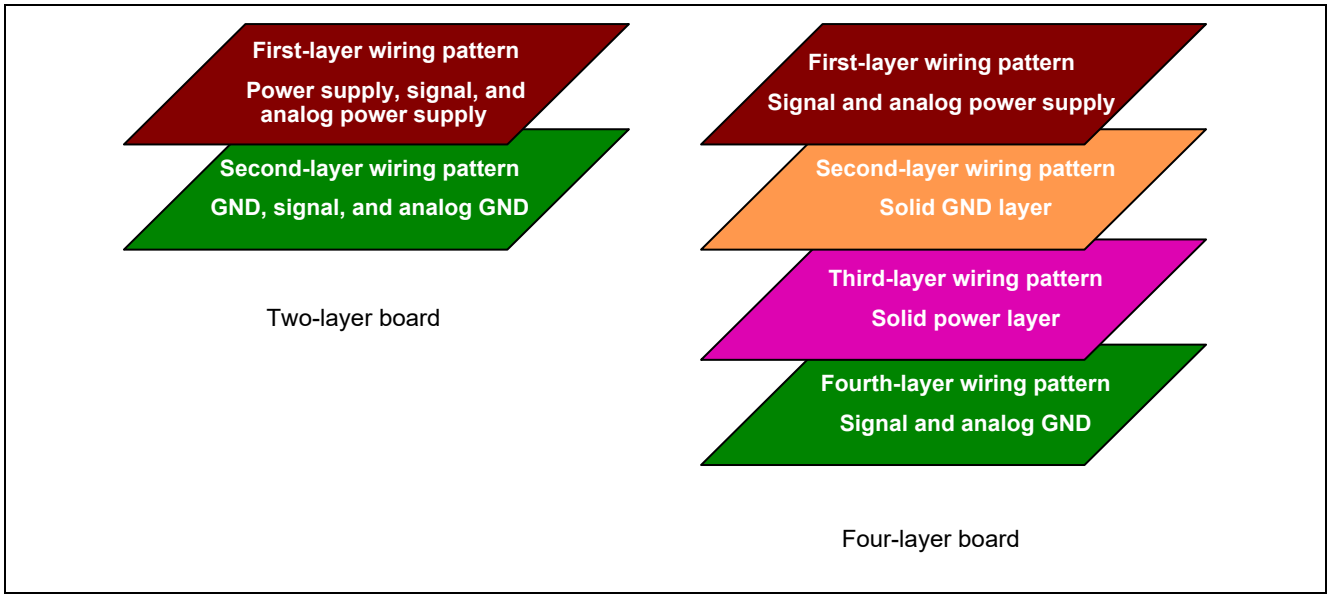


Figure 1.4 Layer Structure Examples

Figure 1.5 shows an example wiring pattern for a two-layer board.

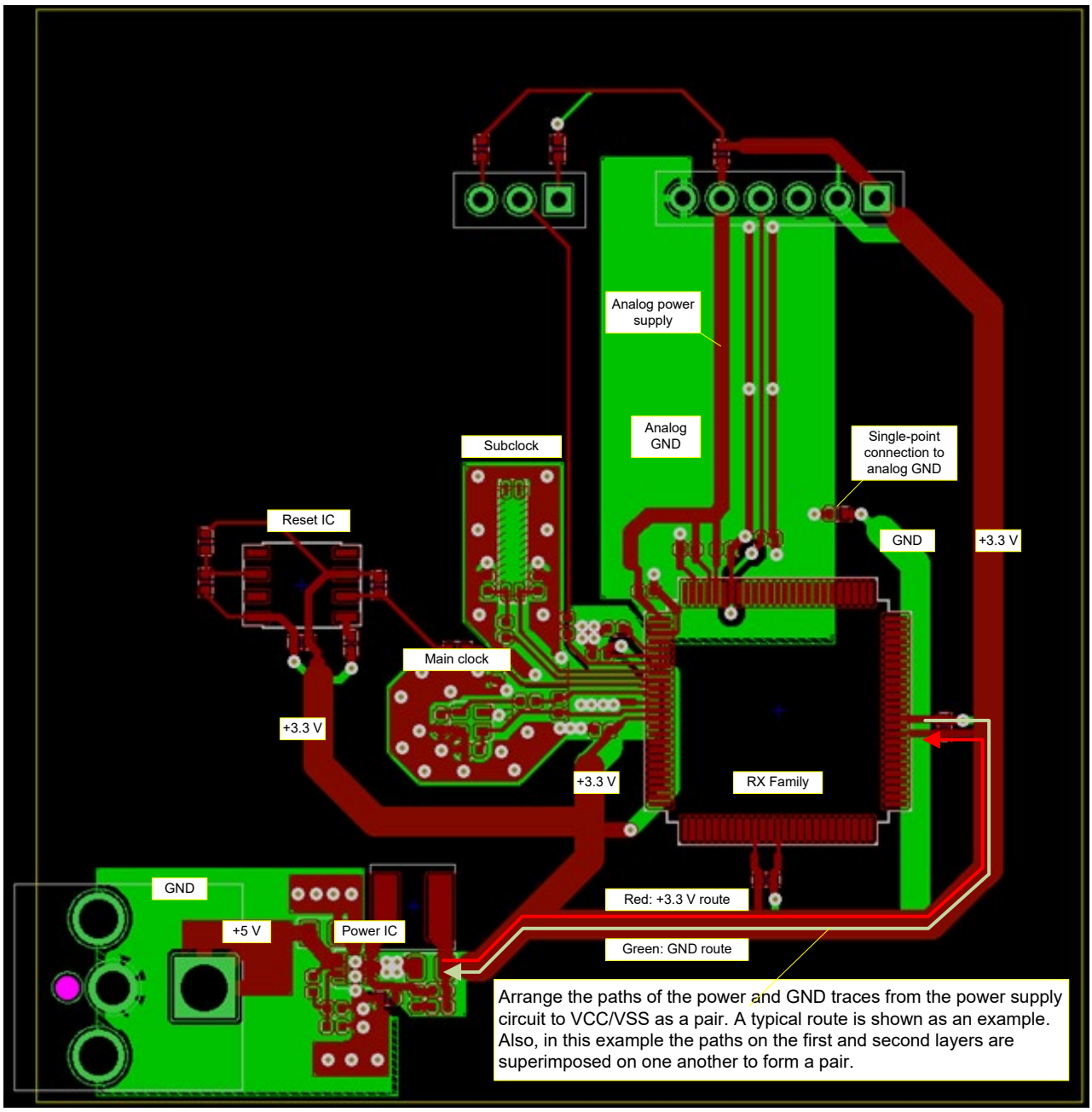


Figure 1.5 Example Wiring Pattern for Two-Layer Board

2. Board Design

2.1 Power Supply Pins

Connect the power supply pins to GND via a bypass capacitor (decoupling capacitor). Use a capacitor with good frequency characteristics, such as a ceramic capacitor. The wiring length between each power supply pin and the bypass capacitor must be equal and as short as possible. In addition, pair the appropriate power supply pins. For example, the VCC pin, AVCC pin, and VREFH pin should be paired with the VSS pin, AVSS pin, and VREFL pin, respectively. Refer to the User's Manual: Hardware of the product used for more details on pairing pins. The traces for the power supply pins must be wider than traces for other signal lines and must be connected to the power supply and GND via a bypass capacitor. Figure 2.1 shows example connections of power supply pins and bypass capacitors.

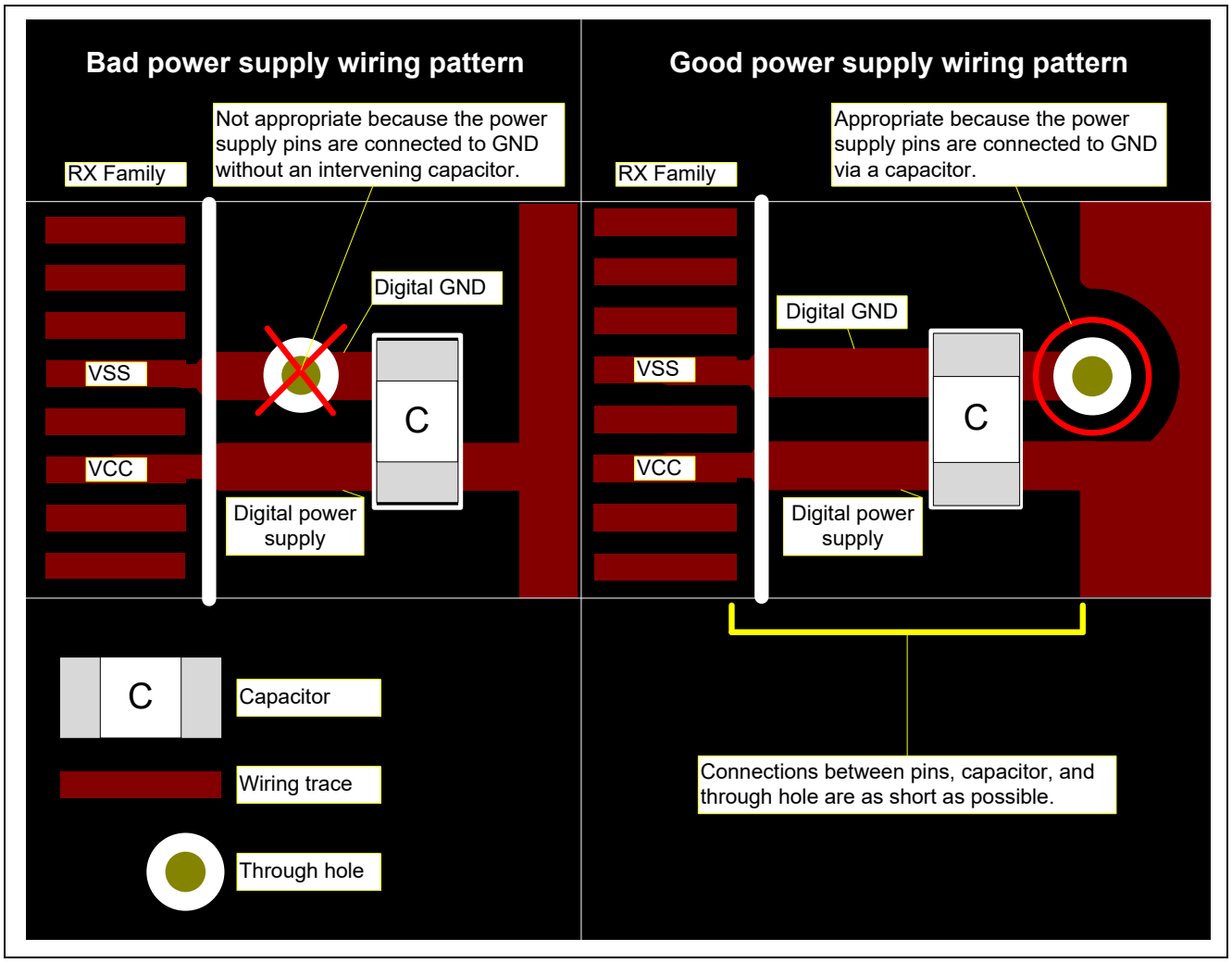


Figure 2.1 Example Connections of Power Supply Pins and Bypass Capacitors

Refer to the application notes below for details of the analog power-supply pins. The latest versions and guides to new products can be downloaded from the Renesas Electronics website.

- RX610 Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0271EJ)
- RX62N Group, RX621 Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0269EJ)
- RX62T Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0638EJ)

Board design hint

A bypass capacitor connected to the power supply pins can be placed so as to route noise to GND during MCU operation.

Figure 2.2 shows an example power supply pin circuit configuration, and Figure 2.3 shows an example power supply pin wiring pattern

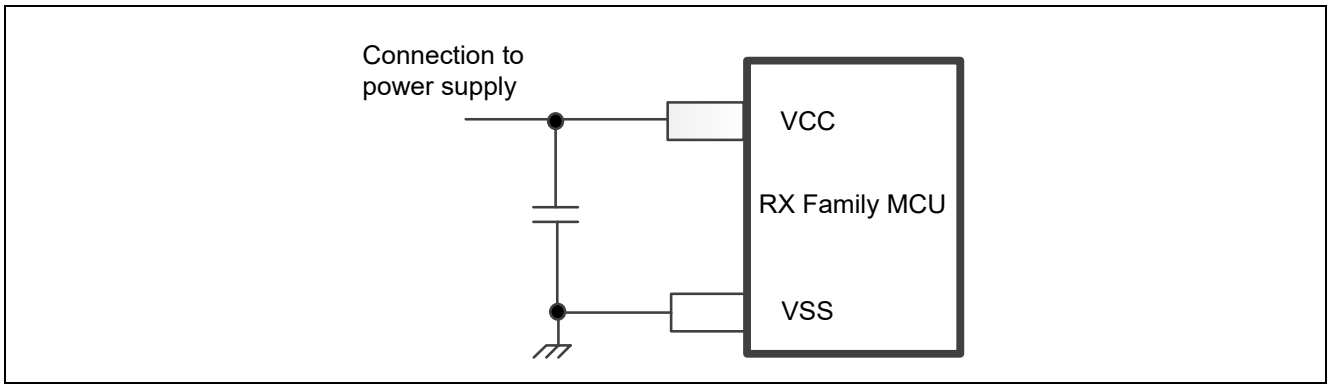


Figure 2.2 Example Power Supply Pin Circuit Configuration

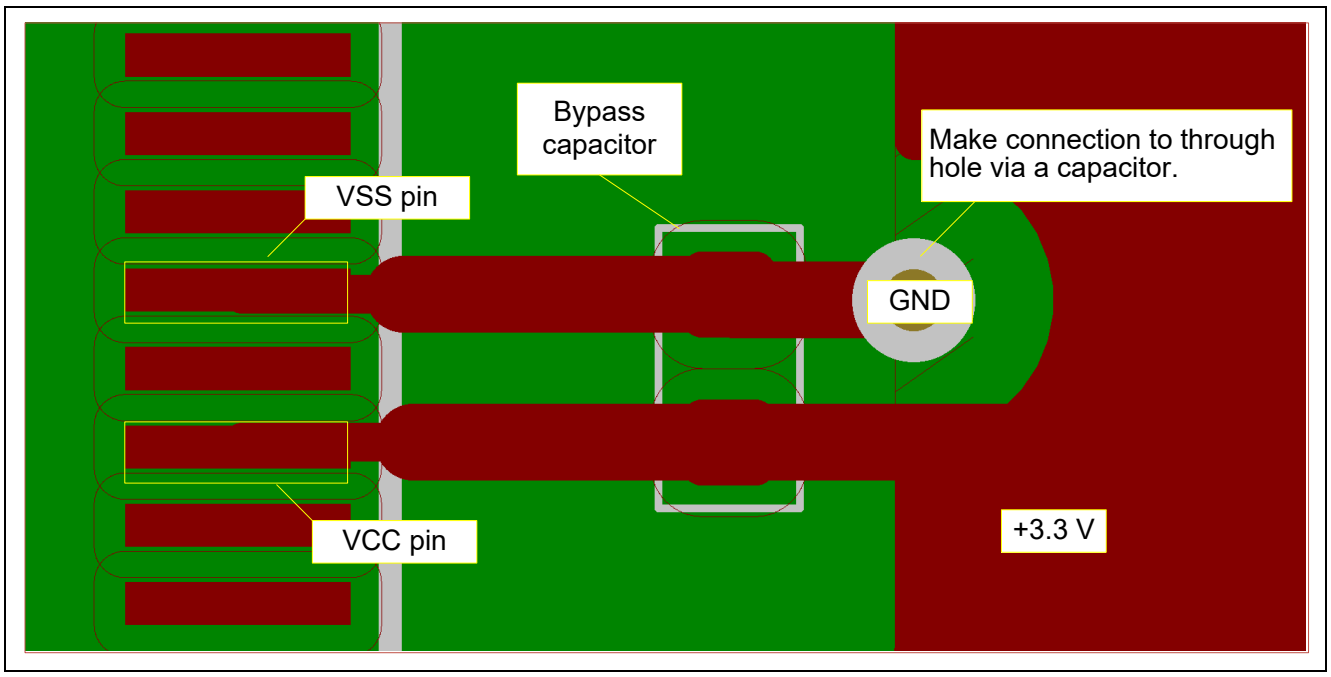


Figure 2.3 Example Power Supply Pin Wiring Pattern

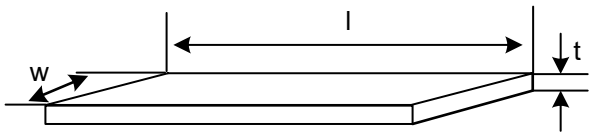
2.2 VCL Pin

Connect the VCL pin to GND via a capacitor with a rated capacitance matching that specified in the user's manual of the device used. The wiring length between the VCL pin and the capacitor should be 8 mm or less (4 mm or less if possible).

Note that GND wiring patterns vary depending on the number of board layers. Section 2.2.1 describes two-layer boards, and section 2.2.2 describes boards with four or more layers.

Board design hint

If the wiring length between the VCL pin and capacitor is longer than 8 mm, the parasitic resistance increases, decreasing the effectiveness of the capacitor and possibly causing noise from the VCC pin. When the wiring length between the VCL pin and capacitor is longer than 8 mm, the wiring pattern should be designed so that the parasitic resistance is less than 1 Ω. Figure 2.4 shows a formula for calculating the parasitic resistance.



Wiring on printed circuit board

$$R = l / \sigma wt\ (\Omega)$$

$$L = 0.2l\left[\ln\left\{2l/(w+t)\right\}+0.5\right]\ (\mu H)$$

$$\omega L = 2\pi fL(\Omega)$$

$$f = 20\ (MHz)\ (\text{internal fluctuation in MCU when power is supplied})$$

$$\text{Parasitic resistance} = R + 2\pi fL\ (\Omega) < 1\ (\Omega)$$

Figure 2.4 Formula for Calculating Parasitic Resistance

In the following example, the formula shown in Figure 2.4 is used to calculate the parasitic resistance.

Example:

Wiring length (l): 0.008 m (8 mm)
Wiring width (w): 0.00025 m (0.25 mm)
Wiring thickness (t): 0.000035 m (0.035 mm)
Resistivity of copper (ρ = 1 / σ): 0.0000000169 Ω • m

Parasitic resistance = R + 2πfL
= (l / σwt) + 2 × π × 20 × (0.2 × l (loge (2 × l / (w + t)) +0.5))
= 0.01545 + 2 × 3.1416 × 20 × 0.00724
≈ 0.9253 (Ω)

Figure 2.5 shows an example circuit configuration for the VCL pin.

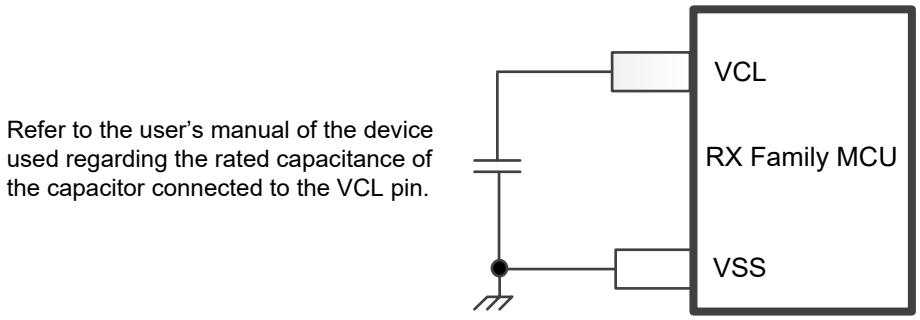


Figure 2.5 Example VCL Pin Circuit Configuration

2.2.1 Two-Layer Board

- Use the GND wiring pattern to form a guard for the portion of the back side between the VCL pin and the capacitor.
- Make connections to GND via at least four through holes.
- Make the GND wiring traces as wide as possible.

Figure 2.6 shows an example VCL pin wiring pattern on a two-layer board.

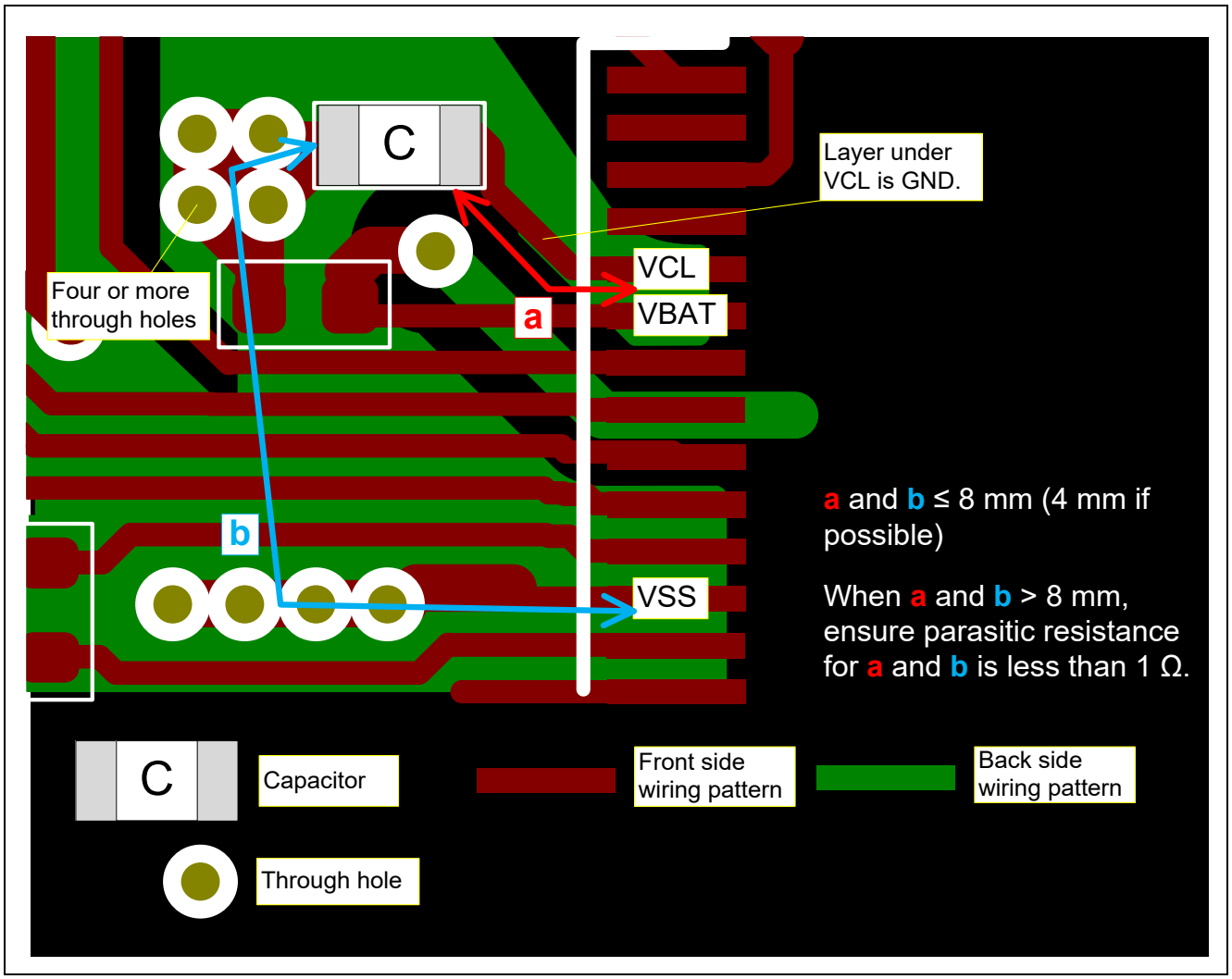


Figure 2.6 Example VCL Pin Wiring Pattern on Two-Layer Board

Figure 2.7 shows an example VCL pin wiring pattern (two-layer board).

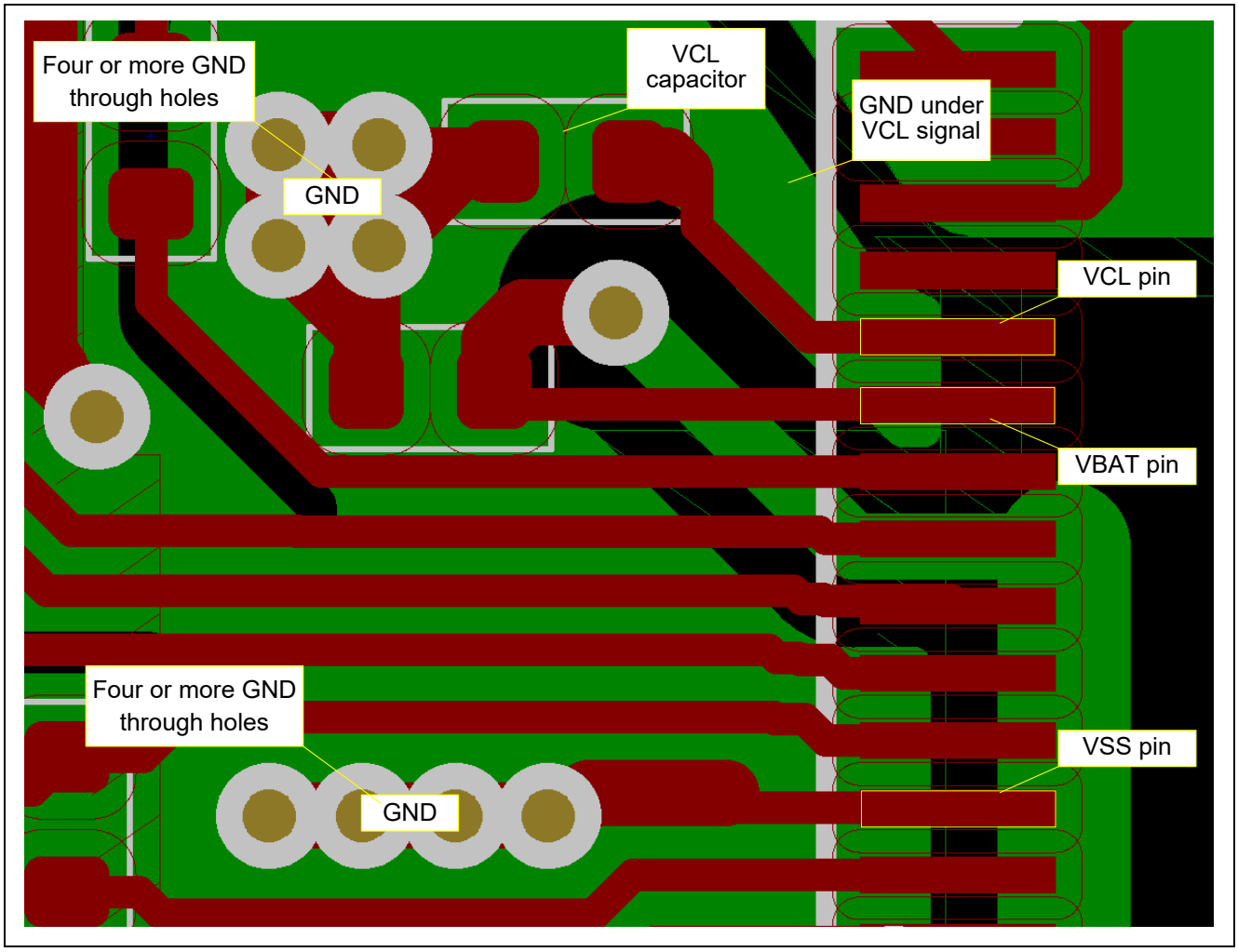


Figure 2.7 Example VCL Pin Wiring Pattern (Two-Layer Board)

2.2.2 Board With Four or More Layers

Figure 2.8 shows an example VCL pin wiring pattern (board with four or more layers).

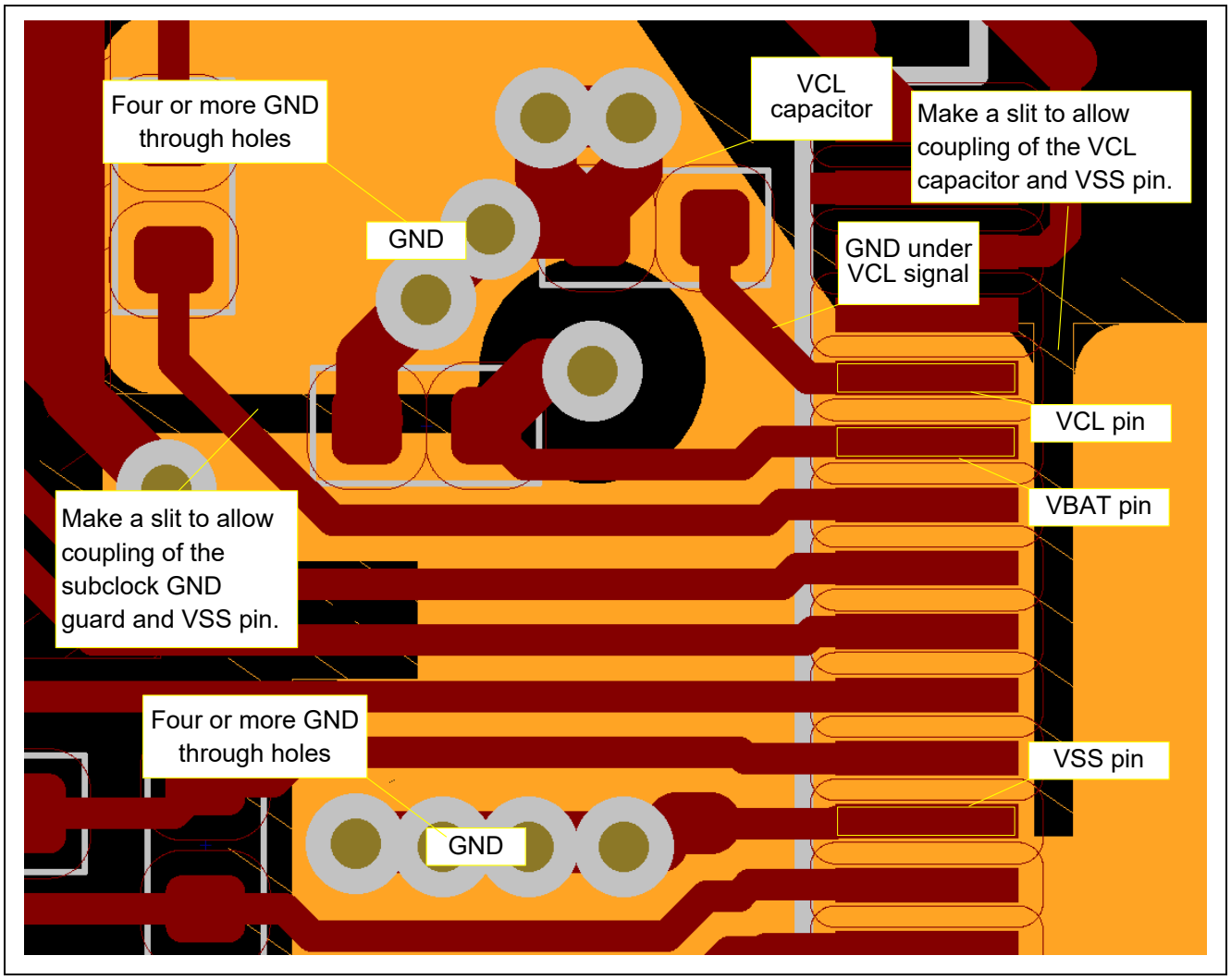


Figure 2.8 Example VCL Pin Wiring Pattern (Board With Four or More Layers)

2.3 Reset Pin

When directly connecting the reset pin to the reset IC, position the reset IC as close as possible. Noise can also be reduced by inserting a low-pass filter. Do not run the trace for the reset pin parallel to other traces (traces with large current flows or rapid level changes). If no low-pass filter is used, shield the trace for the reset pin with the GND trace. The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

Board design hint

The pulse width input to the reset pin is specified in the timing requirements. If the noise input to the reset pin has a shorter width than the specified pulse width, a reset condition may be released before the MCU's internal initialization has completed, possibly causing program runaway.

Figure 2.9 shows an example reset pin circuit configuration, and Figure 2.10 shows an example reset pin wiring pattern (multilayer board).

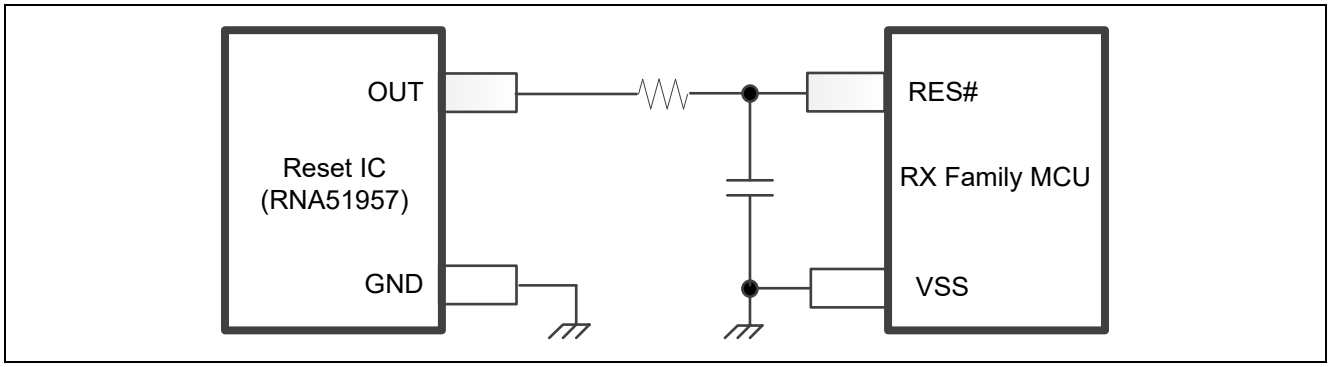


Figure 2.9 Example Reset Pin Circuit Configuration (With Low-Pass Filter)

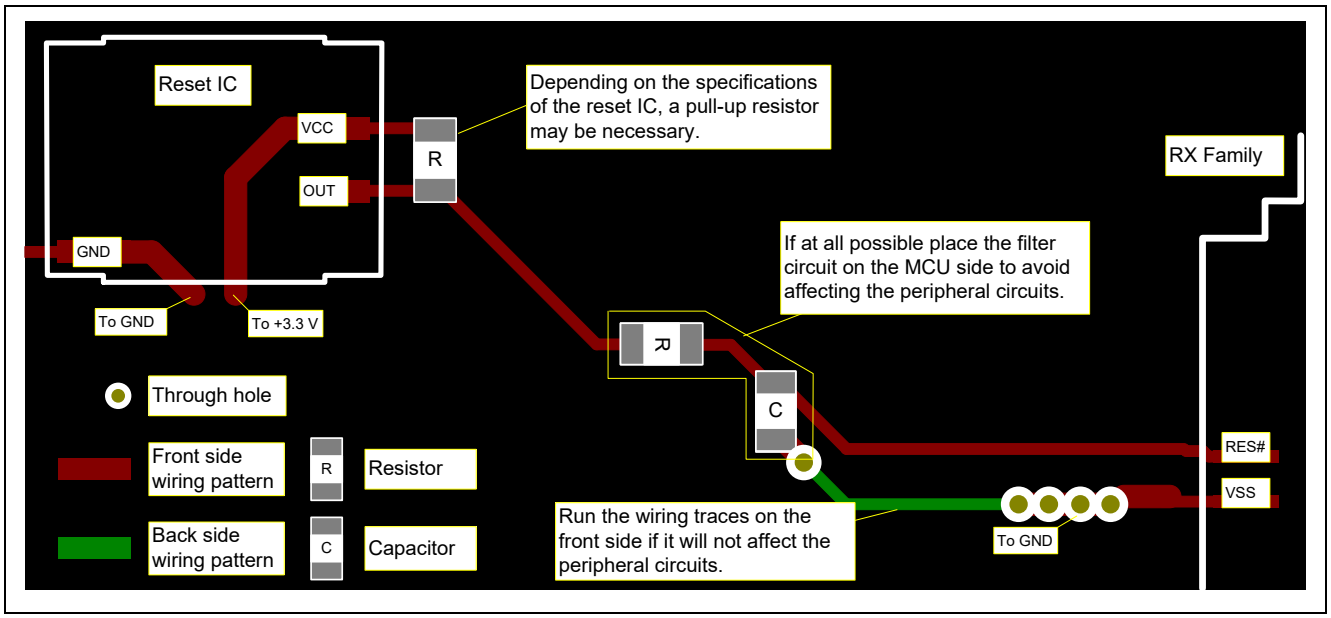


Figure 2.10 Example Reset Pin Wiring Pattern

Figure 2.11 shows an example reset pin wiring pattern.

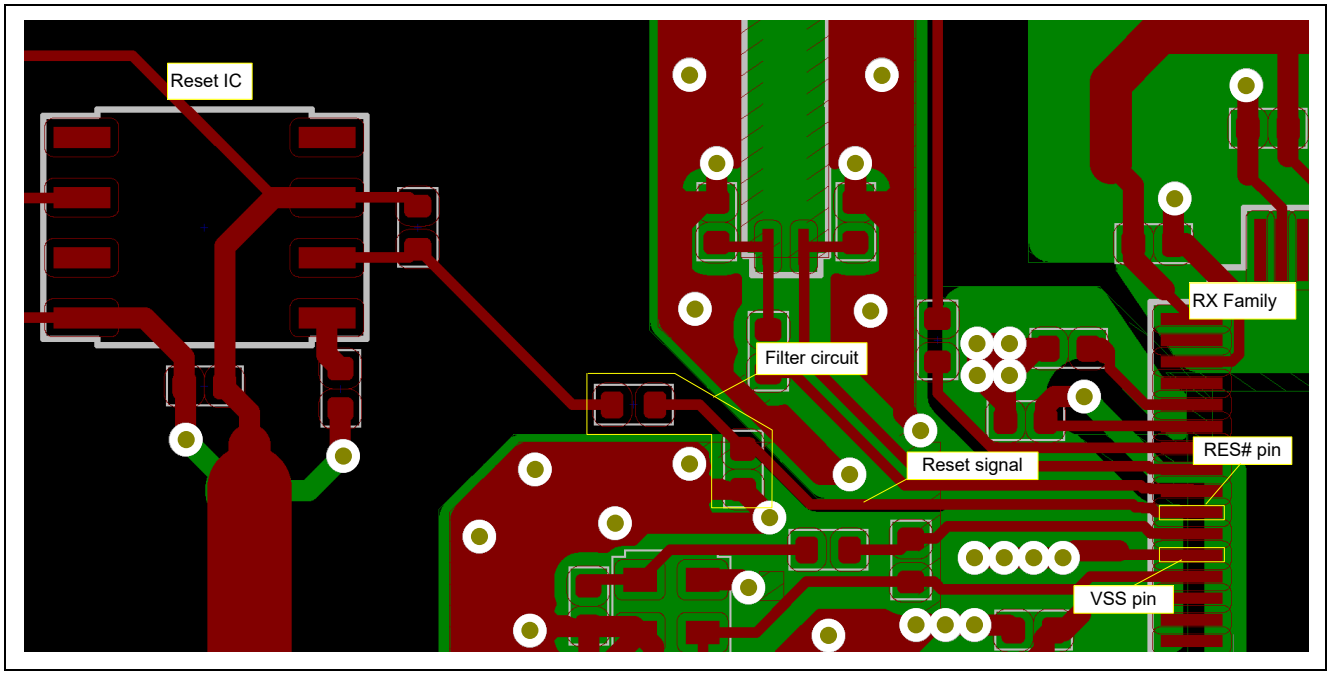


Figure 2.11 Example Reset Pin Wiring Pattern

2.4 Clock I/O Pins

The wiring traces for the clock I/O pins (EXATL, XTAL, XCIN, and XCOUT) should be as short as possible, including peripheral circuits. Shield the wiring pattern for the clock I/O pins with the GND pattern and do not arrange the traces for the clock I/O pins in parallel with or across other traces (traces with large current flows or rapid level changes). The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces. In addition, do not place the GND wiring pattern and power supply wiring pattern in layers under a peripheral circuit incorporating a crystal oscillator.

Refer to the application note below for information on the main clock oscillator circuit and the sub-clock oscillator circuit. The latest versions and guides to new products can be downloaded from the Renesas Electronics website.

- RX and RA families: Design Guide for Main Clock Circuit and Sub-Clock Circuit (R01AN7202EJ)

Board design hint

If noise impinges on the clock I/O pins, the clock waveforms may become distorted, possibly causing an MCU malfunction or program runaway. In addition, accurate clock signals cannot be input to the MCU if there is a potential difference between the VSS inputs to the MCU and oscillators.

Figure 2.12 shows an example clock I/O pin circuit configuration.

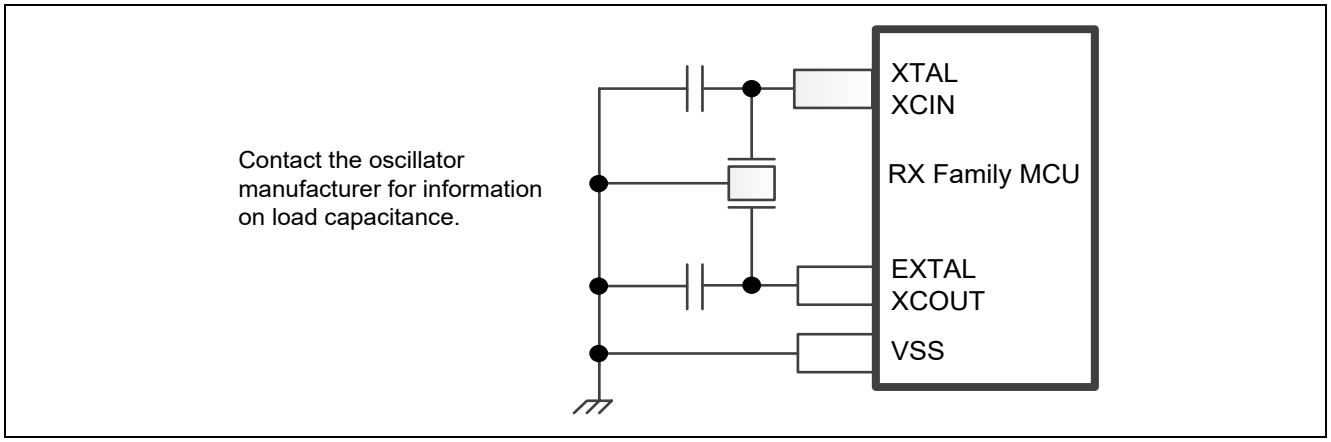


Figure 2.12 Example Clock I/O Pin Circuit Configuration

Figure 2.13, Figure 2.14, and Figure 2.15 show example clock I/O pin wiring patterns.

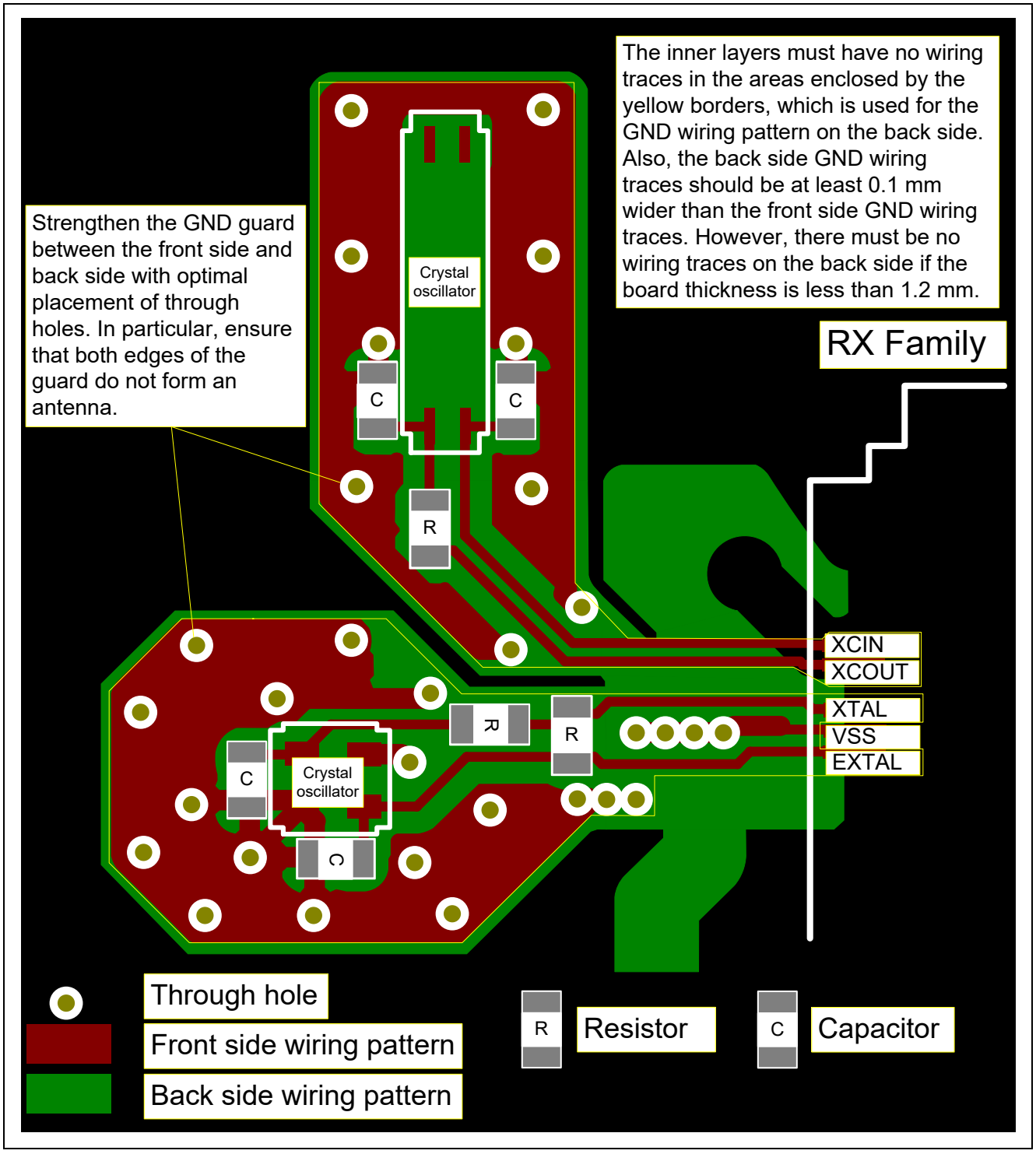


Figure 2.13 Example Clock I/O Pin Wiring Pattern

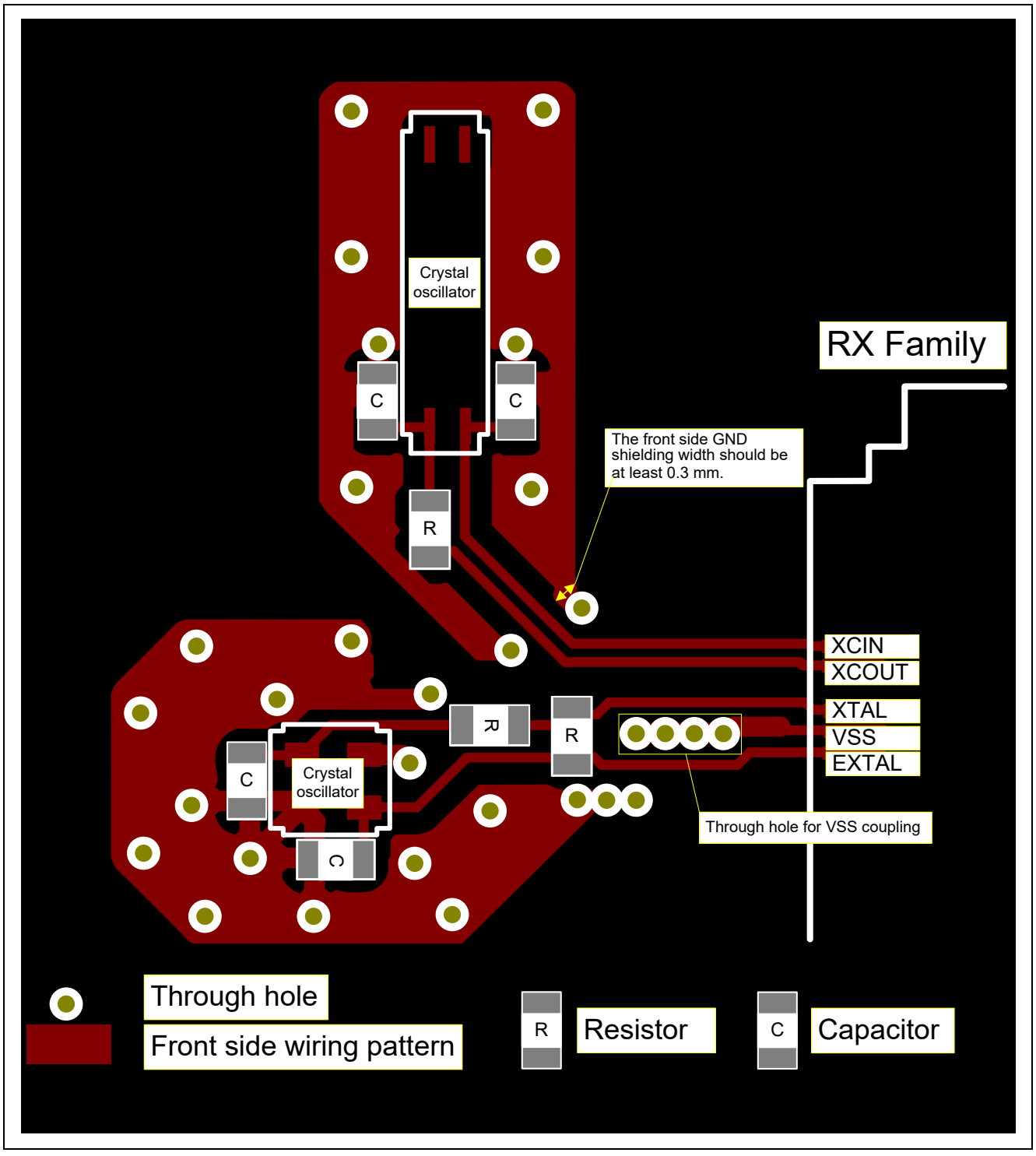


Figure 2.14 Example Clock I/O Pin Wiring Pattern (Front Side)

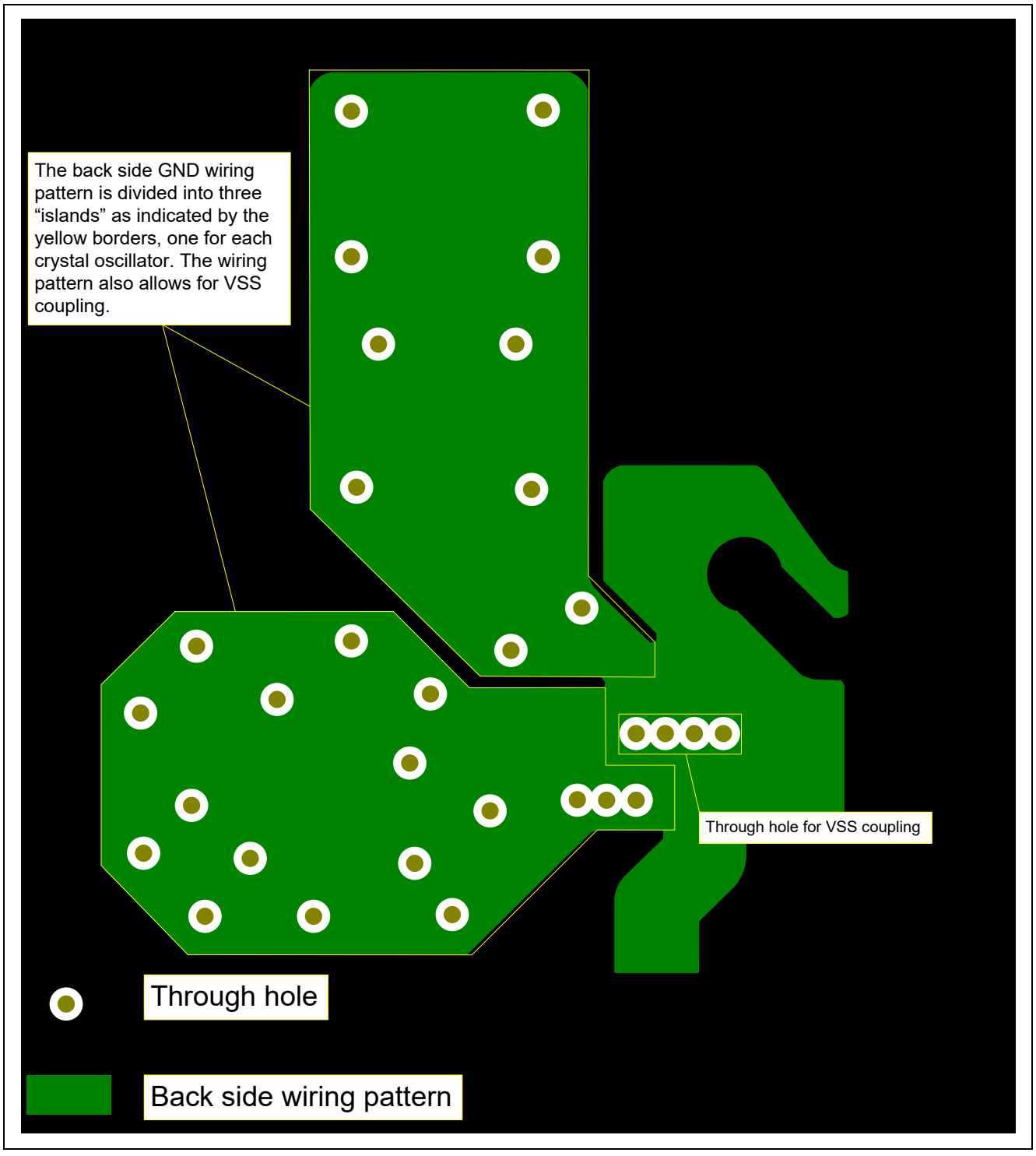


Figure 2.15 Example Clock I/O Pin Wiring Pattern (Back Side)

Figure 2.16 shows an example clock I/O pin wiring pattern.

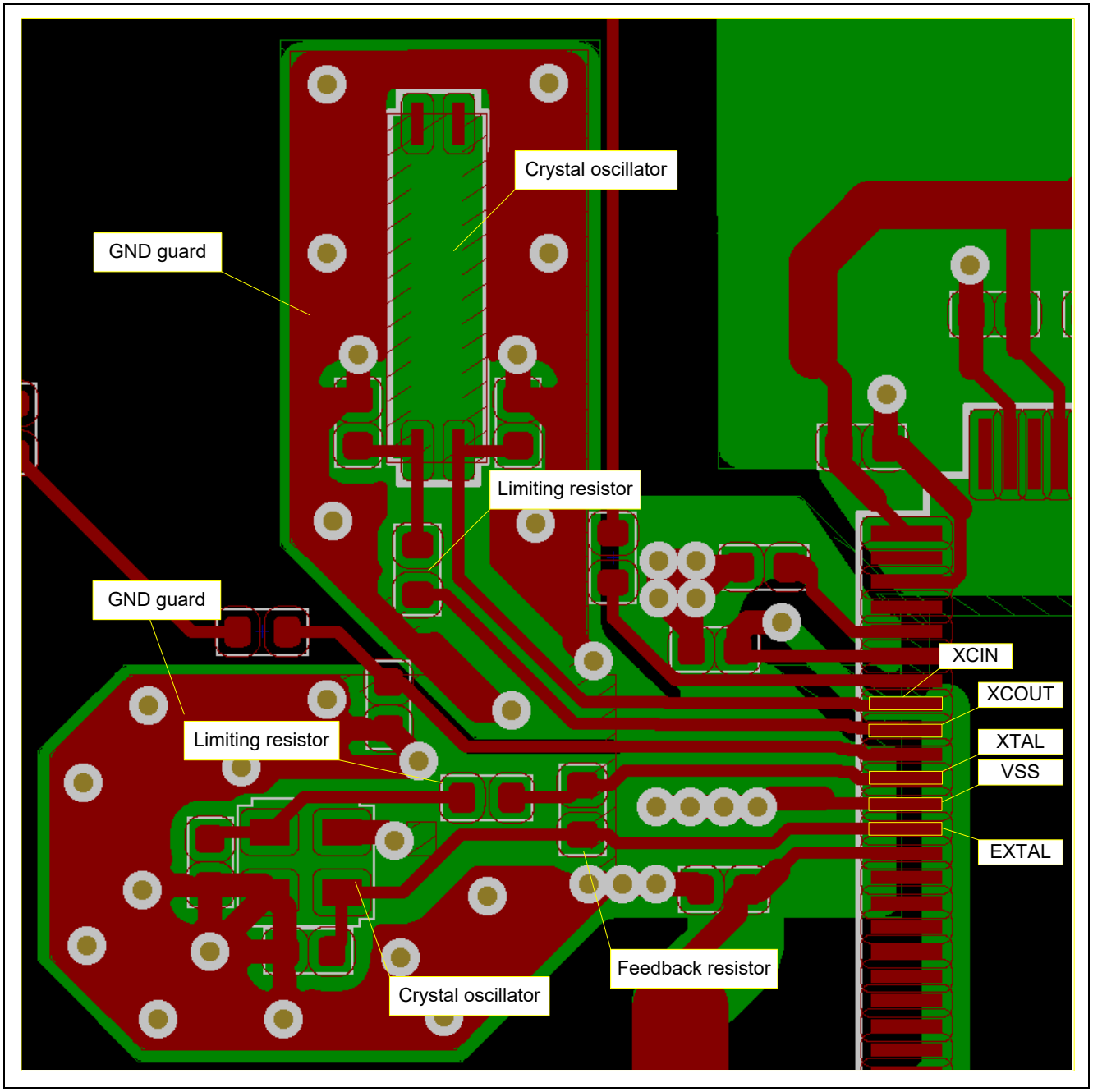


Figure 2.16 Example Clock I/O Pin Wiring

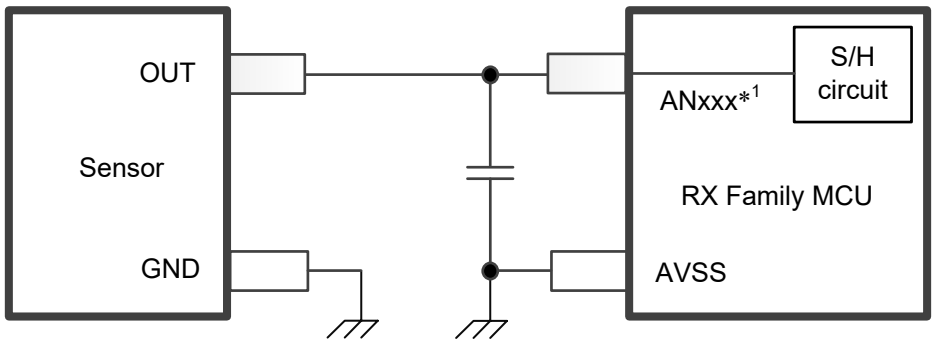
2.5 Analog Input Pins

Connect each analog input pin to GND via a capacitor. Wiring between the analog input pin and capacitor and wiring between the AVSS pin and capacitor must be the same length and as short as possible. Do not run the trace for the analog input pin parallel to or across other traces (traces with large current flows or rapid level changes), and shield the trace for the analog input pin with the GND trace. The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

Board design hint

If noise impinges on the analog input pins, the waveforms may become distorted, possibly reducing A/D converter accuracy. An external capacitor can be used to reduce noise.
An external capacitor can also be used to achieve high-speed conversion. This requires that sufficient electrical charge has accumulated in the external capacitor before conversion starts to reduce the signal source impedance of the input capacitor of the sample and hold circuit. Note that if the voltage level of the analog input pin changes (in continuous scan mode, for example), causing the external capacitor charge to be renewed, an adequate electrical charge cannot be accumulated. In this case, do not connect an external capacitor.

Figure 2.17 shows an example analog input pin circuit configuration, and Figure 2.18 shows an example analog input pin wiring pattern.



Note: 1. ANxxx represents an analog input pin.

Figure 2.17 Example Analog Input Pin Circuit Configuration

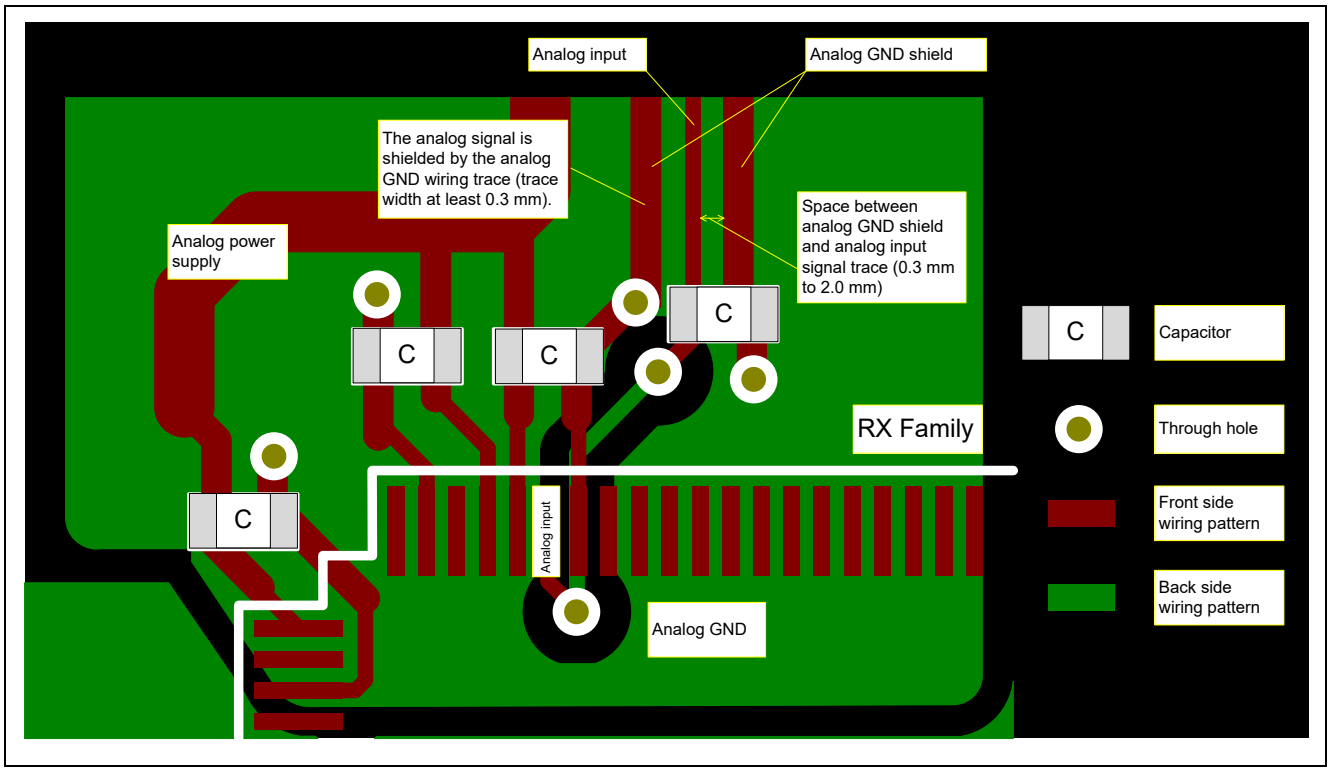


Figure 2.18 Example Analog Input Pin Wiring Pattern

Figure 2.19 shows an example analog input pin wiring pattern.

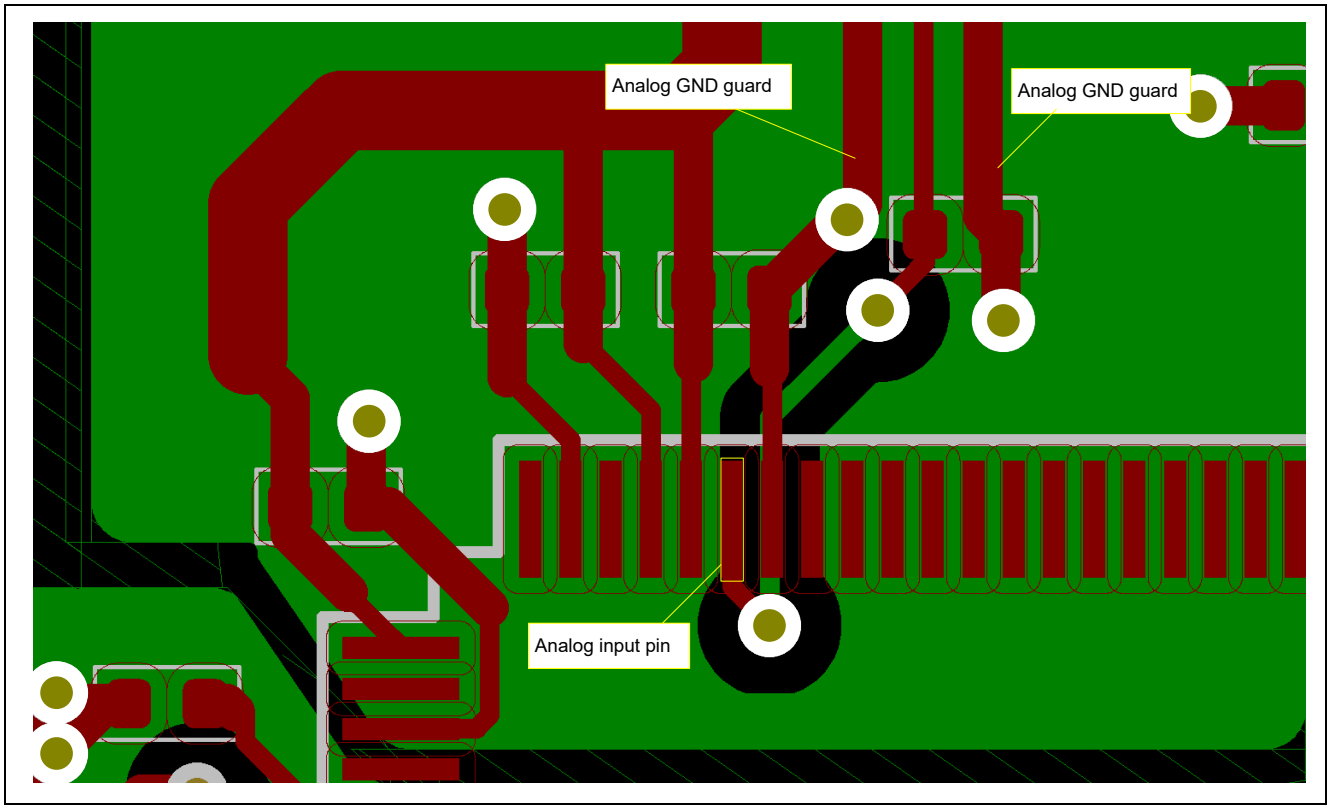


Figure 2.19 Example Analog Input Pin Wiring Pattern

2.6 Signal Pins with Large Current Flows

When a large current exceeding the current range supported by the MCU flows in a signal line, place the signal line as far from the MCU (and the oscillators in particular) as possible, and do not arrange the signal line in parallel with or across the traces of the reset pin, clock I/O pins, or analog input pins.

Board design hint

In systems using an MCU there are signal lines to control motors, LEDs, thermal heads, etc. If large currents flow in these signal lines, mutual inductance with parallel wiring traces can cause noise.

2.7 Signal Pins with Rapid Level Changes

Place signal lines with rapid level changes as far from the oscillators and the wiring traces of the oscillators as possible. Do make such signal lines any longer than necessary and ensure they do not run parallel to or across the clock-related signal lines or other lines that are easily affected by noise.

Board design hint

Signal lines with rapid level changes can easily affect other signal lines when the level changes at the rising and falling edges. In particular, when such signal lines cross clock-related signal lines, the clock waveform can be distorted, possibly resulting in malfunction or program runaway.

3. Board Wiring Pattern Examples

3.1 Example Two-Layer Board Wiring Pattern

Figure 3.1 shows an example two-layer board wiring pattern for an RX Family MCU, and Figure 3.2 and Figure 3.3 show the wiring patterns for the first and second layers separately.

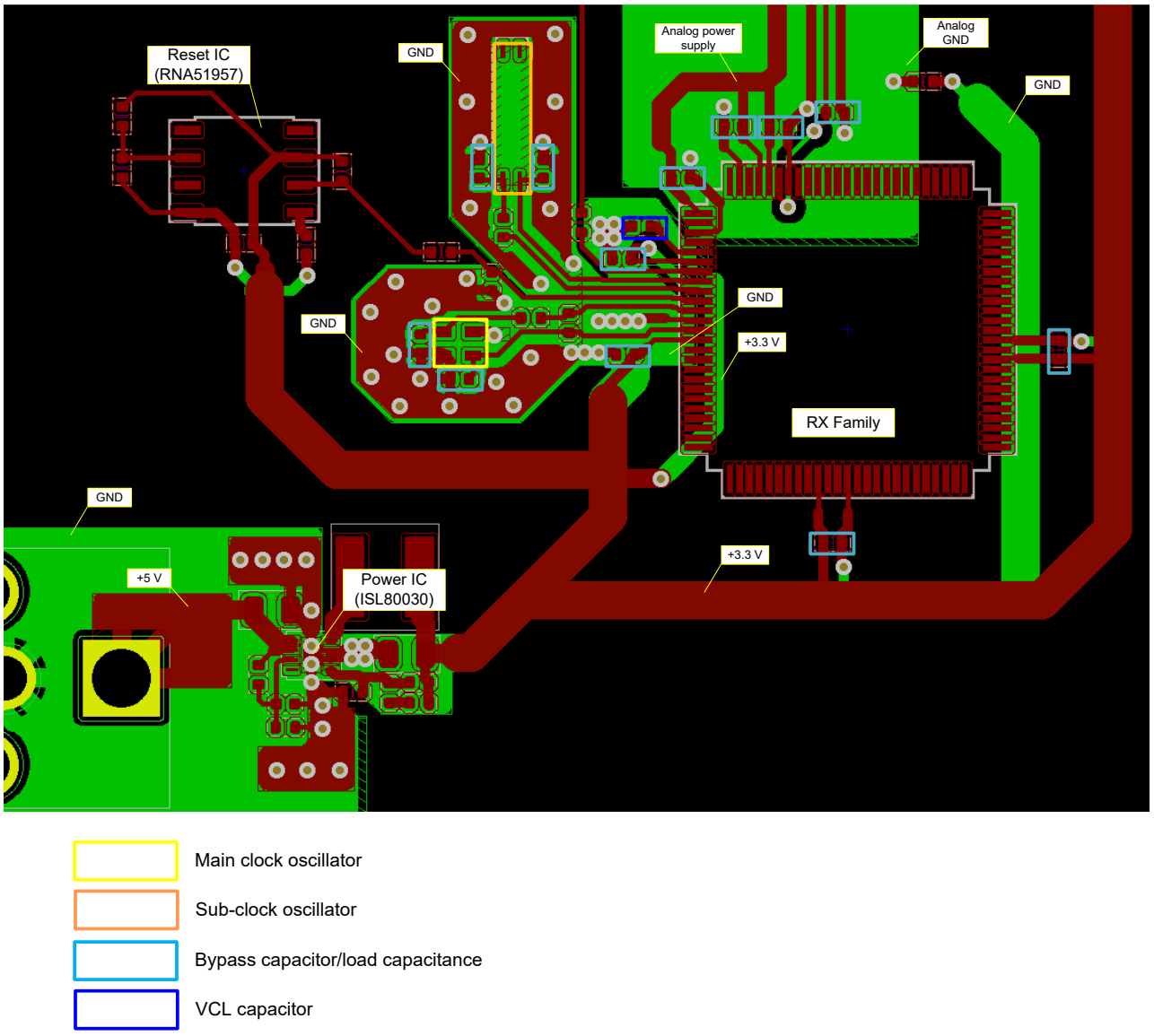


Figure 3.1 Example Board Wiring Pattern (Two-Layer Board)

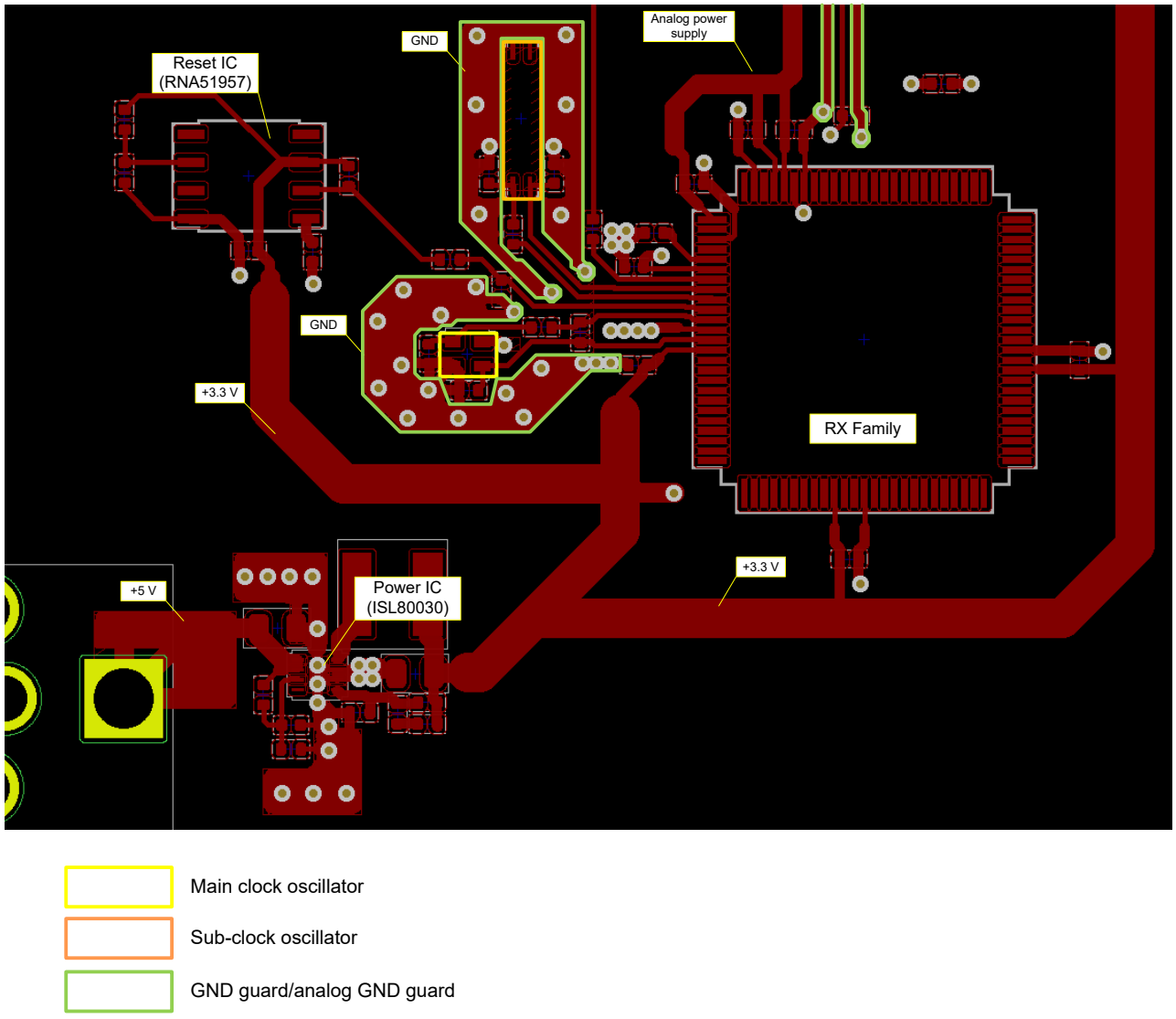


Figure 3.2 Example Board Wiring Pattern (First Layer Wiring Pattern)

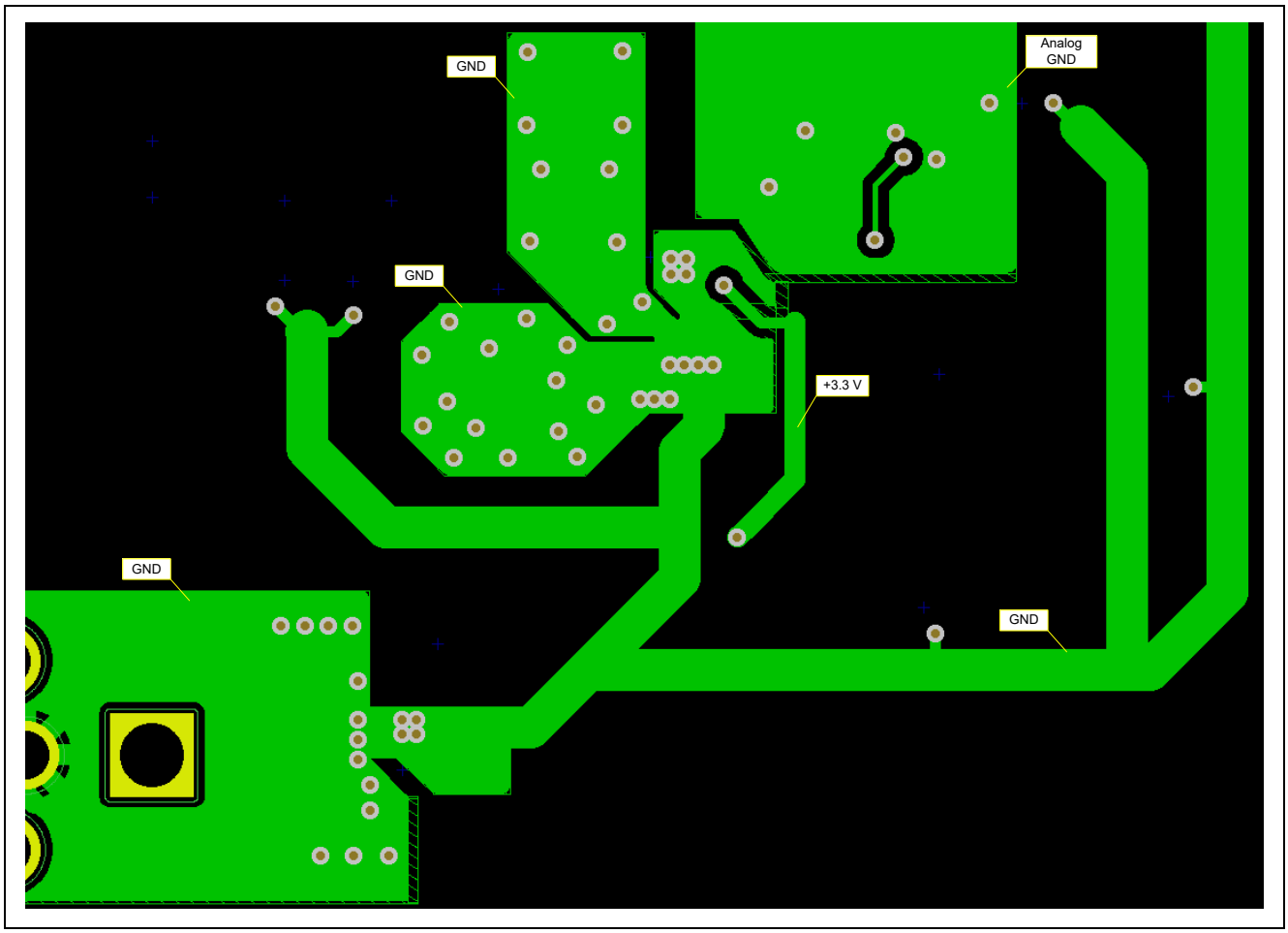


Figure 3.3 Example Board Wiring Pattern (Second Layer Wiring Pattern)

3.2 Example Four-Layer Board Wiring Pattern

Figure 3.4 shows an example four-layer board wiring pattern for an RX Family MCU, and Figure 3.5, Figure 3.6, Figure 3.7, and Figure 3.8 show the wiring patterns for each of the individual layers separately.

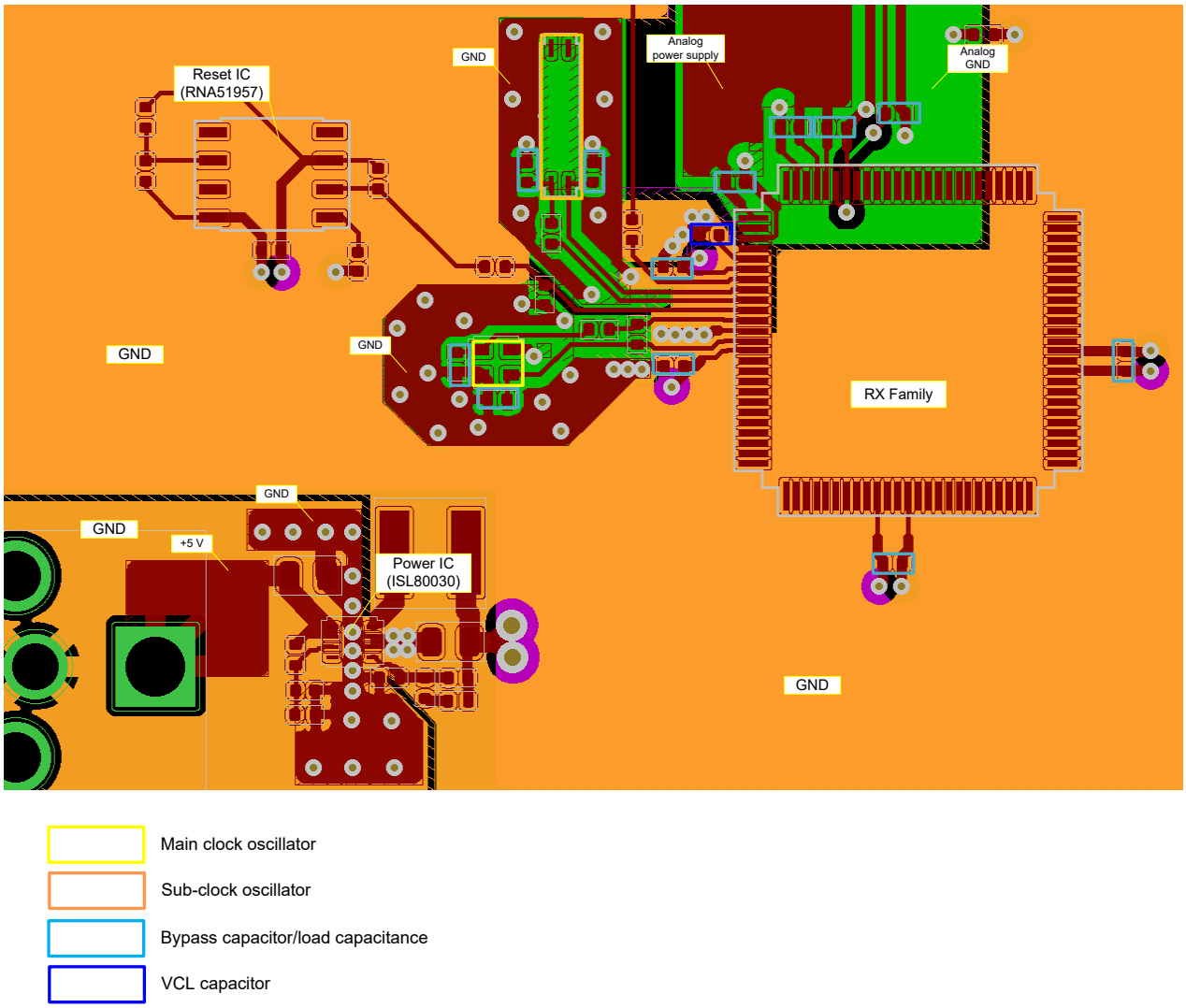


Figure 3.4 Example Board Wiring Pattern (Four-Layer Board)

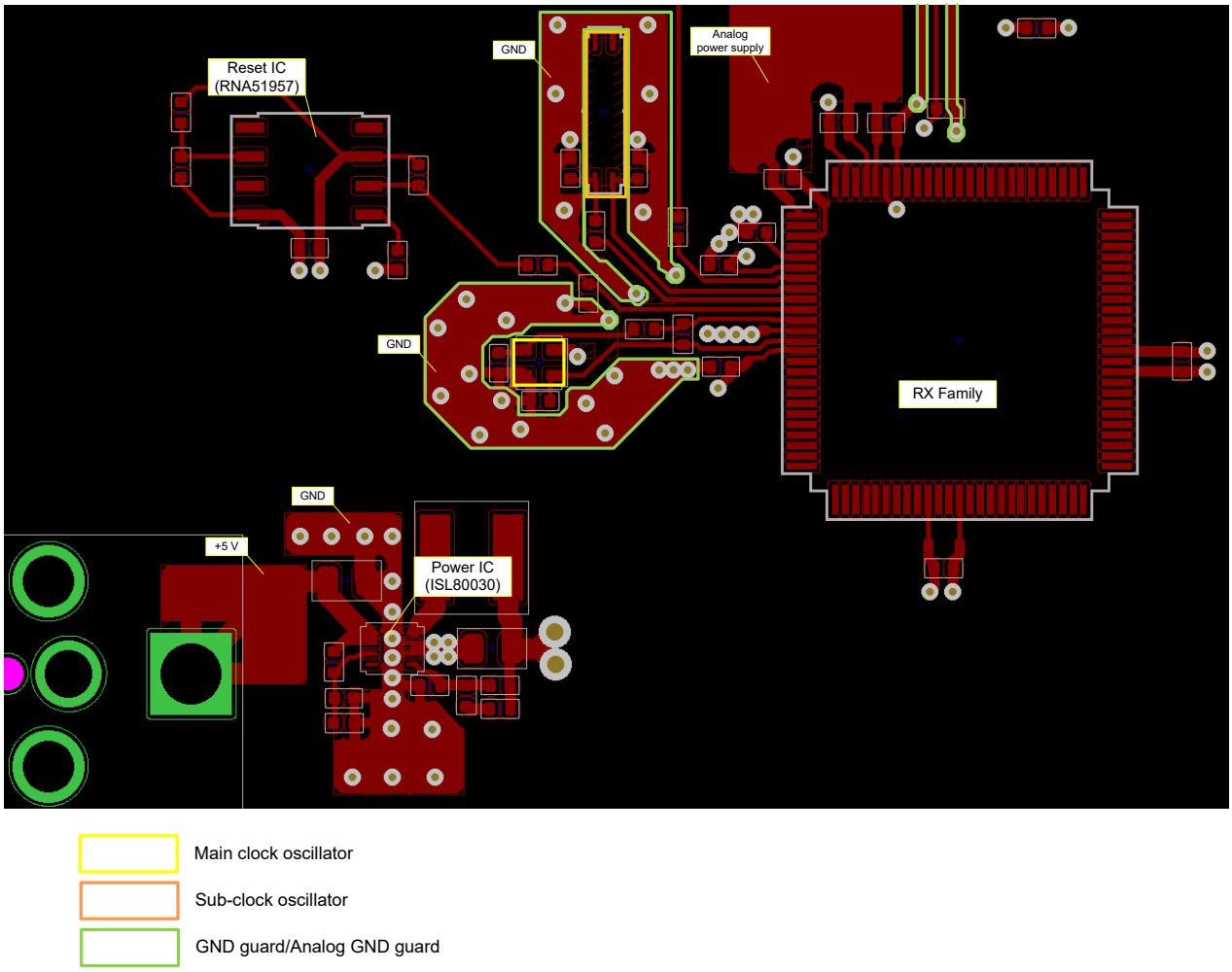


Figure 3.5 Example Board Wiring Pattern (First Layer Wiring Pattern)

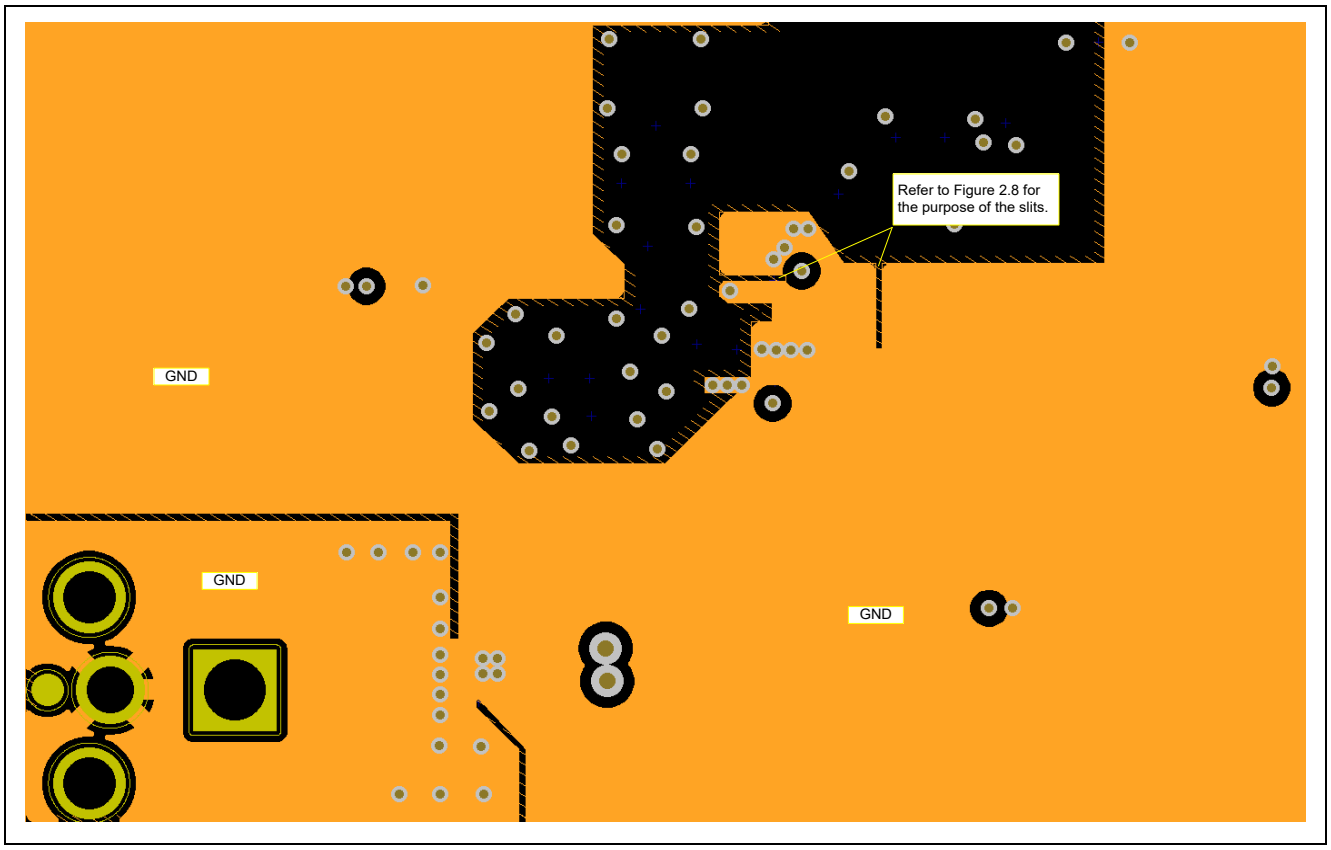


Figure 3.6 Example Board Wiring Pattern (Second Layer Wiring Pattern)

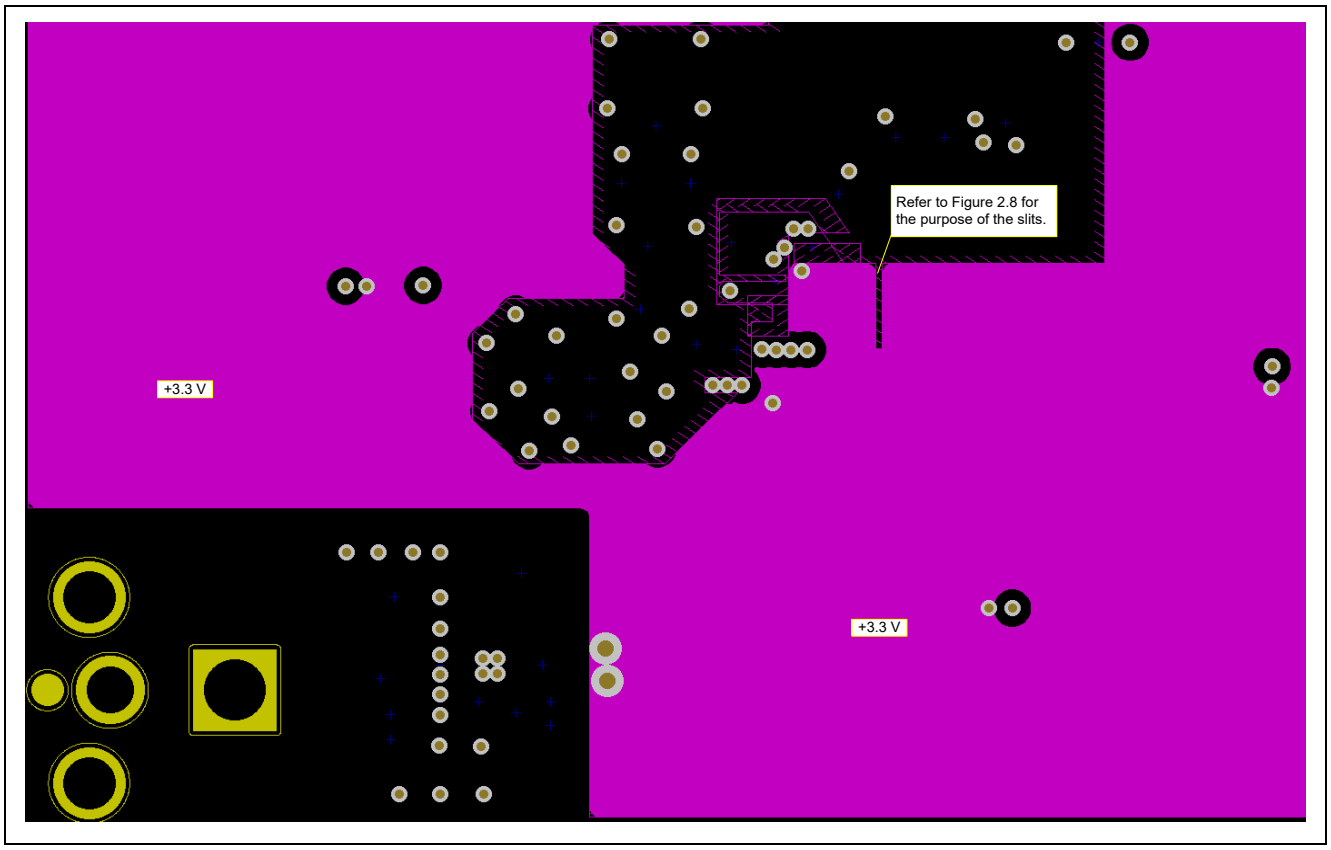


Figure 3.7 Example Board Wiring Pattern (Third Layer Wiring Pattern)

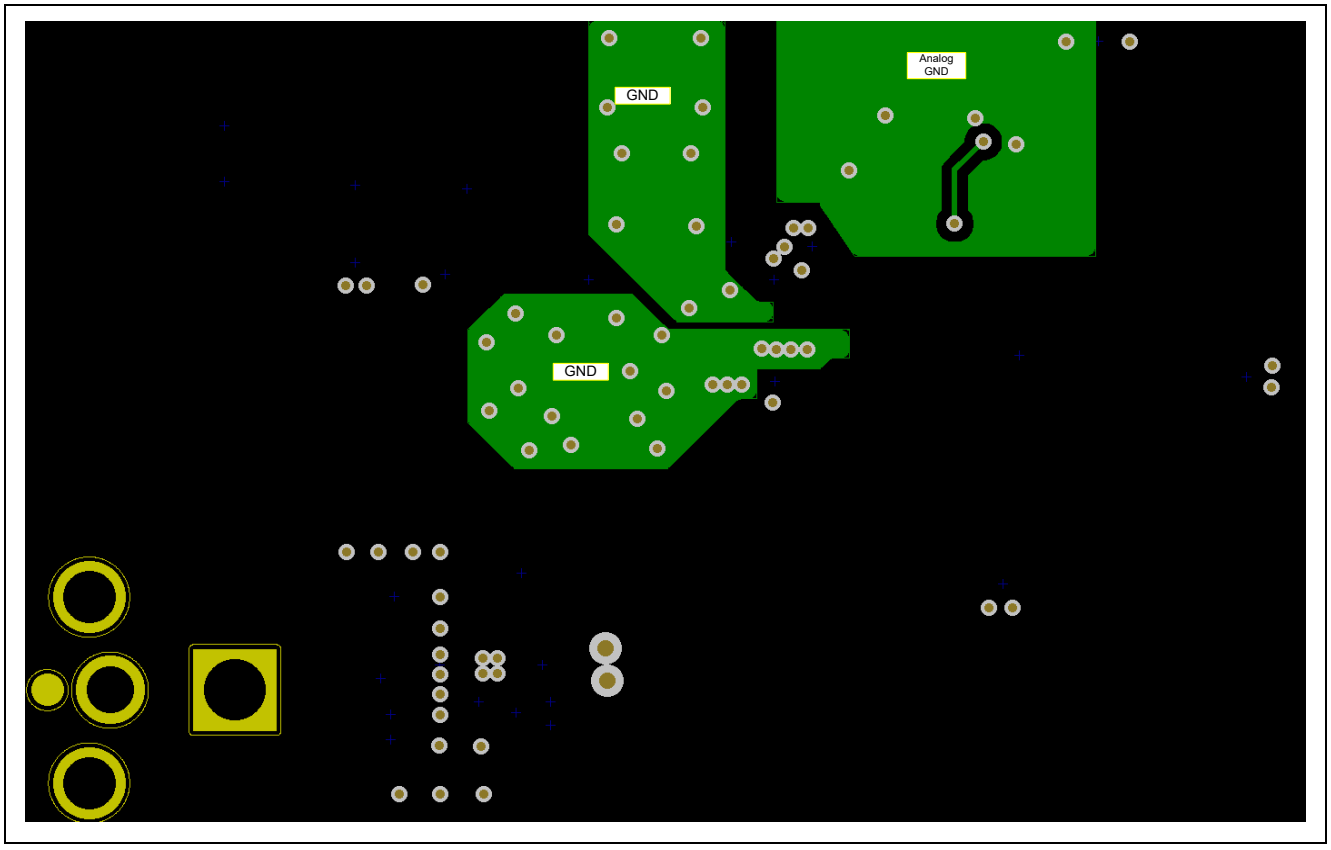


Figure 3.8 Example Board Wiring Pattern (Fourth Layer Wiring Pattern)

4. Reference Documents

- User's Manual: Hardware Catalog
- User's Manual: Hardware for each product group in the RX Family
  (The latest version for each device can be downloaded from the Renesas Electronics website.)
- RX610 Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0271EJ)
- RX62N Group, RX621 Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0269EJ)
- RX62T Group: Notes on Analog Power Supply Printed Circuit Board Patterns (R01AN0638EJ)
- RX and RA families: Design Guide for Main Clock Circuit and Sub-Clock Circuit (R01AN7202EJ)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 29, 2013	—	First edition issued
1.01	Sep. 26, 2014	5	1.2 VCL Pin description modified
		11	Figure 1.14 Pattern Example for the Analog Input Pin modified
		15	3. Reference Documents modified
1.10	Oct. 26, 2021	2	New Section 1 added (subsequent section and figure numbers changed accordingly)
		4	Section 1.2.1 deleted
		7	Section 2 items modified
			VCL capacitor wiring limitations modified
		10	Figure 2.5 note on rated capacitance of VCL capacitor added
		14, 16, 21	GND guard wiring width and spacing conditions added
		16	Figure 2.12 note on load capacitance and VSS pin coupling added
		24 to 30	Example single-layer board and multilayer board changed to example two-layer board and four-layer board
		31	Additions made to Reference Documents
1.11	Feb. 15, 2024	16, 31	Reference Documents updated

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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