RX Family

Example of Using the External Bus

Abstract

This application note describes the use of the external bus of the RX Family by an example of connecting the RX72M Group and SRAM using the separate bus interface.

Target Device

RX72M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Difference of Specifications of External Buses of RX Family

Table 1.1 shows the difference of specifications of external buses of the RX Family, comparing representative groups: the RX231 Group, the RX651 Group, RX65N Group, the RX660 Group, RX66N Group, RX66T Group, the RX671 Group, RX72M Group, the RX72N Group, and the RX72T Group.

Table 1.1 Difference of Specifications of External Buses of RX Family

Item	RX651 Group, RX65N Group, RX66N Group, RX72M Group, RX72N Group	RX671 Group	RX660 Group, RX66T Group, RX72T Group	RX231 Group
Data bus width	32 bits, 16 bits, 8 bits	16 bits, 8 bits		
CS area	8		4	
SDRAM controller	Equipped		Not equipped	
Bus clock	120 MHz (max.)		60 MHz (max.)	32 MHz (max.)

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F572MNDDBG (RX72M Group)
Operating frequencies	Main clock: 12 MHz PLL: 240 MHz (main clock divided by 1 and multiplied by 20) System clock (ICLK): 240 MHz (PLL divided by 1) Peripheral module clock A (PCLKA): 120 MHz (PLL divided by 2) Peripheral module clock B to D (PCLKB to PCLKD): 60 MHz (PLL divided by 4) Flash IF clock (FCLK): 60 MHz (PLL divided by 4) External bus clock (BCLK): 120 MHz (PLL divided by 2)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation e2 studio Version: 2022-10 (22.10.0)
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V3.04.00
	Compile options The default setting is used in the integrated development environment.
iodefine.h version	V1.00C
Endian	Little endian
Operating mode	On-chip ROM enabled expansion mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
SRAM	Infineon Technologies CY7C1061AV33-10ZXI (1 M words × 16 bits)

3. Specifications

In this application note, the SRAM is connected by the separate bus interface using the RX72M external bus to write, read, and verify data in 16-bit bus width.

After a reset, data is written in words to a 16-Mbit SRAM area which is an external address space. When all SRAM areas have been written, the written data are read.

If the read value matches the written value (verification succeeded), LED0 is turned on. If the values do not match (verification error), LED1 is turned on. If a bus error occurs, LED2 is turned on.

Table 3.1 shows the peripheral functions to be used and their applications, Table 3.2 shows the specification of the SRAM (CY7C1061AV33), and Figure 3.1 provides a block diagram.

Table 3.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Bus (external bus)	Connection to the SRAM
Interrupt controller	Bus error detection
I/O ports	Turn on LEDs

Table 3.2 Specification of the SRAM (CY7C1061AV33)

Peripheral Function	Application
Product	CY7C1061AV33-10ZXI
Organization	1 M words × 16 bits
Memory size	16 M bits
Access time	10 ns

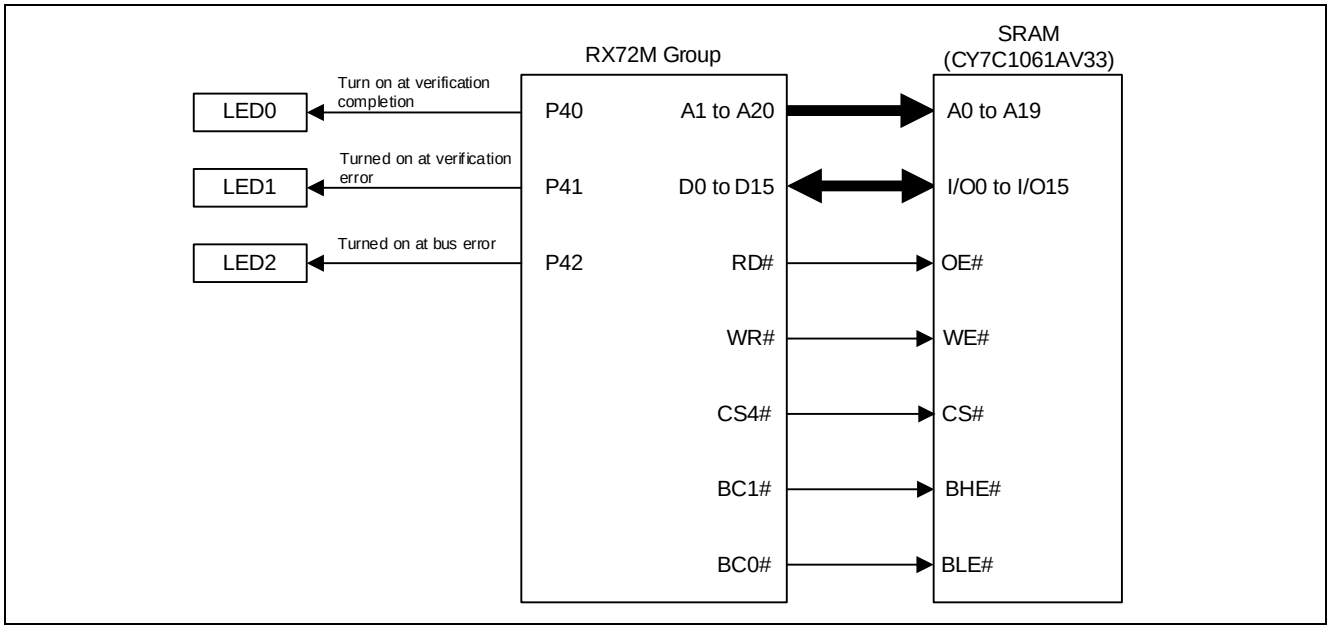


Figure 3.1 Block Diagram

4. Hardware

4.1 Hardware Configuration

In this application note, the SRAM is accessed by connecting with 16-bit data bus using the separate bus interface.

Figure 4.1 shows the Connection Example with 16-Bit Separate Bus.

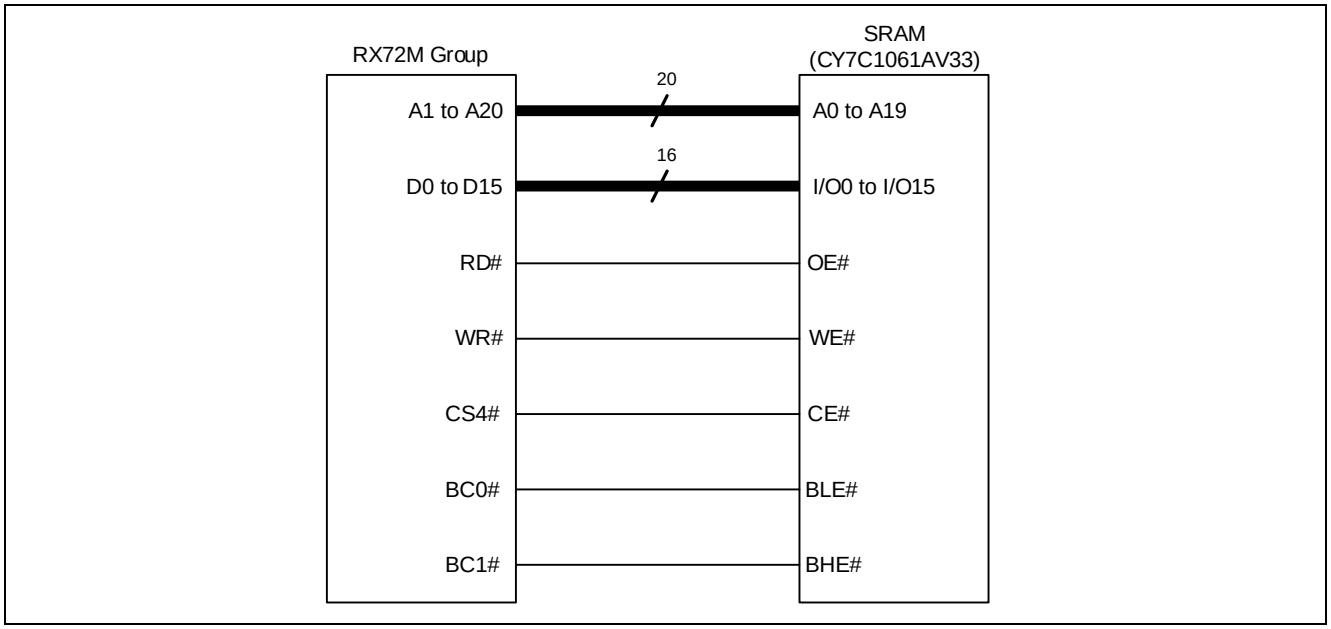


Figure 4.1 Connection Example with 16-Bit Separate Bus

4.2 Pins Used

Table 4.1 lists the pins that are used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P40	Output	LED0 output (Port output High: turned on, Low: turned off)
P41	Output	LED1 output (Port output High: turned on, Low: turned off)
P42	Output	LED2 output (Port output High: turned on, Low: turned off)
PA7 to PA1/A7 to A1	Output	Pins to output addresses
PB7 to PB0/A15 to A8	Output	Pins to output addresses
P94 to P90/A20 to A16	Output	Pins to output addresses
PD7 to PD0/D7 to D0	I/O	Data I/O pins
PE7 to PE0/D15 to D8	I/O	Data I/O pins
PA0/A0/BC0#	Output	Pin to output a strobe signal which indicates D7 to D0 are enabled
P51/BC1#	Output	Pin to output a strobe signal which indicates D15 to D8 are enabled
P52/RD#	Output	Pin to output a strobe signal which indicates read operation is in progress
P50/WR0#/WR#	Output	Pin to output a strobe signal which indicates write operation is in progress
P74/CS4#	Output	Pin to output the chip select signal for area 4 (CS4)

5. Software

After a reset, the width of the CS4 area of the external bus is set to 16-bit and on-chip ROM enabled expansion mode is selected.

The incremented data is written in the entire 2-Mbyte area from the start address of the CS4 area allocated in SRAM.

The written data is read from the start address of the CS4 area and verified with the incremented data. If all data in the SRAM match, LED0 is turned on.

If the data in SRAM and the data for verification do not match, LED1 is turned on.

If a bus error occurs, LED2 is turned on.

5.1 Operation Overview

16-bit data is written to and read from the address in the CS4 area.

The external bus controller controls read/write operations by control signals that are issued according to the configured timings.

The driving capability of external bus pins and signal control timings need to be specified taking in account the external bus clock cycle (approximately 8.33 ns in this application note), the AC characteristic of the SRAM, the impact on the signal path between the MCU and SRAM, and so on.

Table 5.1 shows the Wait Control Setting Cycles of the external bus in this example. High driving ability output is selected for external bus pins.

Table 5.1 Wait Control Setting Cycles

Wait Control Name	Symbol	Setting Cycles
Wait for CS assertion	CSON	0 cycles
Wait for write data output	WDON	1 cycle
Wait for WR assertion	WRON	1 cycle
Wait for normal write cycle	CSWWAIT	2 cycles
Extension cycle of write data output	WDOFF	1 cycle
Write-access CS extension cycle	CSWOFF	1 cycle
Wait for RD assertion	RDON	0 cycles
Wait for normal read cycle	CSRWAIT	3 cycles
Read-access CS extension cycle	CSROFF	1 cycle

5.1.1 SRAM Control Timing

Figure 5.1 shows the CY7C1061AV33 Control Timing for Read/Write Operations.

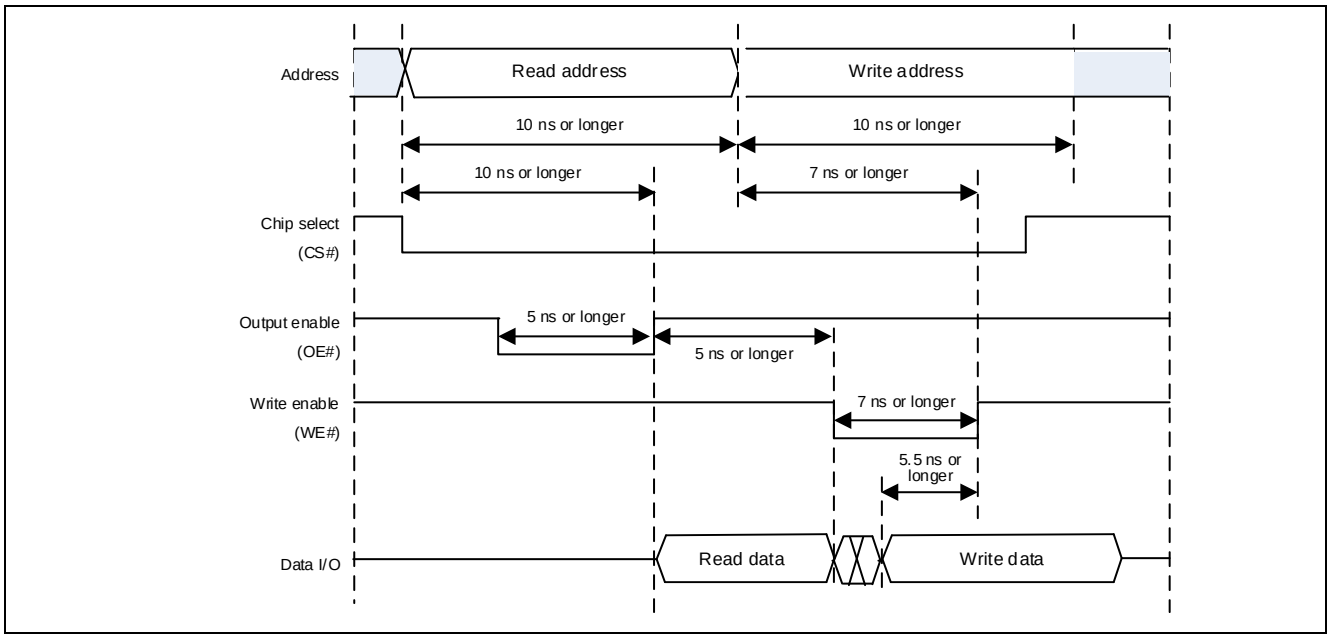


Figure 5.1 CY7C1061AV33 Control Timing for Read/Write Operations

5.1.2 Writing Data to the SRAM

Figure 5.2 shows Bus Timing for Normal Write in 1-Write Strobe Mode (m = 0 and 1) when writing data in SRAM.

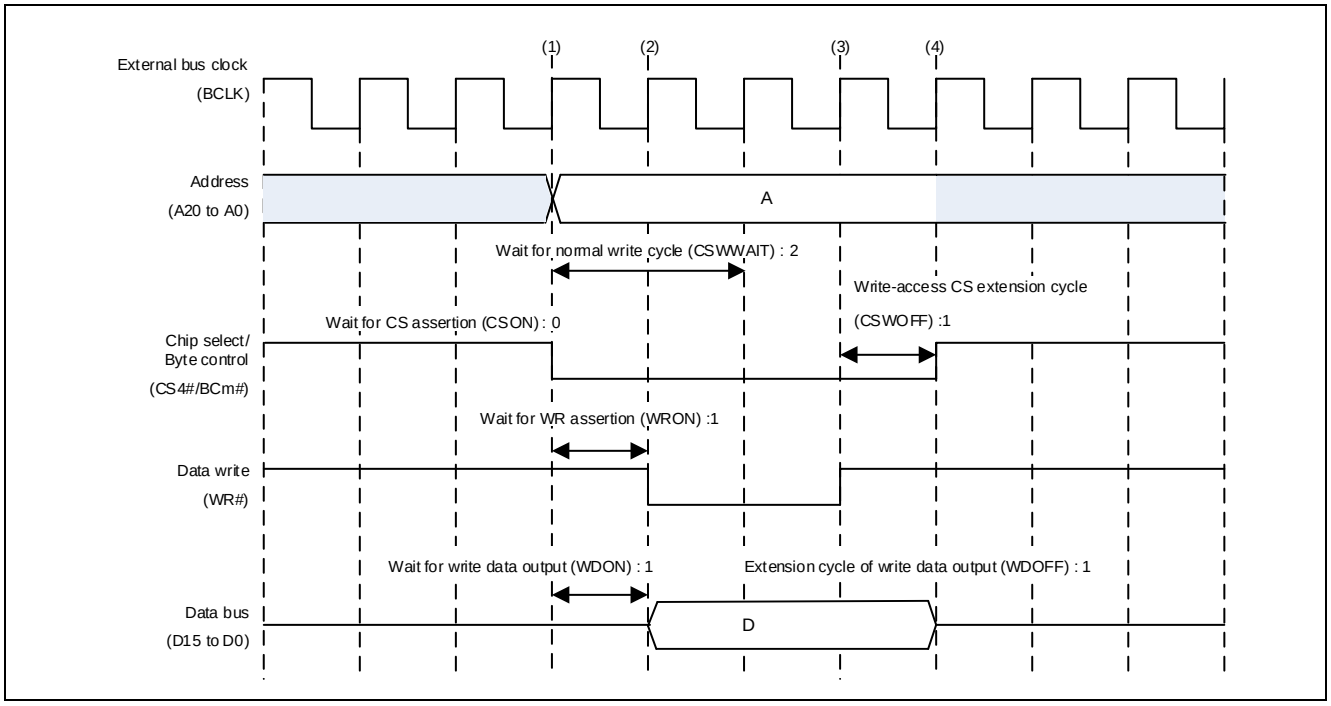


Figure 5.2 Bus Timing for Normal Write in 1-Write Strobe Mode (m = 0 and 1)

(1) Address output and CS assertion

When the write destination address for the data is output, the CS4# signal is asserted and normal write access is started.

(2) WR assertion and write data output

The WR# signal is asserted and the write data is output at the same time.

(3) WR negation

The WR# signal is negated at the next cycle of the cycle which the wait period for normal write cycle is completed.

(4) CS negation and completion of write data output extension

The CS4# signal is negated and the extension cycle of write data output is completed at the same time, and normal write access is completed.

5.1.3 Reading Data from the SRAM

Figure 5.3 shows Bus Timing for Normal Read (m = 0 and 1) when reading data from SRAM.

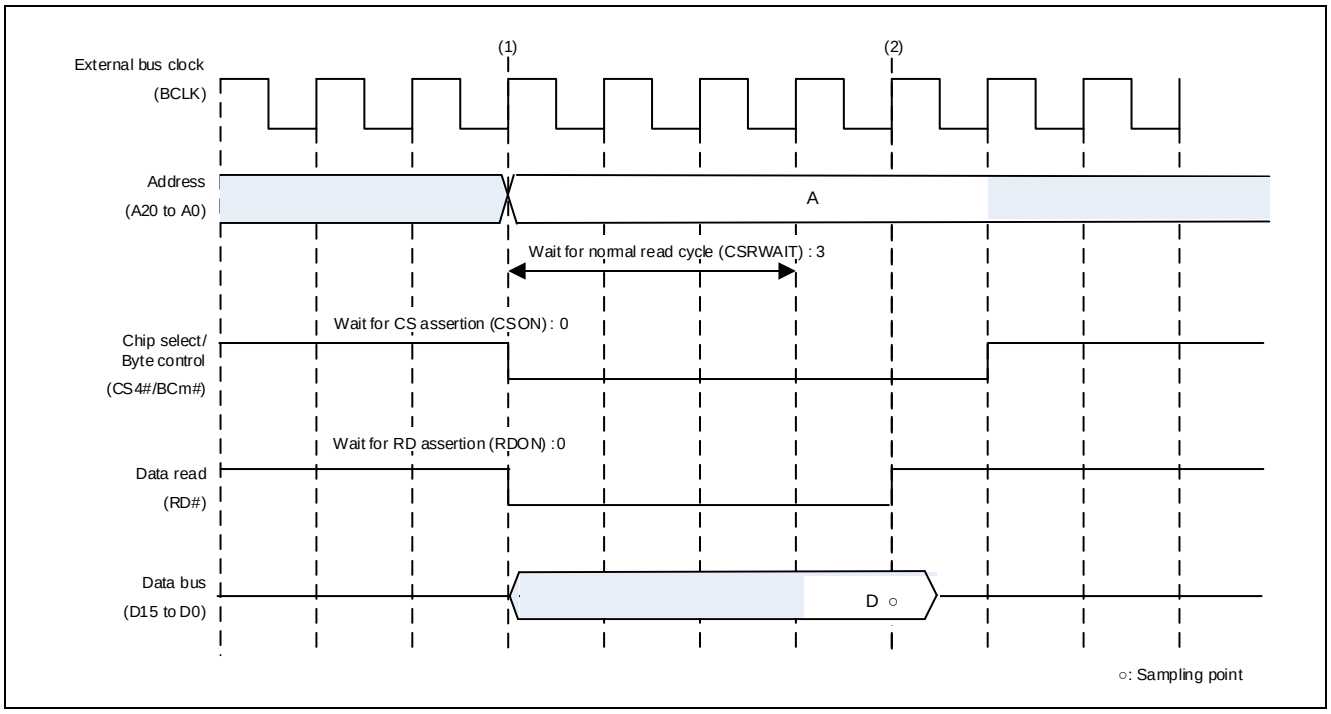


Figure 5.3 Bus Timing for Normal Read (m = 0 and 1)

(1) Address output, CS assertion, and RD assertion

When the read source address for the data is output, the CS4# and RD# signals are asserted and normal read access is started.

(2) Read data sampling and the completion of the process

The RD# signal is negated at the next cycle of the cycle which the wait period for normal read cycle is completed, and the read data is sampled. Also, the CS4# signal is negated and normal read access is completed.

5.2 Code Generation

This sample code sets the clock, peripheral functions (bus controller and port output), and pin allocation using the Smart Configurator. Settings are shown below.

5.2.1 Clock Setting

Table 5.2 lists the clock settings.

Table 5.2 Clock Settings

Item		Setting
Main clock	Oscillation source	Oscillator
	Frequency (MHz)	12
PLL circuit	Multiplication ratio	×20
SCKCR (ICLK)		×1
SCKCR (PCKA[3:0])		×1/2
SCKCR (PCKB[3:0])		×1/4
SCKCR (PCKC[3:0])		×1/4
SCKCR (PCKD[3:0])		×1/4
SCKCR (FCK[3:0])		×1/4
SCKCR (BCK[3:0])		×1/2
BCKCR (BCLKDIV)		Enabled
		×1/2

5.2.2 Bus Controller Settings

Table 5.3 and Table 5.4 show the settings of the bus controller (Config_BSC).

Table 5.3 Bus Controller Settings (General Settings)

Item	Setting
On-chip ROM setting	Enabled
External bus area setting	CS4 used (0400 0000h to 04FF FFFFh)
CS external bus controller setting	Strobe signal is used (WR1#/BC1# pin).
Bus priority order setting	Fixed priority order
CS recovery cycle insertion permission for separate bus	Not set
CS recovery cycle insertion permission for address/data multiplex bus	Not set
Pins to output addresses	A0 to A20
Bus error monitoring setting	Detection of invalid address access
	Detection of timeout
	Enabling bus error interrupt
	Priority order level 1

Table 5.4 Bus Controller Settings (CS4)

Item		Setting
Area setting	Bus width	16 bits
	Endian	The endian is the same as that of operating mode.
	Interface	Separate bus
	Write access mode	1-write strobe mode
	Page read access	Disabled
	Page write access	Disabled
	External wait	Disabled
Bus timing setting	Read recovery period	0
	Write recovery period	0
	Wait for normal read cycle	3
	Wait for normal write cycle	2
	Read-access CS extension cycle	1
	Write-access CS extension cycle	1
	Write data output delay cycle	1
	Wait for RD assertion	0
	Wait for WR assertion	1
	Wait for write data output	1
	Wait for CS assertion	0

5.2.3 Port Setting

Table 5.5 shows port (Config_PORT) settings.

Table 5.5 Port Settings

Item		Setting
PORT4	P40 to P42	Output
PORT5	P50 to P53	High driving ability output
PORT7	P74	High driving ability output
PORT9	P90 to P94	High driving ability output
PORTA	PA0 to PA7	High driving ability output
PORTB	PB0 to PB7	High driving ability output
PORTD	PD0 to PD7	High driving ability output
PORTE	PE0 to PE7	High driving ability output

5.2.4 Pin Allocation

Table 5.6 shows the pin allocation.

Table 5.6 Pin Allocation

Hardware resource	Function	Pin Allocation
Clock pulse generator	BCLK	P53/BCLK
	EXTAL	P36/EXTAL
	XTAL	P37/XTAL
Bus control	A0 to A7	PA0 to PA7
	A8 to A15	PB0 to PB7
	A16 to A20	P90 to P94
	BC0#	PA0
	BC1#	P51
	CS4#	P74
	BCLK	P53
	D0 to D7	PD0 to PD7
	D8 to D15	PE0 to PE7
	RD#	P52
	WR#	P50
IO port	P40	P40
	P41	P41
	P42	P42

5.3 File Composition

Table 5.7 shows File Used for Sample Code, and Table 5.8 shows Files Used for Adding Codes to Code Generation File.

Table 5.7 File Used for Sample Code

File Name	Outline
r01an6594_rx72m_bus_main.c	Main processing

Table 5.8 Files Used for Adding Codes to Code Generation File

File Name	Changed content
Config_PORT.h	Macro definition for LED control
Config_BSC_user.c	Adding an error process to the BUSERR interrupt service routine

5.4 Constants

Table 5.9 lists the Constants Used in Sample Code.

Table 5.9 Constants Used in Sample Code

Constant Name	Setting Value	Contents	Definition file
SRAM_TOP	(void*)(0x04000000)	Start address of the SRAM area	r01an6594_rx72m_bus_main.c
SRAM_END	(void*)(0x04200000)	End address of the SRAM area + 1	
LED0_REG_PODR	PORT4.PODR.BIT.B0	Output data store bit for LED0	Config_PORT.h
LED1_REG_PODR	PORT4.PODR.BIT.B1	Output data store bit for LED1	
LED2_REG_PODR	PORT4.PODR.BIT.B2	Output data store bit for LED2	
LED_ON	1	LED output data: turned on	
LED_OFF	0	LED output data: turned off	

5.5 Variables

Table 5.10 lists the static Variables.

Table 5.10 static Variables

Variable Name	Type	Contents	Function Used
sp_sram_adr	volatile static uint16_t *	SRAM access address	main
s_sram_data	static uint16_t	Write data	
s_sram_cmp_data	static uint16_t	Verification data	

5.6 Functions

Table 5.11 shows the functions that were created and added to the code generation file.

Table 5.11 List of functions

Function Name	Outline	Definition file
main	Main processing	r01an6594_rx72m_bus_main.c
sram_verify_err	SRAM verification error processing	
r_Config_BSC_buserr_interrupt	Bus error interrupt handling	Config_BSC_user.c

5.7 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	This function enables the bus error interrupt, and then makes SRAM writing, SRAM reading, and SRAM verification.
Arguments	None
Return Value	None

sram_verify_err	
Outline	SRAM verification error processing
Header	None
Declaration	static void sram_verify_err(void)
Description	When an SRAM verification error occurs, this function turns on LED1 and performs endless loop processing.
Arguments	None
Return Value	None

r_Config_BSC_buserr_interrupt	
Outline	Bus error interrupt handler
Header	None
Declaration	void r_Config_BSC_buserr_interrupt(void)
Description	When a bus error occurs, this function turns on LED2 and performs endless loop processing.
Arguments	None
Return Value	None

5.8 Flowcharts

5.8.1 Main Processing

Figure 5.4 shows the flow chart of the main processing.

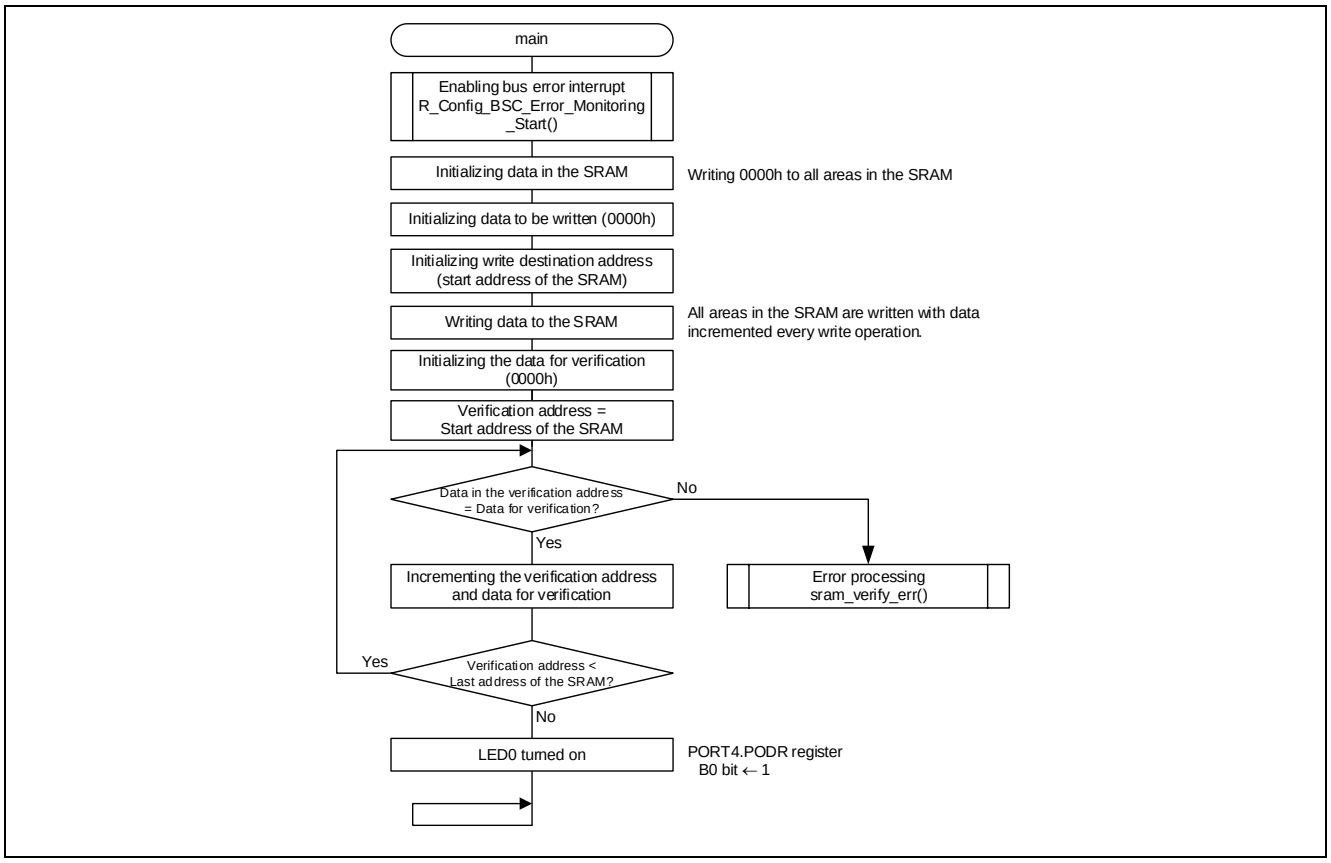


Figure 5.4 Main Processing

5.8.2 SRAM Verification Error Processing

Figure 5.5 shows the SRAM Verification Error Processing.

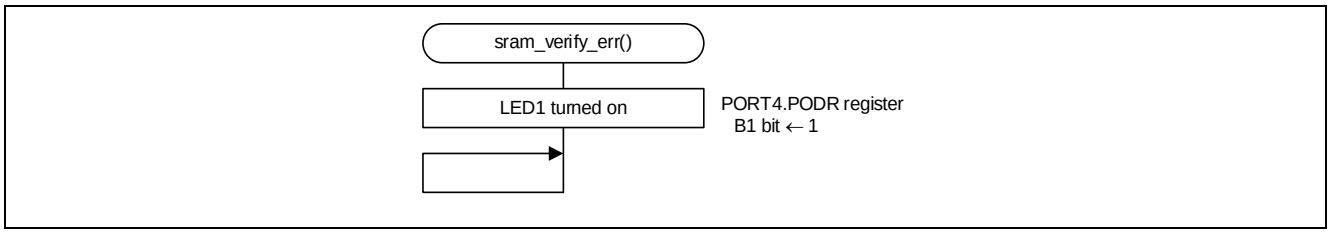


Figure 5.5 SRAM Verification Error Processing

5.8.3 SRM Bus Error Handling

Figure 5.6 shows the Bus Error Interrupt Handling.

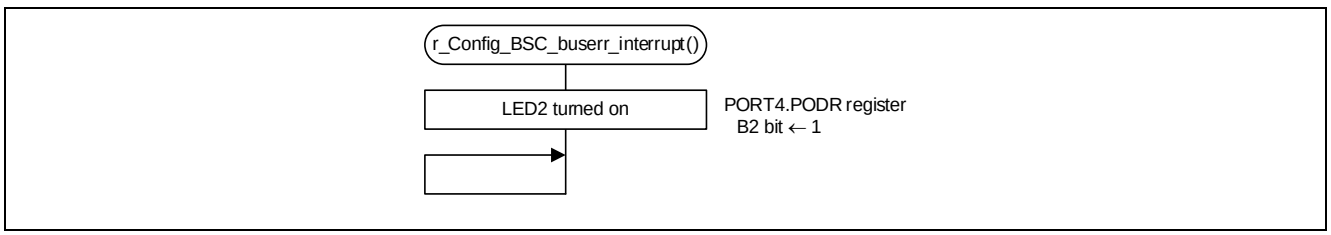


Figure 5.6 Bus Error Interrupt Handling

6. Application Example

6.1 Selecting 1-Write Strobe Mode or Byte Strobe Mode

For the RX Family, "1-write strobe mode" means an operating mode in which there is one write signal and the effective byte position is specified by byte control signals. On the contrary, "byte strobe mode" means an operating mode in which the bus control signal is not used and multiple write signals are used.

Either of the strobe modes is used according to the specification of the connected device.

The 1-write strobe mode is selected for a device whose bus width is 16 bits and that are controlled by one write signal (WR#) and byte control signals (BHE# and BLE#). The SRAM used in this example is a device of this type.

The byte strobe mode is selected for a device that does not have a byte control signal due to cases such as a bus width of 8 bits.

6.2 Inserting the Recovery Cycle

The external bus may not be accessed continuously due to the influence of the circuit connected to the SRAM. In this case, inserting the recovery cycle allows the external bus to be accessed continuously. Cycles to be inserted as the recovery cycle can be specified for each set of read/write operations. Refer to the section “Insertion of Recovery Cycles of Buses” in the User’s Manual: Hardware for details.

Figure 6.1 shows Operation Example of the Recovery Cycle with Separate Bus Interface (m = 0 and 1).

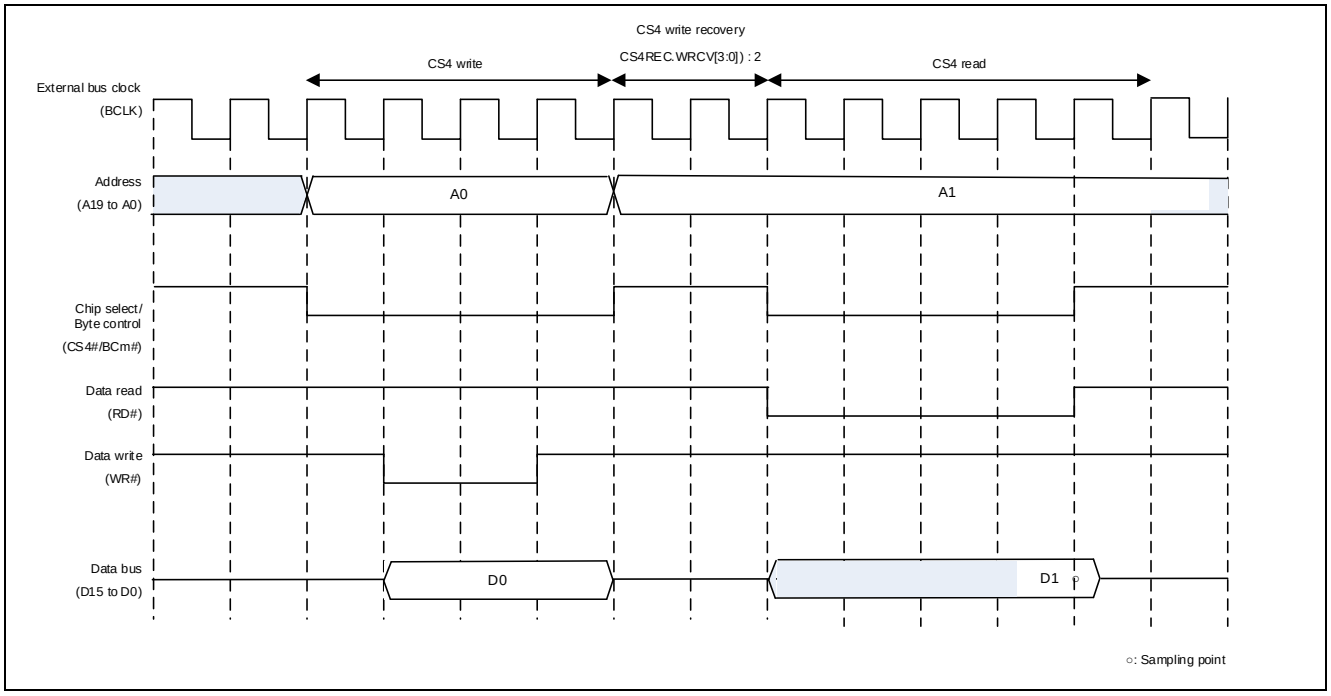
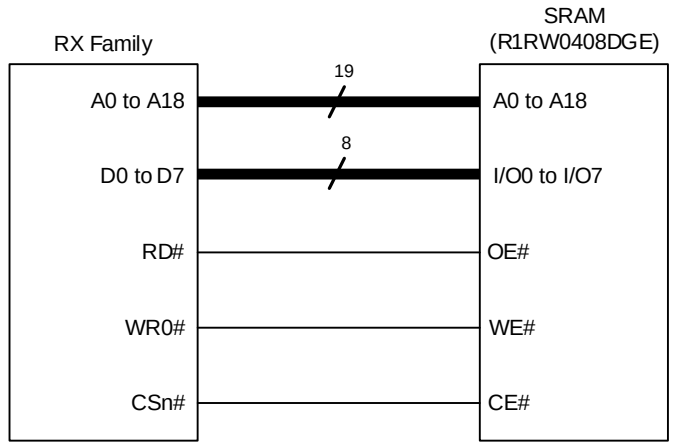


Figure 6.1 Operation Example of the Recovery Cycle with Separate Bus Interface (m = 0 and 1)

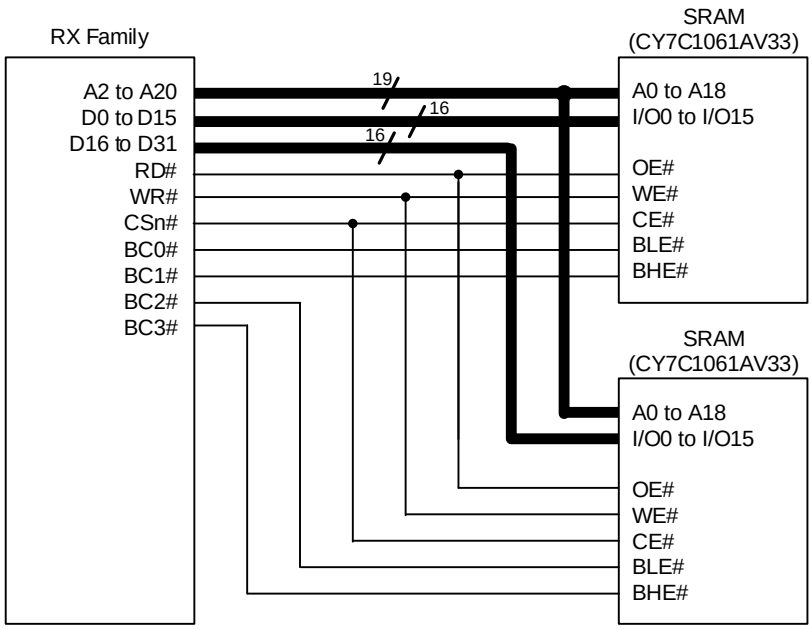
6.3 Other Connection Examples

Figure 6.2 shows a Connection Example with 8-Bit Separate Bus, and Figure 6.3 shows a Connection Example with 32-Bit Separate Bus.



Note: n = 0 to 7

Figure 6.2 Connection Example with 8-Bit Separate Bus



Note: n = 0 to 7

Figure 6.3 Connection Example with 32-Bit Separate Bus

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User’s Manual: Hardware
RX72M Group User’s Manual: Hardware (01UH0804EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

User’s Manual: Development Tools
RX Family CC-RX Compiler User's Manual (R20UT3248EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 10, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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