RX Family

Example of Operation Near PWM 0% and 100% Duty Cycles Using MTU3 or GPTW

Introduction

This application note describes how to perform operation using the MTU3 or GPTW with complementary PWM output near 0% and 100% duty cycles.

RX66T Group microcontrollers (MCUs) are equipped with the multi-function timer pulse unit 3 (MTU3) and the general-purpose PWM timer (GPTW) capable of generating PWM (pulse-width modulation) waveforms. This application note applies to RX Family devices equipped with the MTU3 and GPTW.

When using this application note with Renesas MCUs other than the RX66T Group, careful evaluation is recommended after making modifications to accommodate the target MCU.

Target Devices

RX Family devices equipped with the MTU3 and GPTW

Operation Confirmation Devices

RX66T Group

Multi-function timer pulse unit 3 is referred to as “the MTU” throughout this document.

Contents

1. Differences in Complementary PWM Using MTU and GPTW

Differences in the complementary PWM output when using the MTU and GPTW are summarized below.

Table 1.1 Complementary PWM Output Functionality

Item		MTU	GPTW
Channel		MTU3-MTU4, MTU6-MTU7	GPTn (n = 0 to 9)
Modes	Transfer at crest	Complementary PWM mode 1 (16-bit)	—
	Transfer at trough	Complementary PWM mode 2 (16-bit)	Triangle-wave PWM mode 1 (32-bit) Triangle-wave PWM mode 3 (64-bit)
	Transfer at crest and trough	Complementary PWM mode 3 (16-bit)	Triangle-wave PWM mode 2 (32-bit)
Output pins		• MTU3-MTU4 MTIOC3B: PWM output pin 1 (positive phase) MTIOC3D: PWM output pin 1 (negative phase) MTIOC4A: PWM output pin 2 (positive phase) MTIOC4C: PWM output pin 2 (negative phase) MTIOC4B: PWM output pin 3 (positive phase) MTIOC4D: PWM output pin 3 (negative phase) • MTU6-MTU7 MTIOC6B: PWM output pin 4 (positive phase) MTIOC6D: PWM output pin 4 (negative phase) MTIOC7A: PWM output pin 5 (positive phase) MTIOC7C: PWM output pin 5 (negative phase) MTIOC7B: PWM output pin 6 (positive phase) MTIOC7D: PWM output pin 6 (negative phase)	GTIOCnA (positive phase) GTIOCnB (negative phase)

Refer to 4.6, Triangle-Wave PWM Mode 1, 4.7, Triangle-Wave PWM Mode 2, and 4.8, Triangle-Wave PWM Mode 3, in the application note RX Family: PWM Output Methods Using MTU3/GPTW for instructions on producing multi-phase output using the GPTW.

Refer to 1.2, Buffer Functions, in the application note RX Family: PWM Output Methods Using MTU3/GPTW, for the differences in the buffer functions.

Refer to 1.4, Automatic Dead Time Setting Function, in the application note RX Family: PWM Output Methods Using MTU3/GPTW for the differences in the automatic dead time setting functions.

1.1 Complementary PWM Mode Using MTU and GPTW and Operation Examples

1.1.1 Complementary PWM Mode Using MTU and Operation Examples

(1) Complementary PWM Mode Using MTU

In complementary PWM mode using the MTU, three counters, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB), perform up or down count operation, and compare, buffer, and temporary registers are used to control the duty cycle of the PWM output.

(2) Dead Time

The dead time in complementary PWM mode is set in the timer dead time data registers (TDDRA and TDDRB). The setting value of TDDRA (TDDRB) is used as the start value of counter MTU3.TCNT (MTU6.TCNT), and the no-overlap duration (dead time) of MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) is generated automatically.

(3) Complementary PWM Mode Operation Example

Figure 1.1 shows an operation example of the counters (MTU3.TCNT and MTU4.TCNT), compare register (MTU3.TGRB), buffer register (MTU3.TGRD), temporary register (TEMP1A), and pins (MTIOC3B and MTIOC3D) in complementary PWM mode 3.

The elements in Figure 1.1 and the MTU-related figures on subsequent pages are defined as follows.

- Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
- Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
- Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
- TCDRA: Register value setting upper limit value of MTU4.TCNT
- TDDRA: Dead time value
- Ta: Interval other than Tb1 interval and Tb2 interval
- Tb1: Interval during which crest interval and MTU3.TCNT counter value is TCDRA to MTU3.TGRA
- Tb2: Interval during which trough interval and MTU4.TCNT counter value is TDDRA to 0000h
- Solid black line and solid green line: MTU3.TCNT and MTU4.TCNT counter value changes
- Yellow shaded area: Dead time

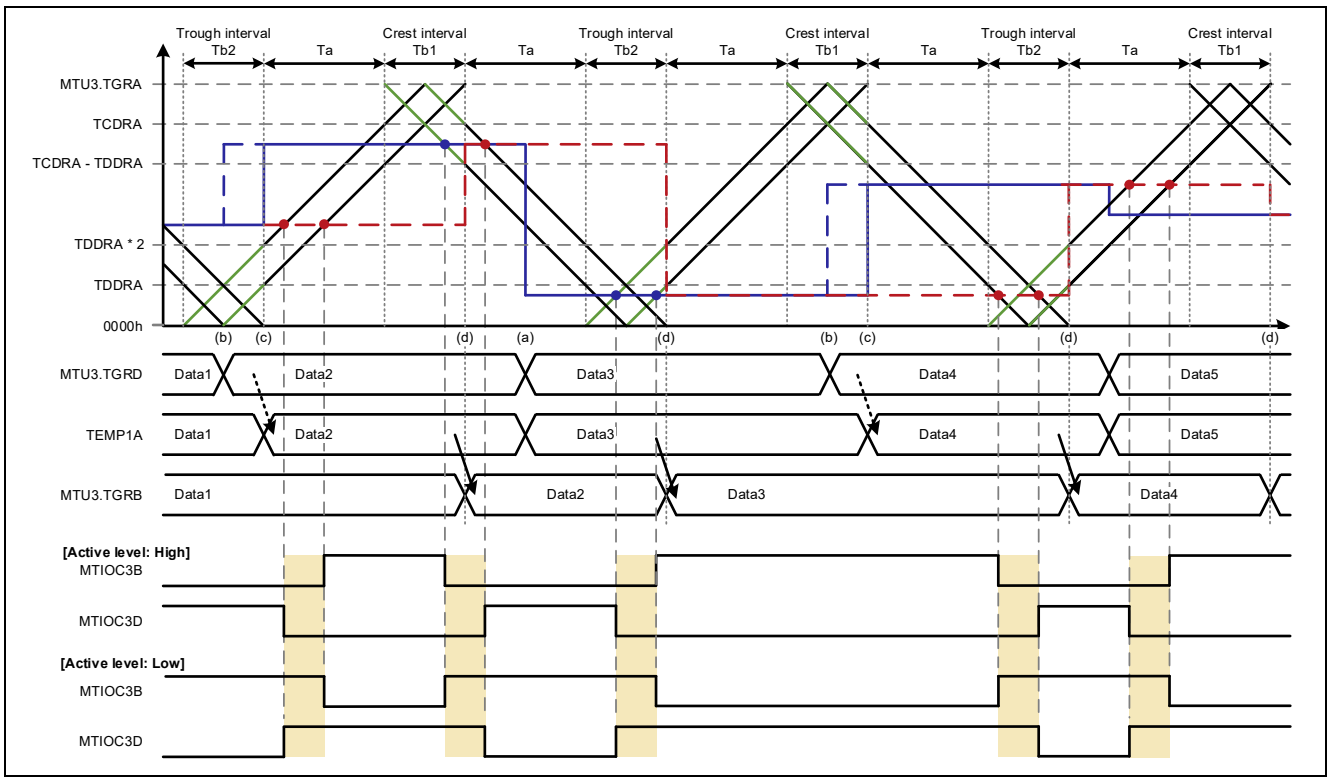


Figure 1.1 Complementary PWM Mode 3 Operation Example

In complementary PWM operation the buffer register is used when updating the data in the compare register. Updated data can be written to the buffer register at any time. There are also temporary registers between the compare register and buffer register.

Data written to the buffer register in the Ta interval is transferred immediately to the temporary register (Figure 1.1 (a)). Data written to the buffer register in the Tb1 and Tb2 intervals is not transferred to the temporary register (Figure 1.1 (b)). Data written to the buffer register during these intervals is transferred to the temporary register after the Tb1 (or Tb2) interval finishes (Figure 1.1 (c)). The timing of transfers from the temporary register to the compare register can be selected by the MD[3:0] bits in timer mode register 1 (TMDR1). When the Tb interval (Tb2 in the case of transfer at trough) in the timing selected by the MD[3:0] bits finishes, data is transferred from the temporary register to the compare register (Figure 1.1 (d)).

The MTU-related figures on subsequent pages are designated “overwrite in Tb interval” to indicate that the buffer register is overwritten during the Tb interval or “overwrite in Ta interval” to indicate that the buffer register is overwritten during the Ta interval.

The switching timing of the output levels of the phases is generated by compare matching of MTU3.TCNT and MTU4.TCNT, represented by the solid black and solid green lines in Figure 1.1, the compare register, represented by the dashed red line, and the temporary register, represented by the solid blue line.

The counter value represented by the solid black line in Figure 1.1 is compared with the compare register, represented by the dashed red line. Compare match points with the compare register are represented by red dots. The counter value represented by the solid green line in Figure 1.1 is compared with the temporary register, represented by the solid blue line. Compare match points with the temporary register are represented by blue dots. Comparisons with both the compare register and the temporary register take place during the Tb interval. The combination of these two compare match operations produces changes in the output waveform.

For details of the MTU's complementary PWM mode, refer to 22.3.8, Complementary PWM Mode, in RX66T Group User's Manual: Hardware and the application note RX Family: PWM Output Methods Using MTU3/GPTW.

1.1.2 GPTW Triangle-Wave PWM Modes 1, 2, and 3 and Operation Examples

(1) GPTW Triangle-Wave PWM Modes 1, 2, and 3

GPTW triangle-wave PWM modes 1, 2, and 3 enable output of PWM waveforms on the GTIOCnA and GTIOCnB (n = 0 to 9) pins by means of compare match operation between the GTCNT counter and the compare registers (GTCCRA and GTCCRB). A buffer register GTCCRm (m = C to F) can be used by configuring the mode and settings.

Triangle-wave PWM mode 3 also uses a temporary register (temporary register A or B). For details, refer to (5) Triangle-Wave PWM Mode 3 (Trough, 64-Bit Transfer) under 24.3.3, PWM Output Operating Modes, in RX66T Group User's Manual: Hardware.

(2) Dead Time

On the GPTW dead time is generated in either or two ways: by compare match operation using the automatic dead time setting function or by configuring the pin output duty setting bits.

The automatic dead time setting function can set the value of the GTCCRB register automatically by generating a compare match value for the negative phase waveform with dead time from the compare match value for the positive phase waveform (GTCCRA register value) and the dead time value (GTDVU or GTDVD register value), based on the setting of the dead time control register (GTDTCR)

However, dead time errors are generated based on the setting value of the GTCCRA register. When a dead time error occurs, the points where the positive phase and negative phase waveforms change are adjusted, as shown in Table 1.2, so that waveforms continue to be generated automatically with sufficient dead time. The adjusted negative phase waveform change point is set in the GTCCRB register automatically, but the adjusted positive phase waveform change point is not automatically set in the GTCCRA register. For details, refer to 24.3.4, Automatic Dead Time Setting Function, in RX66T Group User's Manual: Hardware.

Table 1.2 Change Point Adjustment when Dead Time Errors Occur

Waveform Mode	Count Direction	Dead Time Error Condition	Corrected Positive Phase W aveform Change Point	Corrected Negative Phase Waveform Change Point
Triangle-wave PWM modes 1, 2, and 3	Up-counting	GTCCRA – GTDTU ≤ 0	GTDVU + 1	1
	Down-counting	GTCCRA – GTDTU < 0	GTDVU	0

(3) Triangle-Wave PWM Mode Operation Example

Figure 1.2 shows an operation example of the GTCNT counter, compare registers (GTCCRA and GTCCRB), buffer registers (GTCCRC and GTCCRE), and pins (GTIOC0A and GTIOC0B) in triangle-wave PWM mode 2.

The elements in Figure 1.2 and the GPTW-related figures on subsequent pages are defined as follows.

- Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
- Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
- Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
- Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
  Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
- Solid green line: Positive phase waveform change points when dead time errors occur while using the automatic dead time setting function
- Yellow shaded area: Dead time

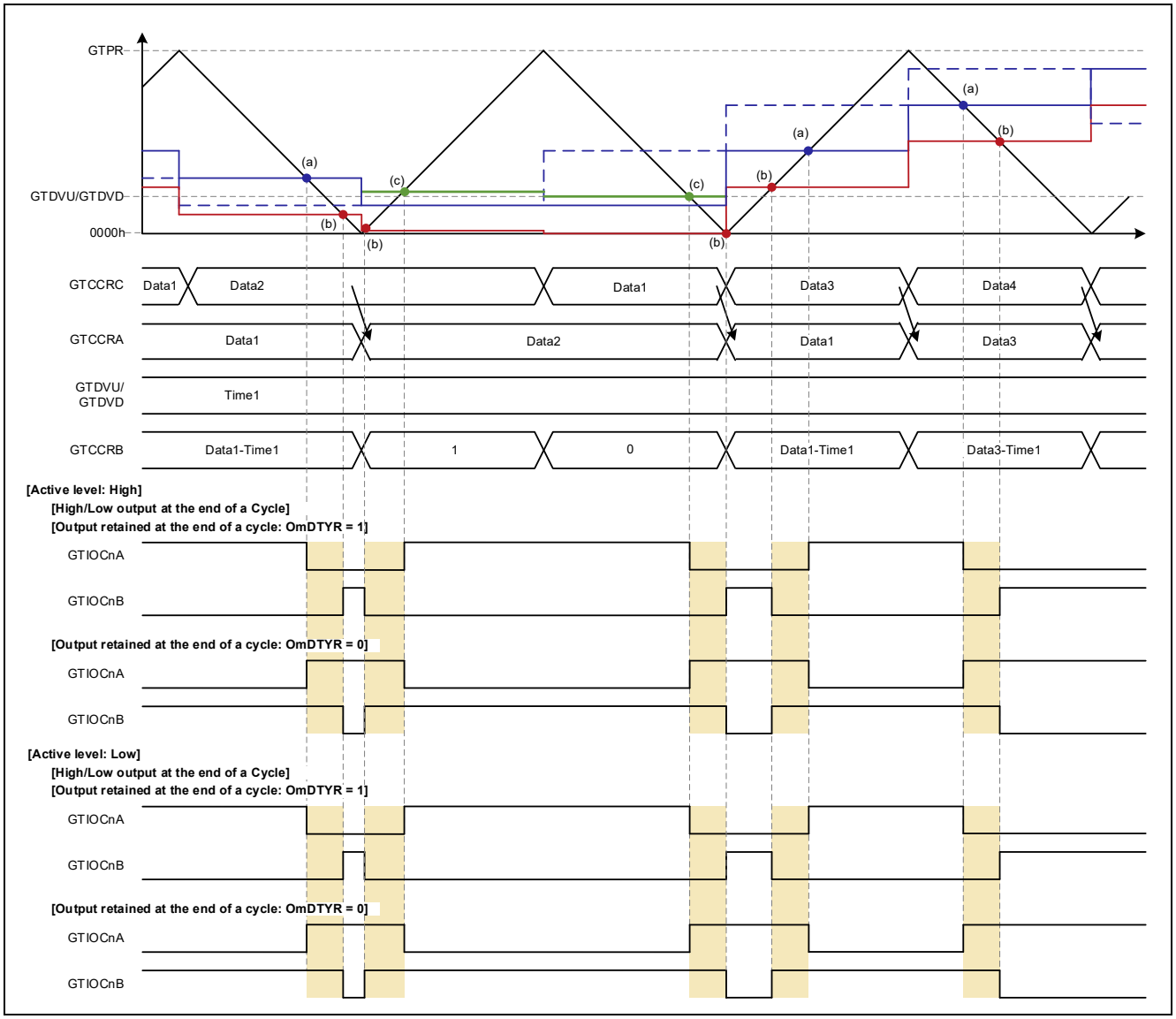


Figure 1.2 Triangle-Wave PWM Mode 2 Operation Examples (Automatic Dead Time Setting Enabled)

In triangle-wave PWM mode the buffer register is used when updating the data in the compare register. Updated data can be written to the buffer register at any time. The timing of transfers from the buffer register to the compare register can be selected by the MD[2:0] bits in the timer control register (GTCR).

The switching timing of the output levels is generated by compare matching of GTCNT and the compare registers (GTCCRA and GTCCRB). The timing of the GTIOCnA pin is generated by compare matching GTCNT and GTCCRA. Compare match points of GTCNT and GTCCRA are represented by blue dots (Figure 1.2 (a)). The timing of the GTIOCnB pin is generated by compare matching GTCNT and GTCCRB. Compare match points of GTCNT and GTCCRB are represented by red dots (Figure 1.2 (b)).

When the automatic dead time setting is used and a value that generates dead time errors is set in GTCCRA, GTCNT is compared with the adjusted value. Compare match points between GTCNT and the positive phase adjusted value are represented by green dots (Figure 1.2 (c)).

For details of the GPTW's triangle-wave PWM mode, refer to 24.3.3, PWM Output Operating Modes, in RX66T Group User's Manual: Hardware and the application note RX Family: PWM Output Methods Using MTU3/GPTW.

1.1.3 Operating Modes and Conditions

Operation under the following conditions is described in this application note.

Table 1.3 MTU Conditions

Mode	Buffer Configuration	Buffer Overwrite
Transfer at trough: complementary PWM mode 2	Single buffer	Tb interval overwrite
		Ta interval overwrite
Transfer at crest and trough: complementary PWM mode 3		Tb interval overwrite
		Ta interval overwrite

Table 1.4 GPTW Conditions

Mode	Buffer Configuration	Automatic Dead Time Setting
Transfer at trough: triangle-wave PWM mode 1	Single buffer	Used
		Not used
Transfer at crest and trough: triangle-wave PWM mode 3		Used
		Not used
Transfer at trough: triangle-wave PWM mode 3	*1	Used
		Not used

Note: 1. Buffer operation in triangle-wave PWM mode 3 differs from ordinary buffer operation in that the buffer is used automatically when the mode is selected. For details, refer to (5) Triangle-Wave PWM Mode 3 (Trough, 64-Bit Transfer) under 24.3.3, PWM Output Operating Modes, in RX66T Group User's Manual: Hardware.

1.2 0% and 100% Duty Cycle Output Methods

How to configure settings for complementary PWM output with 0% and 100% duty cycles on the MTU and GPTW is described below.

Table 1.5 Methods of Setting 0% and 100% Duty Cycles

Timer	Setting Methods	
MTU	Setting using compare register	Set TGR as follows. 100%: TGR = 0000h 0%: TGR = period register value
GPTW	Setting using compare register	Setting using GTCCCR*1
	Setting pin output duty setting bits	Setting using GTUDDTYC.OADTY[1:0] or GTUDDTYC.OBDTY[1:0] 0 x: Duty ratio determined by compare match 1 0: 0% duty 1 1: 100% duty

Note: 1. This may produce unanticipated waveforms. Refer to 1.4 for details.

On the MTU and GPTW there are cases where 0% or 100% duty cycle output cannot be produced due to the combination of the operating mode, the waveform output start timing (trough or crest), and the buffer transfer timing (Tb or Ta interval). Such cases are discussed in the next section.

1.2.1 0% and 100% Duty Cycles on MTU

On the MTU there are cases where 0% or 100% duty cycle output cannot be produced due to the combination of the operating mode, the waveform output start timing (trough or crest), and the buffer transfer timing (Tb or Ta interval). The various combinations are listed in Table 1.6. Operation examples of 0% and 100% duty cycle output are described in 1.2.1.1 and 1.2.1.2.

Table 1.6 0% and 100% Duty Cycle Waveform Output Operation Examples in Each MTU Operating Mode

Operating Mode	0% or 100% Output Start Timing	0% Duty Cycle Output		100% Duty Cycle Output	
		Tb Overwrite	Ta Overwrite	Tb Overwrite	Ta Overwrite
Complementary PWM mode 1	Trough	—	—	—	
	Crest	Figure 1.3	Figure 1.4	—	
Complementary PWM mode 2	Trough	Figure 1.5	Figure 1.6	Figure 1.11	Figure 1.12
	Crest	—	—	—	—
Complementary PWM mode 3	Trough	Figure 1.7	Figure 1.8	Figure 1.13	Figure 1.14
	Crest	Figure 1.9	Figure 1.10	—	—

—: Not possible.

1.2.1.1 0% Duty Cycle Output Operation Examples

The MTU produces 0% duty cycle output when the value of the compare register (TGR register) is the same as that of MTU3.TGRA (MTU6.TGRA).

Of the 0% and 100% duty cycle waveform output operation examples in each MTU operating mode listed in Table 1.6, Figure 1.3 to Figure 1.10 illustrate the 0% duty cycle output operation examples.

- [Operation example 1] Figure 1.3, Complementary PWM Mode 1, Output Start: Crest, Tb Interval Overwrite
- [Operation example 2] Figure 1.4, Complementary PWM Mode 1, Output Start: Crest, Ta Interval Overwrite
- [Operation example 3] Figure 1.5, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite
- [Operation example 4] Figure 1.6, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite
- [Operation example 5] Figure 1.7, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite
- [Operation example 6] Figure 1.8, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite
- [Operation example 7] Figure 1.9, Complementary PWM Mode 3, Output Start: Crest, Tb Interval Overwrite
- [Operation example 8] Figure 1.10, Complementary PWM Mode 3, Output Start: Crest, Ta Interval Overwrite

Key to Operating Conditions and Figures of Operation Examples

- Duty: 50% → 0% → 50%
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: 50% duty cycle compare value
  - Data 2: 0% duty cycle compare value (same value as MTU3.TGRA)

[Operation example 1] Complementary PWM Mode 1, Output Start: Crest, Tb Interval Overwrite

Figure 1.3 shows an operation example of buffer overwrite in the Tb2 interval (trough) in complementary PWM mode 1.

(a) Compare match with temporary register, positive phase turns off.
(b) Compare match with temporary register, negative phase turns on.
(c) Compare match with temporary register, positive phase remains off.
(d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in negative phase.
(e) Compare match for on, but no change in positive phase because (c) off takes precedence.
(f) Compare match with compare register, negative phase turns off.
(g) Compare match with compare register, positive phase turns on.

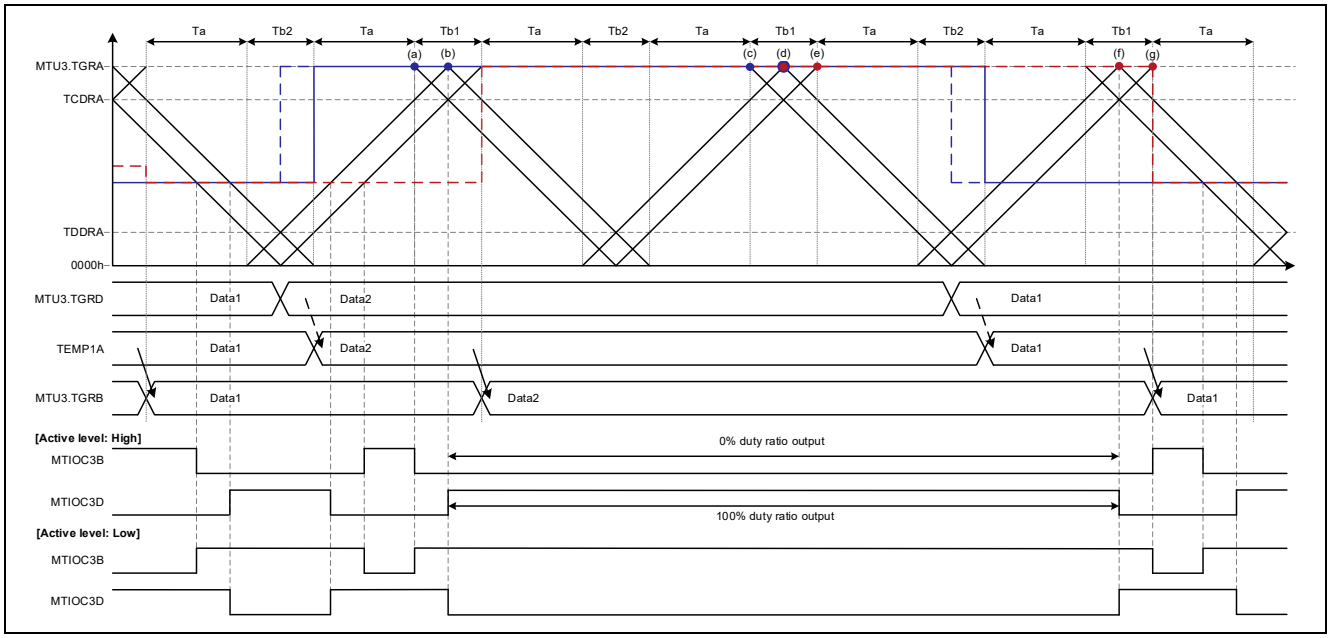


Figure 1.3 Complementary PWM Mode 1 Operation Example
(Output Start: Crest, Overwrite in Tb Interval, Duty: 50% → 0% → 50%)

[Operation example 2] Complementary PWM Mode 1, Output Start: Crest, Ta Interval Overwrite

Figure 1.4 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 1. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.3.

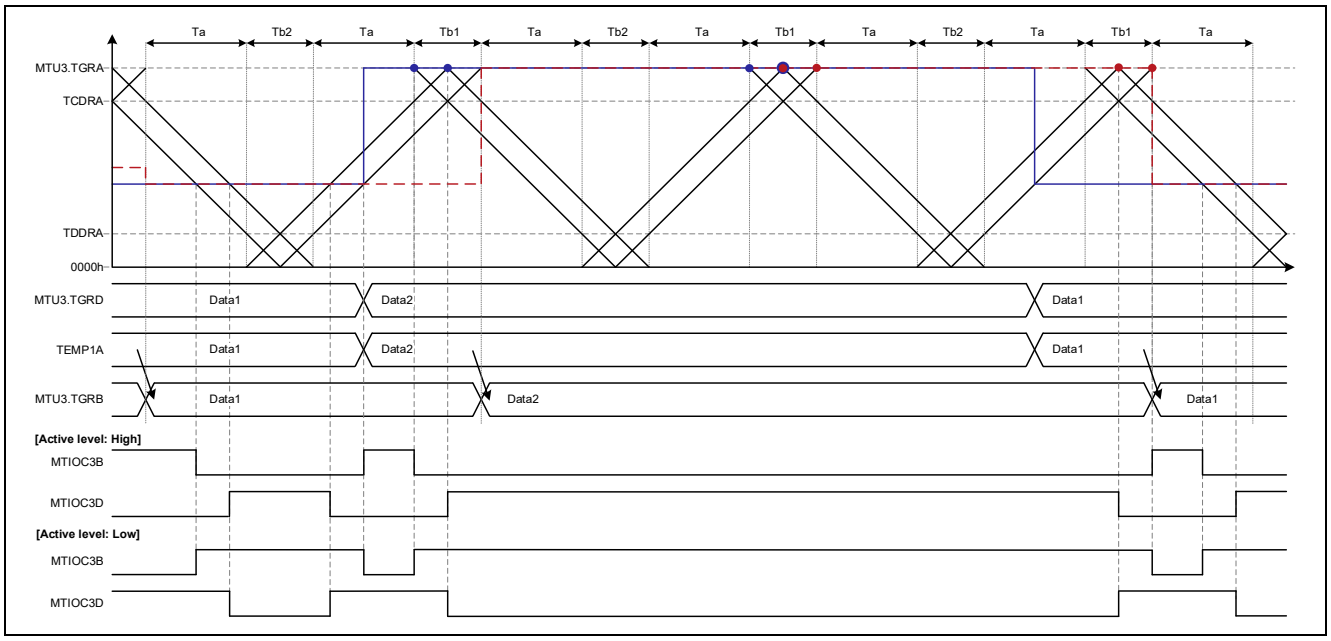


Figure 1.4 Complementary PWM Mode 1 Operation Example (Output Start: Crest, Overwrite in Ta Interval, Duty: 50% → 0% → 50%)

[Operation example 3] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.5 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with temporary register, positive phase remains off.
(b) Simultaneous compare matches for on (blue dots) and off (red dots), no change in negative phase.
(c) Compare match for on, but no change in positive phase because (a) off takes precedence.

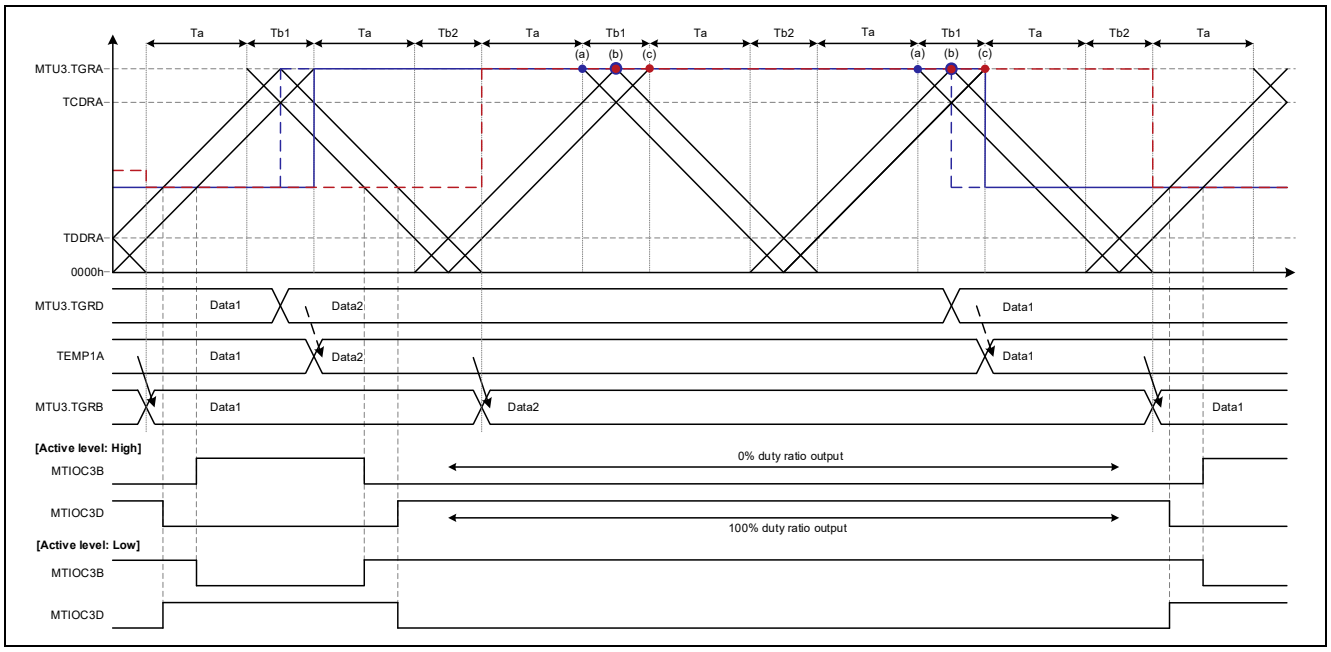


Figure 1.5 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: 50% → 0% → 50%)

[Operation example 4] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.6 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.5.

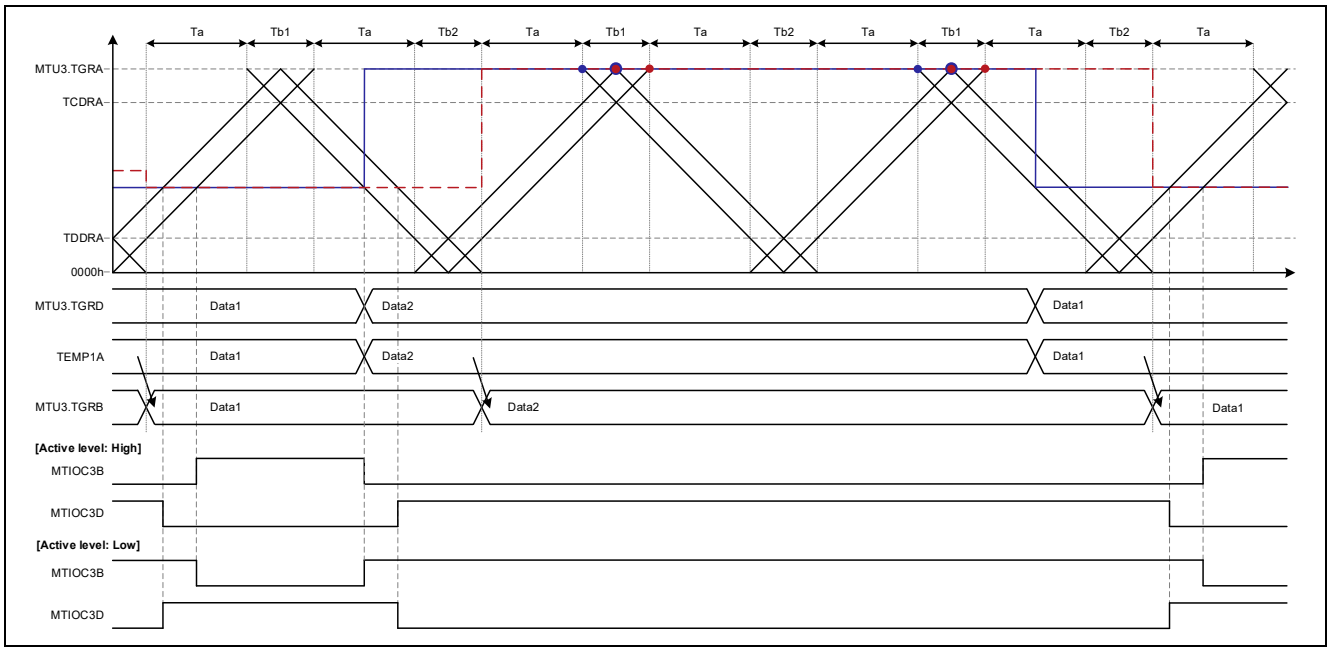


Figure 1.6 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: 50% → 0% → 50%)

[Operation example 5] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.7 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with temporary register, positive phase remains off.
(b) Simultaneous compare matches for on (blue dots) and off (red dots), no change in negative phase.
(c) Compare match for on, but no change in positive phase because (a) off takes precedence.

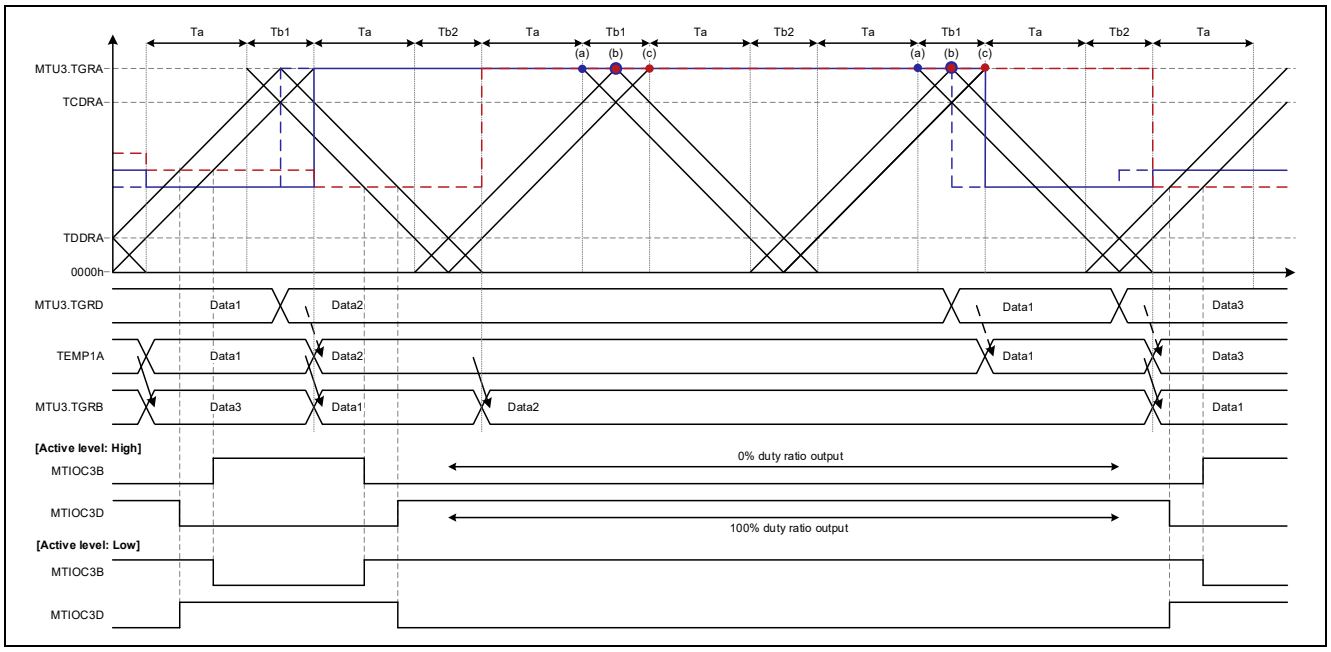


Figure 1.7 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: 50% → 0% → 50%)

[Operation example 6] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.8 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.7.

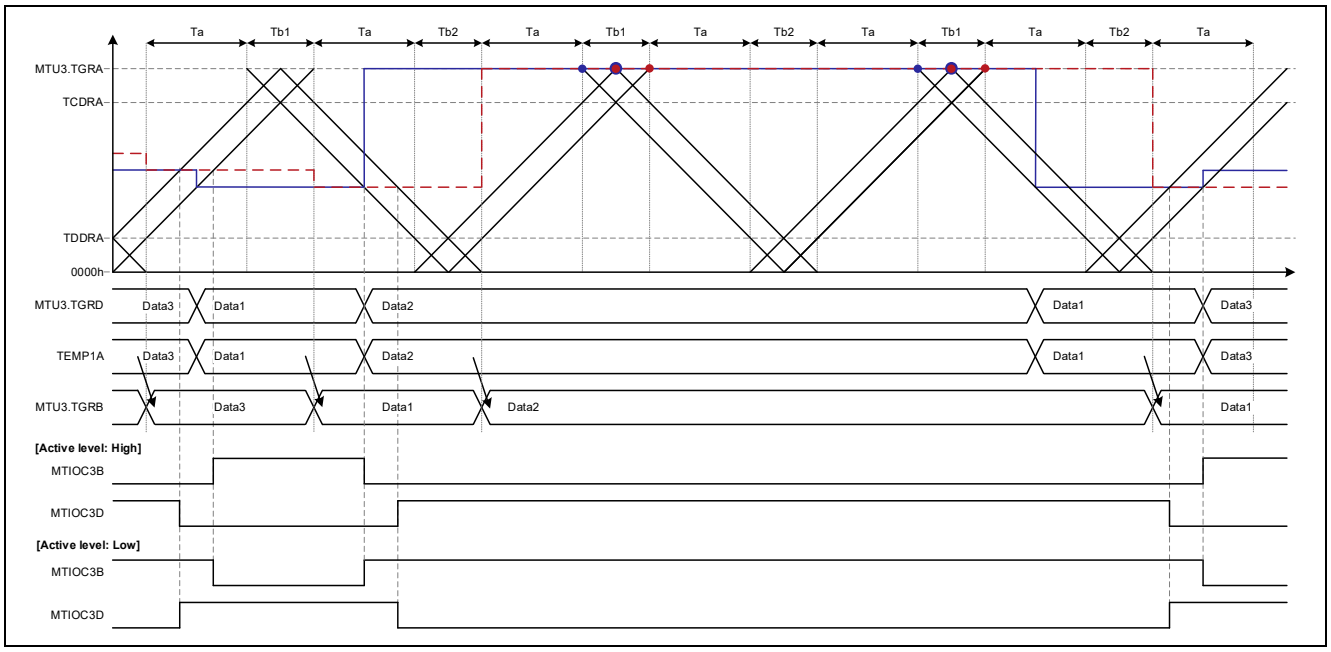


Figure 1.8 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: 50% → 0% → 50%)

[Operation example 7] Complementary PWM Mode 3, Output Start: Crest, Tb Interval Overwrite

It is possible to produce 0% output at the counter crests in complementary PWM mode 3. Figure 1.9 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with temporary register, positive phase turns off.
(b) Compare match with temporary register, negative phase turns on.
(c) Compare match with temporary register, positive phase remains off.
(d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in negative phase.
(e) Compare match for on, but no change in positive phase because (c) off takes precedence.
(f) Compare match with compare register, negative phase turns off.
(g) Compare match with compare register, positive phase turns on.

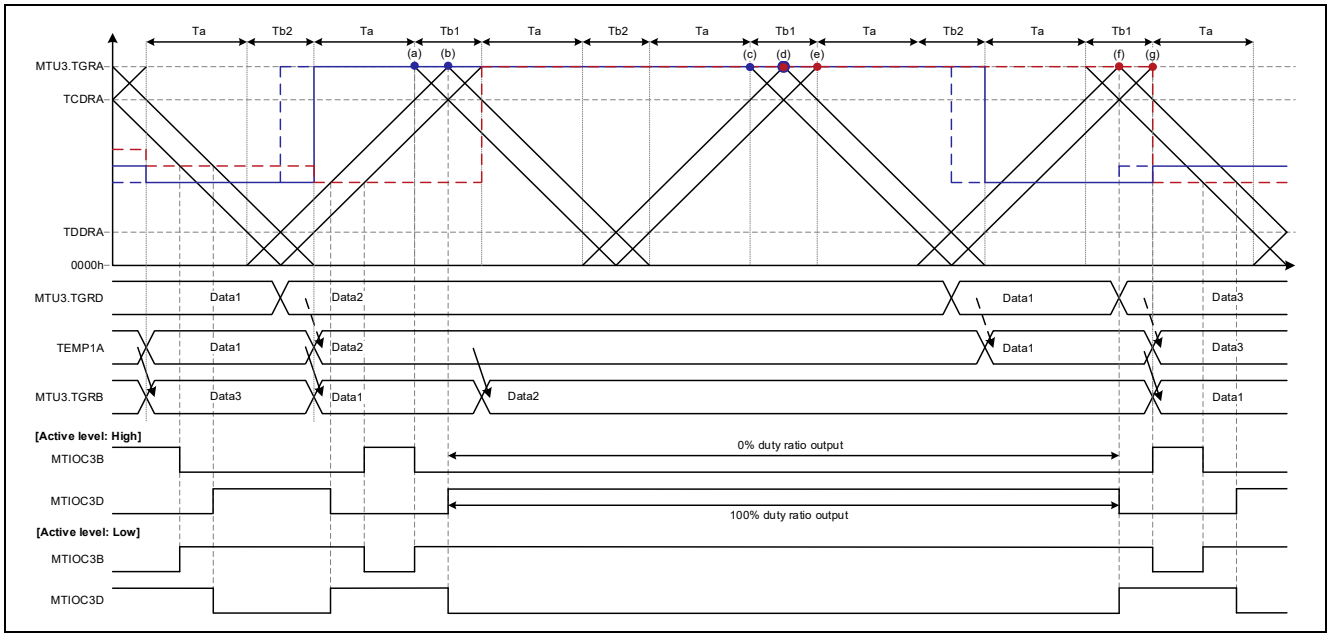


Figure 1.9 Complementary PWM Mode 3 Operation Example
(Output Start: Crest, Overwrite in Tb Interval, Duty: 50% → 0% → 50%)

[Operation example 8] Complementary PWM Mode 3, Output Start: Crest, Ta Interval Overwrite

Figure 1.10 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.9.

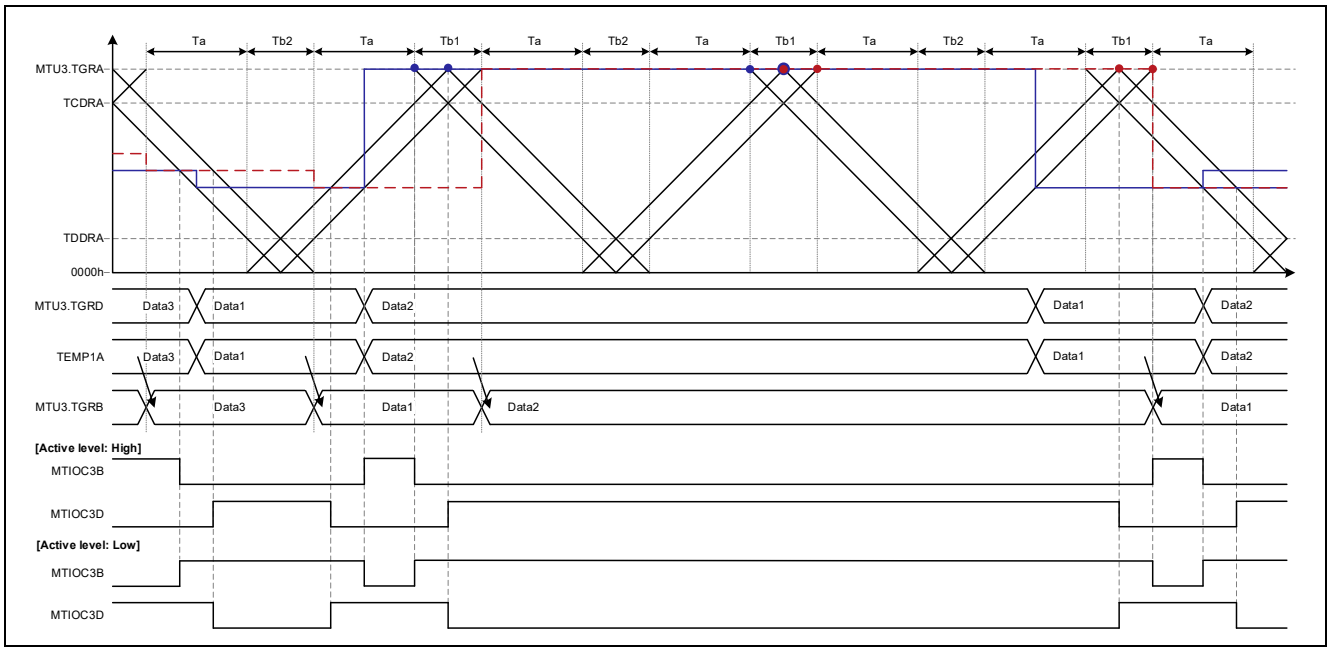


Figure 1.10 Complementary PWM Mode 3 Operation Example (Output Start: Crest, Overwrite in Ta Interval, Duty: 50% → 0% → 50%)

1.2.1.2 100% Duty Cycle Output Operation Examples

Output with 100% duty cycle is produced when the MTU compare register is set to 0000h.

Of the 0% and 100% duty cycle waveform output operation examples in each MTU operating mode listed in Table 1.6, Figure 1.11 to Figure 1.14 illustrate the 100% duty cycle output operation examples.

- [Operation example 1] Figure 1.11, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite
- [Operation example 2] Figure 1.12, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite
- [Operation example 3] Figure 1.13, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite
- [Operation example 4] Figure 1.14, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Key to Operating Conditions and Figures of Operation Examples

- Duty: 50% → 100% → 50%
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: 50% duty cycle compare value
  - Data 2: 100% duty cycle compare value (0000h)

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.11 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with temporary register, negative phase turns off.
(b) Compare match with temporary register, positive phase turns on.
(c) Compare match with temporary register, negative phase remains off.
(d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in positive phase.
(e) Compare match for on, but no change in negative phase because (c) off takes precedence.
(f) Compare match with compare register, positive phase turns off.
(g) Compare match with compare register, negative phase turns on.

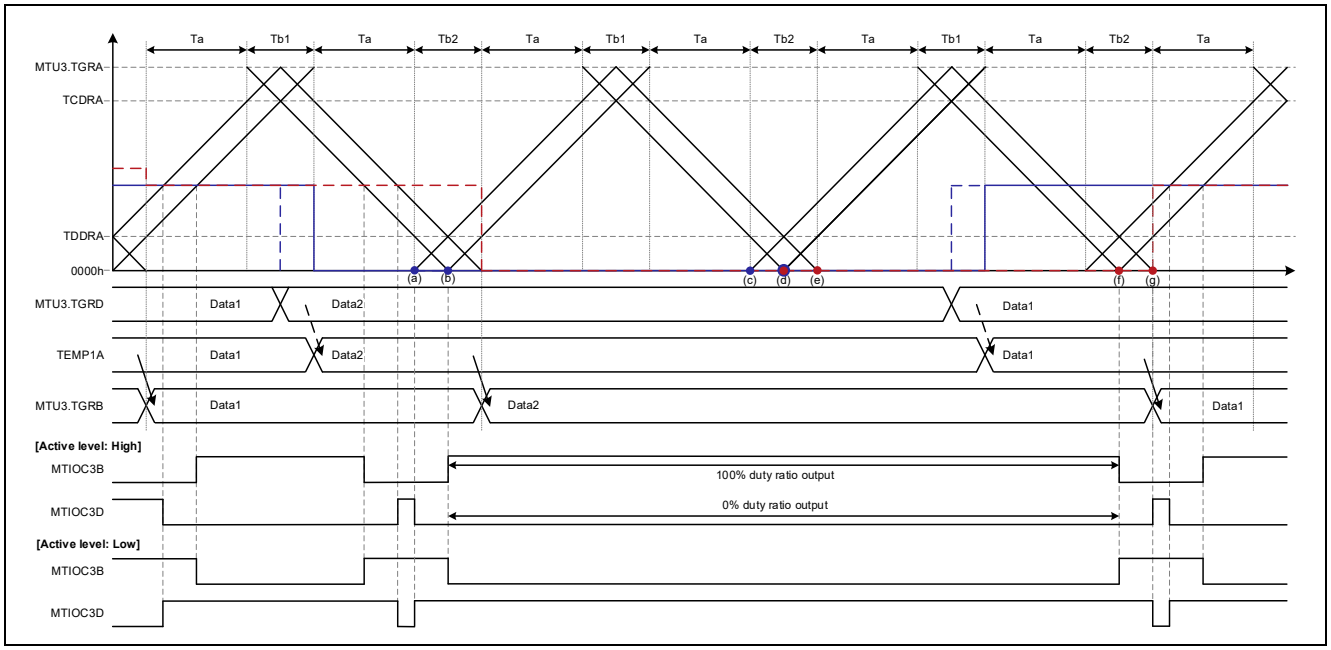


Figure 1.11 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: 50% → 100% → 50%)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.12 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.11.

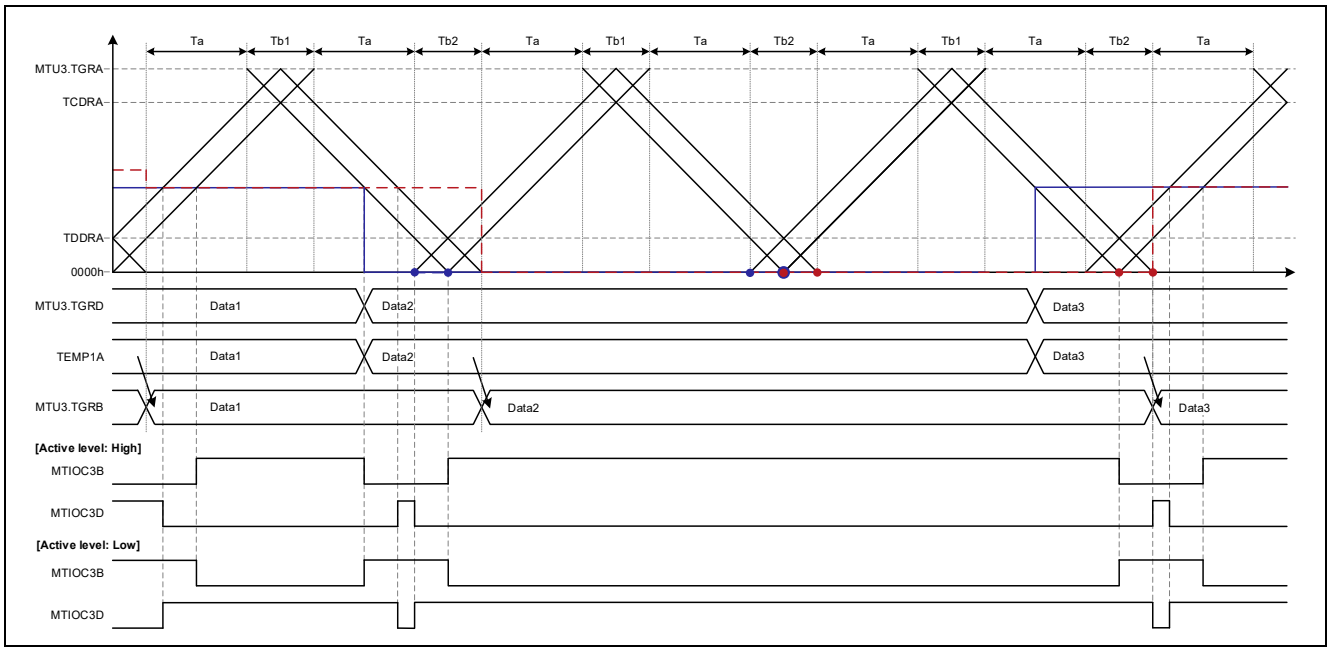


Figure 1.12 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: 50% → 100% → 50%)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.13 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with temporary register, negative phase turns off.
(b) Compare match with temporary register, positive phase turns on.
(c) Compare match with temporary register, negative phase remains off.
(d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in positive phase.
(e) Compare match for on, but no change in negative phase because (c) off takes precedence.
(f) Compare match with compare register, positive phase turns off.
(g) Compare match with compare register, negative phase turns on.

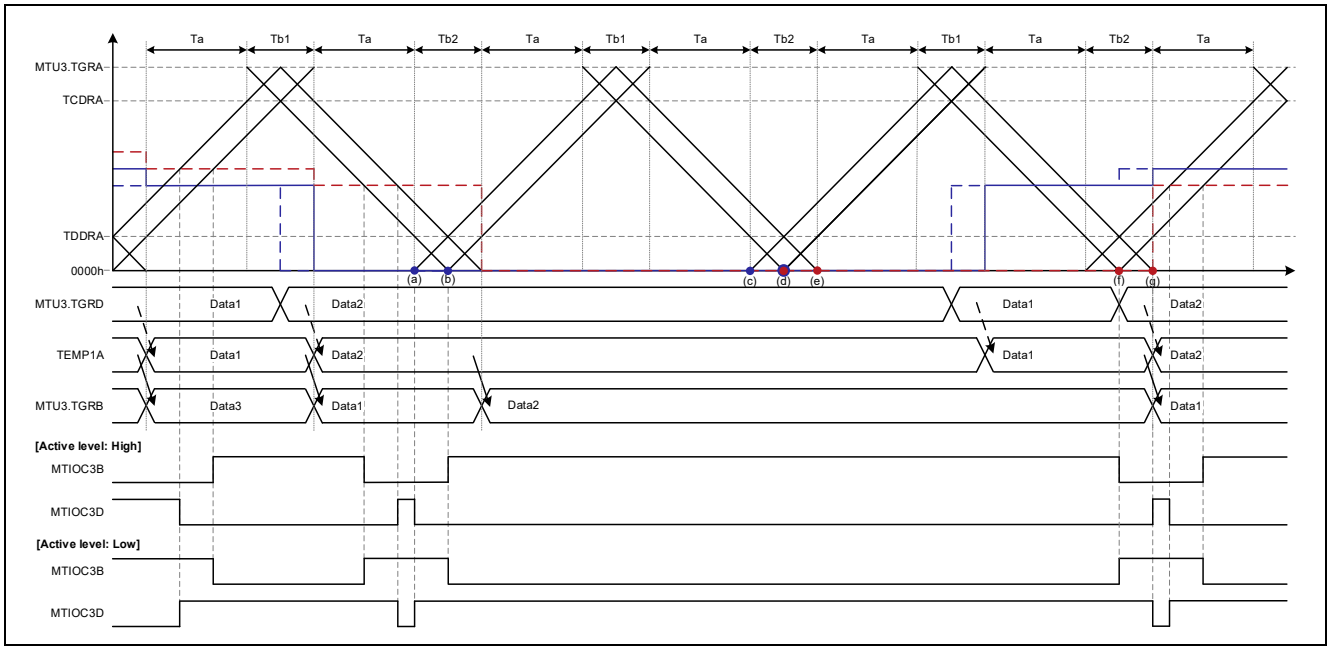


Figure 1.13 Complementary PWM Mode 3 Operation Example
(Output Start: Trough, Overwrite in Tb Interval, Duty: 50% → 100% → 50%)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.14 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.13.

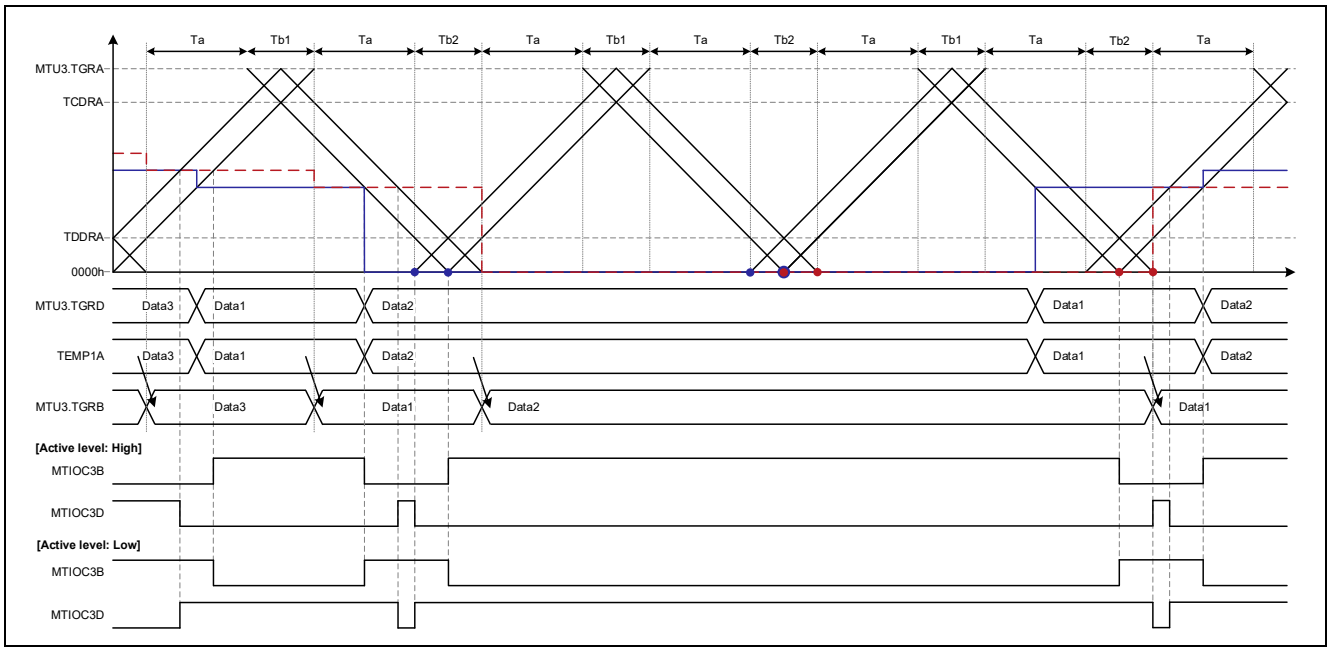


Figure 1.14 Complementary PWM Mode 3 Operation Example
(Output Start: Trough, Overwrite in Ta Interval, Duty: 50% → 100% → 50%)

1.2.2 0% and 100% Duty Cycles on GPTW

On the GPTW there are cases where 0% or 100% duty cycle output cannot be produced due to the combination of the operating mode, the waveform output start timing (trough or crest), and the automatic dead time generation setting. The various combinations are listed in Table 1.7. Operation examples of 0% and 100% duty cycle output are described in the next section.

Table 1.7 0% and 100% Duty Cycle Waveform Output Operation Examples in Each GPTW Operating Mode

Operating Mode	0% or 100% Output Start Timing	Automatic Dead Time Setting Enabled		Automatic Dead Time Setting Disabled	
		0% Duty Cycle Output	100% Duty Cycle Output	0% Duty Cycle Output	100% Duty Cycle Output
Triangle-Wave PWM mode 1	Trough	Figure 1.15	Figure 1.15	Figure 1.16	Figure 1.16
	Crest	—	—	—	—
Triangle-Wave PWM mode 2	Trough	Figure 1.17	Figure 1.17	Figure 1.18	Figure 1.18
	Crest	—	—	—	—
Triangle-Wave PWM mode 3	Trough	Figure 1.19	Figure 1.19	Figure 1.20	Figure 1.20
	Crest	—	—	—	—

—: Not possible.

The GPTW produces 0% or 100% duty cycle output when the value of the OADTY[1:0] or OBDTY[1:0] bits in GTUDDTYC changes. Changing the value of the OADTY[1:0] or OBDTY[1:0] bits in GTUDDTYC during count operation applies the output duty cycle setting that was changed to when an underflow (trough) occurred.

Changes to 0% or 100% duty cycle during count operation are described in this application note. For details of 0% and 100% duty cycle output after count operation start, refer to 4.13, Triangle-Wave PWM Mode Duty Cycles 0% and 100%, in the application note RX Family: PWM Output Methods Using MTU3/GPTW.

The GPTW continues compare match operation internally during operation with 0% and 100% duty cycle settings, and interrupt output and buffer operation take place.

When a change from 0% or 100% duty cycle output to output based on compare match operation occurs, the output value at the end of the period is determined by the setting values of the GTIOm[3:2] bits (m = A or B) and OmDTYR bits (m = A or B) in GTIOR.

Table 1.8 lists output values at the end of the period when a change from a 0% or 100% duty cycle setting to output based on compare match operation has occurred, as described in this application note.

Table 1.8 Output Values after Cancellation of 0% and 100% Duty Cycles

GTIOR.GTIOm[3:2]	Value at End of Period when Compare Match Output Was Masked by 0% and 100% Duty Cycle Settings	GTUDDTYC.OmDTYR Value at 0% Duty Cycle Setting		GTUDDTYC.OmDTYR Value at 100% Duty Cycle Setting	
		0	1	0	1
00b (output maintained at end of period)	Low	Low	Low	High	Low
	High	Low	High	High	High
01b (low output at end of period)	—	Low	Low	Low	Low
10b (high output at end of period)	—	High	High	High	High

m = A or B

1.2.2.1 0% and 100% Duty Cycle Output Operation Examples

Figure 1.15 to Figure 1.20 illustrate the 0% and 100% duty cycle waveform output operation examples in each GPTW operating mode listed in Table 1.7.

- [Operation example 1] Figure 1.15, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Function Enabled
- [Operation example 2] Figure 1.16, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Function Disabled
- [Operation example 3] Figure 1.17, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Function Enabled
- [Operation example 4] Figure 1.18, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Function Disabled
- [Operation example 5] Figure 1.19, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Function Enabled
- [Operation example 6] Figure 1.20, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Function Disabled

In the figures, the dotted black lines for the GTIOCnA and GTIOCnB pins represent operation masked by 0% and 100% duty cycle settings.

Key to Operating Conditions and Figures of Operation Examples

- Duty: 50% → 0%/100% → 50%
- Key to figures
  - Dashed blue line: Setting value transition of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting value transition of positive phase compare register (GTCCRA)
  - Dashed red line: Setting value transition of negative phase buffer register (GTCCRD)
  - Solid red line: Setting value transition of negative phase compare register (GTCCRB)
  - Data 1: 50% duty cycle compare value

[Operation example 1] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Function Enabled

Figure 1.15 shows an operation example with the automatic dead time setting function enabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% duty cycle output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Output inverted before 0%/100% duty cycle setting when value of OmDTYR bit is 0b.

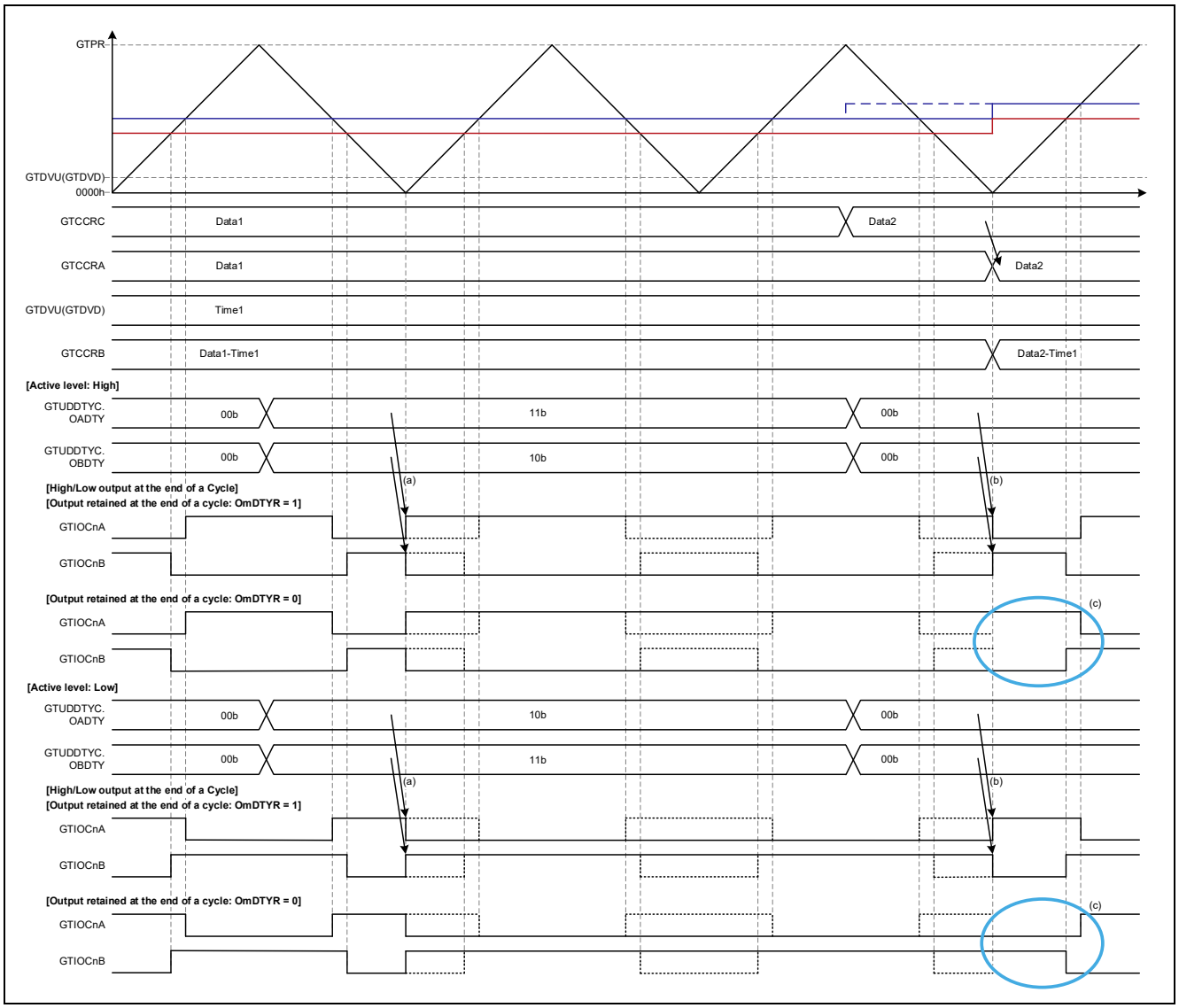


Figure 1.15 Triangle-Wave PWM Mode 1 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: 50% → 0%/100% → 50%)

[Operation example 2] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Function Disabled

Figure 1.16 shows an operation example with the automatic dead time setting function disabled in triangle-wave PWM mode 1. Except for the operation of the GTCCRB and GTCCRE registers, the operation is the same as that shown in Figure 1.15.

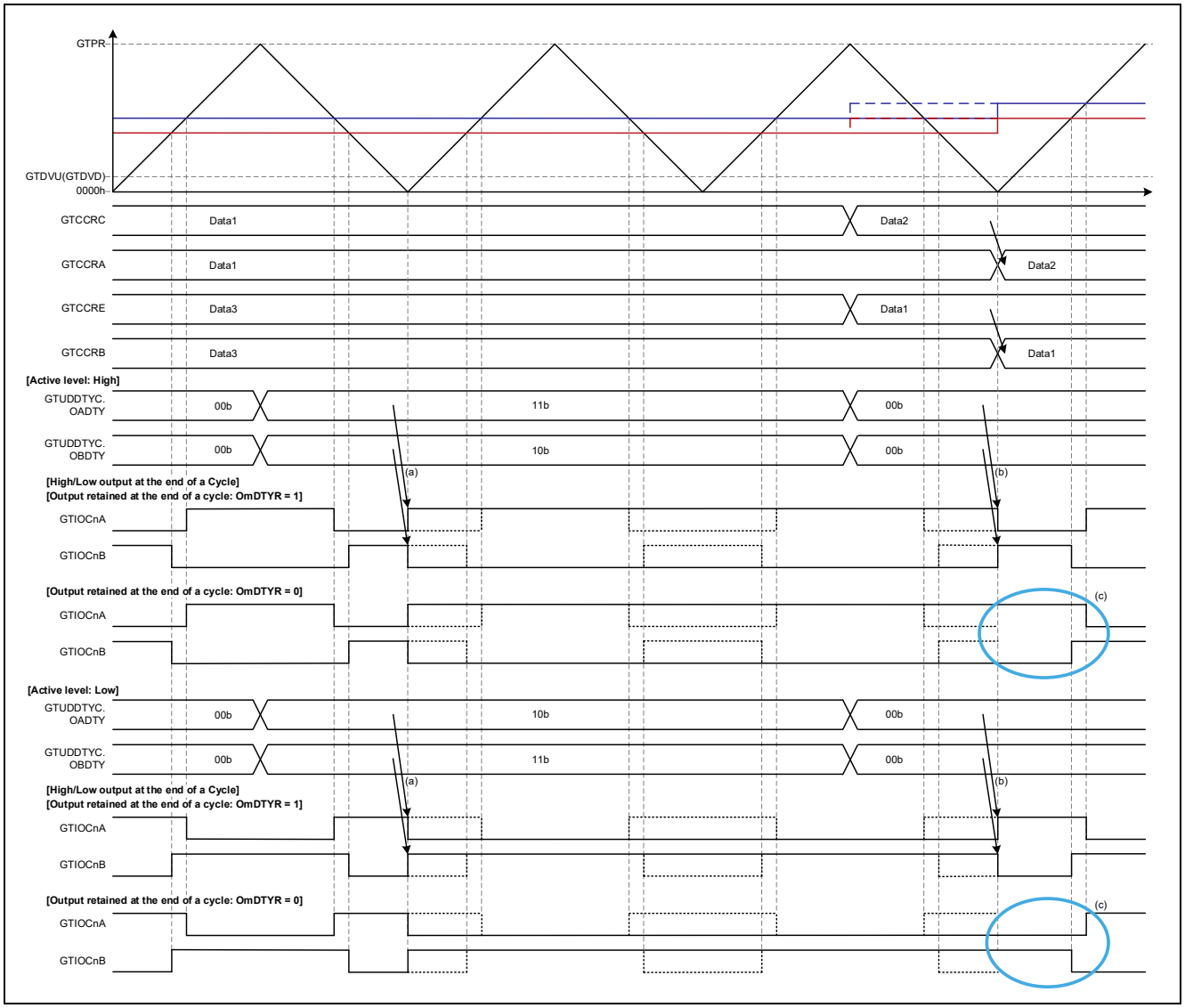


Figure 1.16 Triangle-Wave PWM Mode 1 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: 50% → 0%/100% → 50%)

[Operation example 3] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Function Enabled

Figure 1.17 shows an operation example with the automatic dead time setting function enabled in triangle-wave PWM mode 2.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% duty cycle output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Output inverted before 0%/100% duty cycle transition when value of OmDTYR bit is 0b.

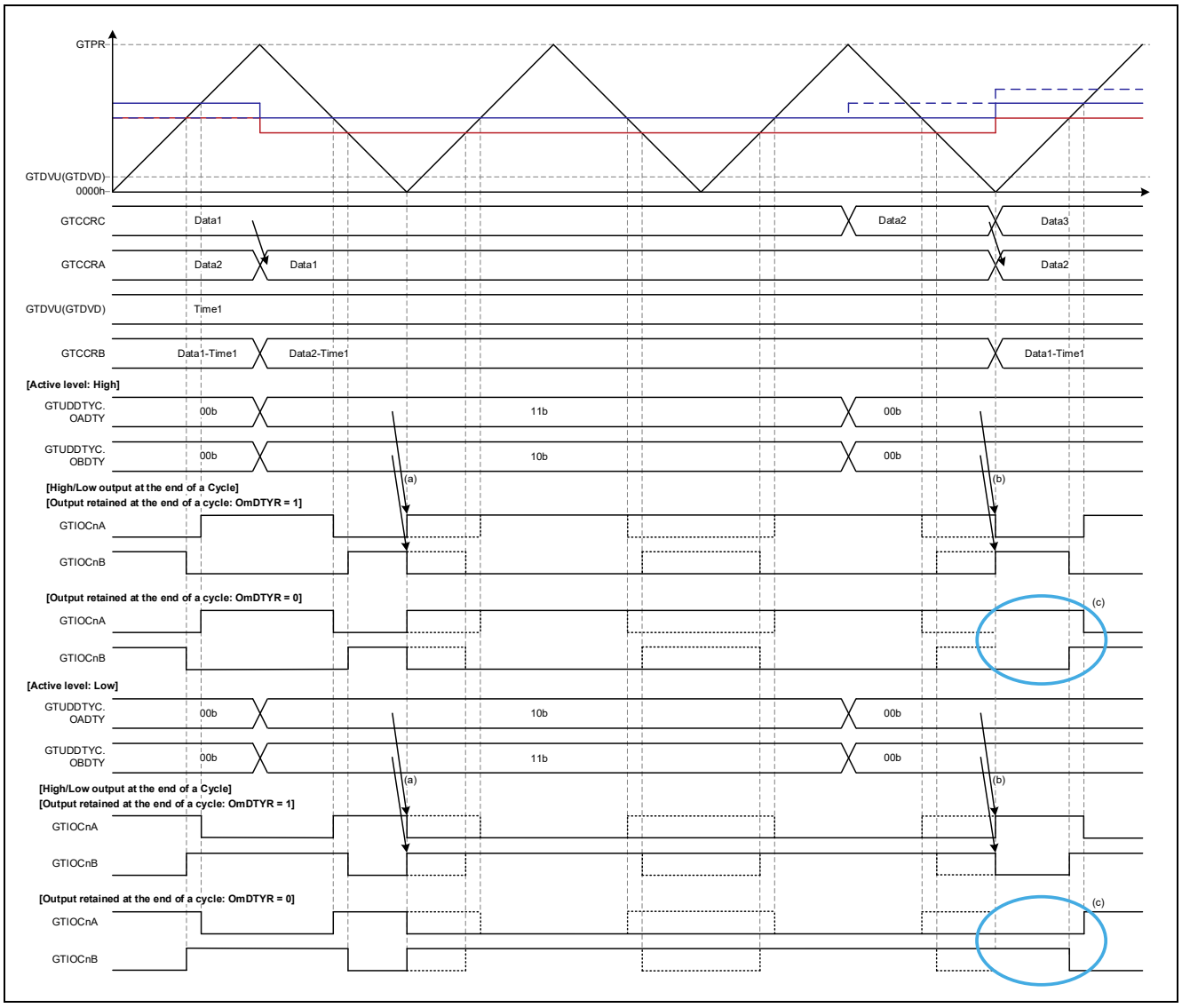


Figure 1.17 Triangle-Wave PWM Mode 2 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: 50% → 0%/100% → 50%)

[Operation example 4] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Function Disabled

Figure 1.18 shows an operation example with the automatic dead time setting function disabled in triangle-wave PWM mode 2. Except for the operation of the GTCCRB and GTCCRE registers, the operation is the same as that shown in Figure 1.17.

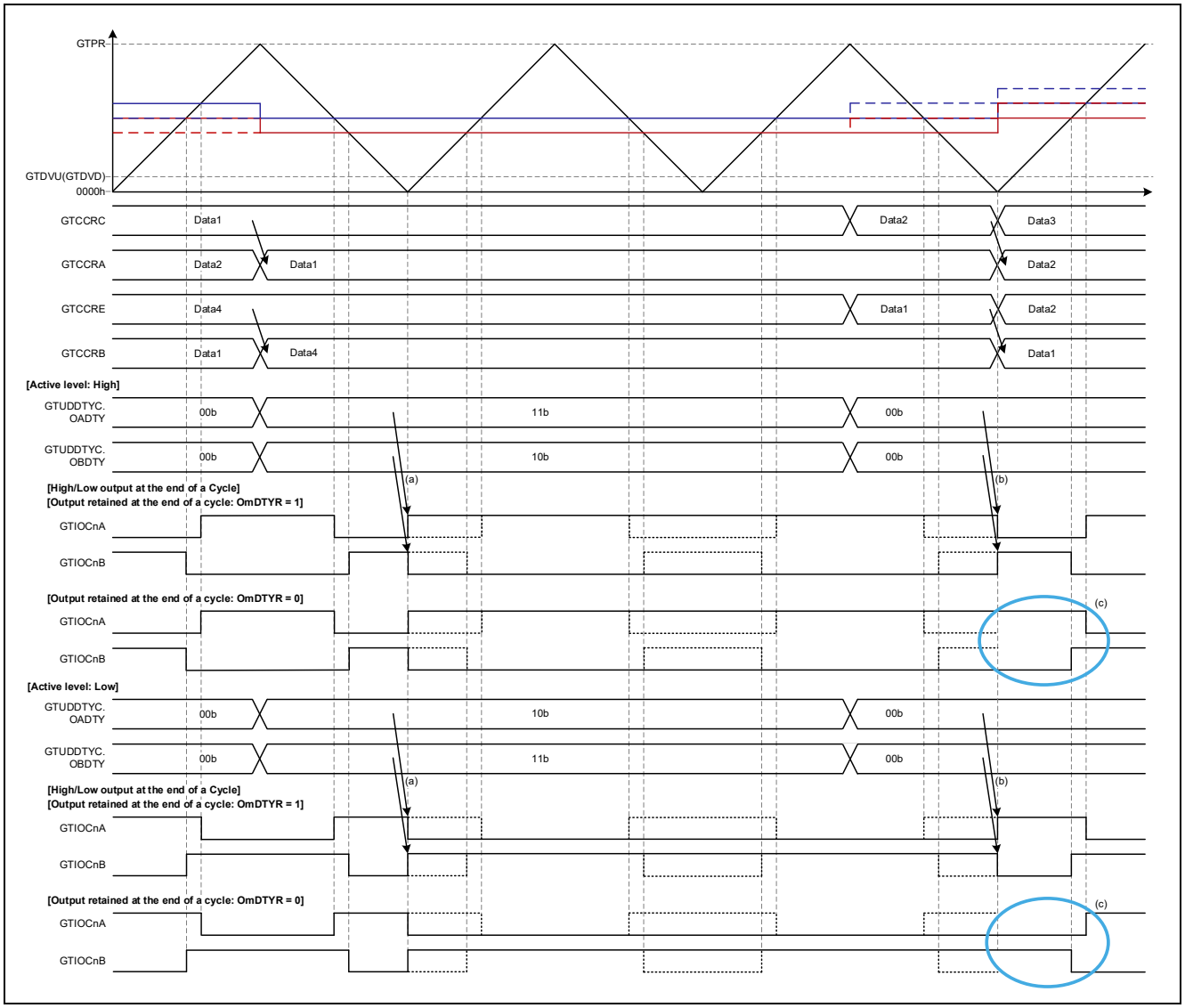


Figure 1.18 Triangle-Wave PWM Mode 2 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: 50% → 0%/100% → 50%)

[Operation example 5] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Function Enabled

Figure 1.19 shows an operation example with the automatic dead time setting function enabled in triangle-wave PWM mode 3.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% duty cycle output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Output inverted before 0%/100% duty cycle setting when value of OmDTYR bit is 0b.

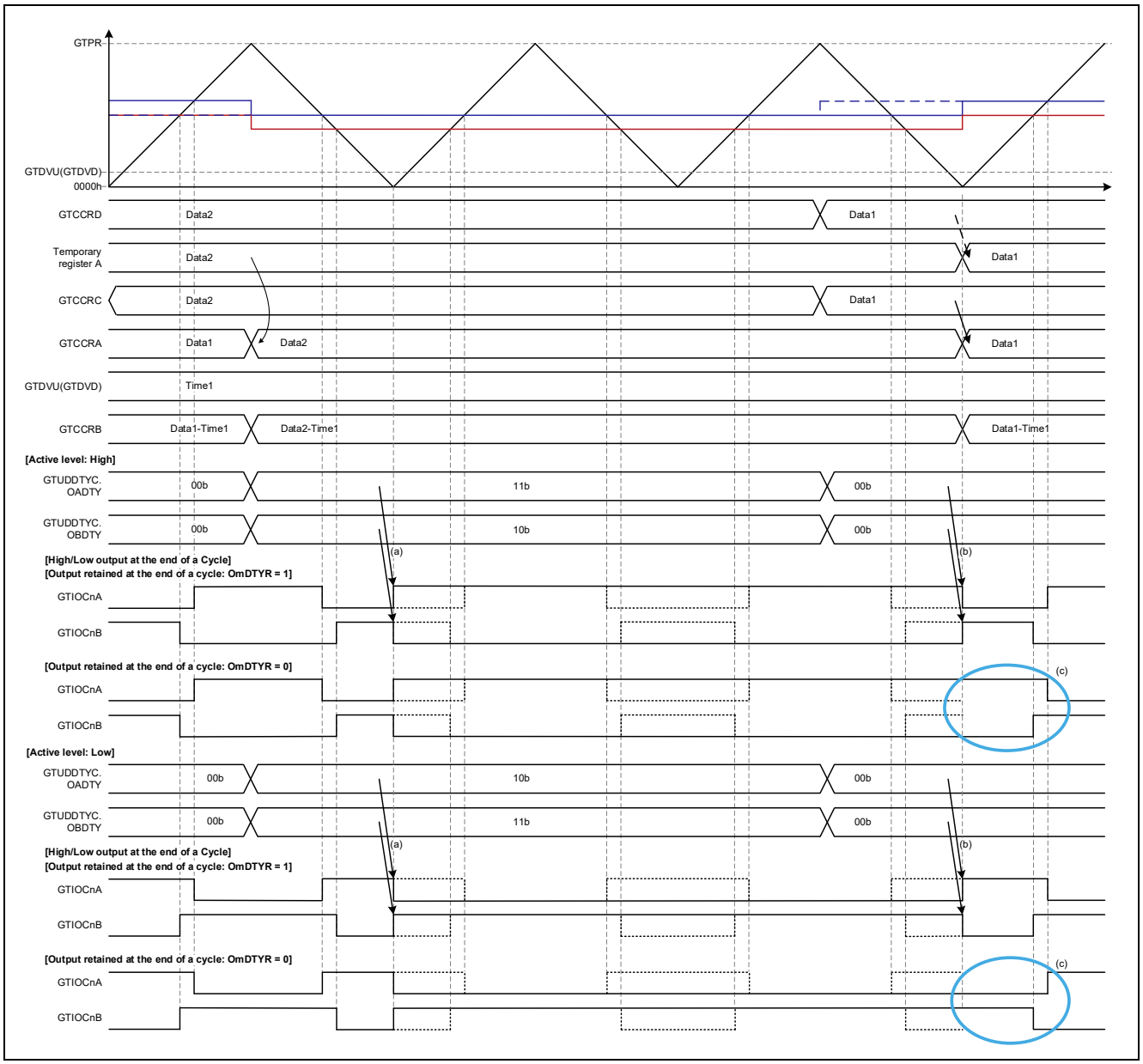


Figure 1.19 Triangle-Wave PWM Mode 3 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: 50% → 0%/100% → 50%)

[Operation example 6] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Function Disabled

Figure 1.20 shows an operation example with the automatic dead time setting function disabled in triangle-wave PWM mode 3. Except for the operation of the GTCCRB and GTCCRE registers, the operation is the same as that shown in Figure 1.19.

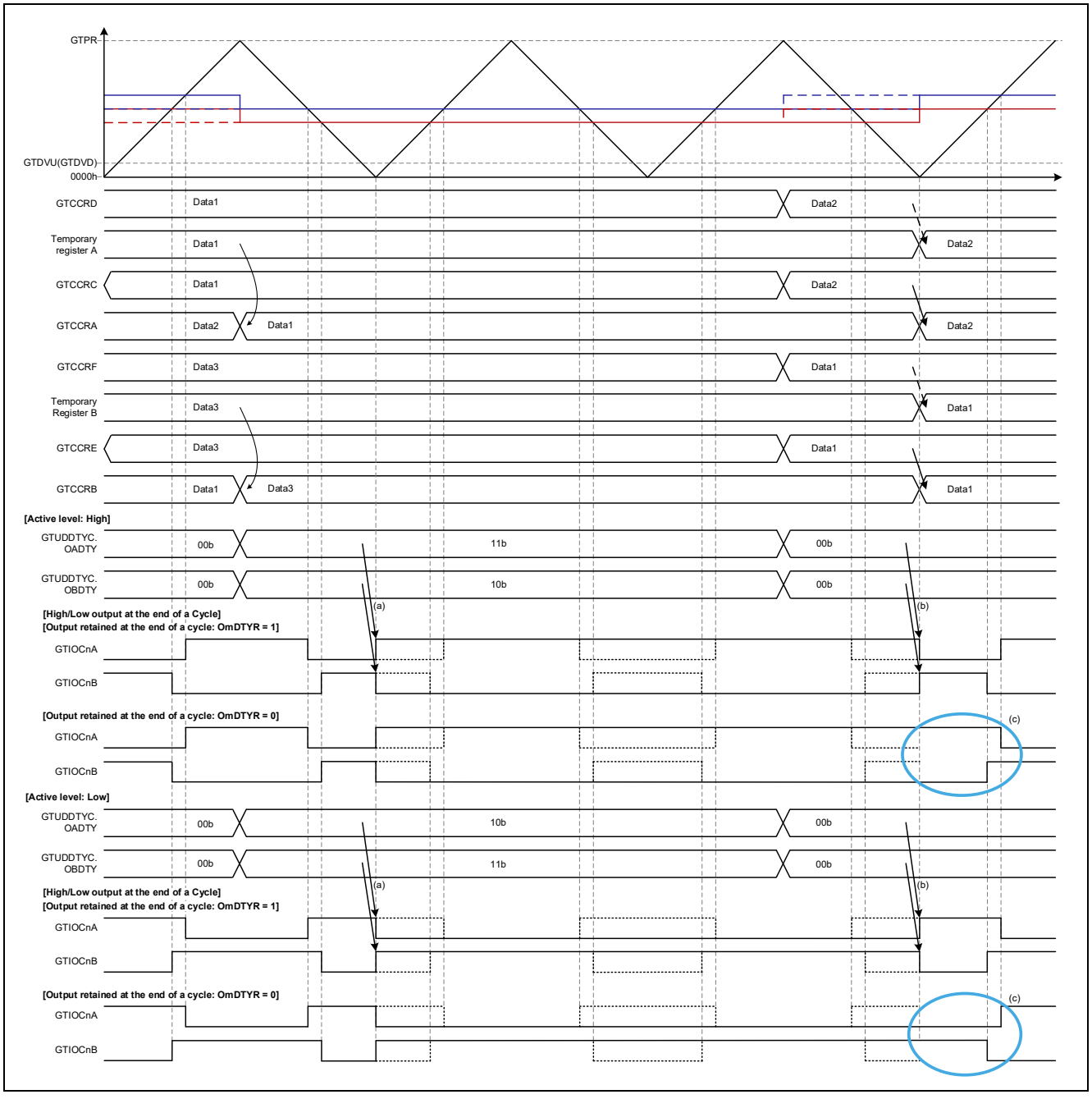


Figure 1.20 Triangle-Wave PWM Mode 3 Operation Example (Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: 50% → 0%/100% → 50%)

1.3 Cautions Regarding Waveform Output Near 0% and 100% Duty Cycles

When using compare matches with the compare register and temporary register that occur near 0% or 100% duty cycles (Tb interval) on the MTU3, or compare matches with GTCCCR that occur near 0% or 100% duty cycles (dead time interval) on the GPTW, there are cautions to be considered regarding the resulting output waveforms. These cautions are described in this section.

Figure 1.21 defines the compare register patterns and compare register values to which these points apply. The shaded portions in Figure 1.21 show the ranges near 0% and 100% duty cycles on the MTU and GPTW.

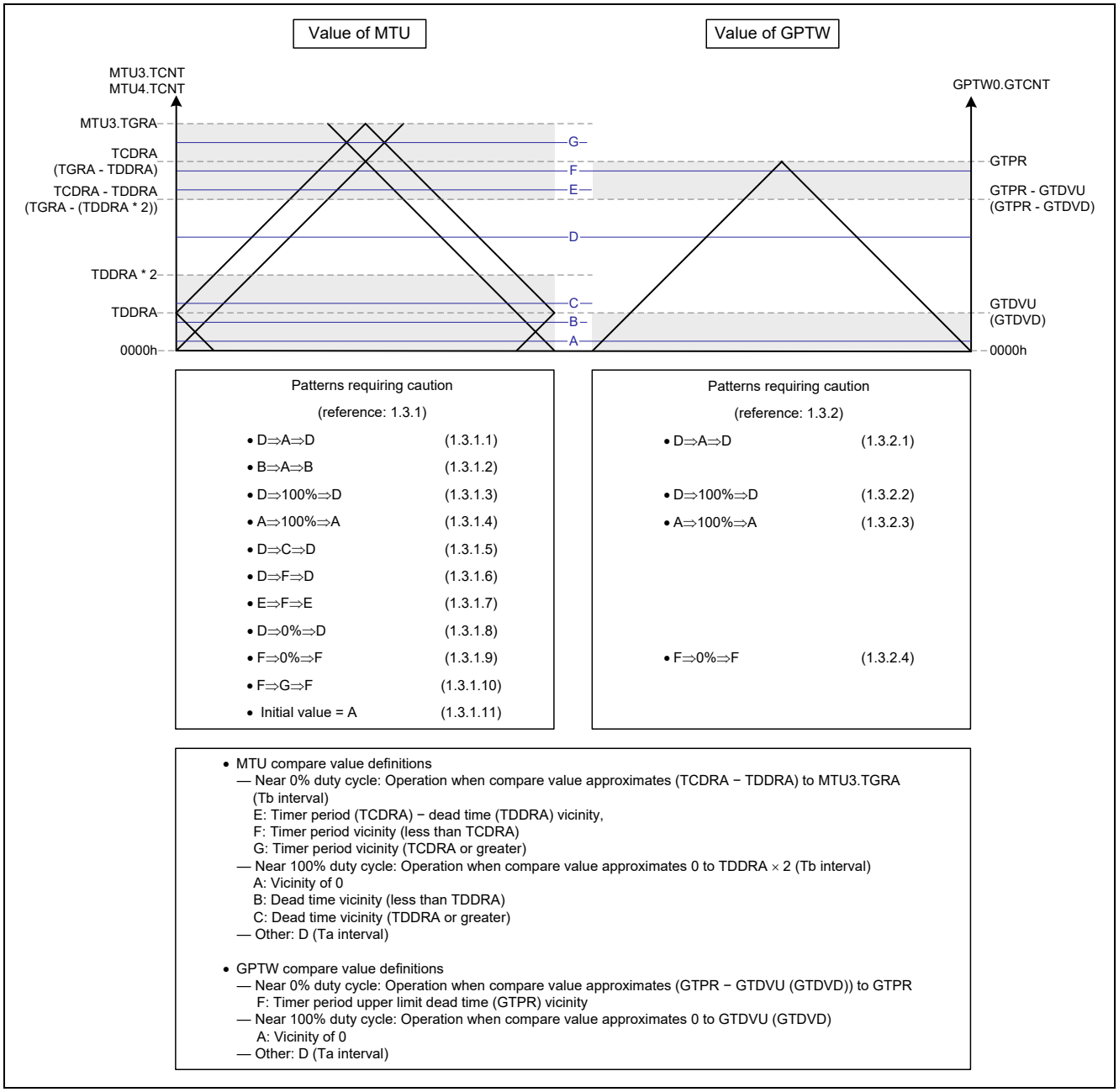


Figure 1.21 Compare Registers and Patterns Requiring Caution

1.3.1 Output Waveforms Near 0% and 100% Duty Cycles on MTU

Table 1.9 lists cautions and operation examples for waveform output with various buffer register overwrite timings (Ta/Tb interval) and compare match timings (near 0% or 100% duty cycles) in complementary PWM modes 2 and 3.

Table 1.9 List of MTU Cautions and Operating Modes

Section	Section Title	Complementary PWM Mode 2		Complementary PWM Mode 3	
		Tb Overwrite Ta Overwrite	Cautions	Tb Overwrite Ta Overwrite	Cautions
1.3.1.1	Change from Near 100% to Near 100% (D → A → D)	Figure 1.22 Figure 1.23	*1, *2	Figure 1.24 Figure 1.25	*1, *2
1.3.1.2	Change from Near 100% to Near 100% (B → A → B)	Figure 1.26 Figure 1.27	*2, *3	Figure 1.28 Figure 1.29	*2, *3
1.3.1.3	Change from Near 100% to 100% (D → 100% → D)	Figure 1.30 Figure 1.31	*4	Figure 1.32 Figure 1.33	*4
1.3.1.4	Change from Near 100% to 100% (A → 100% → A)	Figure 1.34 Figure 1.35	*2	Figure 1.36 Figure 1.37	*2
1.3.1.5	Change to Near Dead Time Value (D → C → D)	Figure 1.38 Figure 1.39	*4	Figure 1.40 Figure 1.41	*4
1.3.1.6	Change from Near 0% to Near 0% (D → F → D)	Figure 1.42 Figure 1.43	*6, *8	Figure 1.44 Figure 1.45	*6, *8
1.3.1.7	Change from Near 0% to Near 0% (E → F → E)	Figure 1.46 Figure 1.47	*6, *7	Figure 1.48 Figure 1.49	*6, *7
1.3.1.8	Change from Near 0% to 0% (D → 0% → D)	Figure 1.50 Figure 1.51	*8	Figure 1.52 Figure 1.53	*5
1.3.1.9	Change from Near 0% to 0% (F → 0% → F)	Figure 1.54 Figure 1.55	*6	Figure 1.56 Figure 1.57	*9
1.3.1.10	Change from Near 0% to Near 0% (F → G → F)	Figure 1.58 Figure 1.59	*6, *10	Figure 1.60 Figure 1.61	*10
1.3.1.11	Initial output (initial value = A)	Figure 1.62 Figure 1.63	*11	Figure 1.64 Figure 1.65	*11

Notes: 1. When the value of D is closer to TDDRA × 2, the negative phase becomes minute pulses to the extent that the value A of is close to 0.
2. The positive phase becomes minute pulses to the extent that the value A of is close to 0.
3. The positive phase becomes minute pulses to the extent that the values of A and B are close to 0.
4. The negative phase becomes minute pulses to the extent that the value of D is close to TDDRA × 2.
5. The positive phase becomes minute pulses to the extent that the value of D is close to TCDRA − TDDRA.
6. The positive phase becomes minute pulses to the extent that the value of F is close to TCDRA.
7. The positive phase becomes minute pulses to the extent that the value of E is close to TCDRA.
8. When the value of D is close to TCDRA − TDDRA, the positive phase becomes minute pulses the smaller the value of TDDRA is.
9. The negative phase becomes minute pulses to the extent that the value of F is close to TCDRA.
10. The negative phase becomes minute pulses to the extent that the value of G is close to MTU3.TGRA.
11. The initial output level of the negative phase is maintained at the value set in TOCR1m.OLSN (m = A or B).

1.3.1.1 Change from Near 100% to Near 100% (D → A → D)

Figure 1.22 to Figure 1.25 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.22, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, cautions 1 and 2
- [Operation example 2] Figure 1.23, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, cautions 1 and 2
- [Operation example 3] Figure 1.24, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, cautions 1 and 2
- [Operation example 4] Figure 1.25, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, cautions 1 and 2

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → A → D
  - D > TDDRA × 2
  - A < TDDRA
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: D
  - Data 2: A
- Cautions
  1. When the value of D is closer to TDDRA × 2, the negative phase becomes minute pulses to the extent that the value A of is close to 0.
  2. The positive phase becomes minute pulses to the extent that the value A of is close to 0.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.22 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, negative phase turns on.
(b) Compare match with temporary register, negative phase turns off.
(c) Compare match with temporary register, negative phase remains off.
(d) Compare match with compare register, positive phase turns off.
(e) Compare match with temporary register, positive phase turns on.
(f) Compare match for on, but no change in negative phase because (c) off takes precedence.
(g) Compare match with compare register, negative phase turns on.
(h) Compare match with compare register, negative phase turns off.

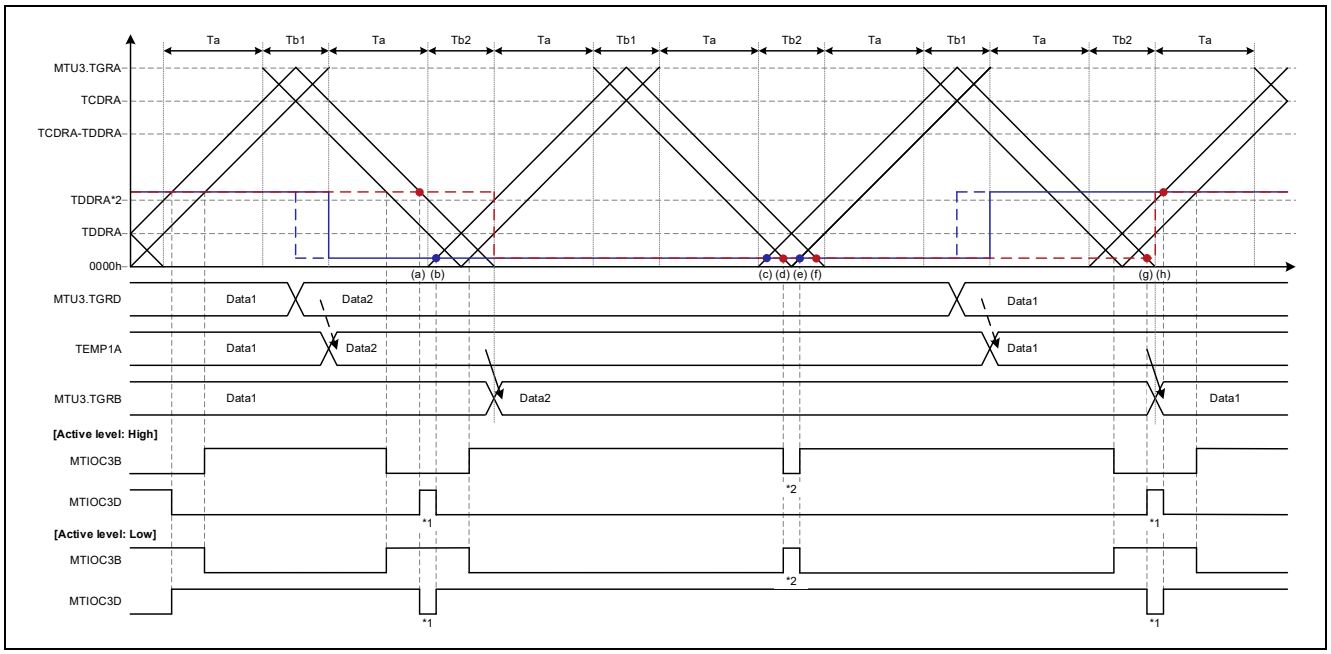


Figure 1.22 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → A → D)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.23 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.22.

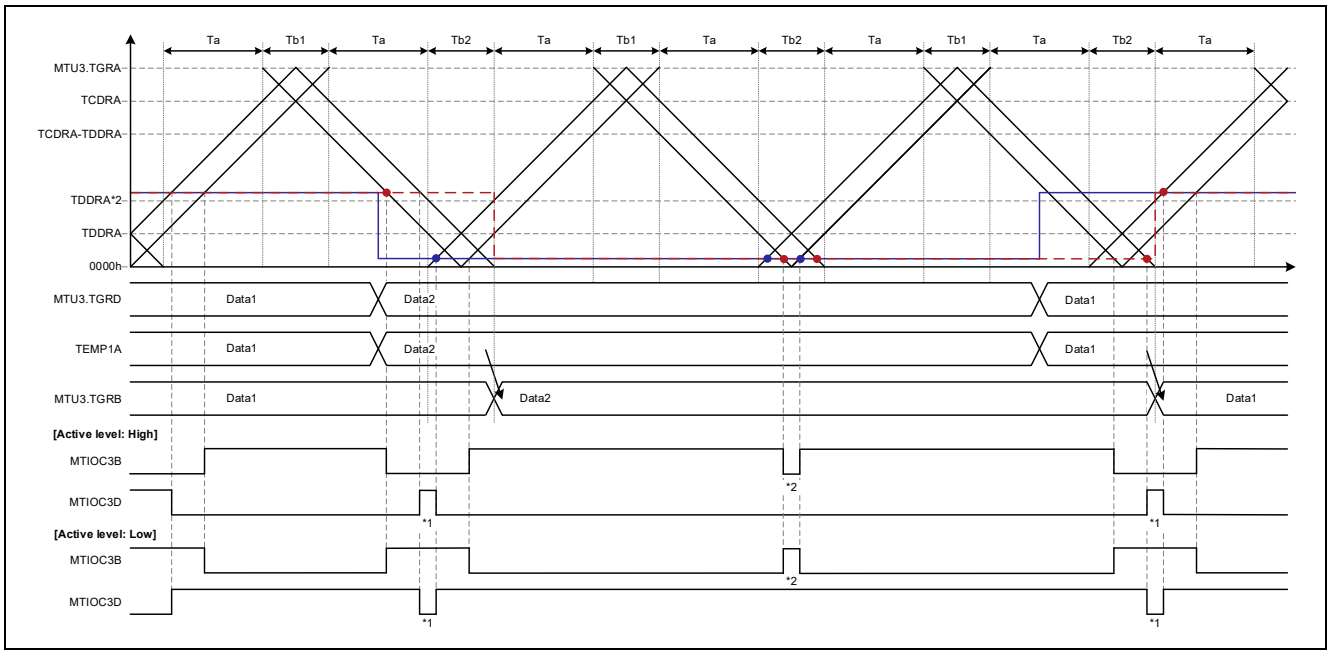


Figure 1.23 Complementary PWM Mode 2 Operation Example
(Output Start: Trough, Overwrite in Ta Interval, Duty: D → A → D)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.24 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.22.

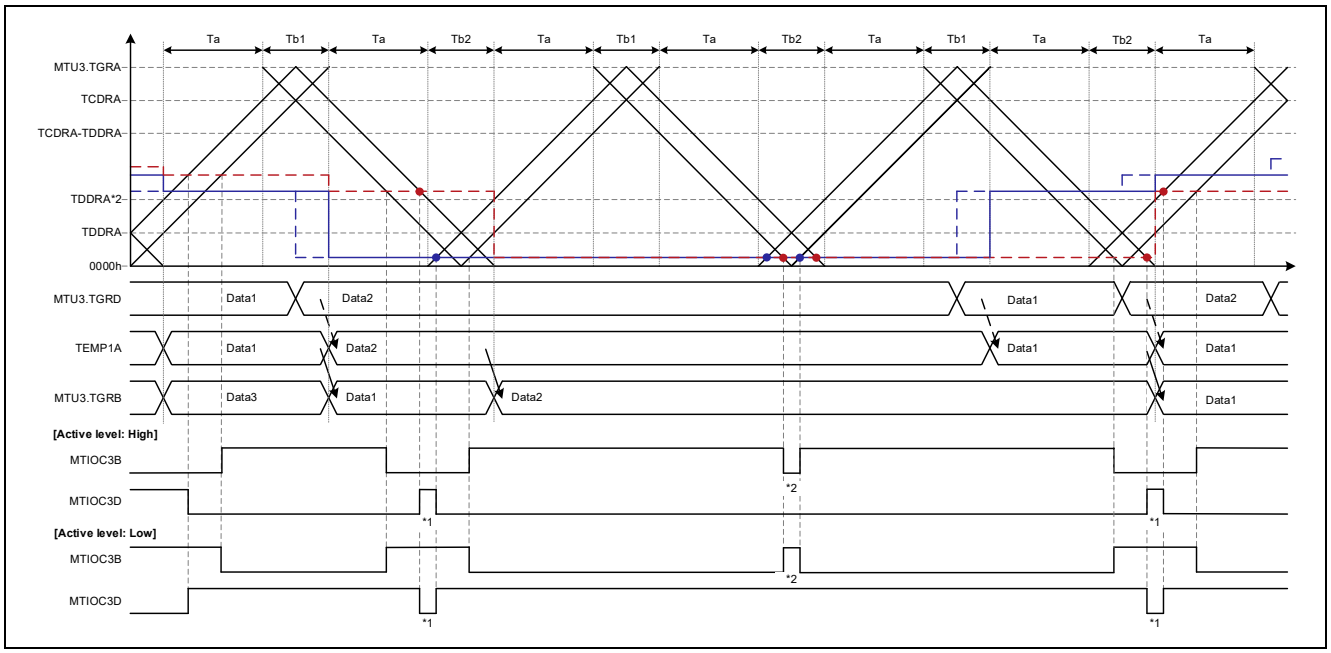


Figure 1.24 Complementary PWM Mode 3 Operation Example
(Output Start: Trough, Overwrite in Tb Interval, Duty: D → A → D)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.25 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.22.

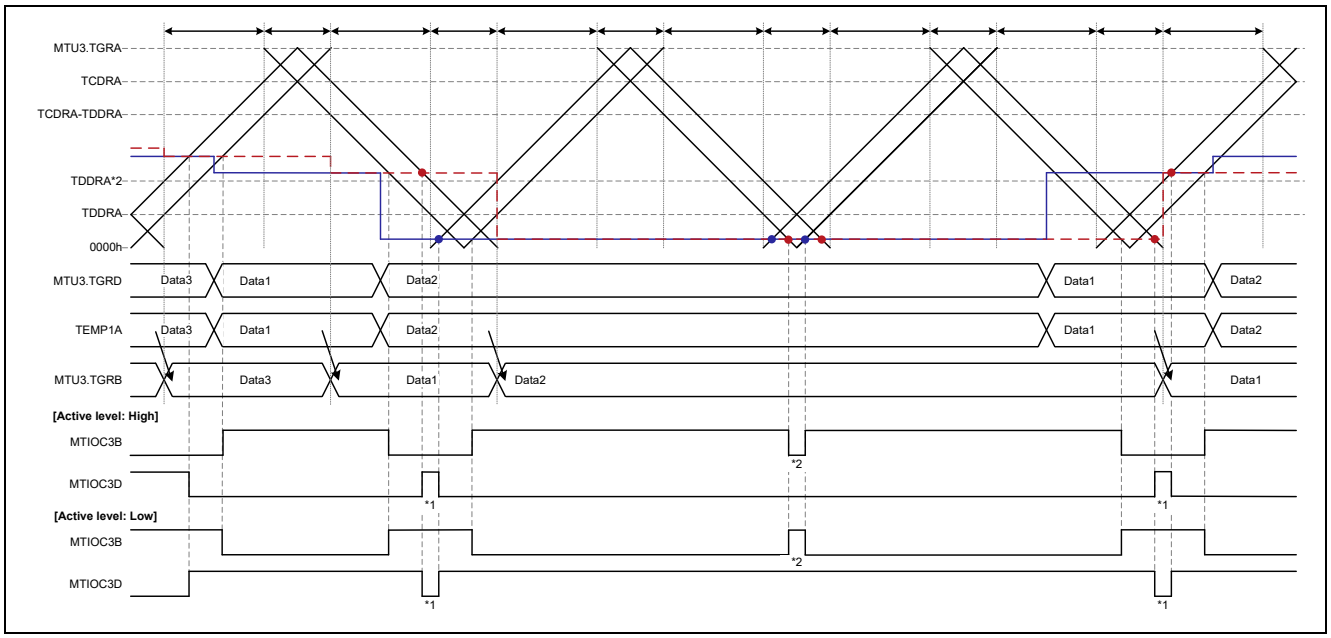


Figure 1.25 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → A → D)

1.3.1.2 Change from Near 100% to Near 100% (B → A → B)

Figure 1.26 to Figure 1.29 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.26, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, cautions 2 and 3
- [Operation example 2] Figure 1.27, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, cautions 2 and 3
- [Operation example 3] Figure 1.28, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, cautions 2 and 3
- [Operation example 4] Figure 1.29, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, cautions 2 and 3

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: B → A → B
  - B < TDDRA, B > A
  - A < TDDRA
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: B
  - Data 2: A
- Cautions
  2. The positive phase becomes minute pulses to the extent that the value A of is close to 0.
  3. The positive phase becomes minute pulses to the extent that the values of A and B are close to 0.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.26 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with temporary register, negative phase remains off.
(b) Compare match for on, but no change in negative phase because (a) off takes precedence.
(c) Compare match with temporary register, negative phase remains off.
(d) Compare match with compare register, positive phase turns off.
(e) Compare match with temporary register, positive phase turns on.
(f) Compare match for on, but no change in negative phase because (c) off takes precedence.
(g) Compare match with temporary register, negative phase remains off.
(h) Compare match for on, but no change in negative phase because (g) off takes precedence.

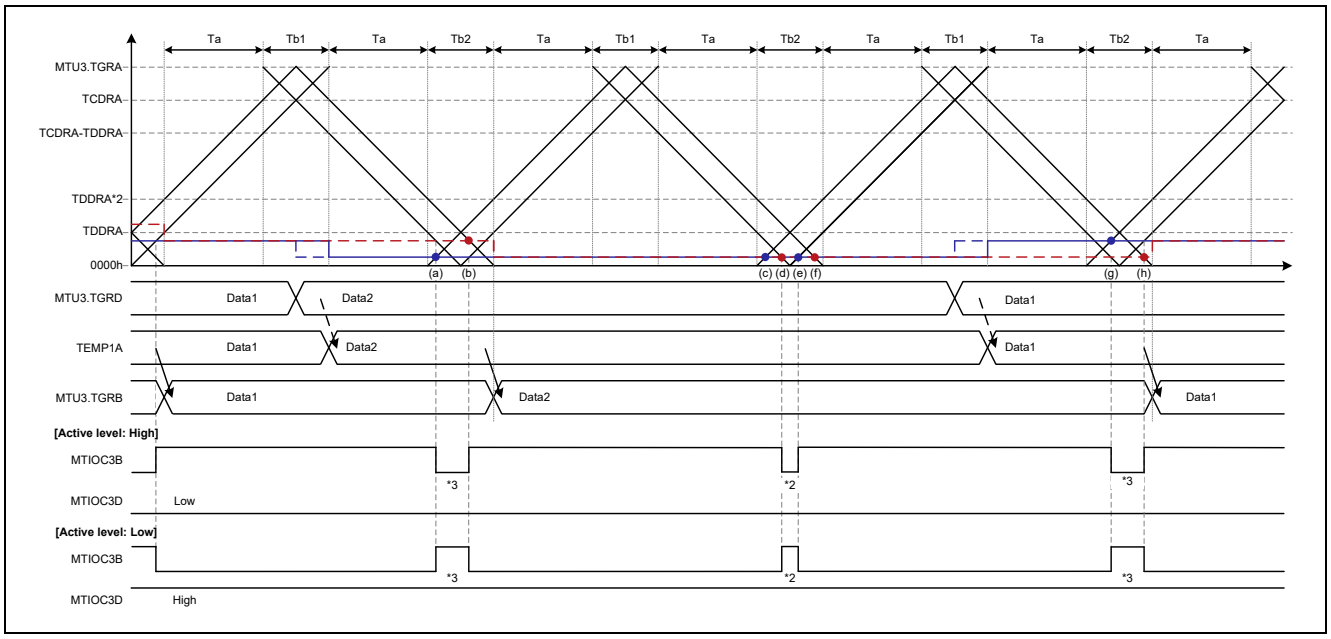


Figure 1.26 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: B → A → B)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.27 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.26.

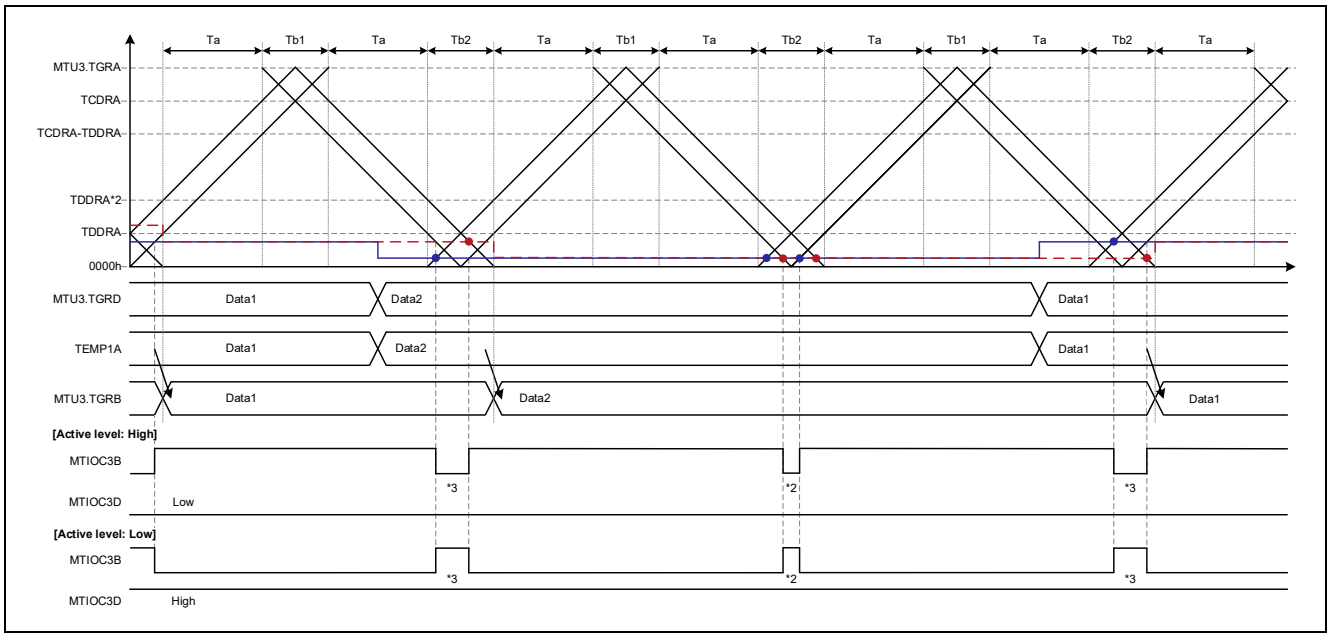


Figure 1.27 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: B → A → B)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.28 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.26.

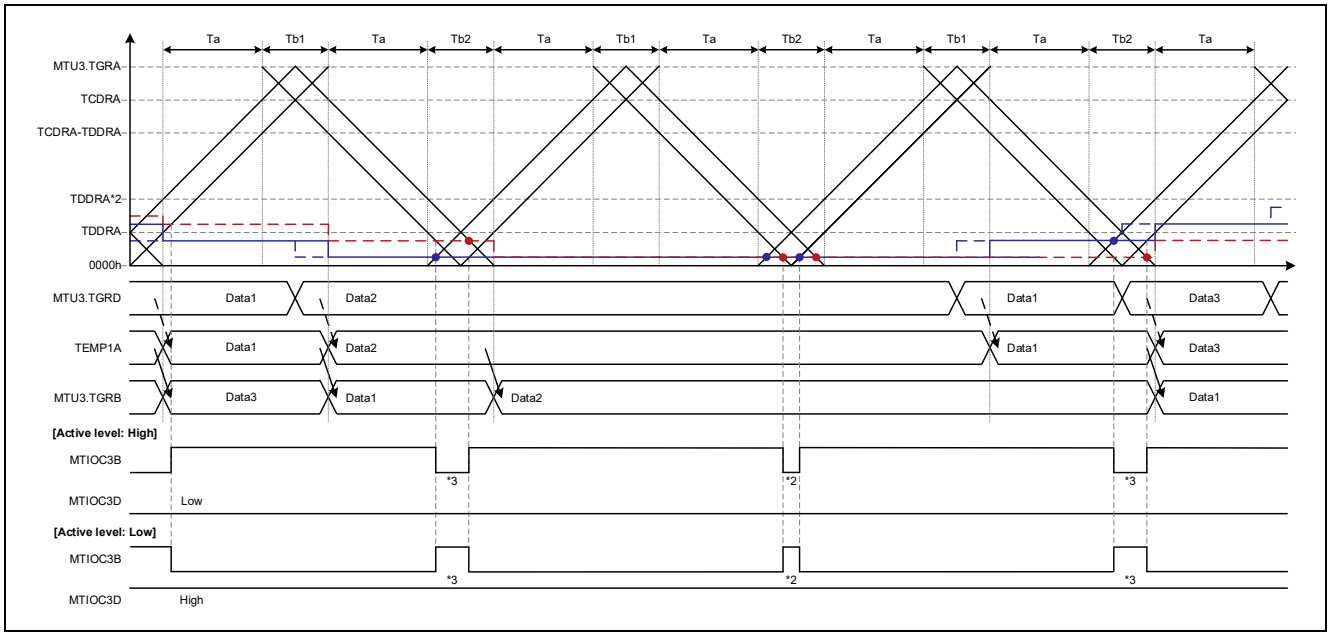


Figure 1.28 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: B → A → B)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.29 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.26.

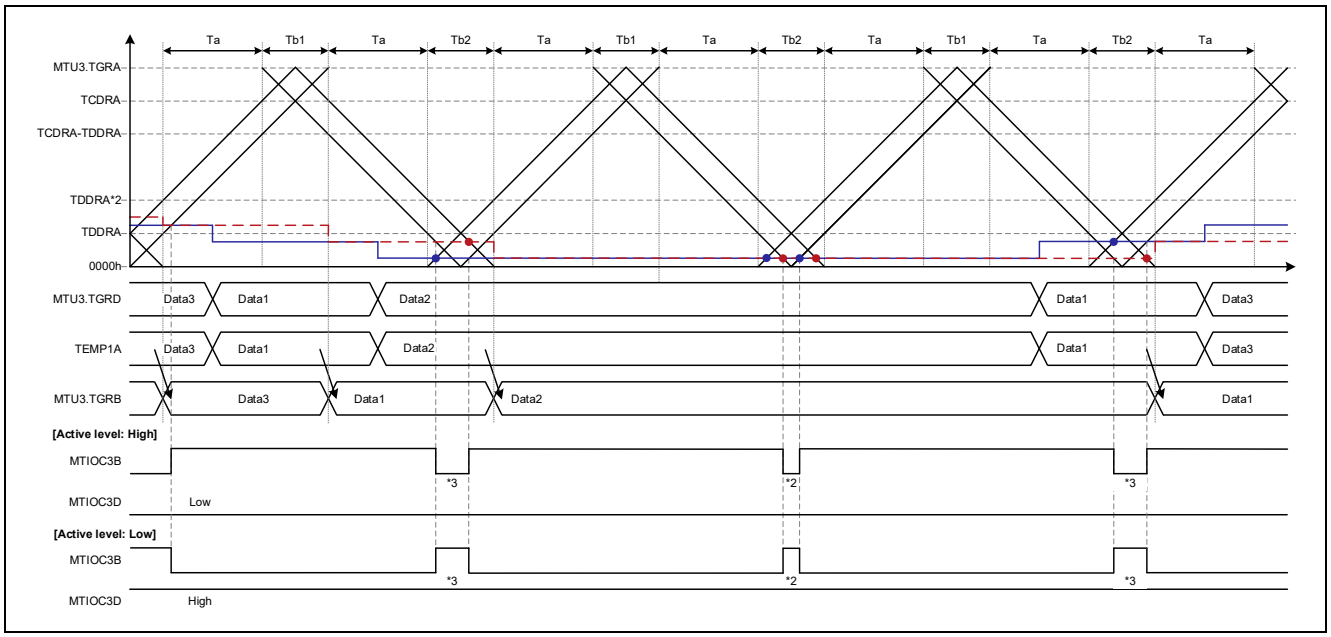


Figure 1.29 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: B → A → B)

1.3.1.3 Change from Near 100% to 100% (D → 100% → D)

Figure 1.30 to Figure 1.33 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.30, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 4
- [Operation example 2] Figure 1.31, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 4
- [Operation example 3] Figure 1.32, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 4
- [Operation example 4] Figure 1.33, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 4

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → 100% → D
  — B > TDDRA × 2

- Key to figures
  — Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  — Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  — Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  — Data 1: D
  — Data 2: 100% duty cycle compare value (0000h)

- Cautions
  4. The negative phase becomes minute pulses to the extent that the value of D is close to TDDRA × 2.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.30 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, negative phase turns on.
(b) Compare match with temporary register, negative phase turns off.
(c) Compare match with temporary register, negative phase remains off.
(d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in positive phase.
(e) Compare match for on, but no change in negative phase because (c) off takes precedence.
(f) Compare match with compare register, negative phase turns on.
(g) Compare match with compare register, negative phase turns off.

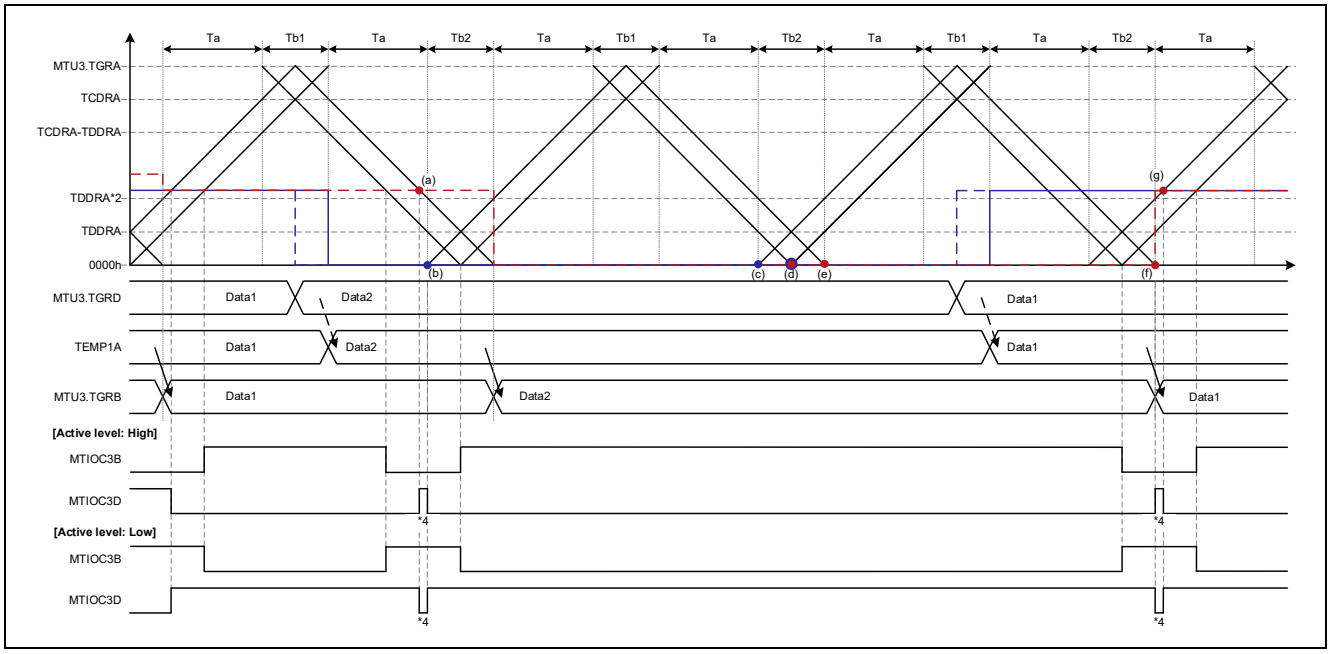


Figure 1.30 Complementary PWM Mode 2 Operation Example
(Output Start: Trough, Overwrite in Tb Interval, Duty: D → 100% → D)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.31 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.30.

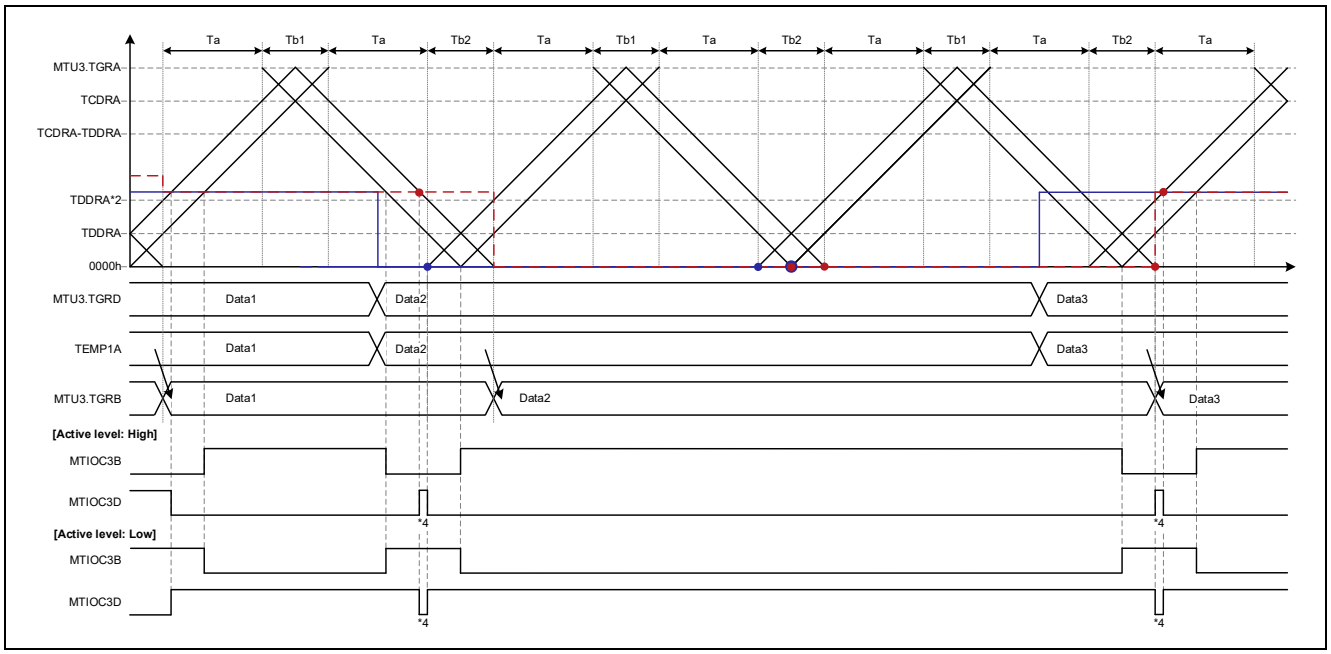


Figure 1.31 Complementary PWM Mode 2 Operation Example
(Output Start: Trough, Overwrite in Ta Interval, Duty: D → 100% → D)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.32 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing and transfer timing, the operation is the same as that shown in Figure 1.30.

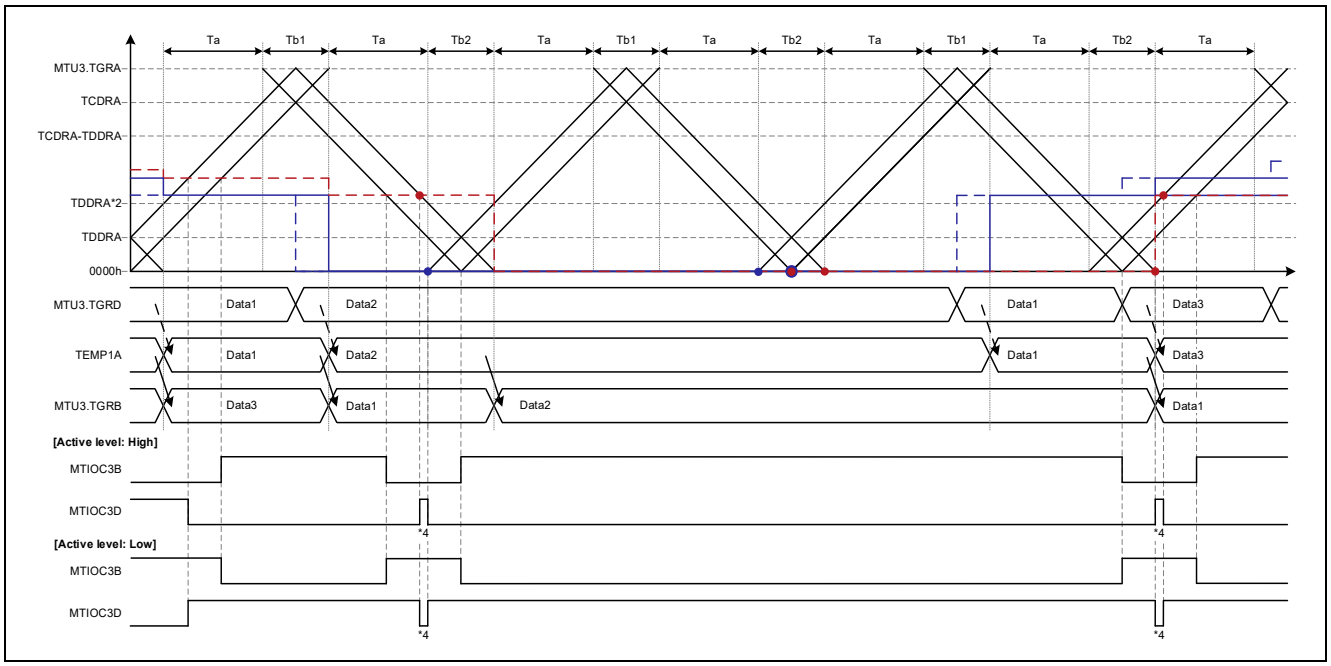


Figure 1.32 Complementary PWM Mode 3 Operation Example
(Output Start: Trough, Overwrite in Tb Interval, Duty: D → 100% → D)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.33 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.30.

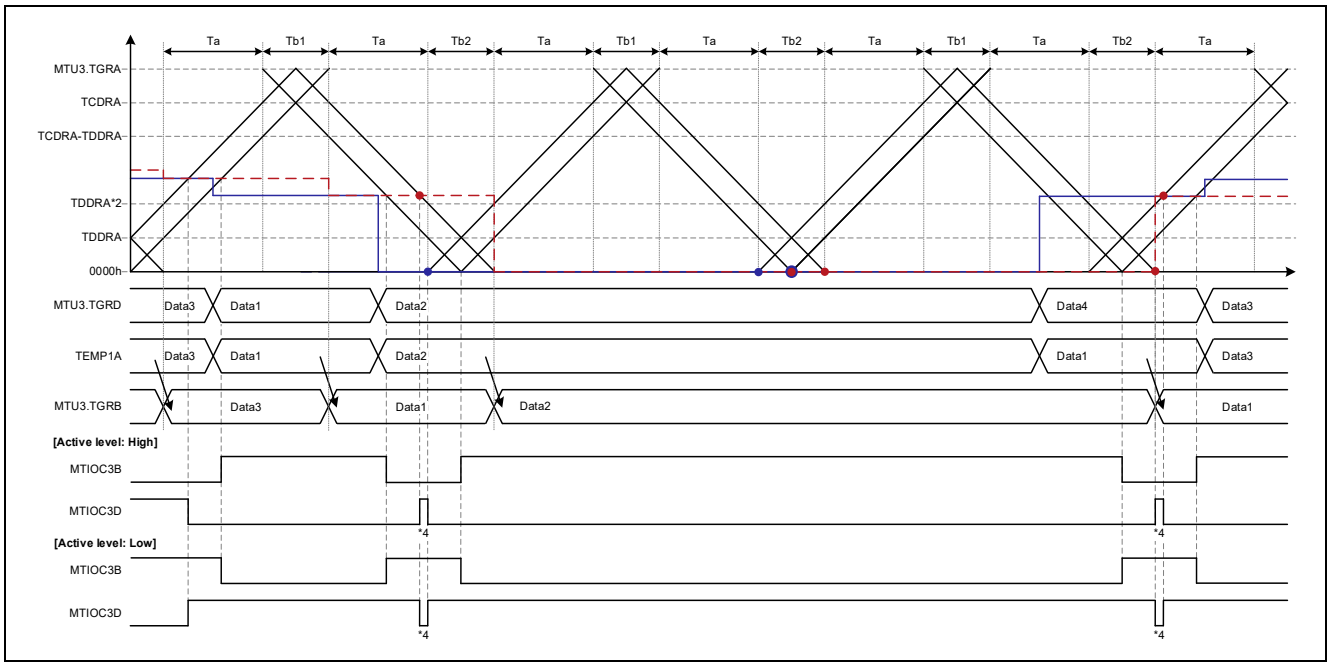


Figure 1.33 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → 100% → D)

1.3.1.4 Change from Near 100% to 100% (A → 100% → A)

Figure 1.34 to Figure 1.37 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.34, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 2
- [Operation example 2] Figure 1.35, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 2
- [Operation example 3] Figure 1.36, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 2
- [Operation example 4] Figure 1.37, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 2

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: A → 100% → A
  — A < TDDRA

- Key to figures
  — Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  — Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  — Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  — Data 1: A
  — Data 2: 100% duty cycle compare value (0000h)

- Cautions
  2. The positive phase becomes minute pulses to the extent that the value A of is close to 0.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.34 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with temporary register, negative phase remains off.
(b) Compare match with compare register, positive phase turns off.
(c) Compare match with temporary register, positive phase turns on.
(d) Compare match for on, but no change in negative phase because (a) off takes precedence.
(e) Compare match with temporary register, negative phase remains off.
(f) Simultaneous compare matches for on (blue dots) and off (red dots), no change in positive phase.
(g) Compare match for on, but no change in negative phase because (e) off takes precedence.
(h) Compare match with temporary register, negative phase remains off.
(i) Compare match with compare register, positive phase turns off.
(j) Compare match with temporary register, positive phase turns on.
(k) Compare match for on, but no change in negative phase because (h) off takes precedence.

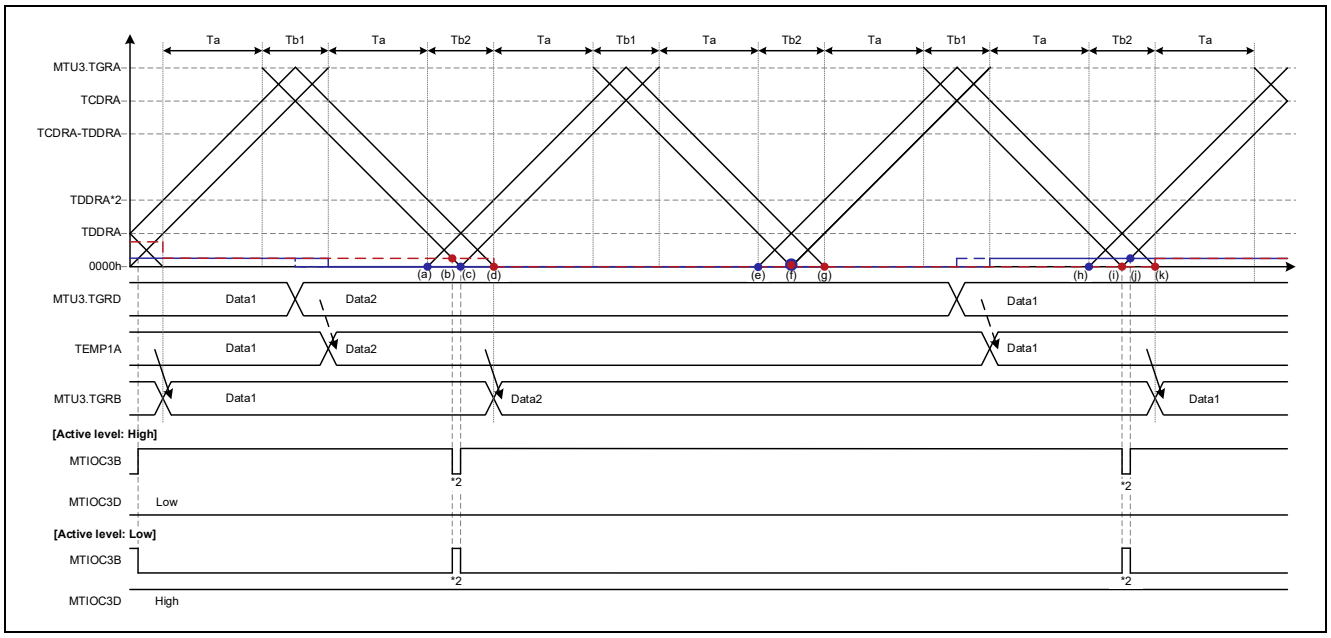


Figure 1.34 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: A → 100% → A)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.35 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.34.

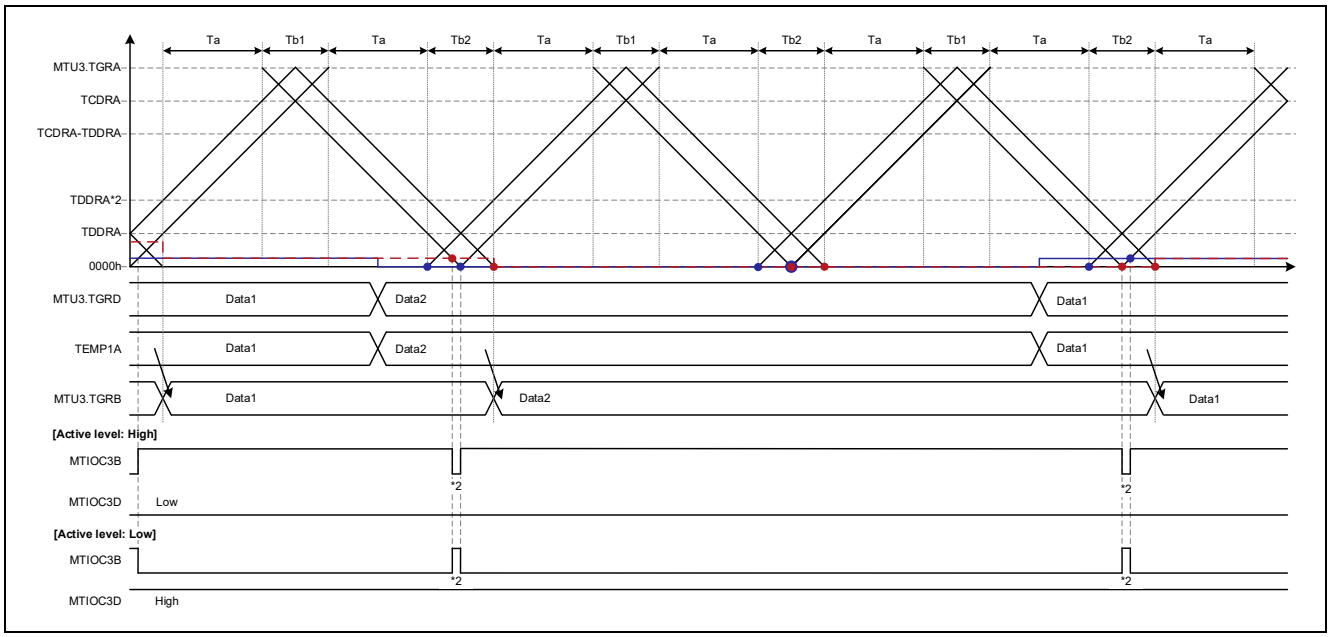


Figure 1.35 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: A → 100% → A)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.36 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.34.

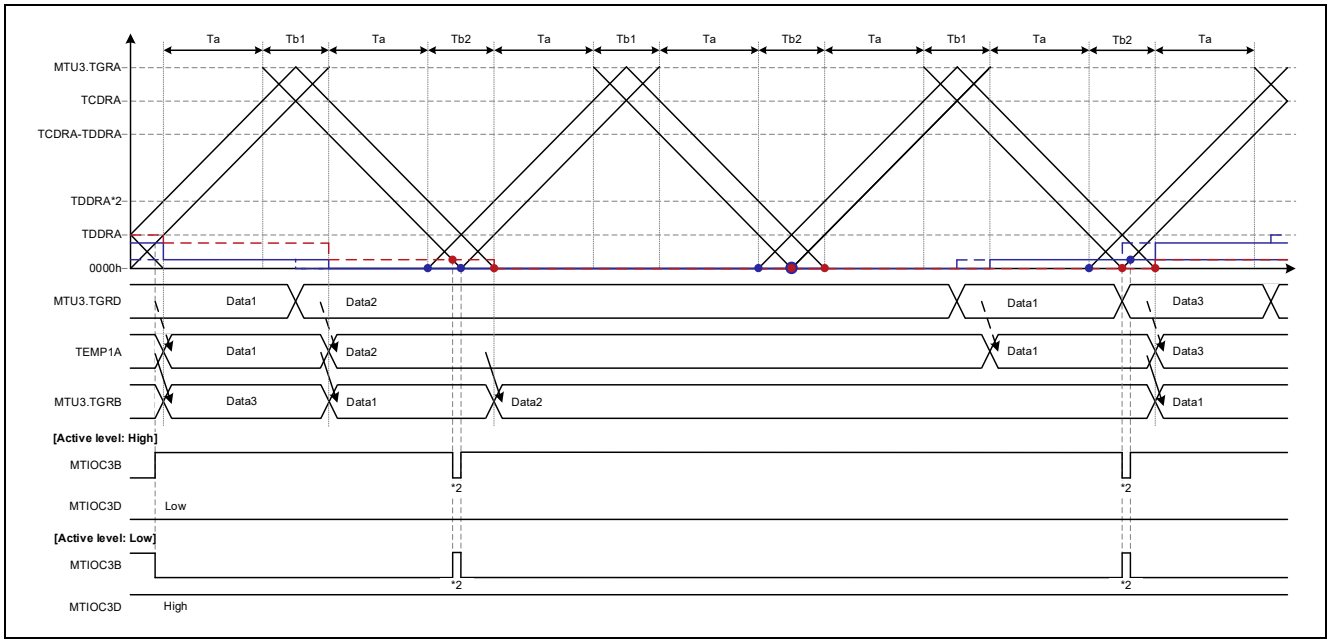


Figure 1.36 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: A → 100% → A)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.37 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.34.

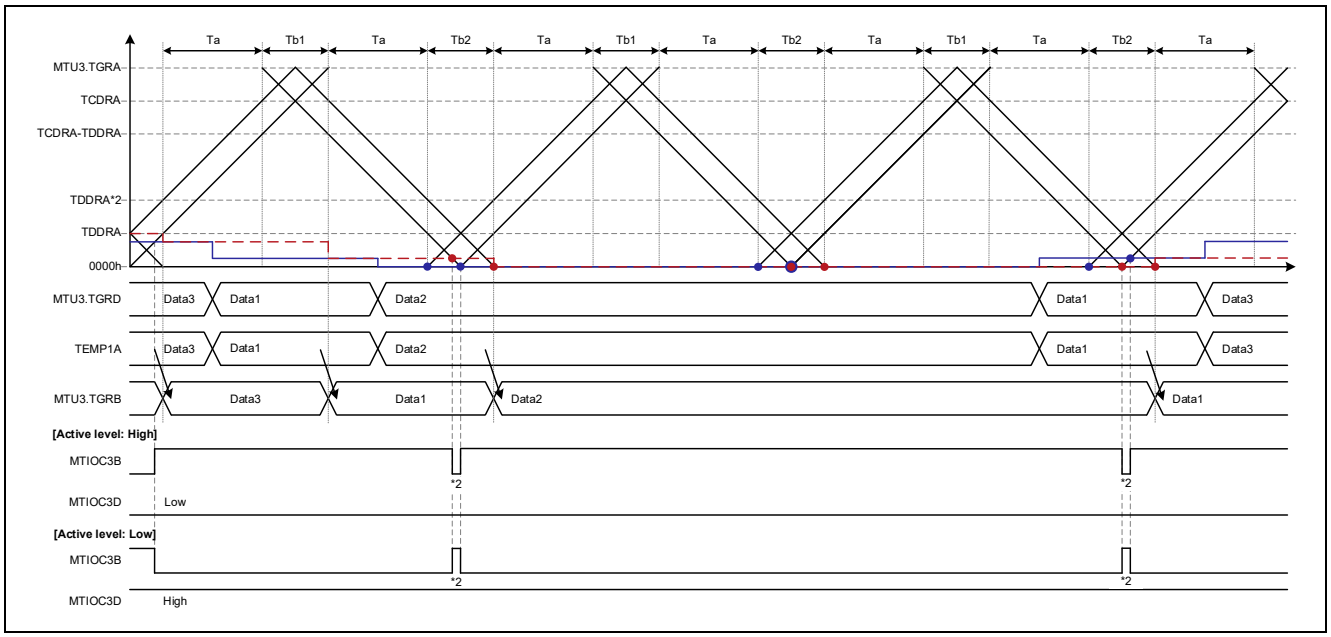


Figure 1.37 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: A → 100% → A)

1.3.1.5 Change to Near Dead Time Value (D → C → D)

Figure 1.38 to Figure 1.41 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.38, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 4
- [Operation example 2] Figure 1.39, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 4
- [Operation example 3] Figure 1.40, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 4
- [Operation example 4] Figure 1.41, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 4

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → C → D
  - D > TDDRA × 2
  - C < TCDRA × 2, C > TDDRA

- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: D
  - Data 2: C

- Cautions
  4. The negative phase becomes minute pulses to the extent that the value of D is close to TDDRA × 2.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.38 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, negative phase turns on.
(b) Compare match with temporary register, negative phase turns off.

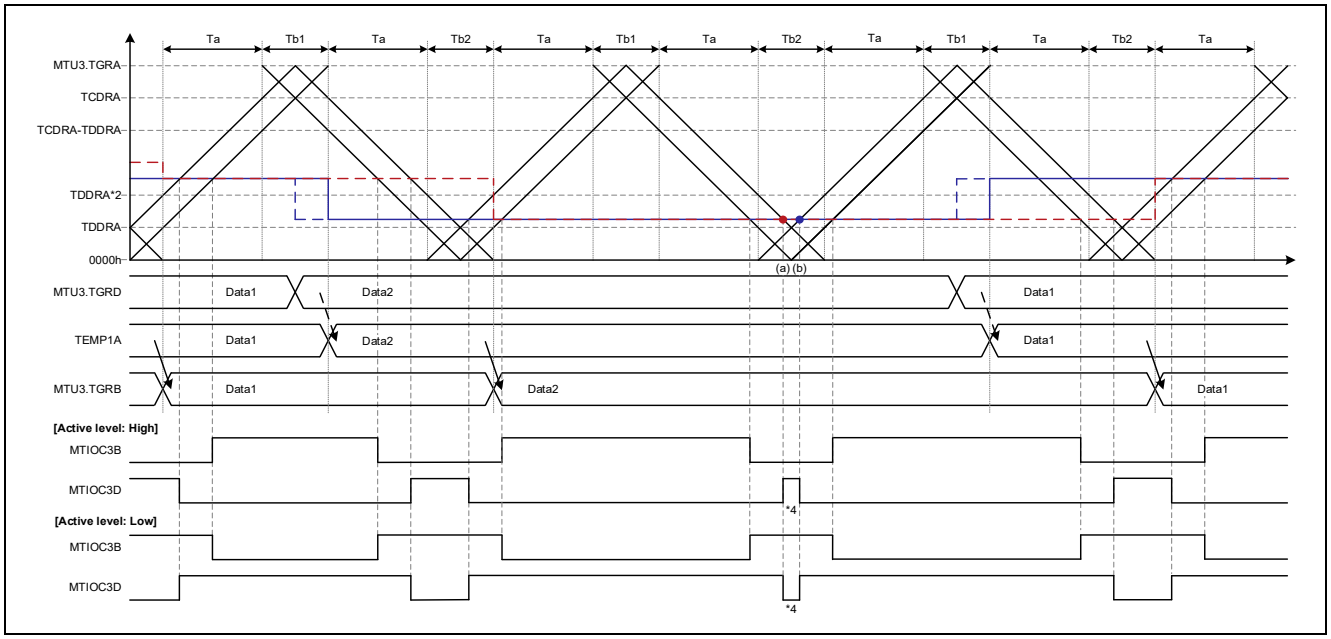


Figure 1.38 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → C → D)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.39 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.38.

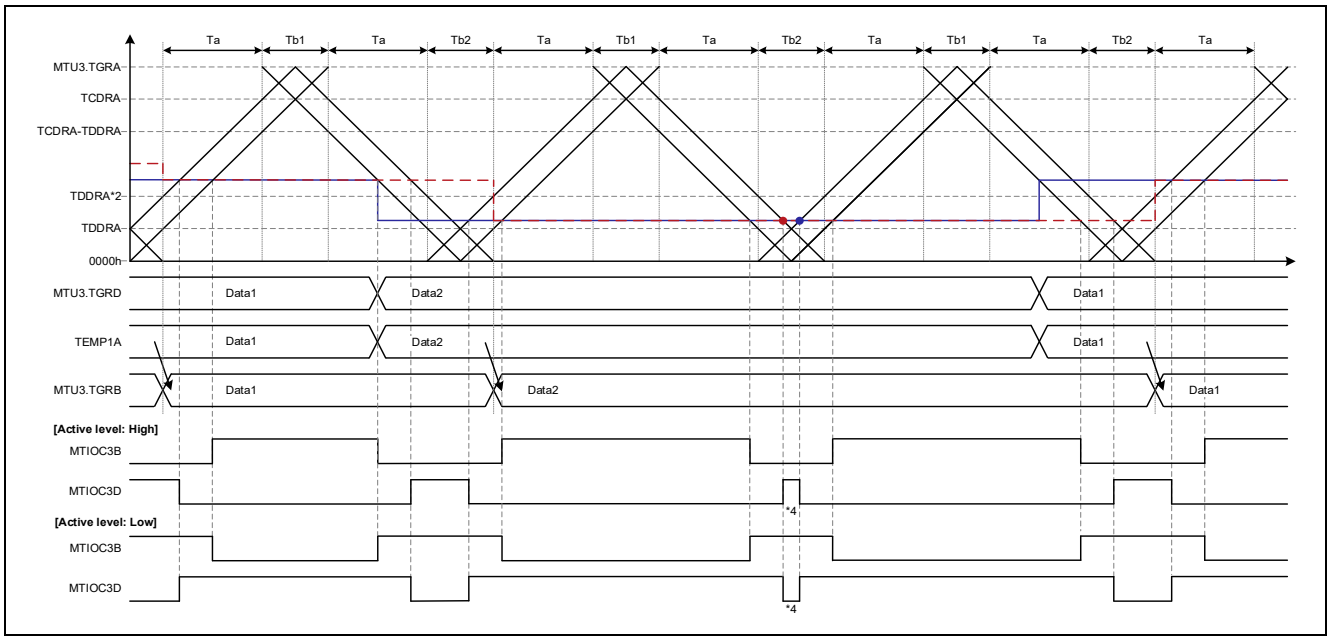


Figure 1.39 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → C → D)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.40 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, negative phase turns on.
(b) Compare match with temporary register, negative phase turns off.

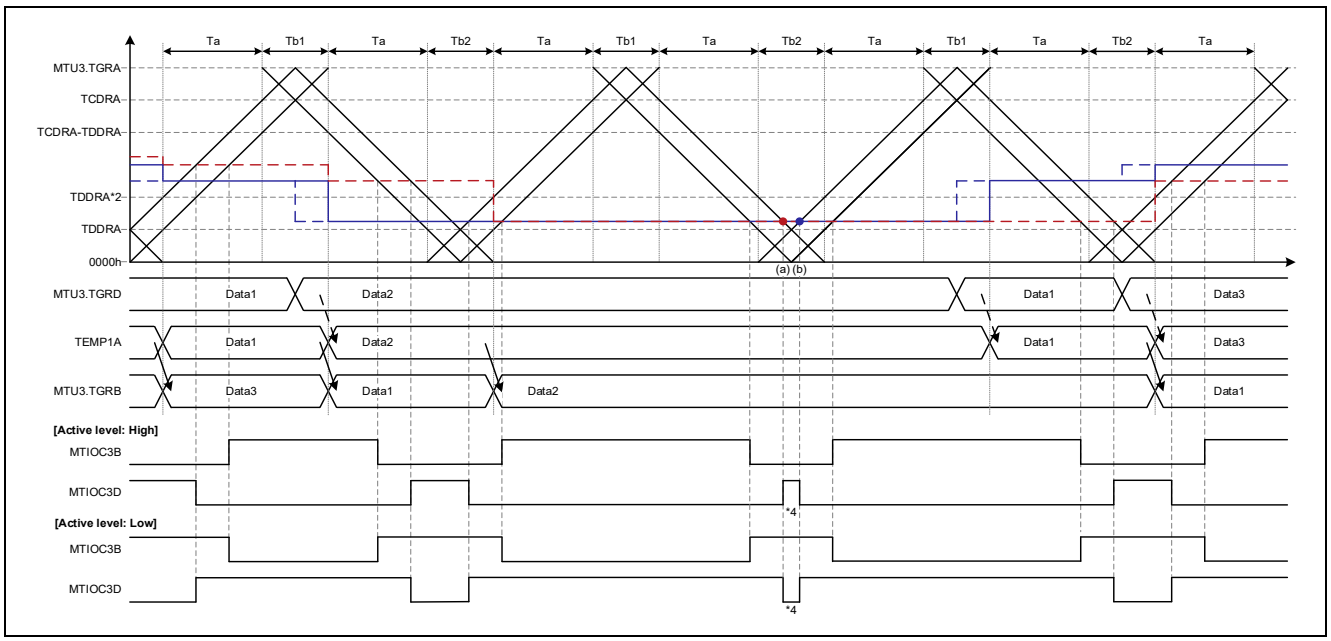


Figure 1.40 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → C → D)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.41 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.40.

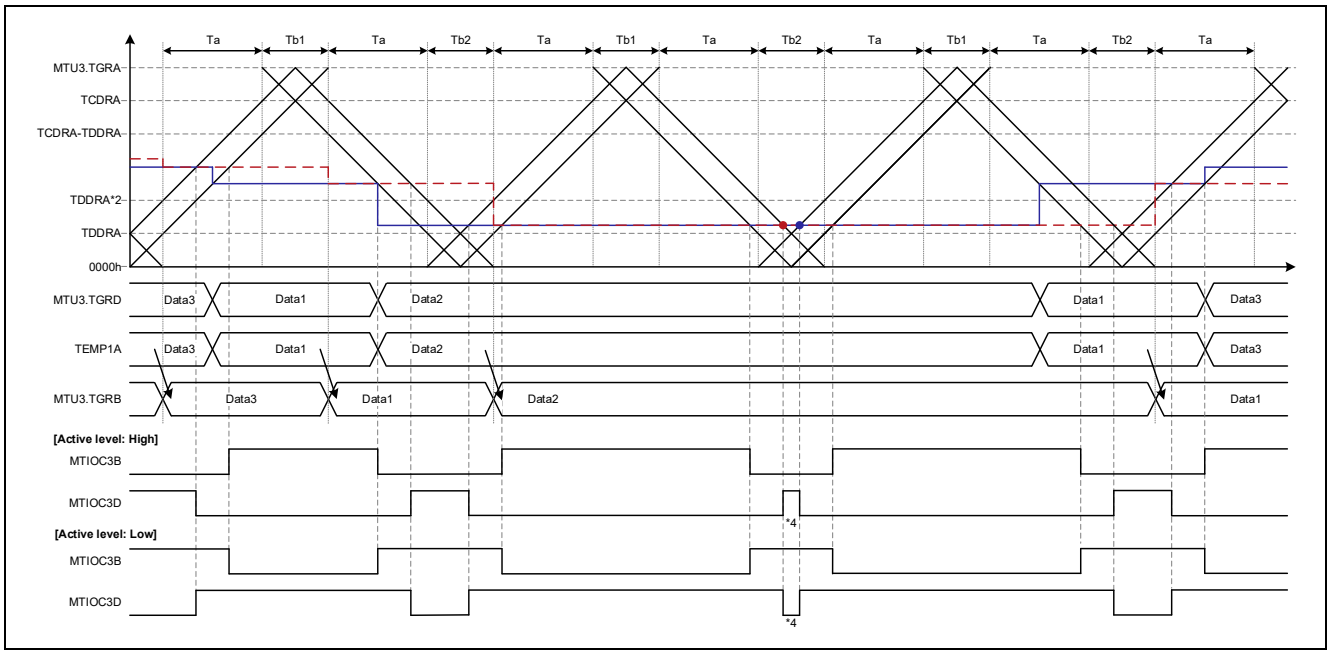


Figure 1.41 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → C → D)

1.3.1.6 Change from Near 0% to Near 0% (D → F → D)

Figure 1.42 to Figure 1.45 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.42, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, cautions 6 and 8
- [Operation example 2] Figure 1.43, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, cautions 6 and 8
- [Operation example 3] Figure 1.44, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, cautions 6 and 8
- [Operation example 4] Figure 1.45, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, cautions 6 and 8

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → F → D
  - D < TCDRA – TDDRA
  - F < TCDRA
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: D
  - Data 2: F
- Cautions
  6. The positive phase becomes minute pulses to the extent that the value of F is close to TCDRA.
  8. When the value of D is close to TCDRA − TDDRA, the positive phase becomes minute pulses the smaller the value of TDDRA is.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.42 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with compare register, positive phase turns off.
(c) Compare match with compare register, positive phase turns on.
(d) Compare match with temporary register, positive phase turns off.

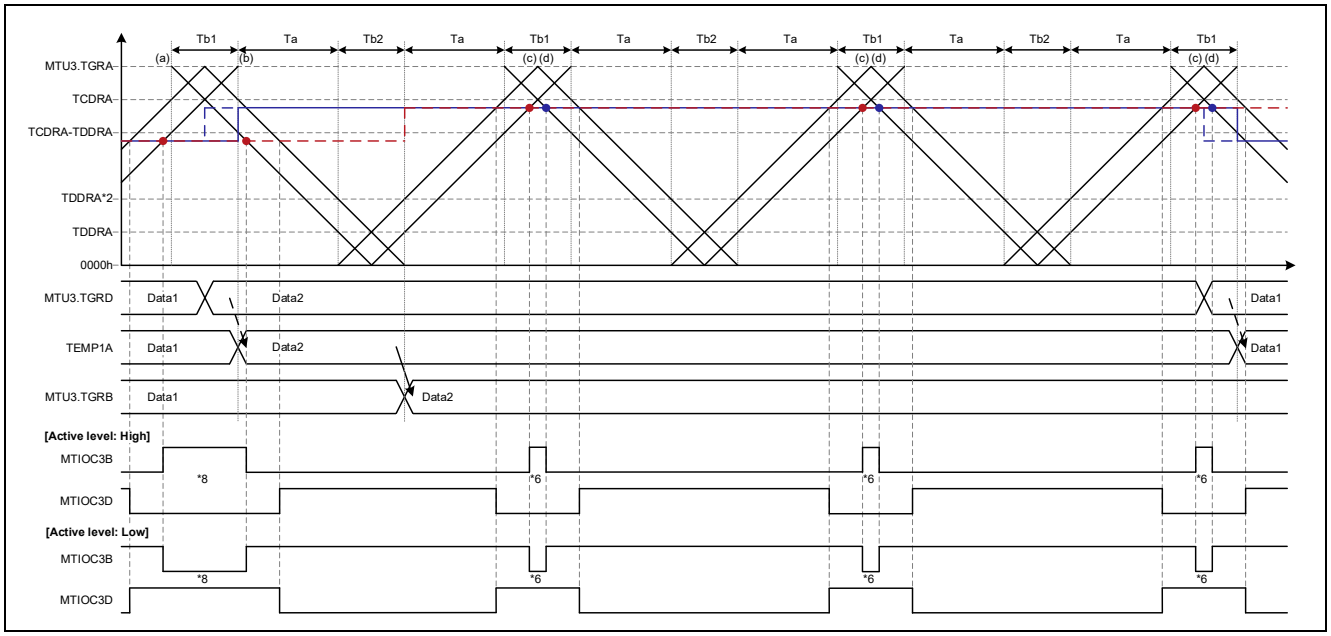


Figure 1.42 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → F → D)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.43 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.42.

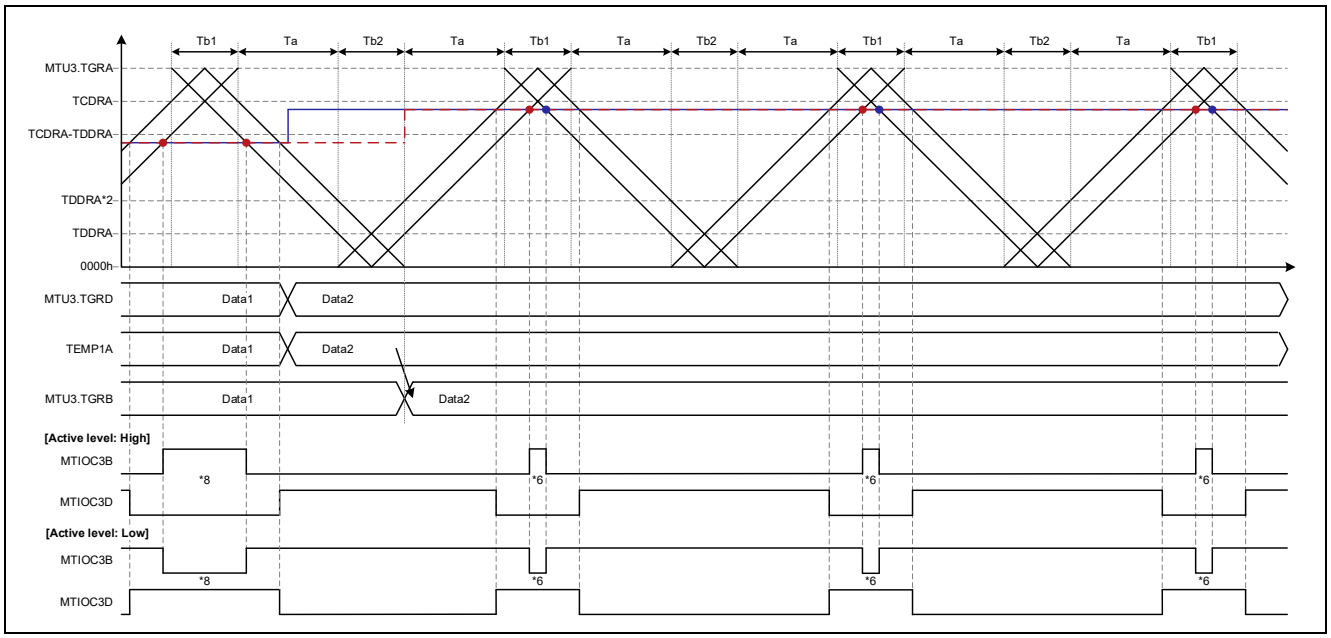


Figure 1.43 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → F → D)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.44 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with compare register, positive phase turns on.
(d) Compare match with temporary register, positive phase turns off.
(e) Compare match with compare register, positive phase turns on.
(f) Compare match with compare register, positive phase turns off.

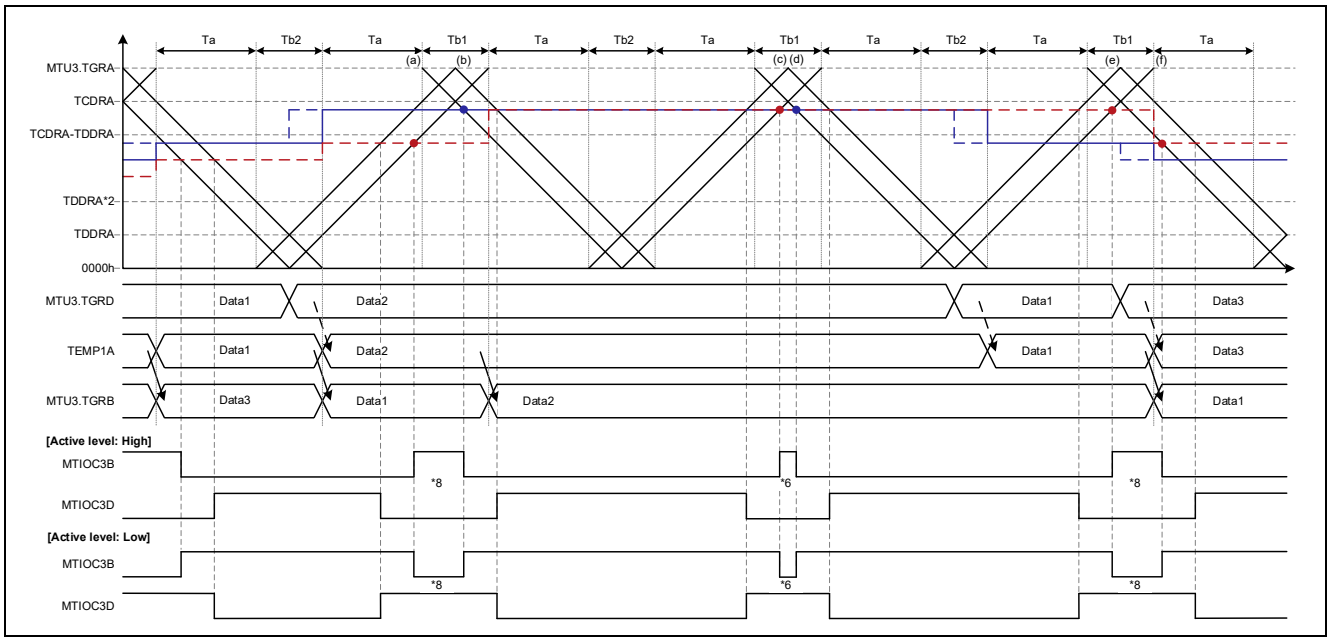


Figure 1.44 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → F → D)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.45 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.44.

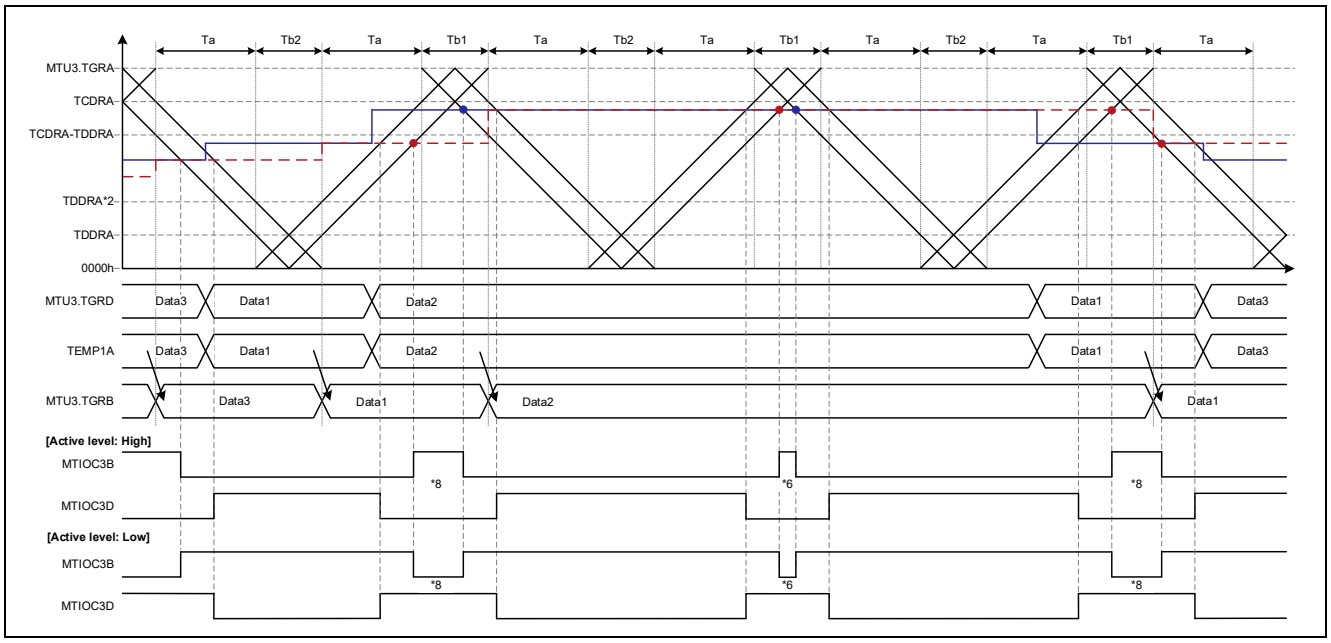


Figure 1.45 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → F → D)

1.3.1.7 Change from Near 0% to Near 0% (E → F → E)

Figure 1.46 to Figure 1.49 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.46, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, cautions 6 and 7
- [Operation example 2] Figure 1.47, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, cautions 6 and 7
- [Operation example 3] Figure 1.48, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, cautions 6 and 7
- [Operation example 4] Figure 1.49, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, cautions 6 and 7

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: E → F → E
  - E < TCDRA, E < F
  - F < TCDRA
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: E
  - Data 2: F
- Cautions
  6. The positive phase becomes minute pulses to the extent that the value of F is close to TCDRA.
  7. The positive phase becomes minute pulses to the extent that the value of E is close to TCDRA.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.46 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with compare register, positive phase turns on.
(d) Compare match with temporary register, positive phase turns off.

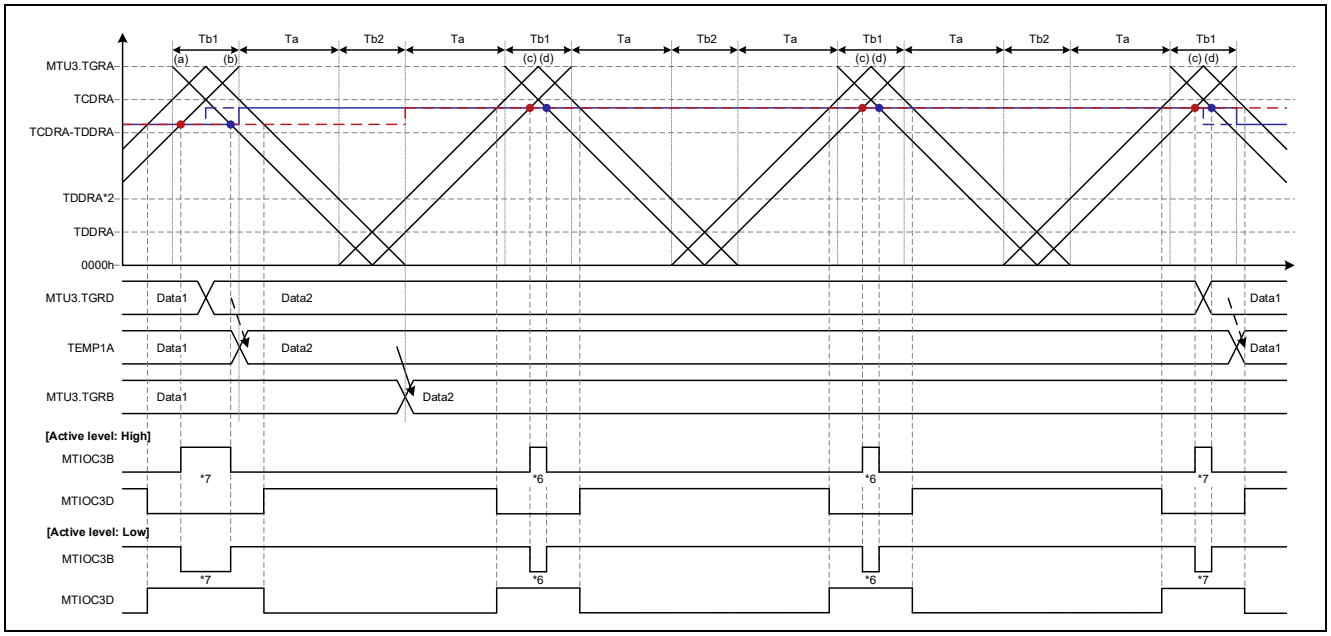


Figure 1.46 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: E → F → E)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.47 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.46.

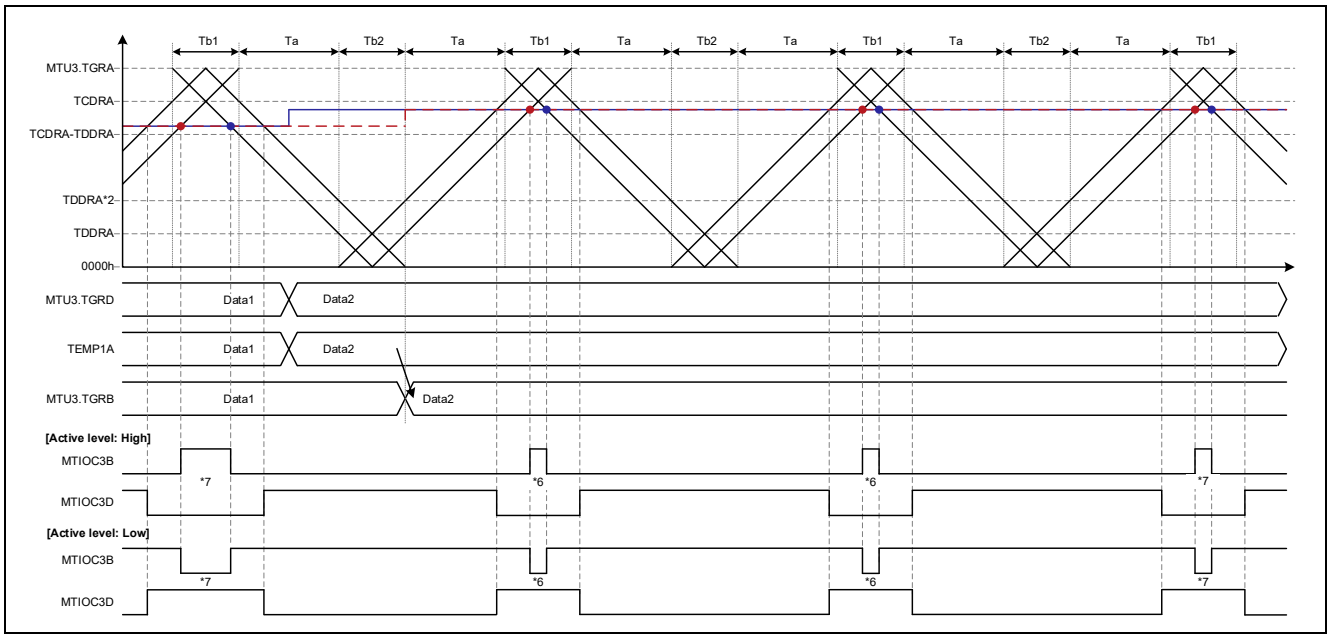


Figure 1.47 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: E → F → E)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.48 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with compare register, positive phase turns on.
(d) Compare match with temporary register, positive phase turns off.
(e) Compare match with compare register, positive phase turns on.
(f) Compare match with temporary register, positive phase turns off.

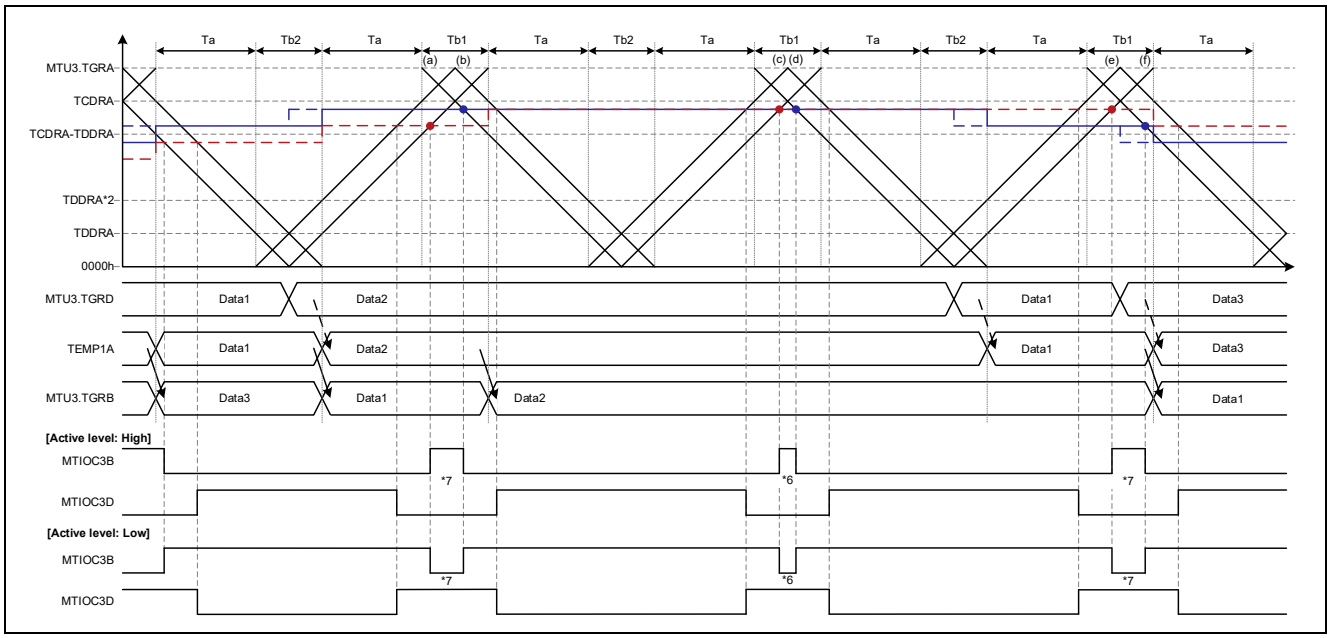


Figure 1.48 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: E → F → E)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.49 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.48.

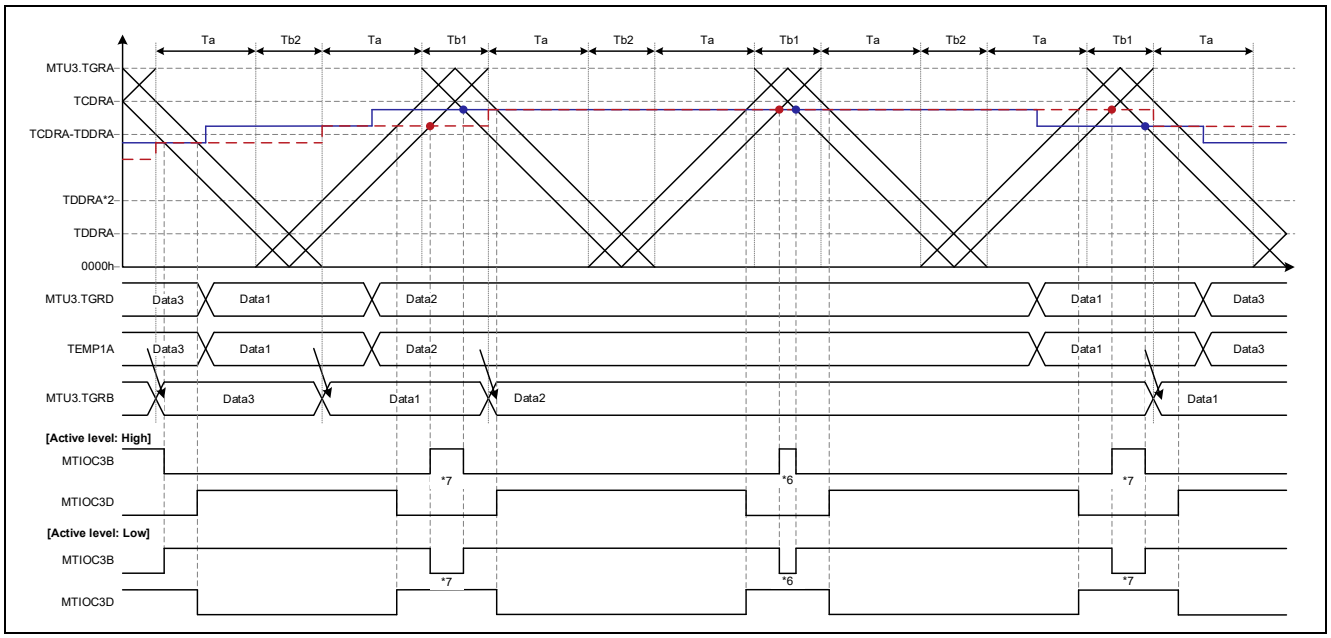


Figure 1.49 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: E → F → E)

1.3.1.8 Change from Near 0% to 0% (D → 0% → D)

Figure 1.50 to Figure 1.53 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.50, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 8
- [Operation example 2] Figure 1.51, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 8
- [Operation example 3] Figure 1.52, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 5
- [Operation example 4] Figure 1.53, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 5

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → 0% → D
  - D < TCDRA – TDDRA

- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: D
  - Data 2: 0% duty cycle compare value (same value as MTU3.TGRA)

- Cautions
  5. The positive phase becomes minute pulses to the extent that the value of D is close to TCDRA − TDDRA.
  8. When the value of D is close to TCDRA − TDDRA, the positive phase becomes minute pulses the smaller the value of TDDRA is.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.50 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with compare register, positive phase turns off.
(c) Compare match with temporary register, positive phase remains off.
(d) Simultaneous compare matches for on (red dots) and off (blue dots), no change in negative phase.
(e) Compare match for on, but no change in positive phase because (c) off takes precedence.

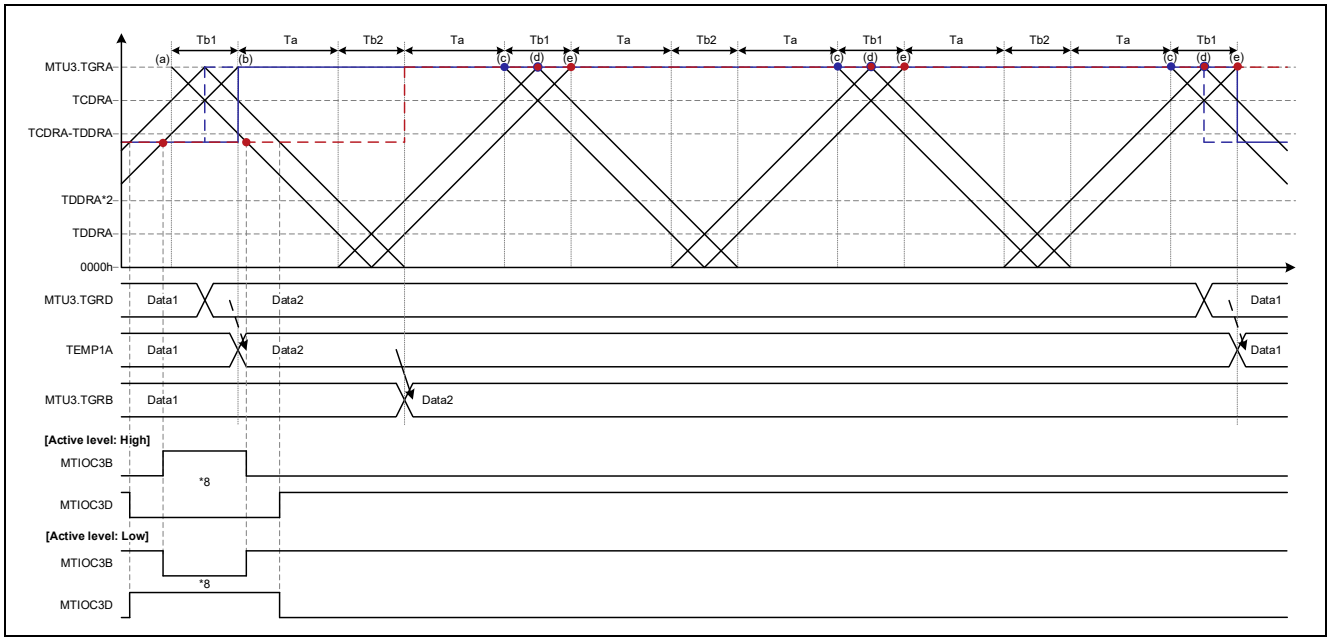


Figure 1.50 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: D → 0% → D)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.51 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.50.

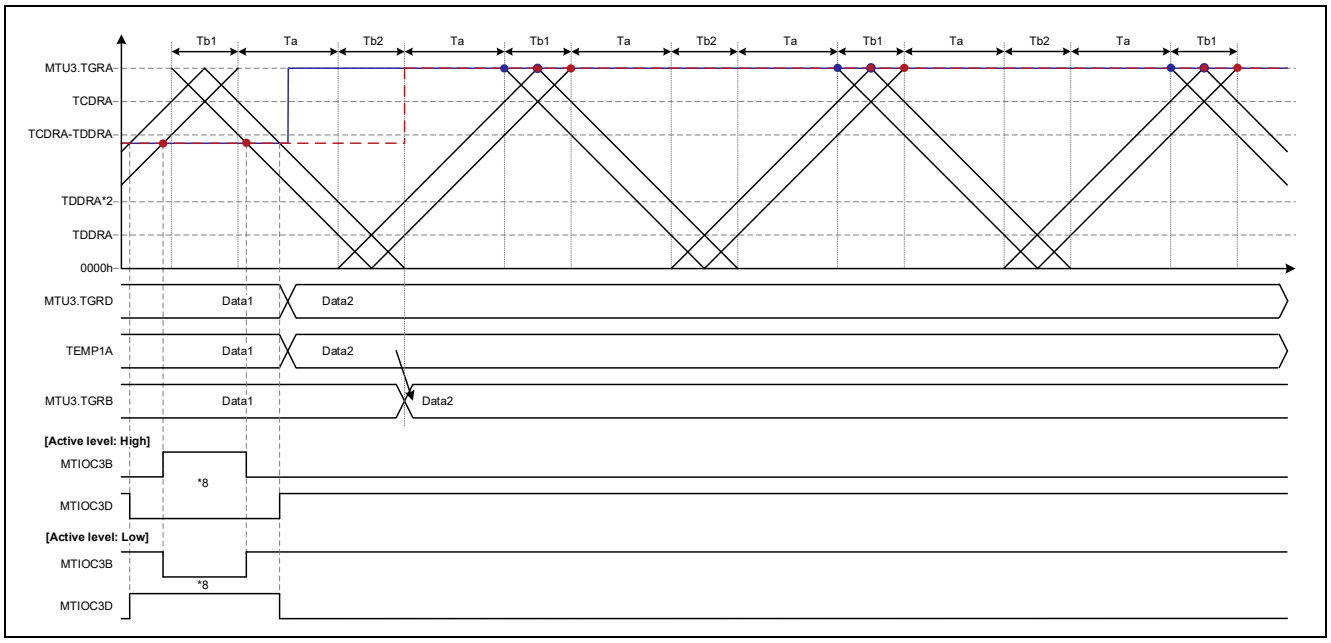


Figure 1.51 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → 0% → D)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.52 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with temporary register, positive phase remains off.
(d) Simultaneous compare matches for on (red dots) and off (blue dots), no change in negative phase.
(e) Compare match for on, but no change in positive phase because (c) off takes precedence.
(f) Compare match with compare register, positive phase turns on.
(g) Compare match with compare register, positive phase turns off.

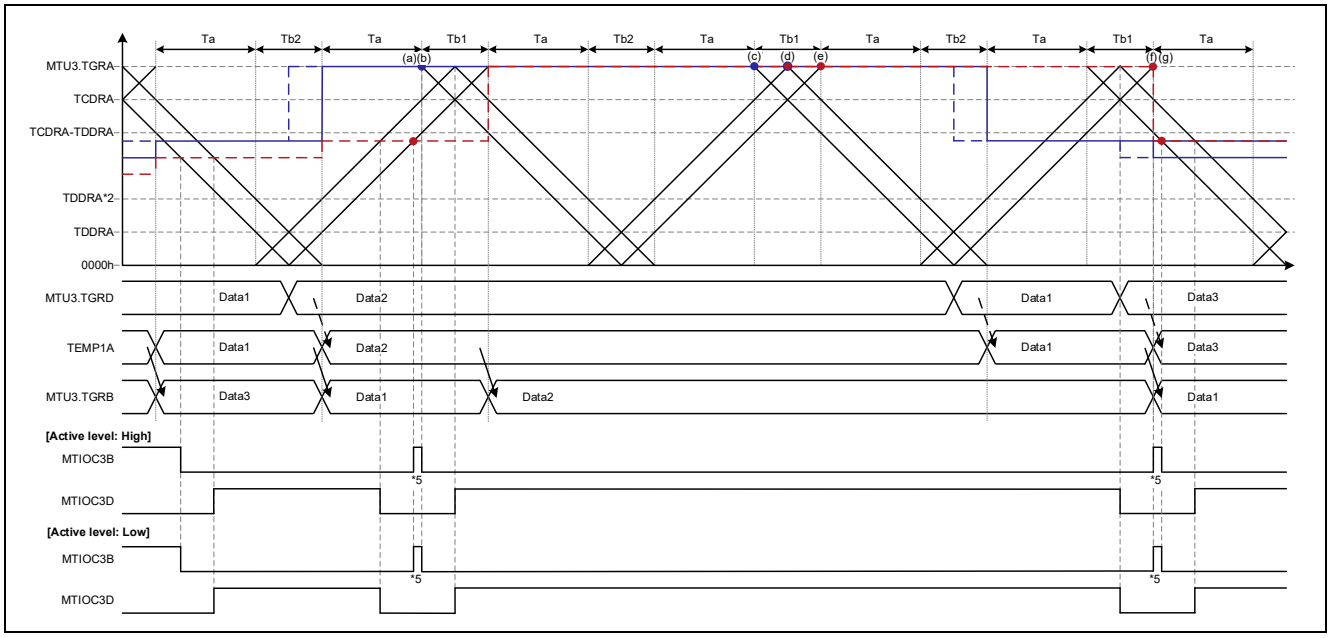


Figure 1.52 Complementary PWM Mode 3 Operation Example
(Output Start: Trough, Overwrite in Tb Interval, Duty: D → 0% → D)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.53 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.52.

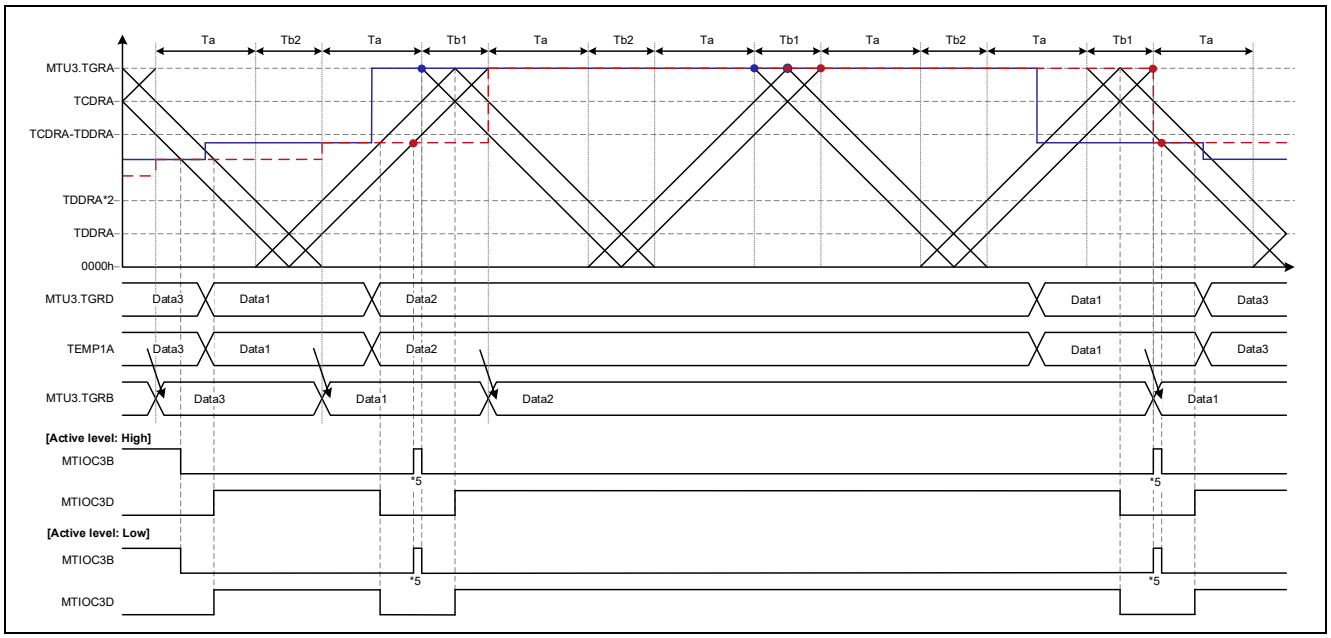


Figure 1.53 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: D → 0% → D)

1.3.1.9 Change from Near 0% to 0% (F → 0% → F)

Figure 1.54 to Figure 1.57 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.54, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 6
- [Operation example 2] Figure 1.55, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 6
- [Operation example 3] Figure 1.56, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 9
- [Operation example 4] Figure 1.57, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 9

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: F → 0% → F
  - F < TCDRA, F > TCDRA – TCDRA

- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: F
  - Data 2: 0% duty cycle compare value (same value as MTU3.TGRA)

- Cautions
  6. The positive phase becomes minute pulses to the extent that the value of F is close to TCDRA.
  9. The negative phase becomes minute pulses to the extent that the value of F is close to TCDRA.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.54 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with temporary register, positive phase remains off.
(d) Simultaneous compare matches for on (red dots) and off (blue dots), no change in negative phase.
(e) Compare match for on, but no change in positive phase because (c) off takes precedence.

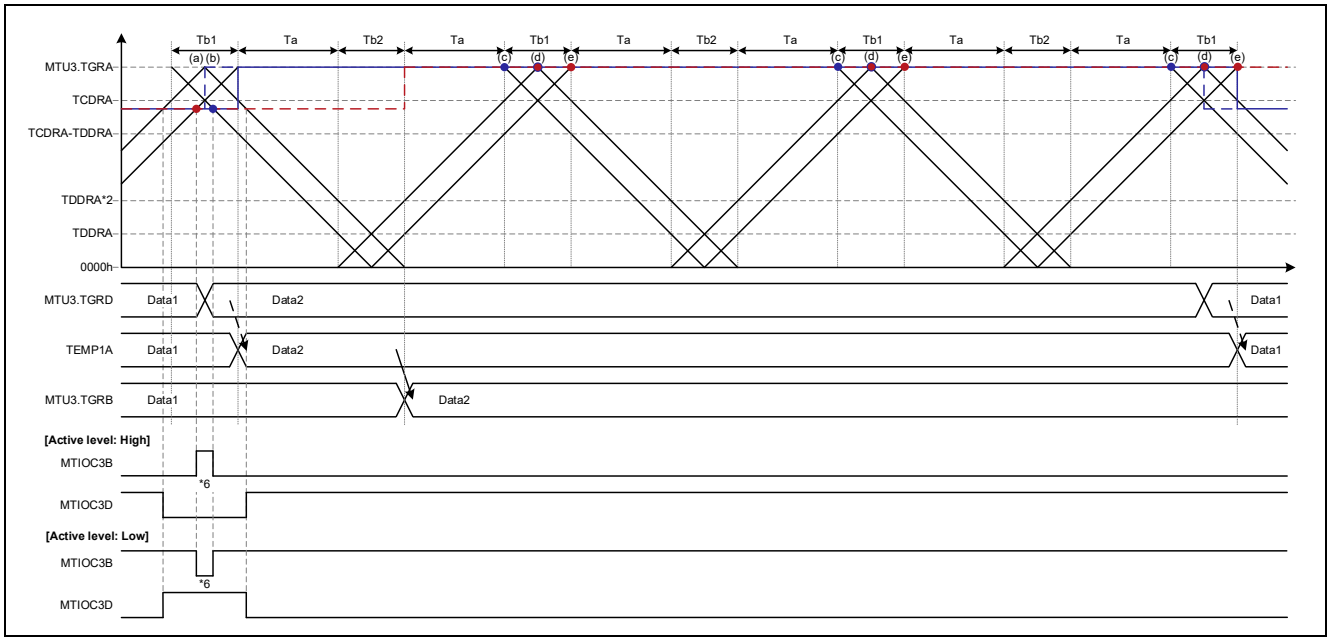


Figure 1.54 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: F → 0% → F)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.55 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.54.

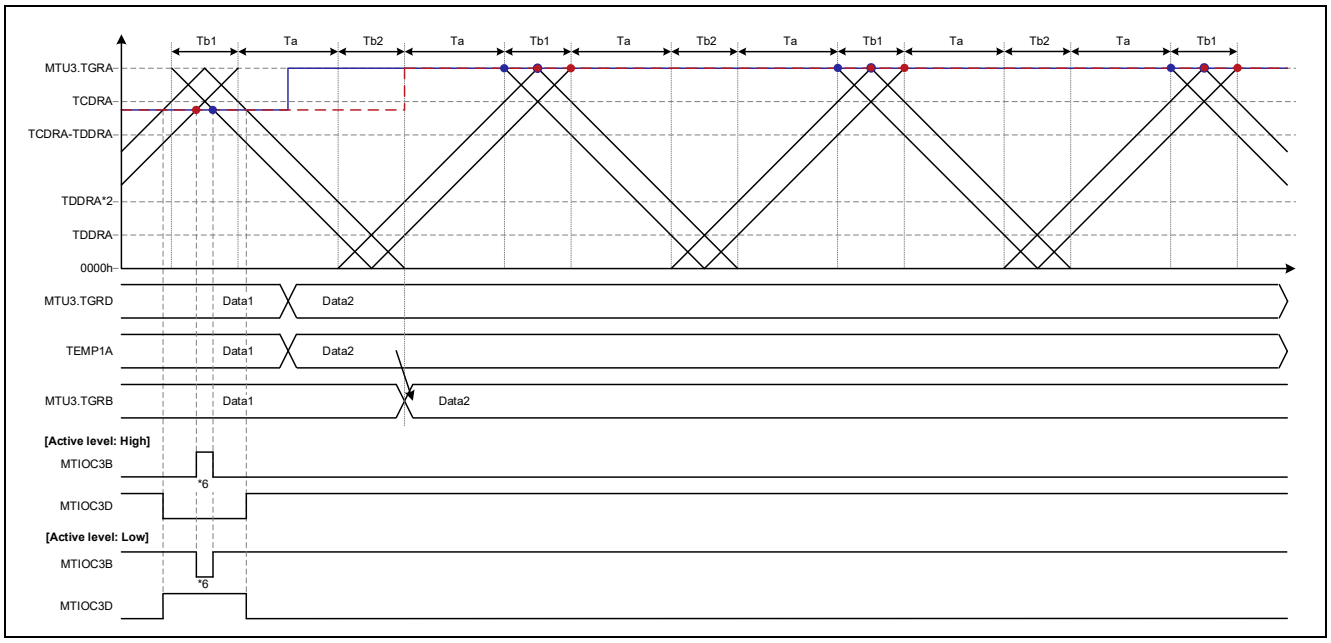


Figure 1.55 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: F → 0% → F)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.56 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, negative phase turns off.
(b) Compare match with temporary register, positive phase remains off.
(c) Compare match for on, but no change in positive phase because (b) off takes precedence.
(d) Compare match with temporary register, negative phase turns on.
(e) Compare match with temporary register, positive phase remains off.
(f) Simultaneous compare matches for on (red dots) and off (blue dots), no change in negative phase.
(g) Compare match for on, but no change in positive phase because (e) off takes precedence.
(h) Compare match with compare register, negative phase turns off.
(i) Compare match with temporary register, positive phase remains off.
(j) Compare match for on, but no change in positive phase because (i) off takes precedence.
(k) Compare match with compare register, negative phase turns on.

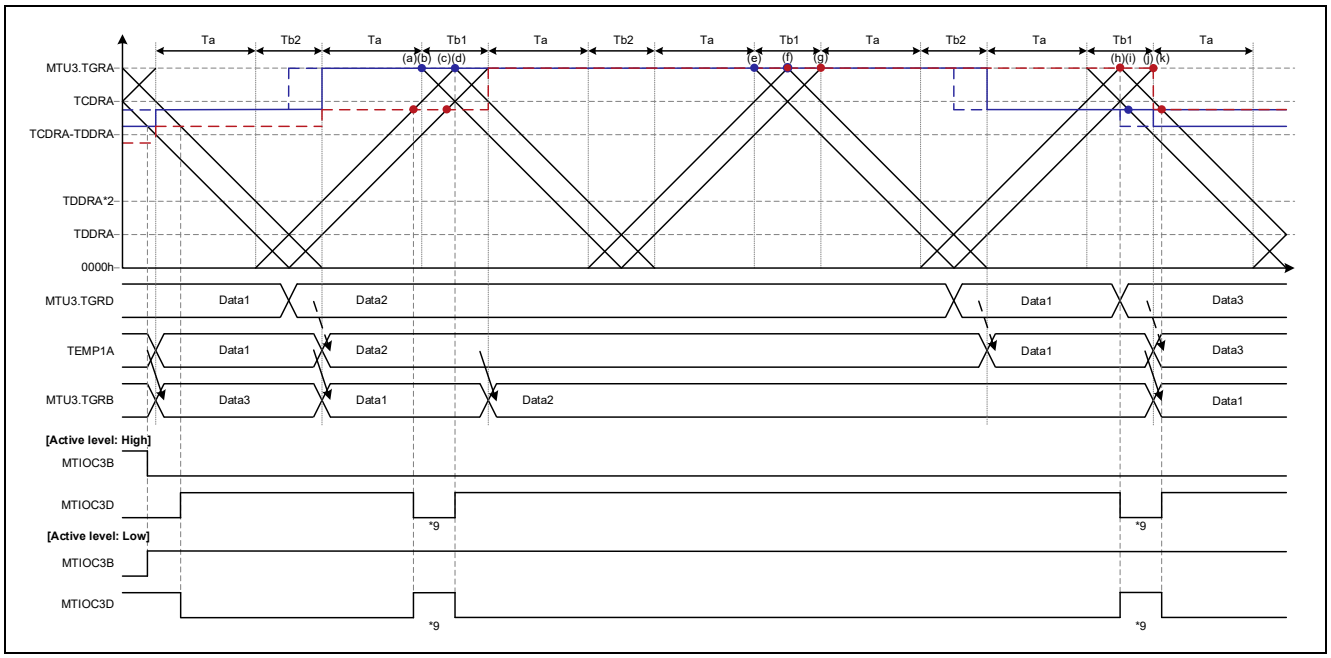


Figure 1.56 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: F → 0% → F)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.57 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.56.

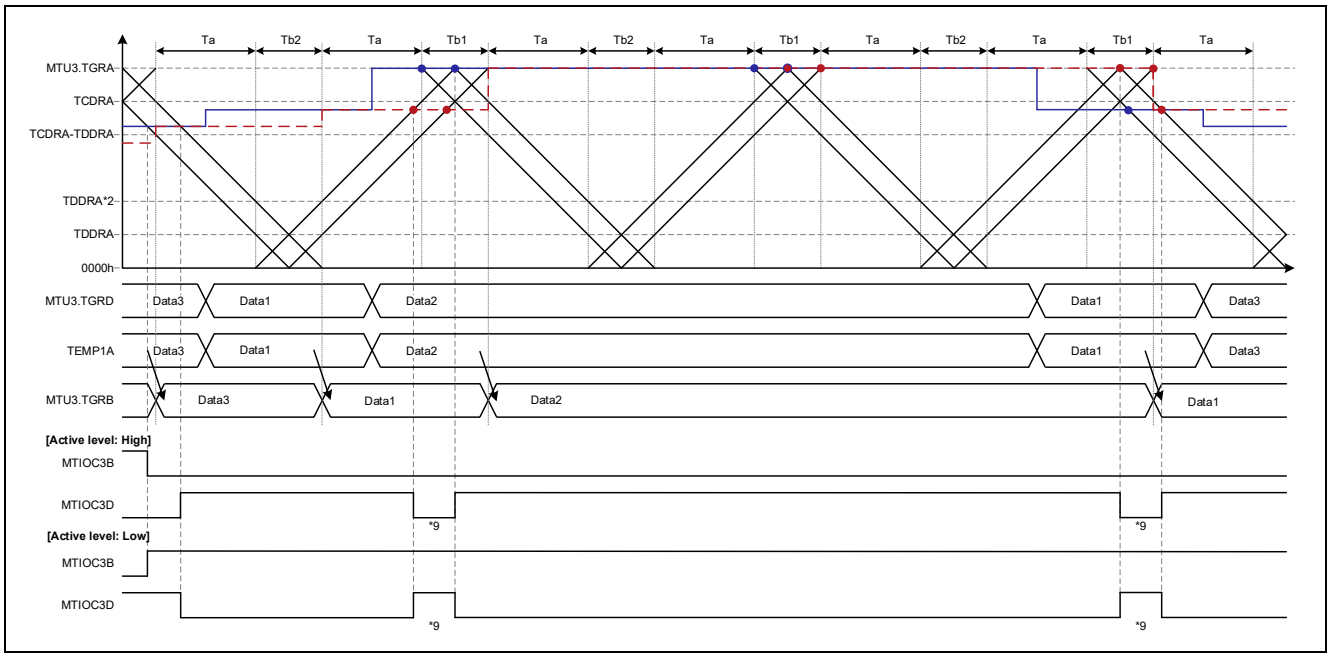


Figure 1.57 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: F → 0% → F)

1.3.1.10 Change from Near 0% to Near 0% (F → G → F)

Figure 1.58 to Figure 1.61 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.58, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, cautions 6 and 10
- [Operation example 2] Figure 1.59, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, cautions 6 and 10
- [Operation example 3] Figure 1.60, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 10
- [Operation example 4] Figure 1.61, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 10

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: F → G → F
  - E < TCDRA, F > TCDRA – TCDRA
  - G > TCDRA

- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: F
  - Data 2: G

- Cautions
  6. The positive phase becomes minute pulses to the extent that the value of F is close to TCDRA.
  10. The negative phase becomes minute pulses to the extent that the value of G is close to MTU3.TGRA.

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.58 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with temporary register, positive phase turns off.
(c) Compare match with temporary register, positive phase remains off.
(d) Compare match with compare register, negative phase turns off.
(e) Compare match with temporary register, negative phase turns on.
(f) Compare match for on, but no change in positive phase because (c) off takes precedence.

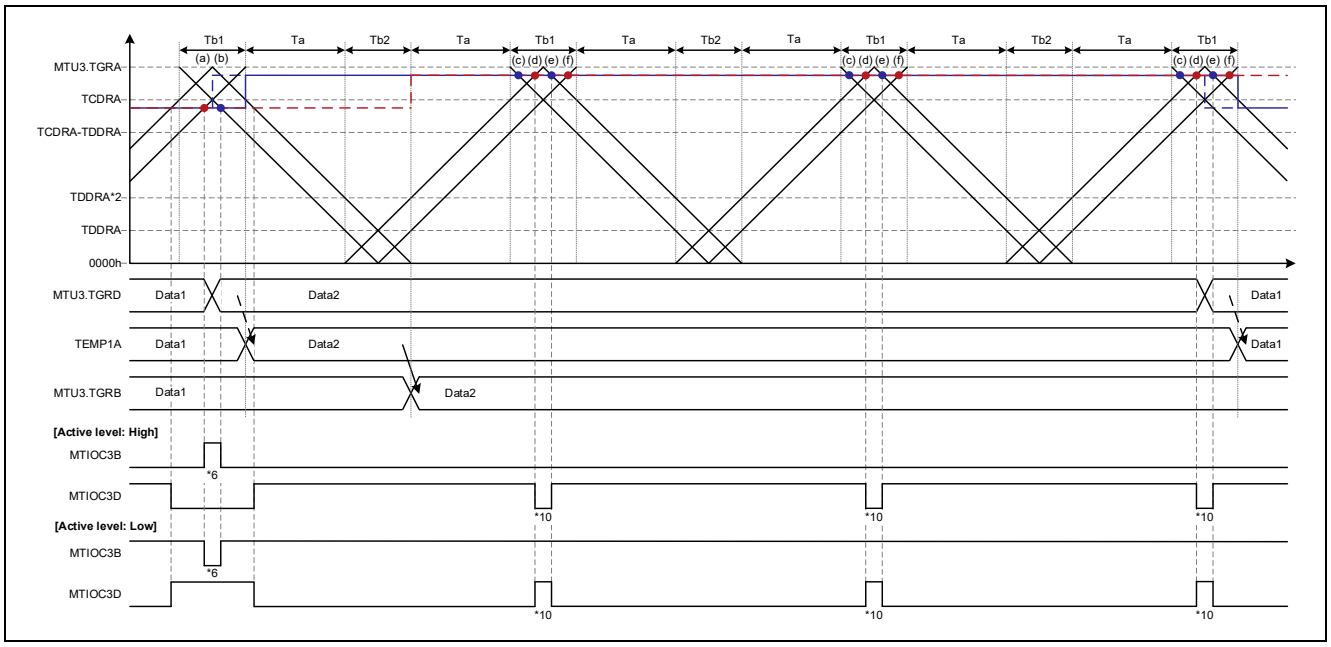


Figure 1.58 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: F → G → F)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.59 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.58.

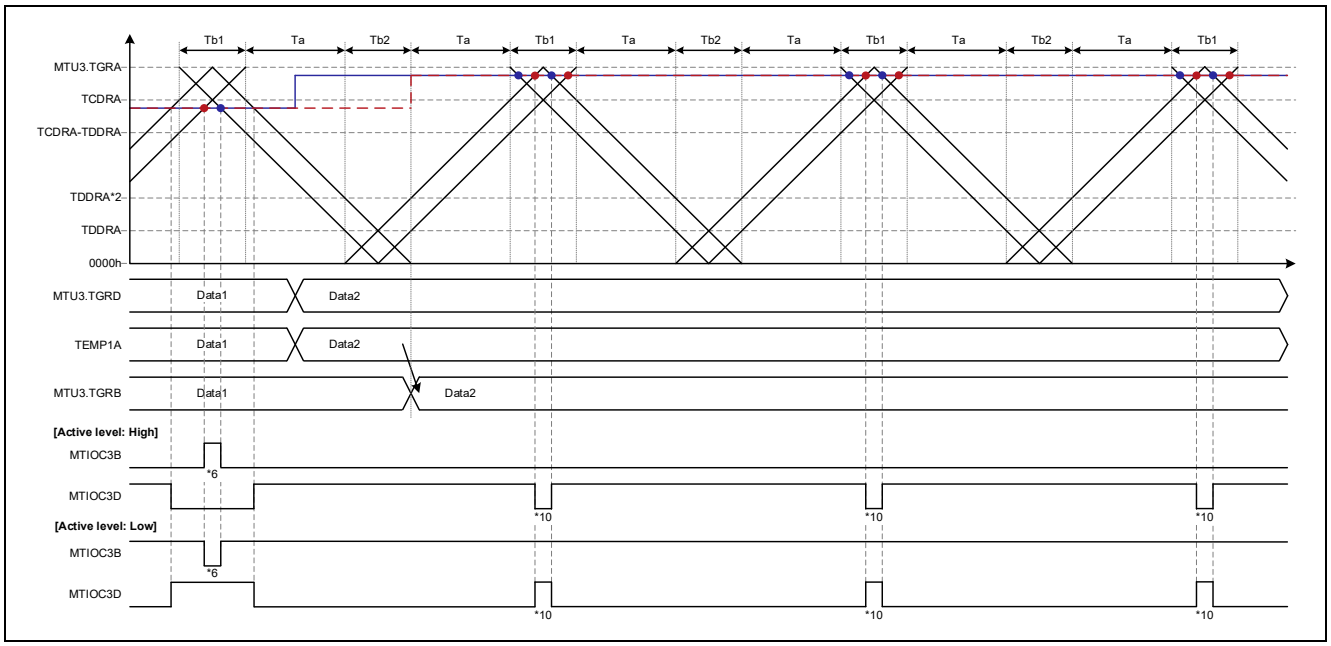


Figure 1.59 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: F → G → F)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.60 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with temporary register, positive phase remains off.
(b) Compare match for on, but no change in positive phase because (a) off takes precedence.
(c) Compare match with temporary register, positive phase remains off.
(d) Compare match with compare register, negative phase turns off.
(e) Compare match with temporary register, negative phase turns on.
(f) Compare match for on, but no change in positive phase because (c) off takes precedence.
(g) Compare match with temporary register, positive phase remains off.
(h) Compare match for on, but no change in positive phase because (g) off takes precedence.

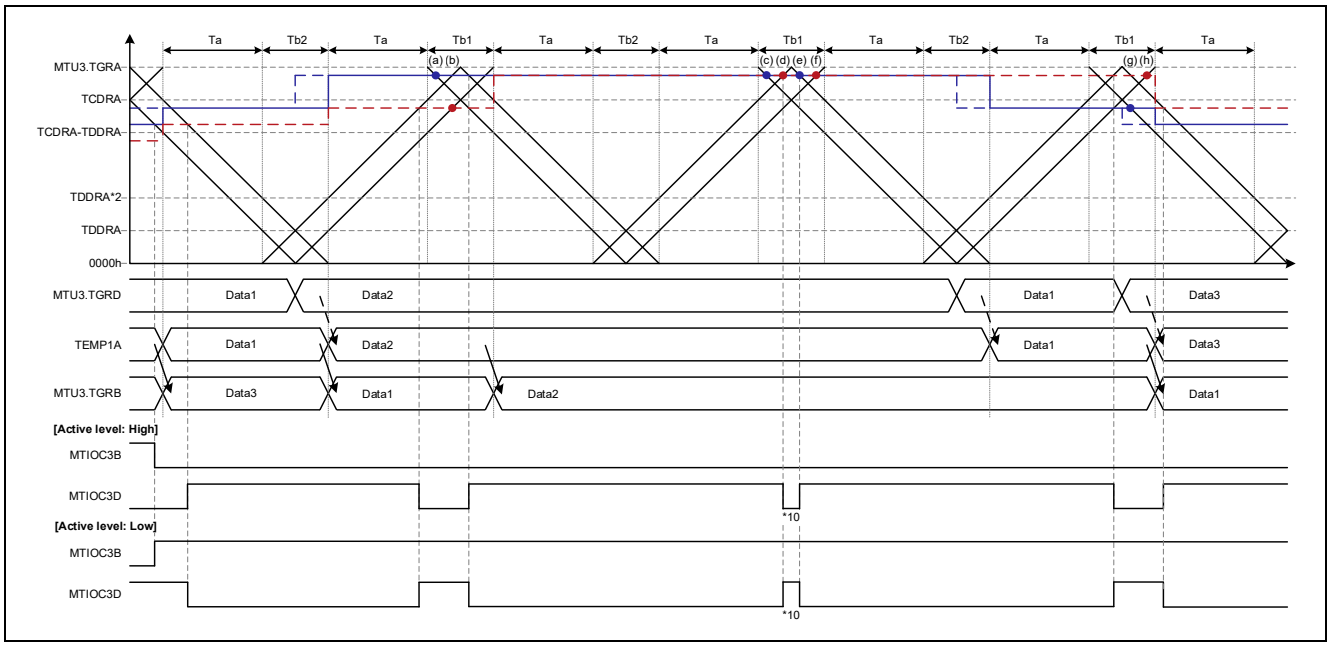


Figure 1.60 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Duty: F → G → F)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.61 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.60.

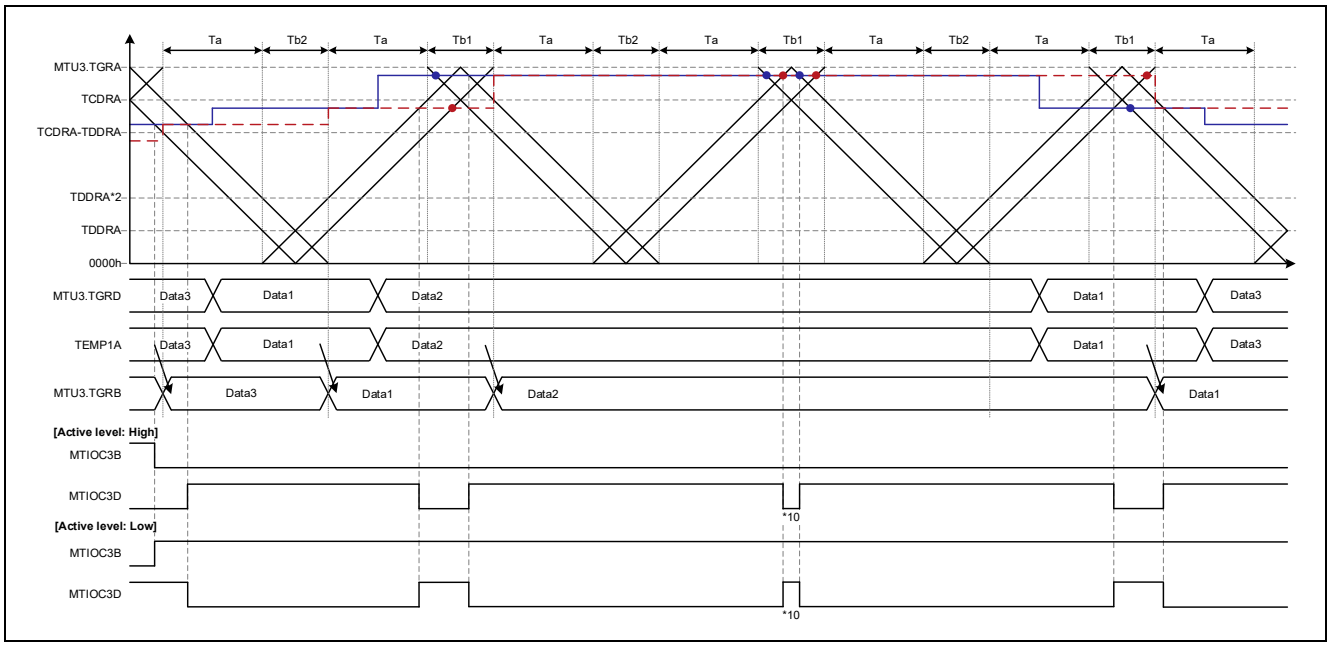


Figure 1.61 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Duty: F → G → F)

1.3.1.11 Initial output (Initial value = A)

Figure 1.62 to Figure 1.65 illustrate the MTU operating modes and cautions listed in Table 1.9.

- [Operation example 1] Figure 1.62, Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite, caution 11
- [Operation example 2] Figure 1.63, Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite, caution 11
- [Operation example 3] Figure 1.64, Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite, caution 11
- [Operation example 4] Figure 1.65, Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite, caution 11

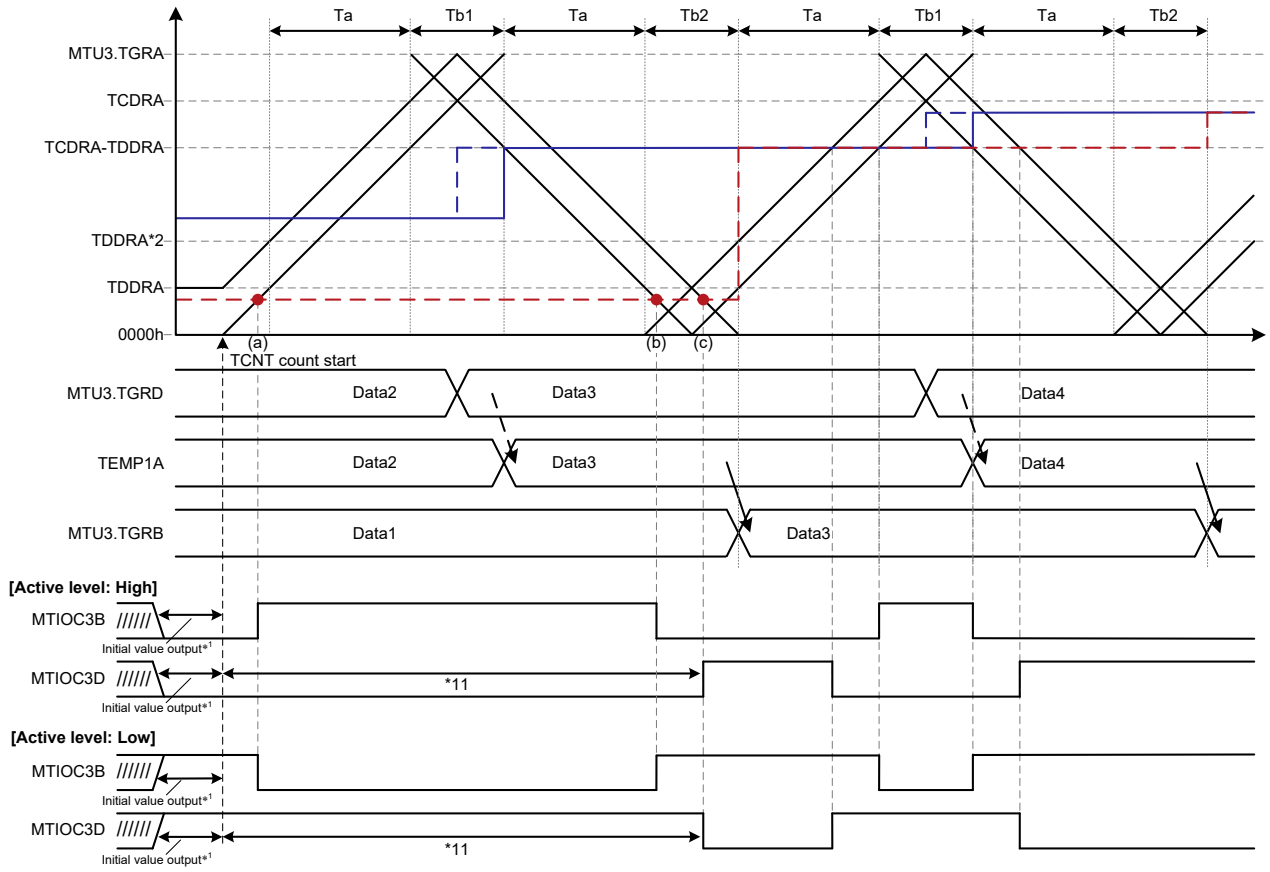
Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: Initial value = A
  - A < TCDRA
- Key to figures
  - Dashed blue line: Setting timing and value changes of buffer register (MTU3.TGRD)
  - Solid blue line: Setting timing and value changes of temporary register (TEMP1A)
  - Dashed red line: Setting timing and value changes of compare register (MTU3.TGRB)
  - Data 1: A
  - Data 2: TDDRA × 2 or greater
- Cautions
  11. The initial output level of the negative phase is maintained at the value set in TOCR1m.OLSN (m = A or B).

[Operation example 1] Complementary PWM Mode 2, Output Start: Trough, Tb Interval Overwrite

Figure 1.62 shows an operation example of buffer overwrite in the Tb1 interval (crest) in complementary PWM mode 2.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with compare register, positive phase turns off.
(c) Compare match with compare register, negative phase turns on.

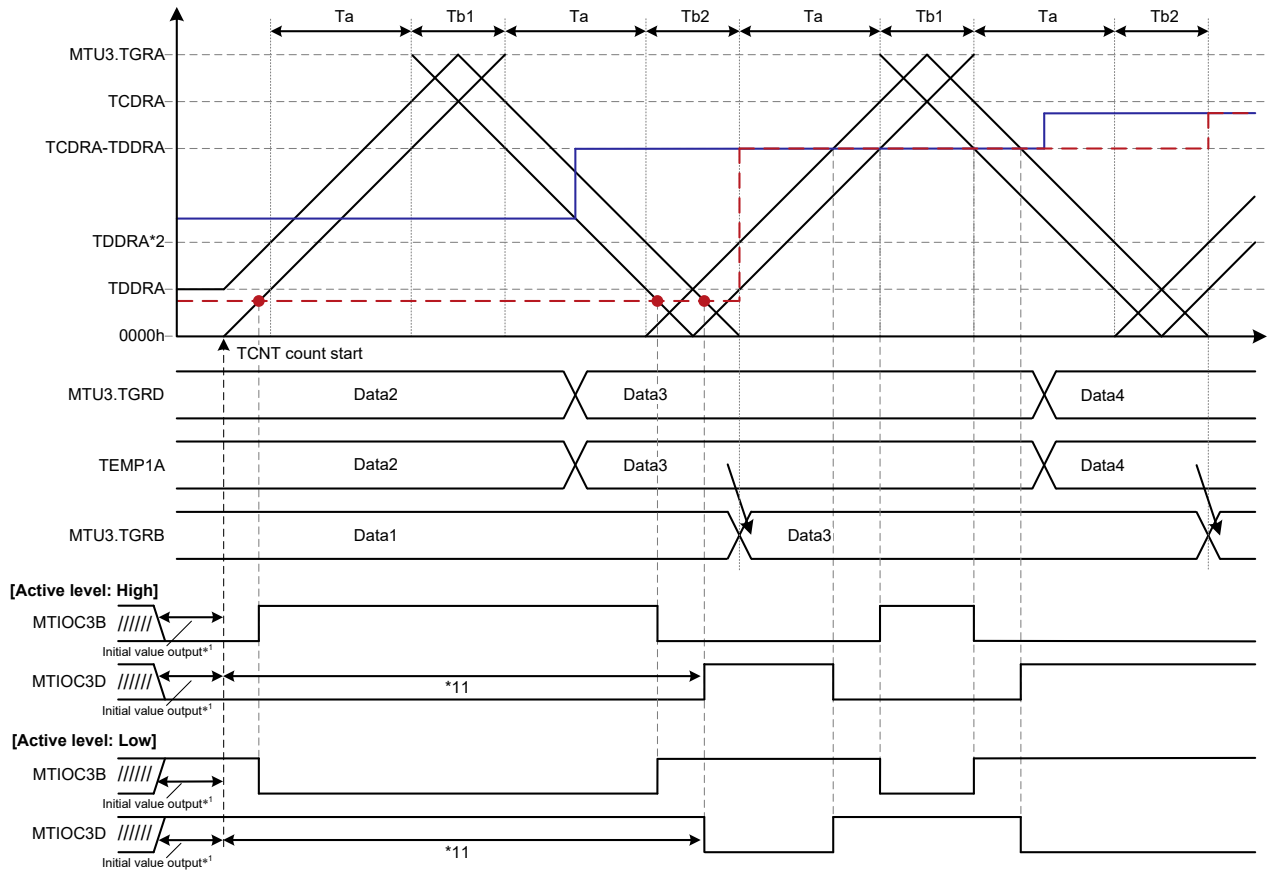


Note: 1. Initial output start when PMR register set.

Figure 1.62 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Initial Value = A)

[Operation example 2] Complementary PWM Mode 2, Output Start: Trough, Ta Interval Overwrite

Figure 1.63 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.62.



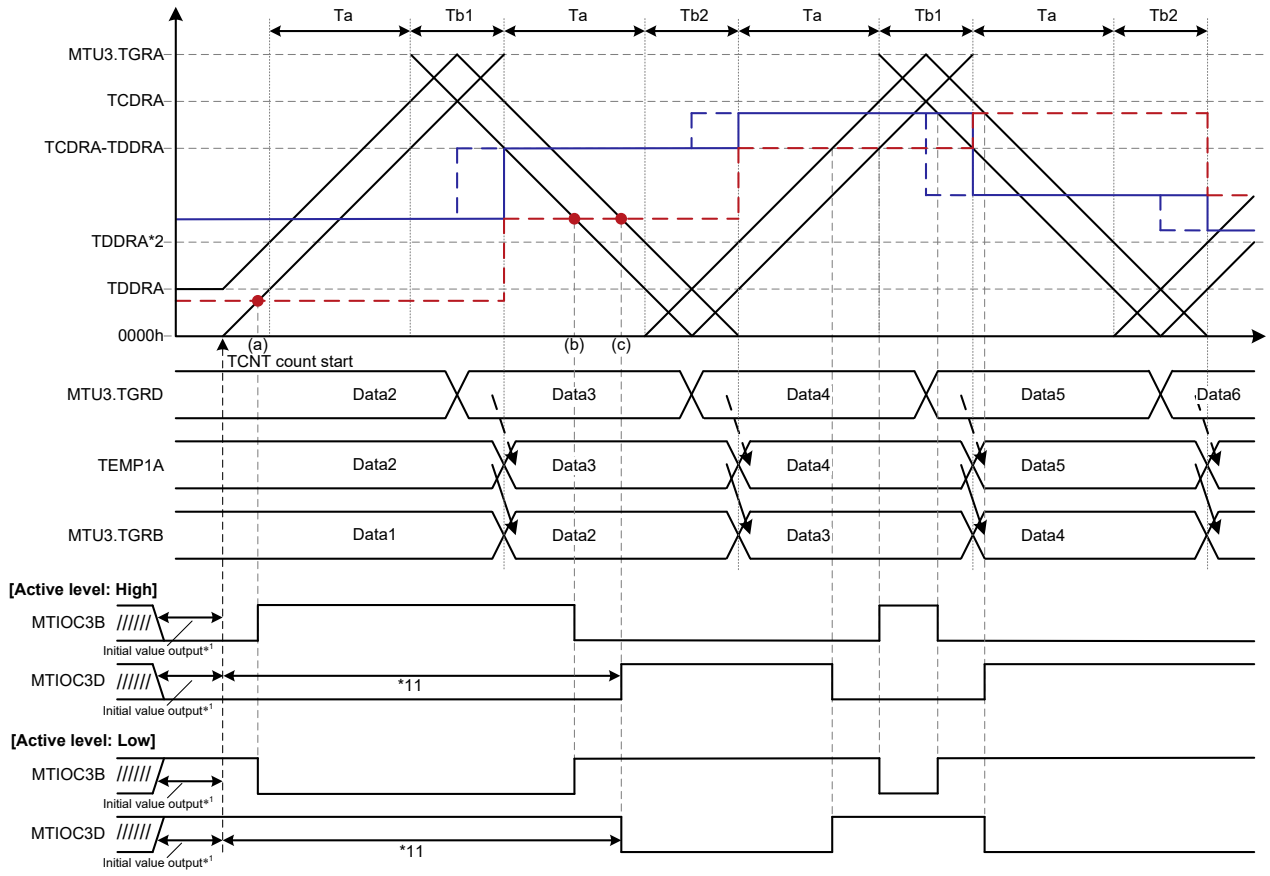
Note: 1. Initial output start when PMR register set.

Figure 1.63 Complementary PWM Mode 2 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Initial Value = A)

[Operation example 3] Complementary PWM Mode 3, Output Start: Trough, Tb Interval Overwrite

Figure 1.64 shows an operation example of buffer overwrite in the Tb interval in complementary PWM mode 3.

(a) Compare match with compare register, positive phase turns on.
(b) Compare match with compare register, positive phase turns off.
(c) Compare match with compare register, negative phase turns on.

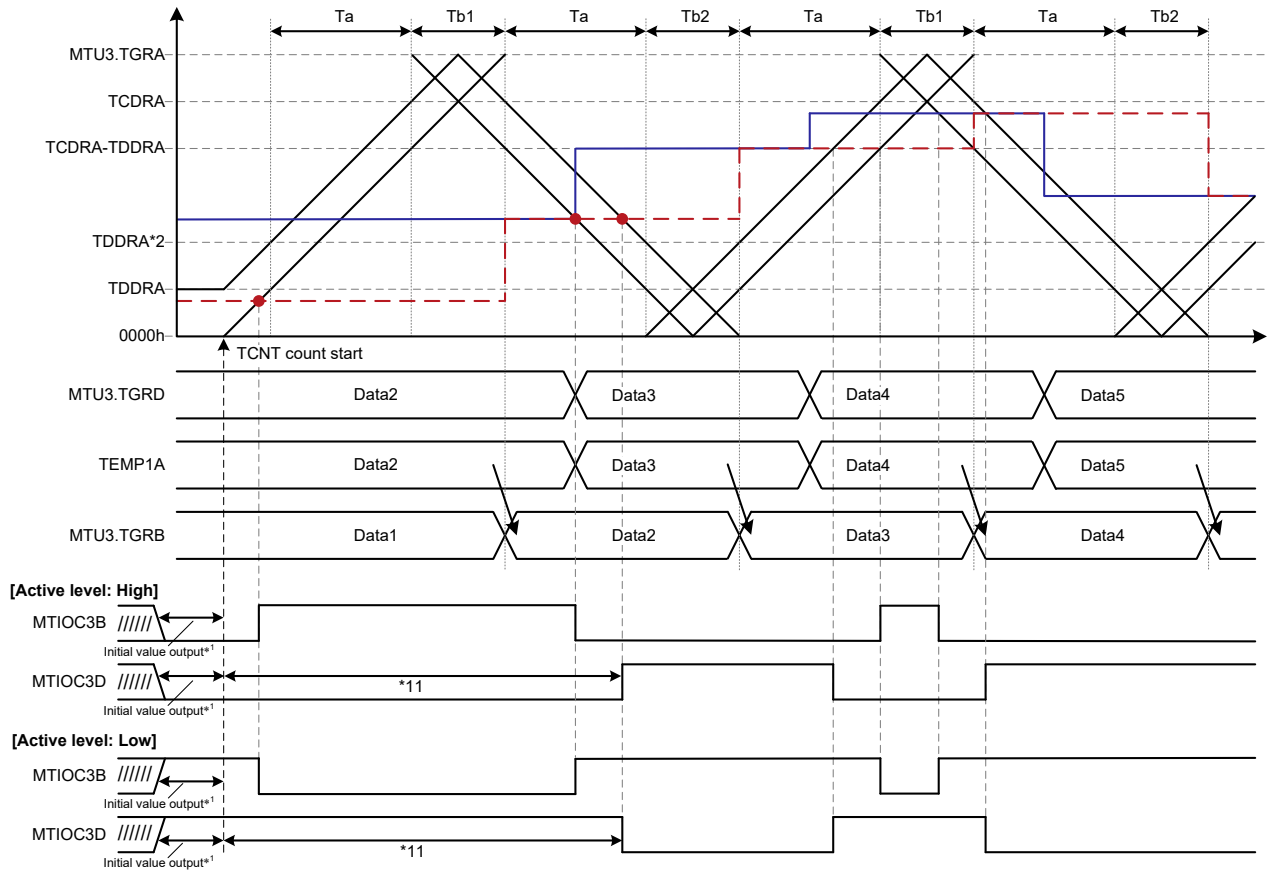


Note: 1. Initial output start when PMR register set

Figure 1.64 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Tb Interval, Initial Value = A)

[Operation example 4] Complementary PWM Mode 3, Output Start: Trough, Ta Interval Overwrite

Figure 1.65 shows an operation example of buffer overwrite in the Ta interval in complementary PWM mode 3. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.64.



Note: 1. Initial output start when PMR register set

Figure 1.65 Complementary PWM Mode 3 Operation Example (Output Start: Trough, Overwrite in Ta Interval, Initial Value = A)

1.3.2 Output Waveforms Near 0% and 100% on GPTW

Table 1.10 lists cautions and operation examples for waveform output with automatic dead time setting function enabled and disabled and different compare match timings (near 0% and 100% duty cycles) in triangle-wave PWM modes 1, 2, and 3.

Table 1.10 List of GPTW Cautions and Operating Modes

Section	Section Title	Triangle-Wave PWM Mode 1		Triangle-Wave PWM Mode 2		Triangle-Wave PWM Mode 3		Cautions	
		Used	Not Used	Used	Not Used	Used	Not Used	Used	Not Used
1.3.2.1	Change from Near 100% to Near 100% Duty Cycle (D → A → D)	Figure 1.66	Figure 1.69	Figure 1.67	Figure 1.70	Figure 1.68	Figure 1.71	*1, *2	*1, *3
1.3.2.2	Change from Near 100% to 100% Duty Cycle (D → 0%/100% → D)	Figure 1.72	Figure 1.75	Figure 1.73	Figure 1.76	Figure 1.74	Figure 1.77	*4, *5	*4, *5
1.3.2.3	Change from Near 100% to 100% Duty Cycle (A → 0%/100% → A)	Figure 1.78	Figure 1.81	Figure 1.79	Figure 1.82	Figure 1.80	Figure 1.83	*2, *4, *5	*3, *4, *5
1.3.2.4	Change from Near 0% to 0% Duty Cycle (F → 0%/100% → F)	Figure 1.84	Figure 1.87	Figure 1.85	Figure 1.88	Figure 1.86	Figure 1.89	*4, *5, *6	*4, *5, *6

Notes: Used: Automatic dead time setting enabled.
Not Used: Automatic dead time setting disabled.

1. The negative phase becomes minute pulses to the extent that the value of D is closer to GTDVU.
2. The correction function causes the negative phase to become minute pulses with a width of 1 count clock cycle.
3. The negative phase becomes minute pulses to the extent that the value of GTCCRB is close to 0 relative to A.
4. When the value of the GTUDDTYC.OmDTYR bit is 0b and that of the GTIOR.GTIOm[3:2] bits is 00b, after the recovery from 0%/100% duty cycle the output level is inverted relative to the output level before the 0%/100% duty cycle setting. (The inversion locations are indicated by blue circles in the figures.)
5. Dead time is not maintained in order to produce 0%/100% duty cycle output.
6. The positive phase becomes minute pulses to the extent that the value of F is close to GTPR.

1.3.2.1 Change from Near 100% to Near 100% Duty Cycle (D → A → D)

Figure 1.66 to Figure 1.71 illustrate the GPTW operating modes and cautions listed in Table 1.10.

- [Operation example 1] Figure 1.66, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 1 and 2
- [Operation example 2] Figure 1.67, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 1 and 2
- [Operation example 3] Figure 1.68, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 1 and 2
- [Operation example 4] Figure 1.69, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 1 and 3
- [Operation example 5] Figure 1.70, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 1 and 3
- [Operation example 6] Figure 1.71, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 1 and 3

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → A → D
  - D > GTDVU
  - A < GTDVU
- Key to figure
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Solid green line: Positive phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: A
- Cautions
  1. The negative phase becomes minute pulses to the extent that the value of D is closer to GTDVU.
  2. The correction function causes the negative phase to become minute pulses with a width of 1 count clock cycle.
  3. The negative phase becomes minute pulses to the extent that the value of GTCCRB is close to 0 relative to A.

[Operation example 1] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.66 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 1.

(a) Compare match with compare register, negative phase turns on.
(b) Change point 1 count clock cycle from trough due to correction function, negative phase turns off.
(c) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(d) Change point at GTDVU due to correction function, positive phase turns off.
(e) Generation of pulse with width of 1 count clock cycle due to correction function.
(f) Change point at trough due to correction function, negative phase turns on.
(g) Compare match with compare register, negative phase turns off.

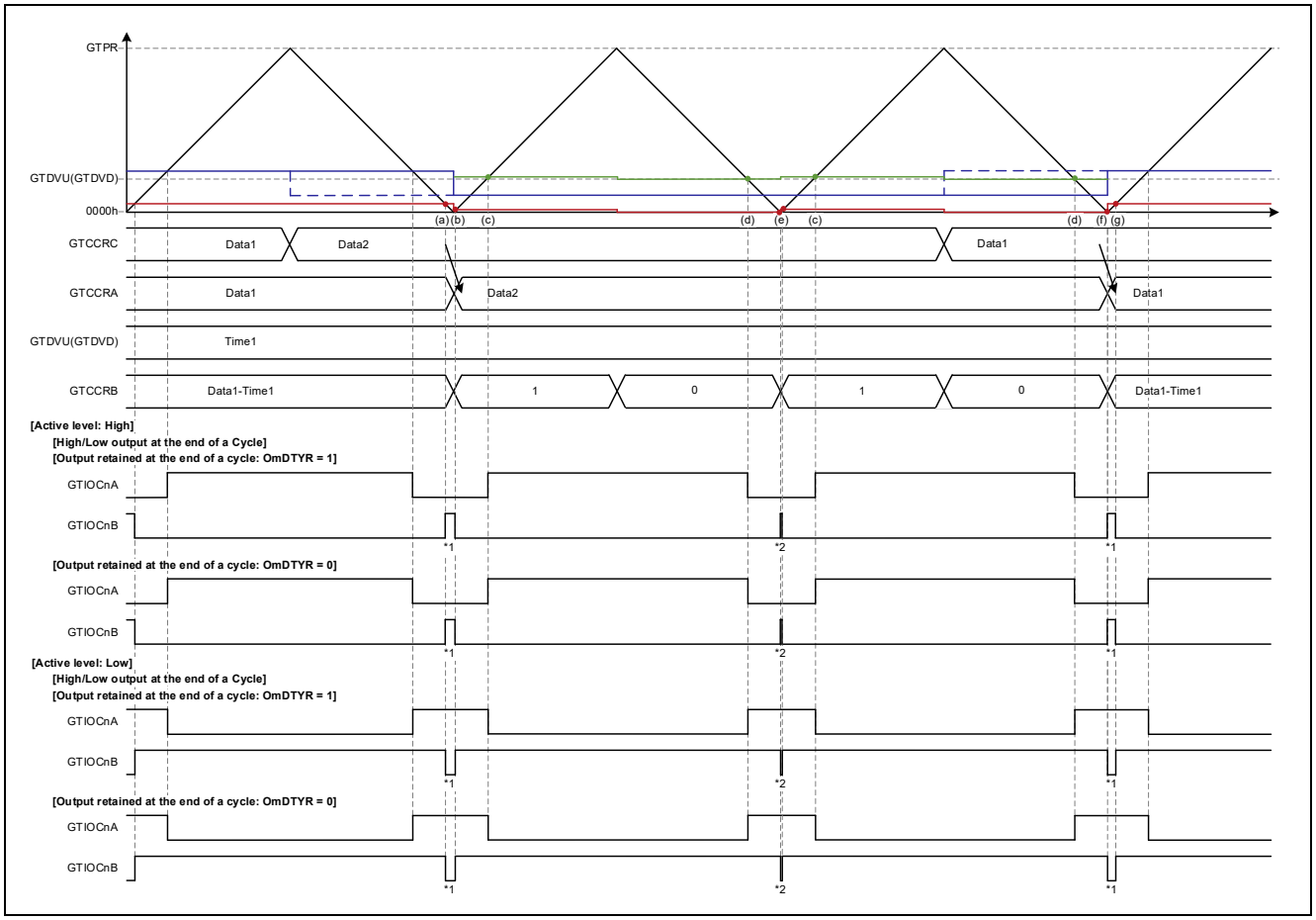


Figure 1.66 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → A → D)

[Operation example 2] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.67 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.66.

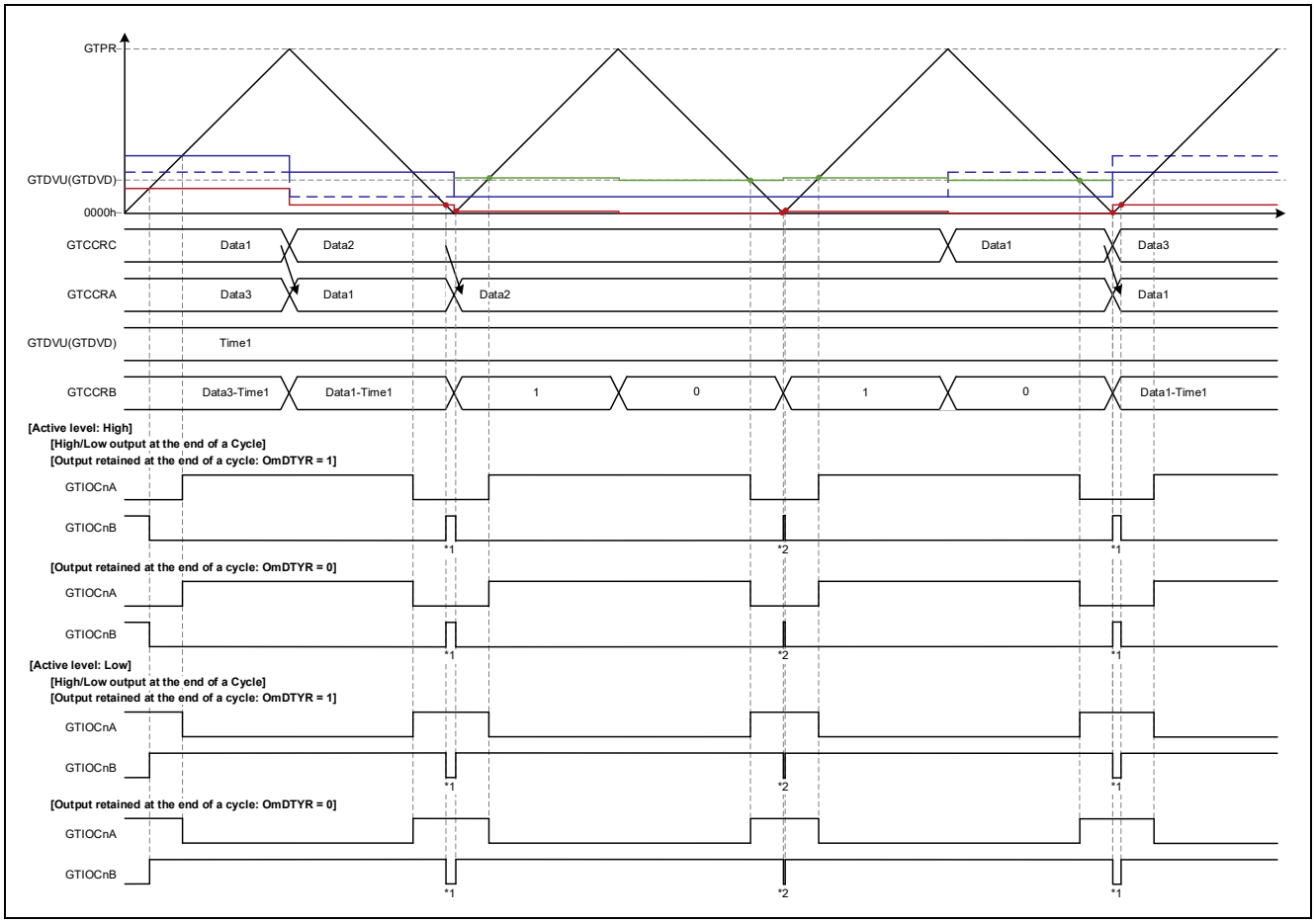


Figure 1.67 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → A → D)

[Operation example 3] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.68 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.66.

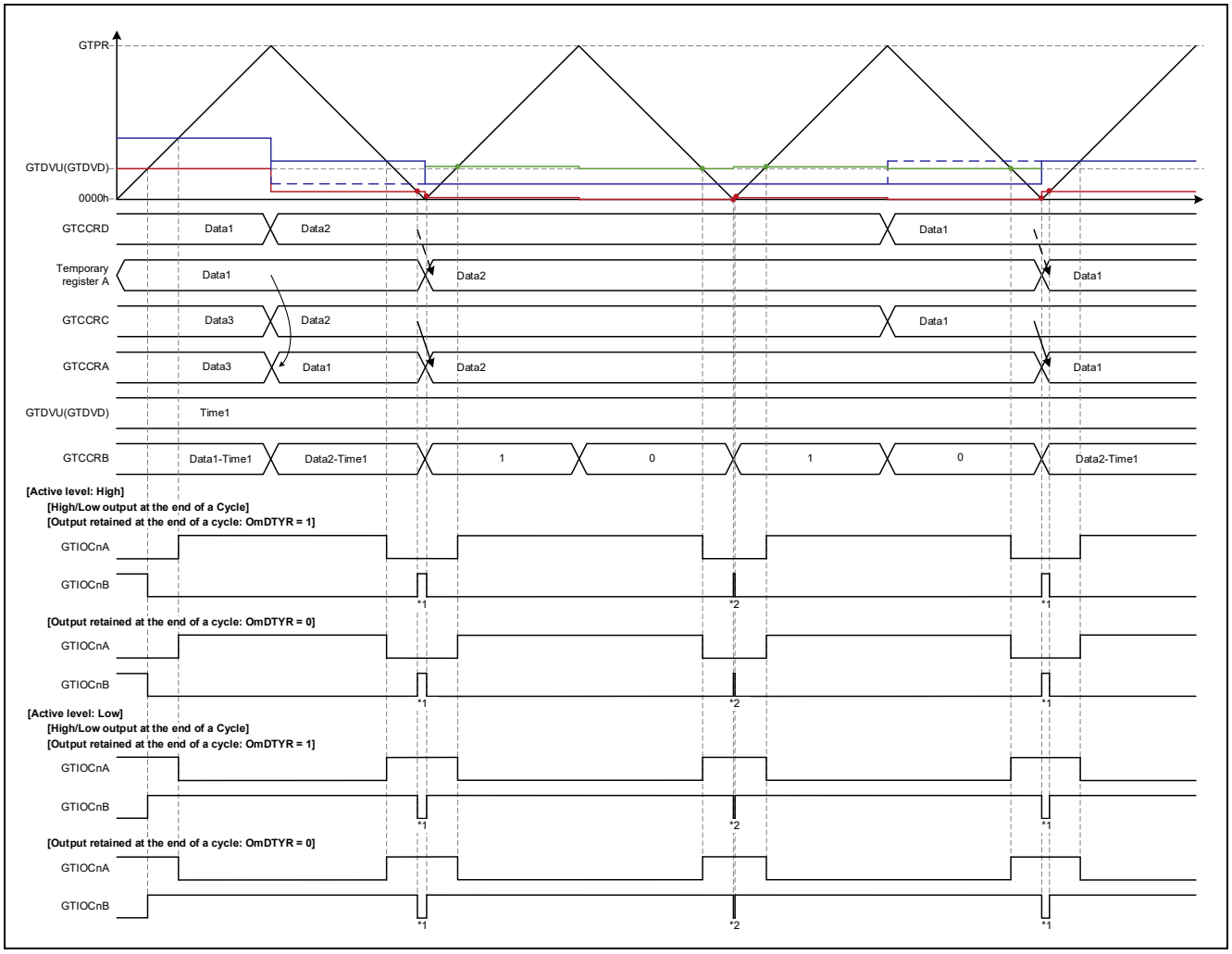


Figure 1.68 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → A → D)

[Operation example 4] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.69 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 1.

(a) Compare match with compare register, negative phase turns on.
(b) Compare match with compare register, negative phase turns off.

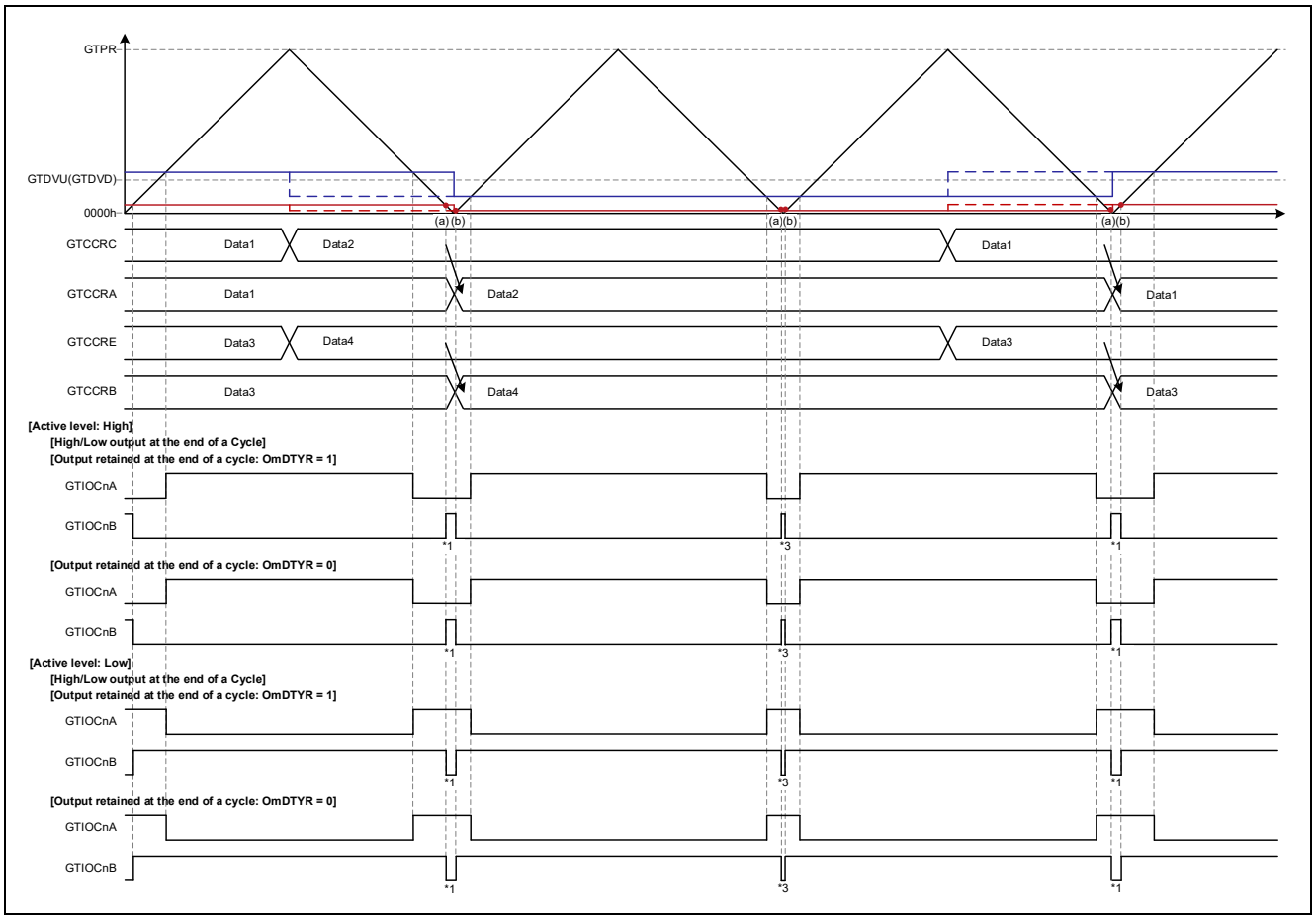


Figure 1.69 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → A → D)

[Operation example 5] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.70 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.69.

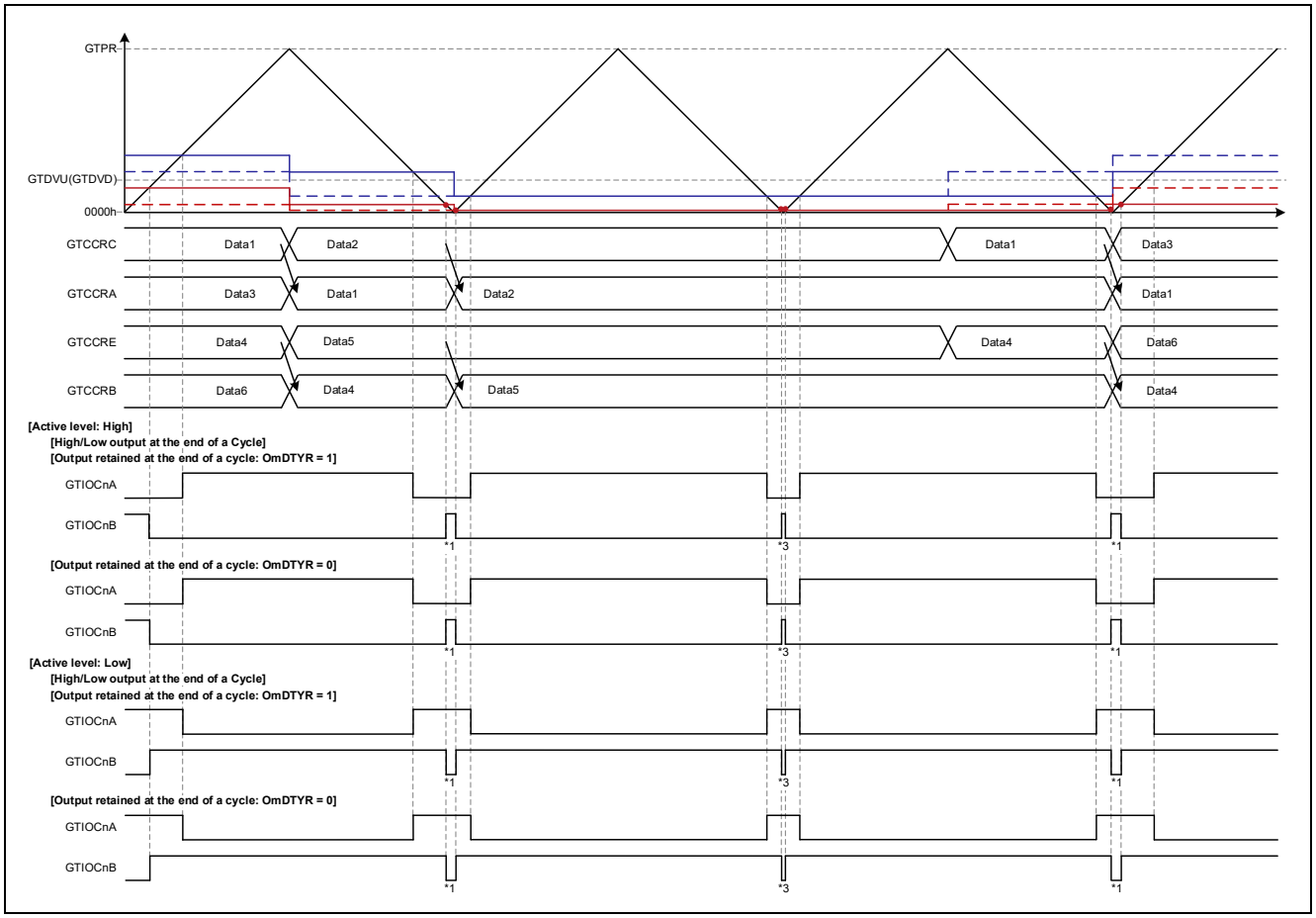


Figure 1.70 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → A → D)

[Operation example 6] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.71 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.69.

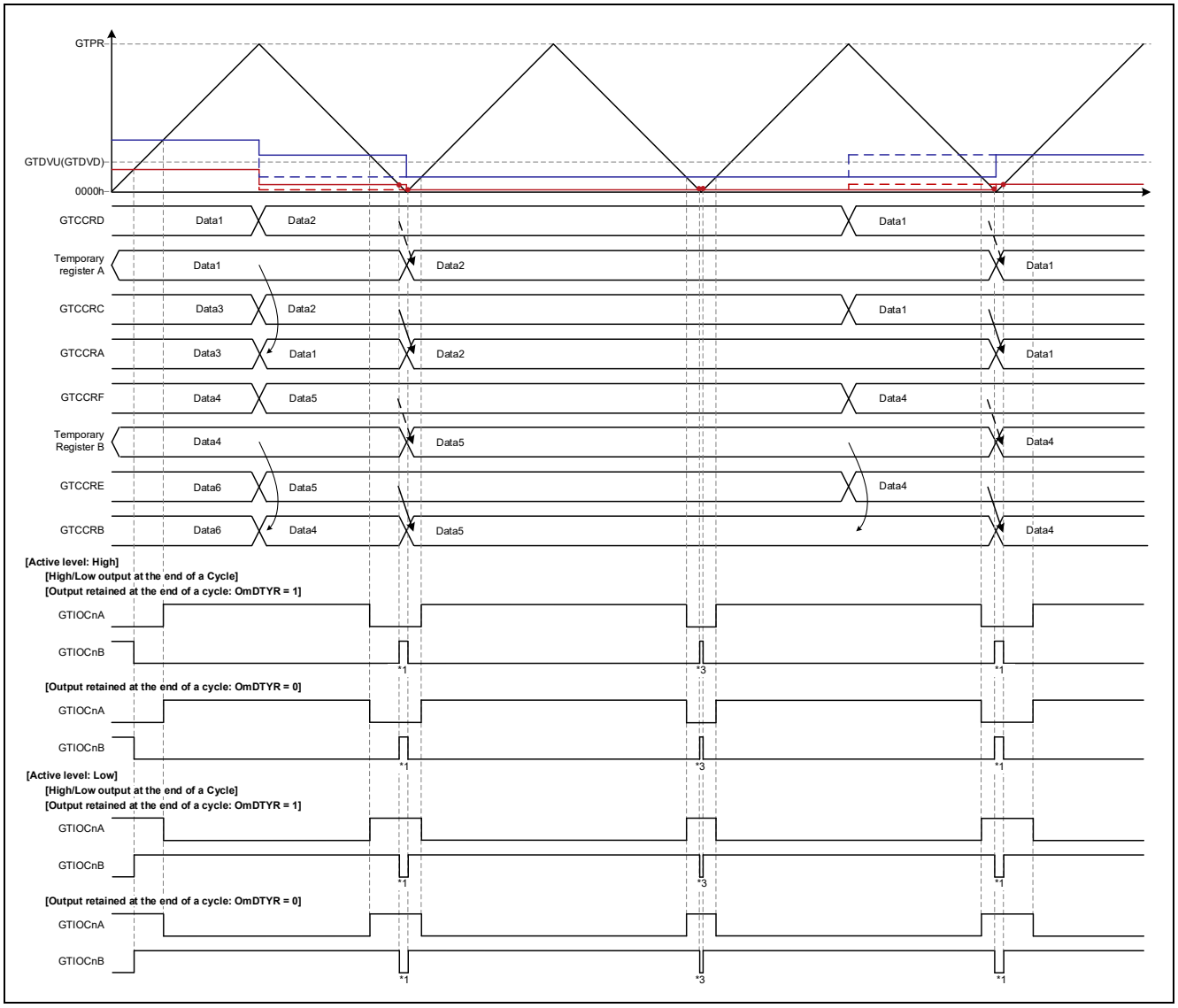


Figure 1.71 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → A → D)

1.3.2.2 Change from Near 100% to 100% Duty Cycle (D → 0%/100% → D)

Figure 1.72 to Figure 1.77 illustrate the GPTW operating modes and cautions listed in Table 1.10.

- [Operation example 1] Figure 1.72, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4 and 5
- [Operation example 2] Figure 1.73, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4 and 5
- [Operation example 3] Figure 1.74, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4 and 5
- [Operation example 4] Figure 1.75, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4 and 5
- [Operation example 5] Figure 1.76, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4 and 5
- [Operation example 6] Figure 1.77, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4 and 5

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → 0%/100% → D
  - D > GTDVU

- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
  - Dotted black lines for GTIOCnA and GTIOCnB pins: Operation masked by 0% and 100% duty cycle settings
  - Data 1: D

- Cautions
  4. When the value of the GTUDDTYC.OmDTYR bit is 0b and that of the GTIOR.GTIOm[3:2] bits is 00b, after the recovery from 0%/100% duty cycle the output level is inverted relative to the output level before the 0%/100% duty cycle setting. (The inversion locations are indicated by blue circles in the figures.)
  5. Dead time is not maintained in order to produce 0%/100% duty cycle output.

[Operation example 1] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.72 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).

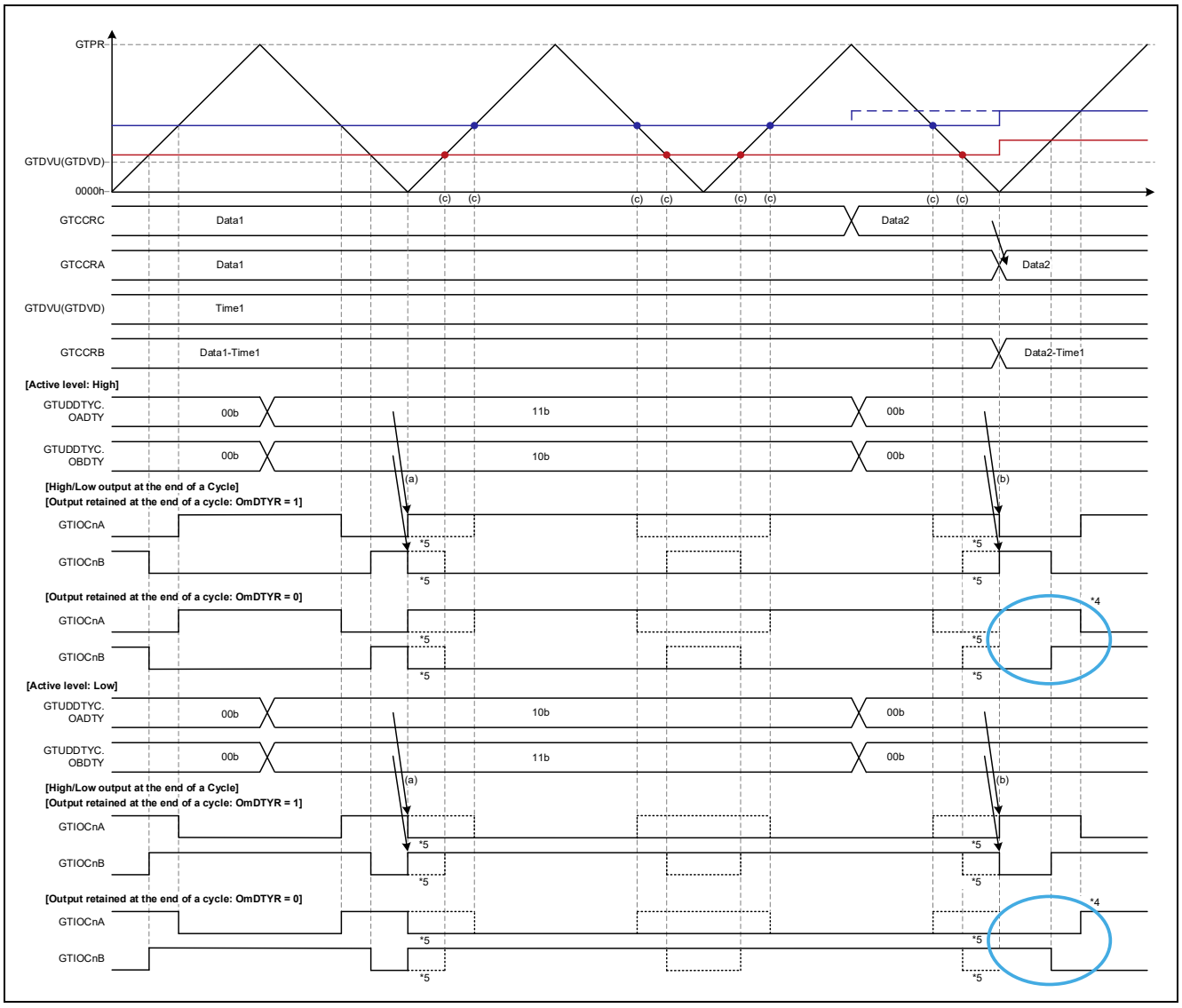


Figure 1.72 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → 0%/100% → D)

[Operation example 2] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.73 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.72.

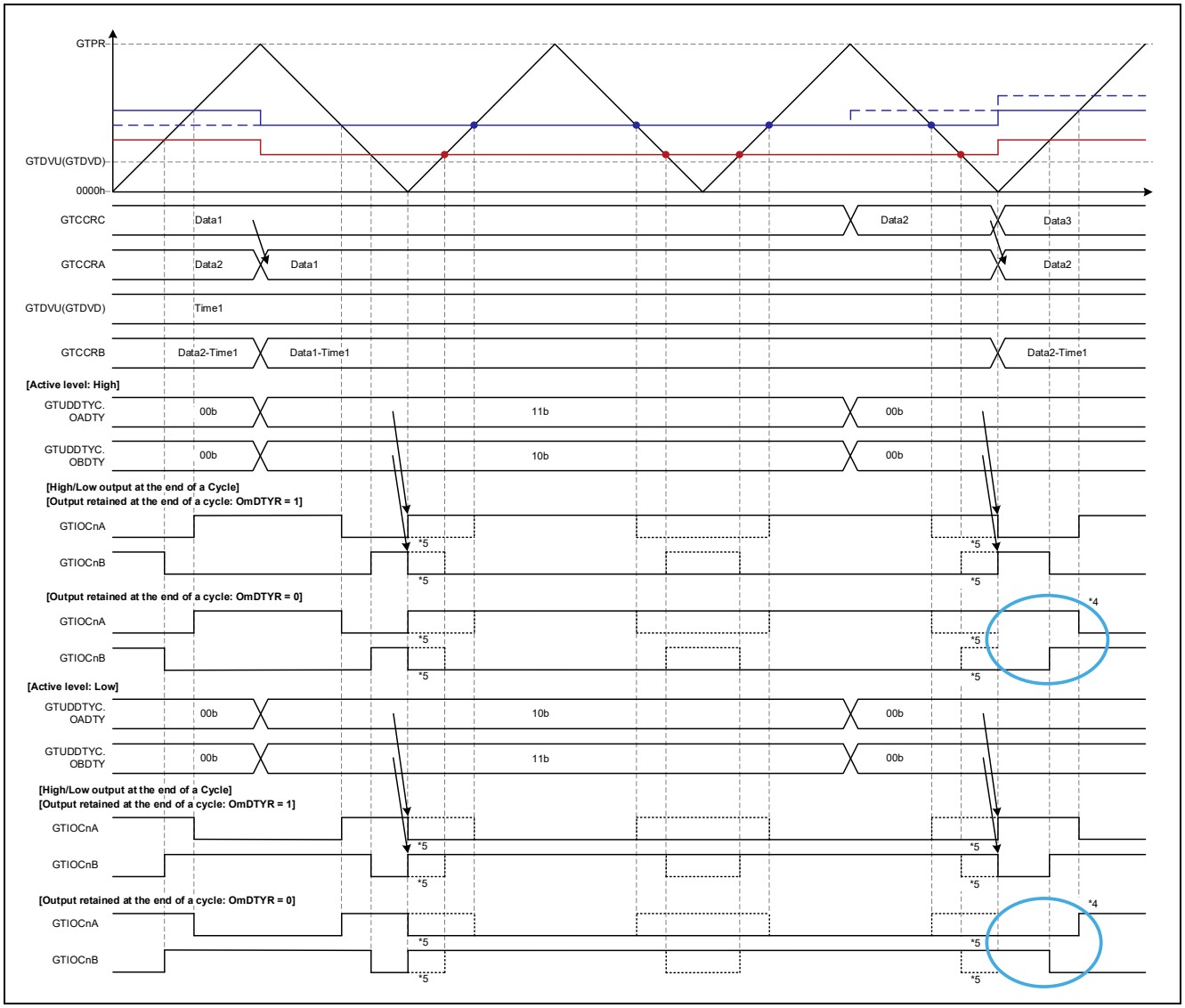


Figure 1.73 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → 0%/100% → D)

[Operation example 3] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.74 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.72.

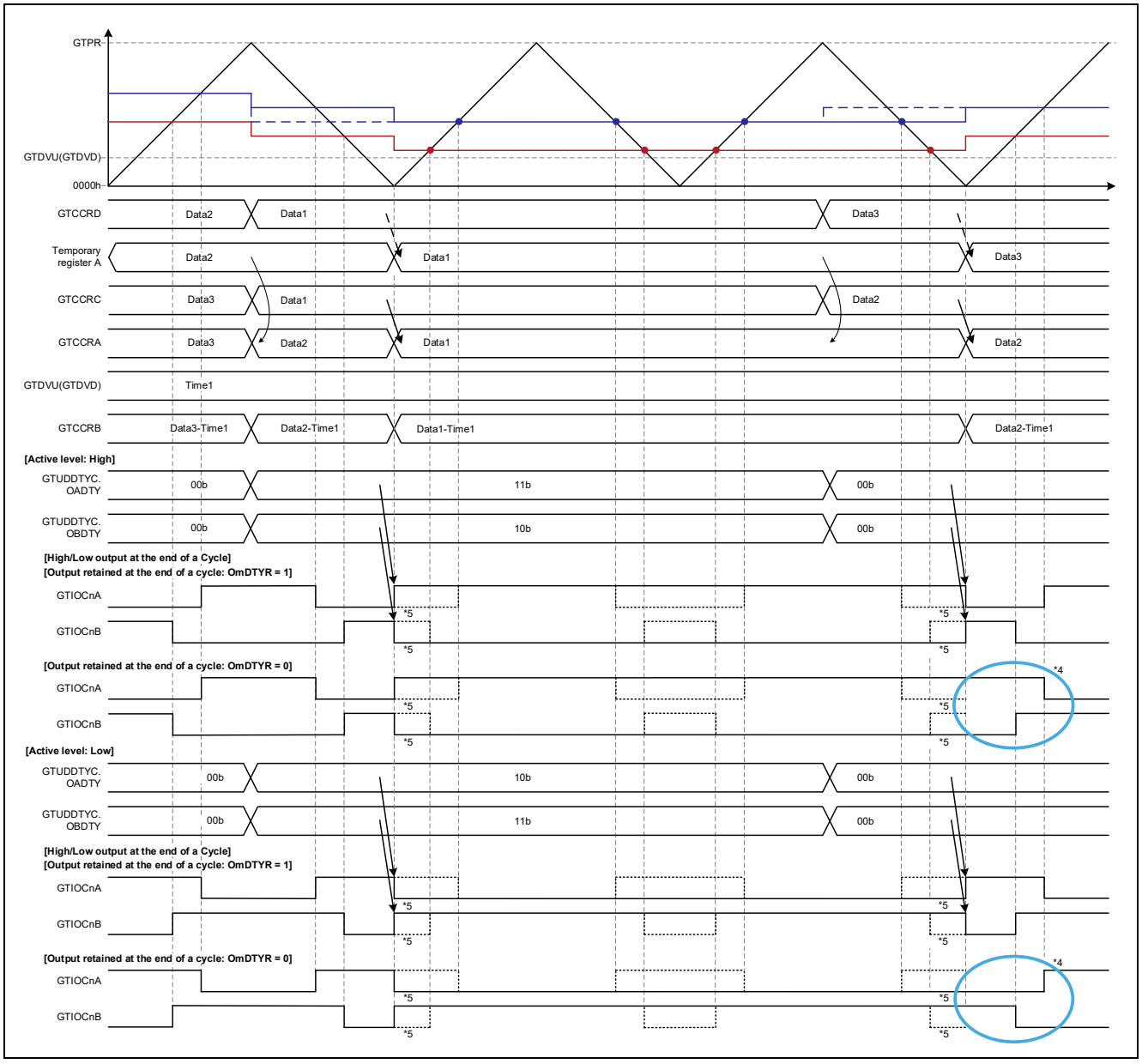


Figure 1.74 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: D → 0%/100% → D)

[Operation example 4] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.75 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).

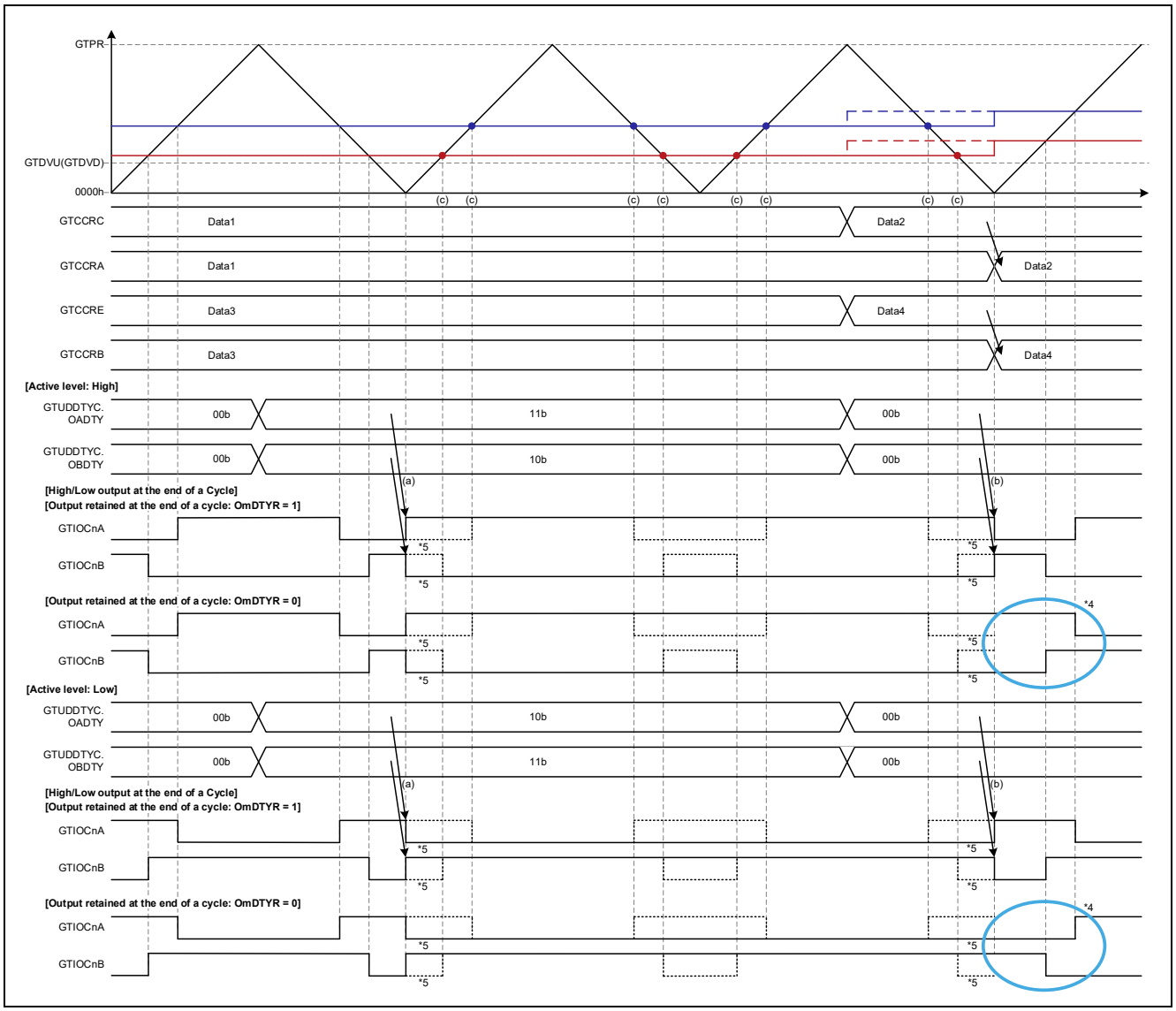


Figure 1.75 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → 0%/100% → D)

[Operation example 5] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.76 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.75.

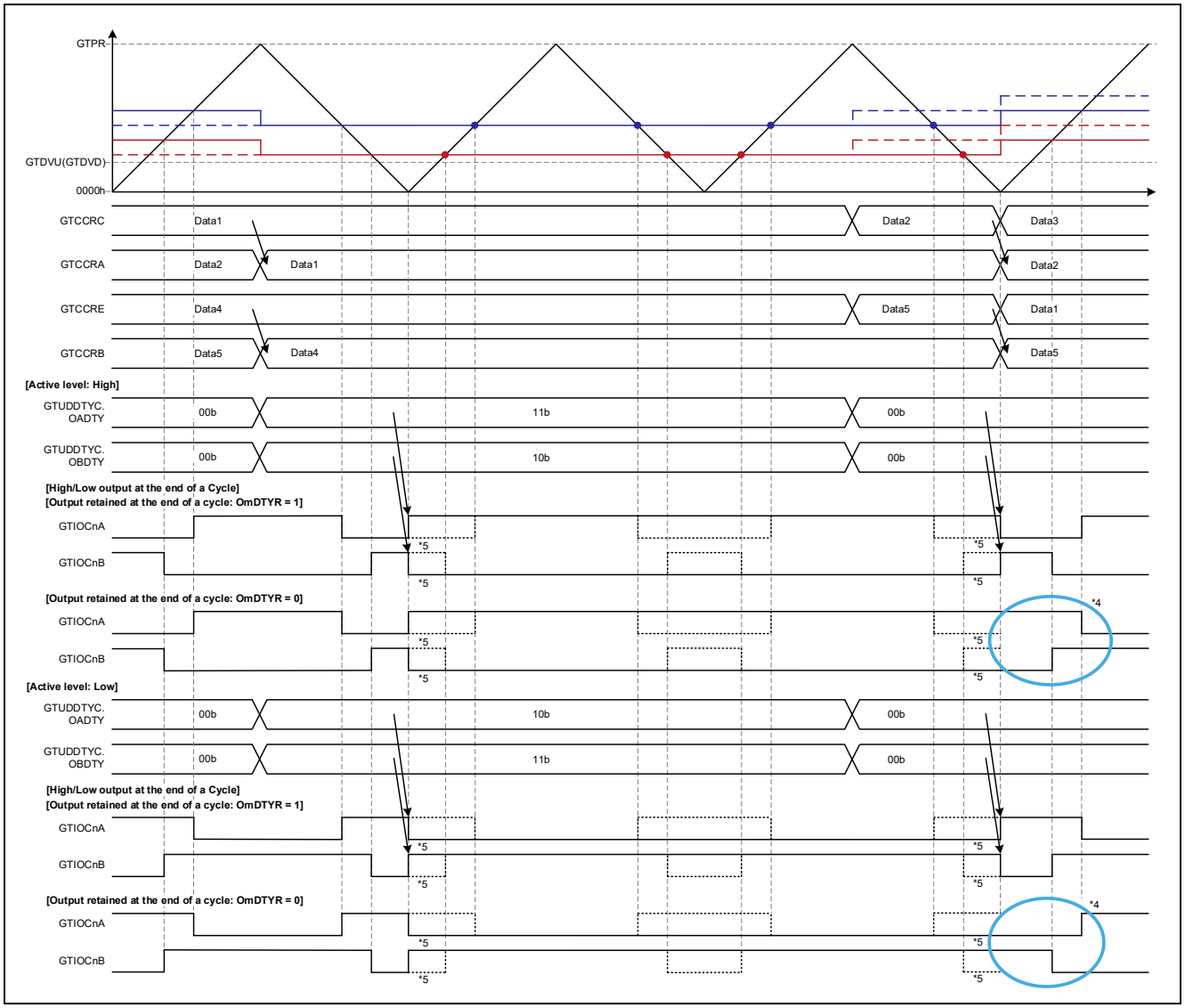


Figure 1.76 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → 0%/100% → D)

[Operation example 6] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.77 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.75.

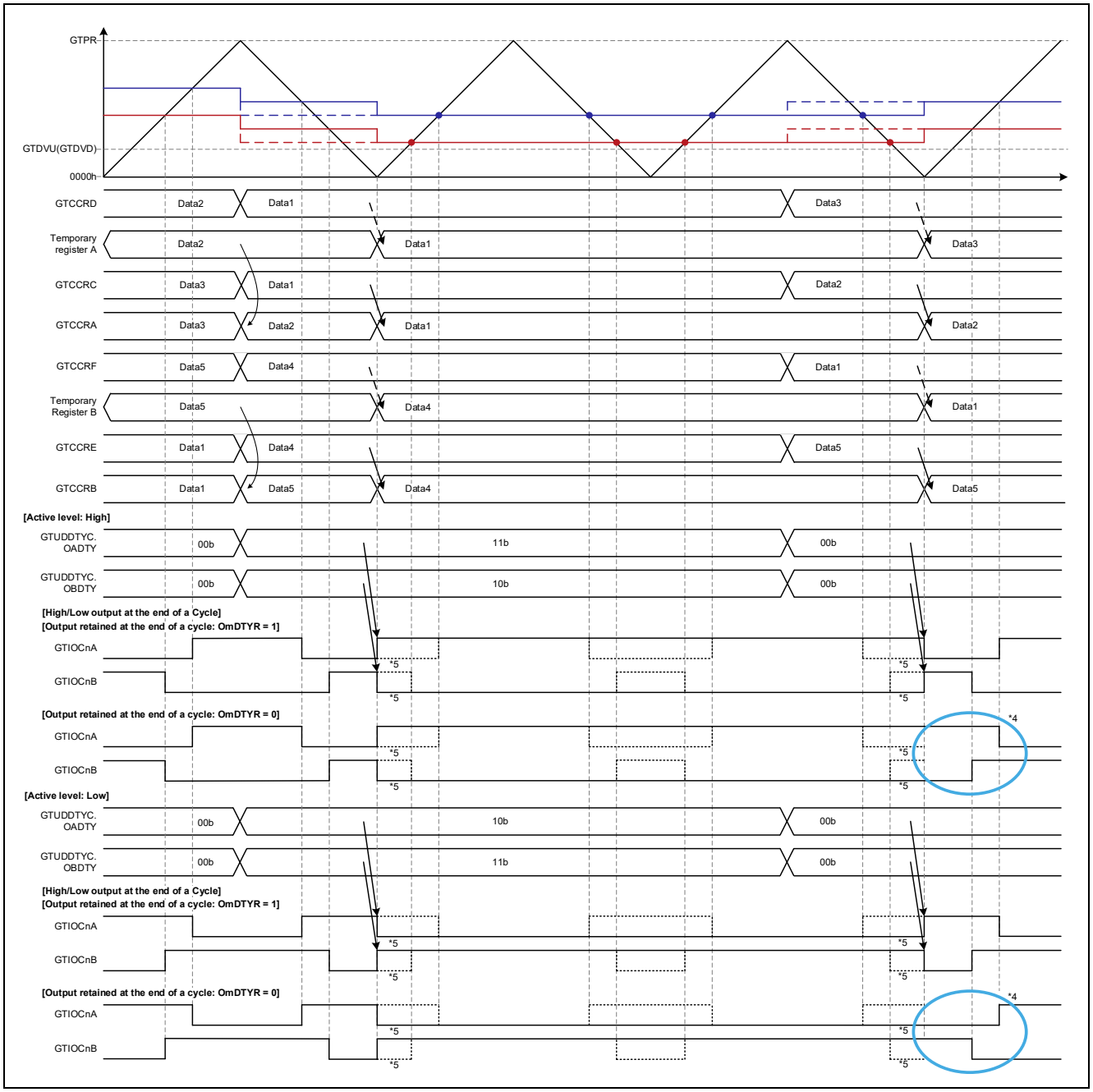


Figure 1.77 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: D → 0%/100% → D)

1.3.2.3 Change from Near 100% to 100% Duty Cycle (A → 0%/100% → A)

Figure 1.78 to Figure 1.83 illustrate the GPTW operating modes and cautions listed in Table 1.10.

- [Operation example 1] Figure 1.78, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 2, 4, and 5
- [Operation example 2] Figure 1.79, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 2, 4, and 5
- [Operation example 3] Figure 1.80, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 2, 4, and 5
- [Operation example 4] Figure 1.81, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 3, 4, and 5
- [Operation example 5] Figure 1.82, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 3, 4, and 5
- [Operation example 6] Figure 1.83, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 3, 4, and 5

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: A → 0%/100% → A
  - A < GTDVU

- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Solid green line: Positive phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Dotted black lines for GTIOCnA and GTIOCnB pins: Operation masked by 0% and 100% duty cycle settings
  - Data 1: A

- Cautions
  2. The correction function causes the negative phase to become minute pulses with a width of 1 count clock cycle.
  3. The negative phase becomes minute pulses to the extent that the value of GTCCRB is close to 0 relative to A.
  4. When the value of the GTUDDTYC.OmDTYR bit is 0b and that of the GTIOR.GTIOm[3:2] bits is 00b, after the recovery from 0%/100% duty cycle the output level is inverted relative to the output level before the 0%/100% duty cycle setting. (The inversion locations are indicated by blue circles in the figures.)
  5. Dead time is not maintained in order to produce 0%/100% duty cycle output.

[Operation example 1] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.78 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).
(d) Due to cancelling of 0%/100% duty cycle output, output changes according to setting value of GTUDDTYC.OmDTYR bit and GTIOR.GTIOm[3:2] bits.
(e) When OmDTY bit is set to 1b, correction function causes negative phase to become pulse with width of 1 count clock cycle.
(f) Change point at GTDVU + 1 due to correction function, positive phase turns on.

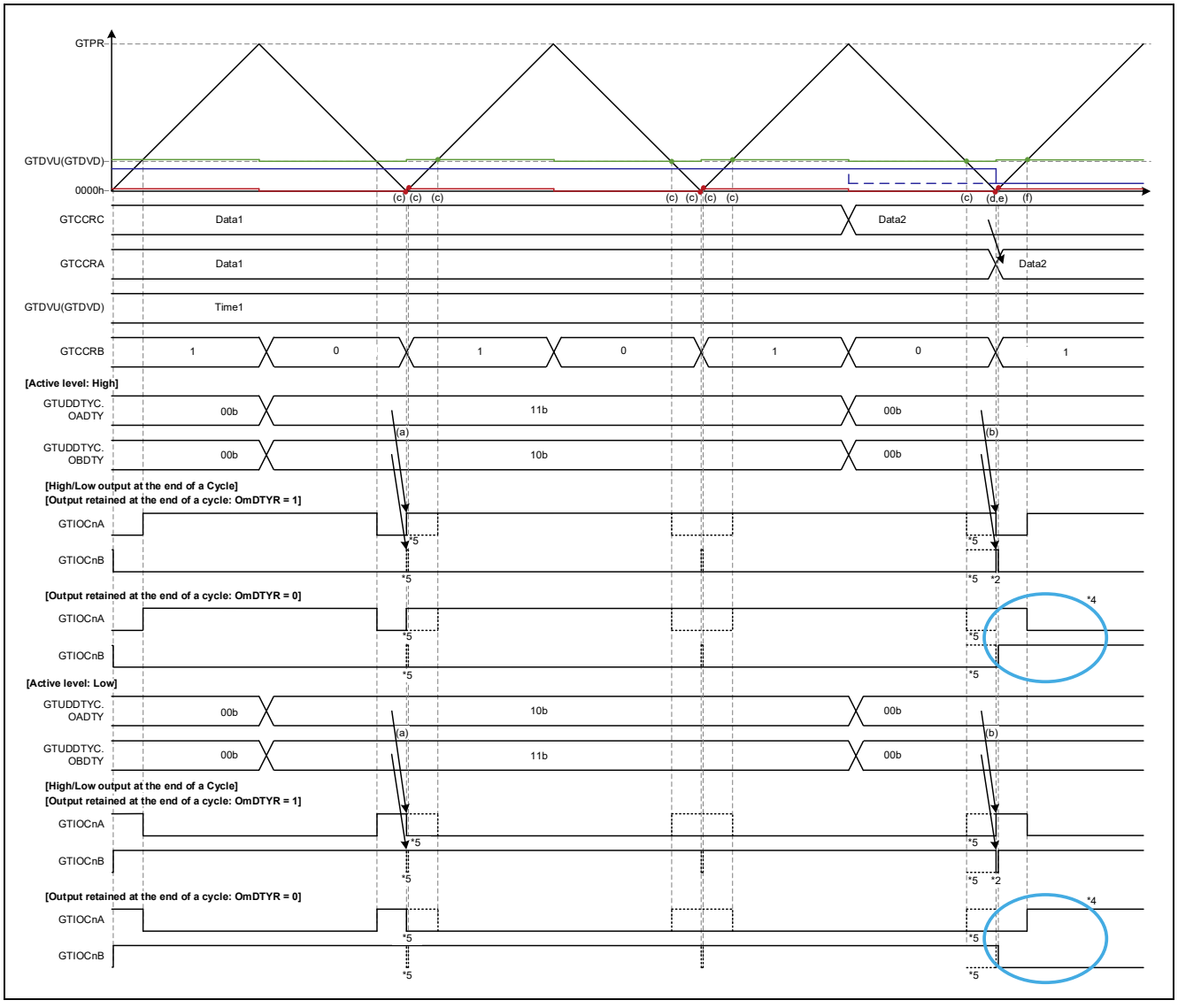


Figure 1.78 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: A → 0%/100% → A)

[Operation example 2] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.79 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.78.

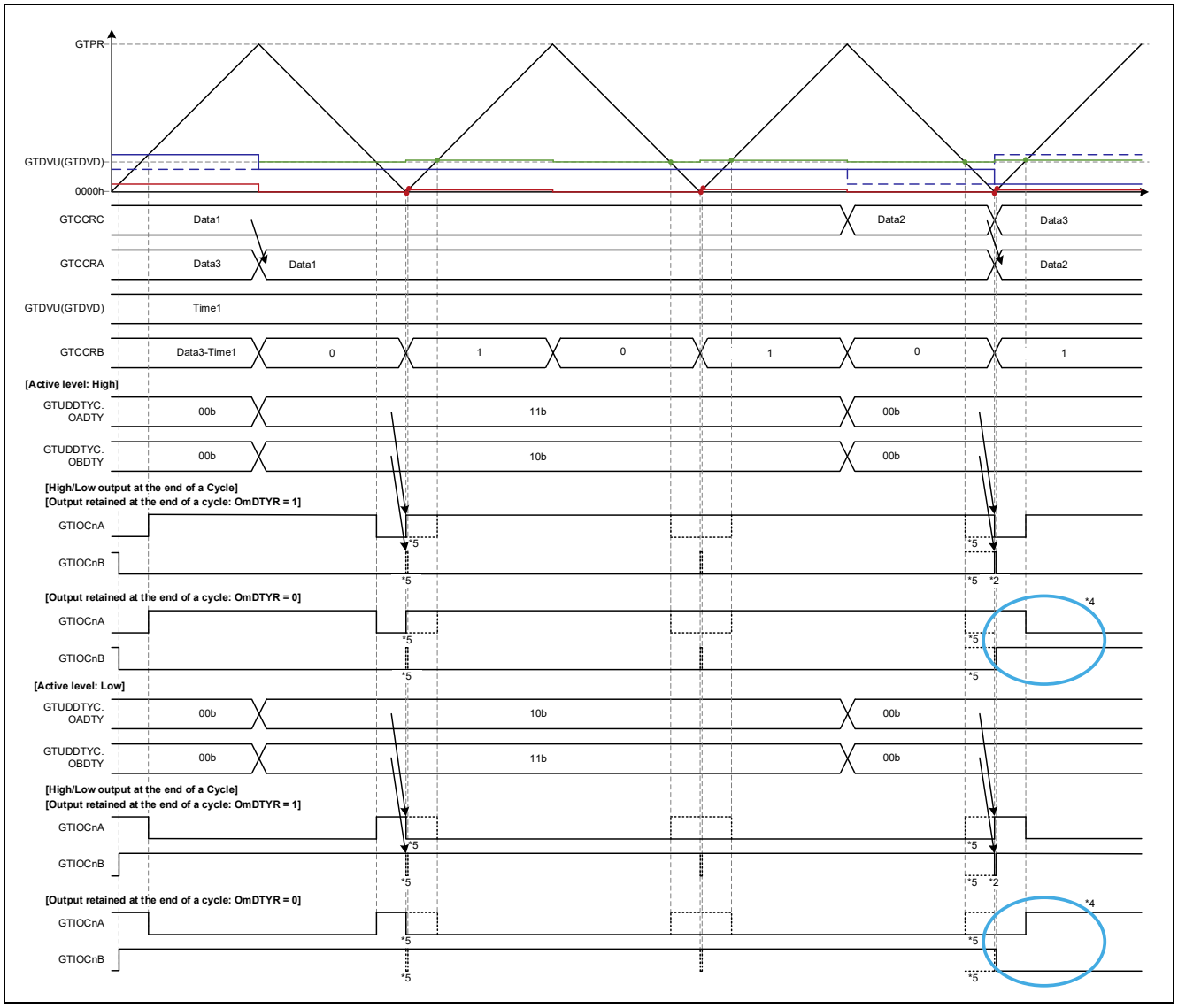


Figure 1.79 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: A → 0%/100% → A)

[Operation example 3] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.80 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.78.

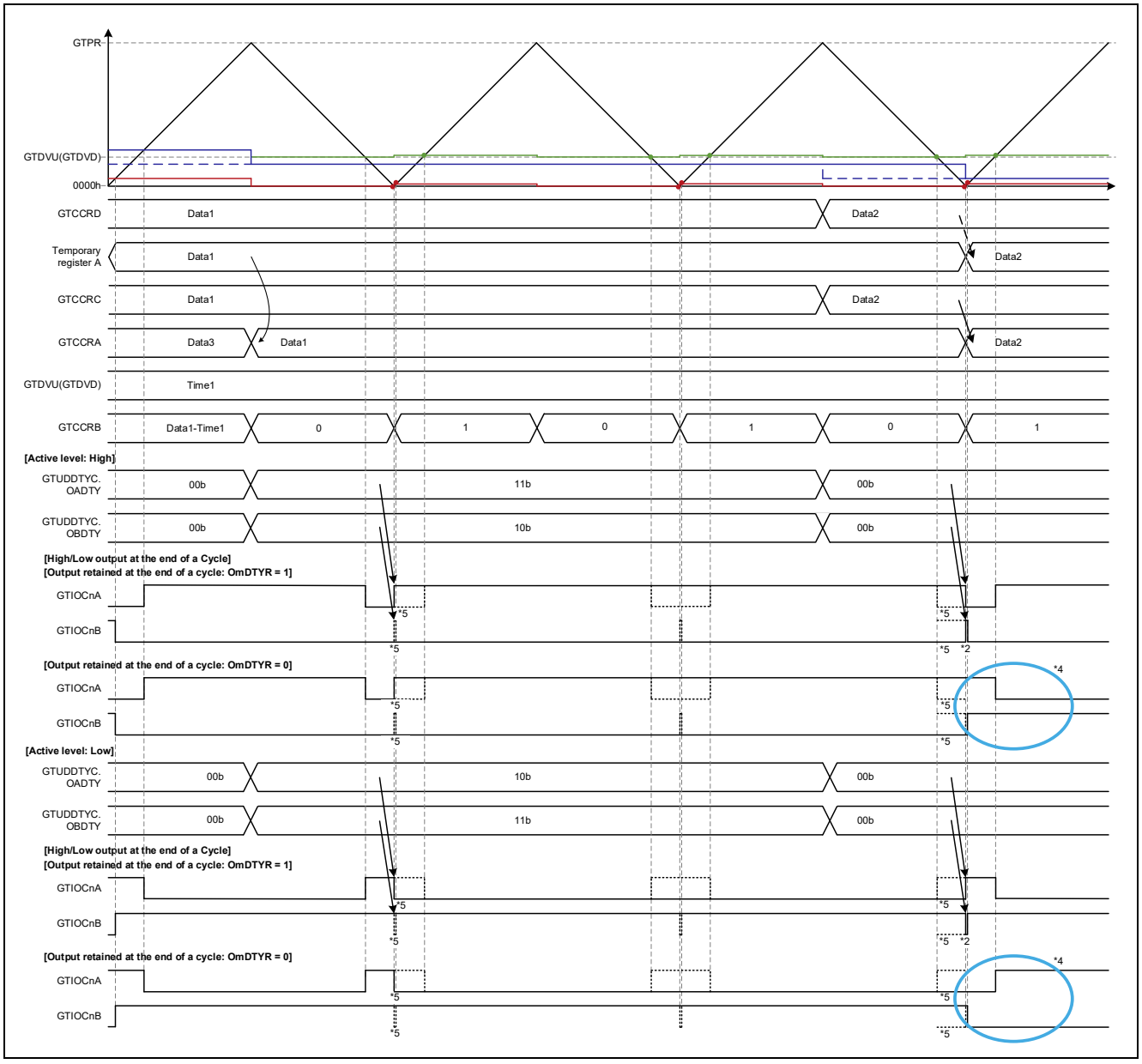


Figure 1.80 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: A → 0%/100% → A)

[Operation example 4] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.81 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Compare match with negative phase compare register.
(d) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).
(e) Due to cancelling of 0%/100% duty cycle output, output changes according to setting value of GTUDDTYC.OmDTYR bit and GTIOR.GTIOm[3:2] bits.

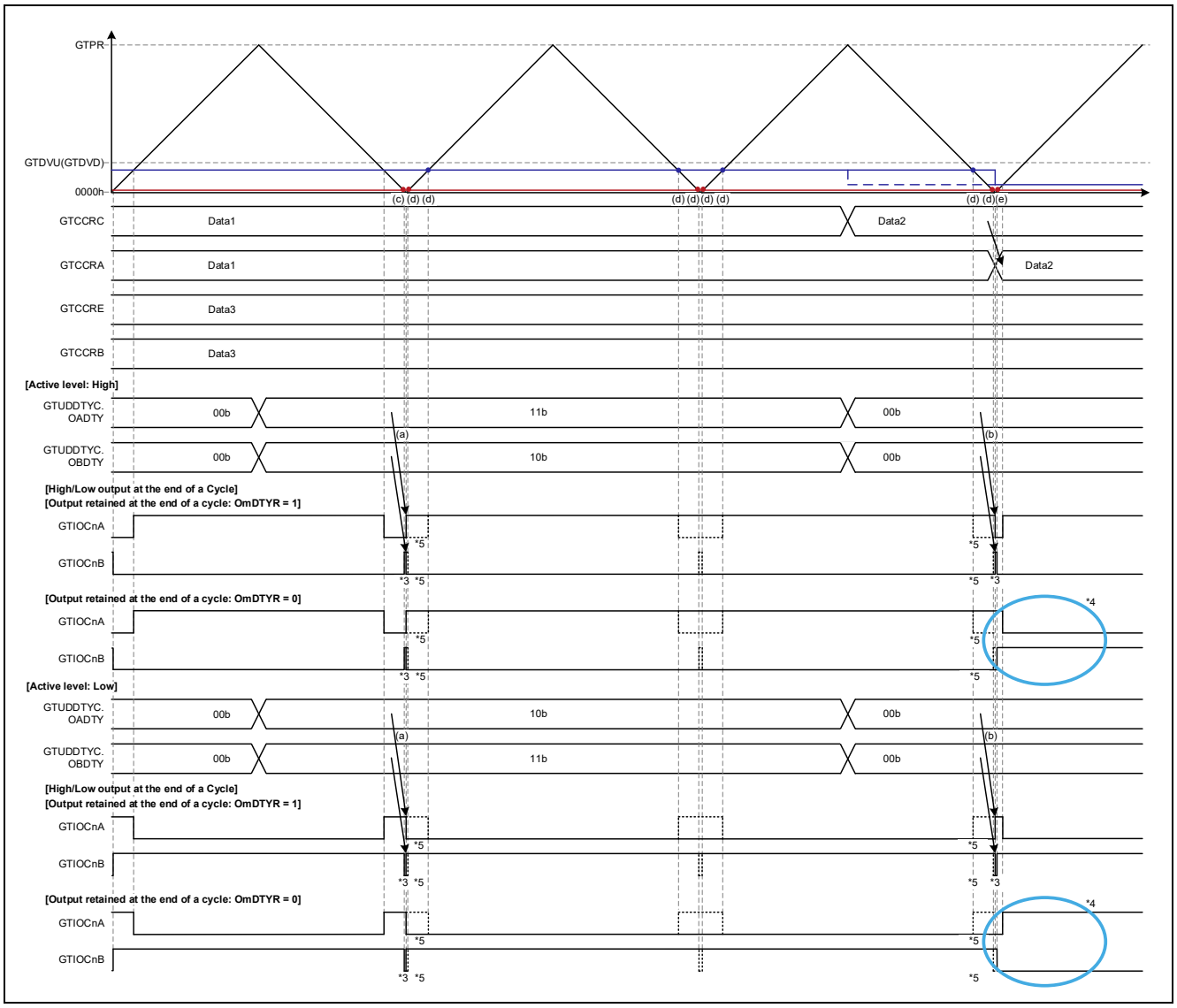


Figure 1.81 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: A → 0%/100% → A)

[Operation example 5] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.82 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.81.

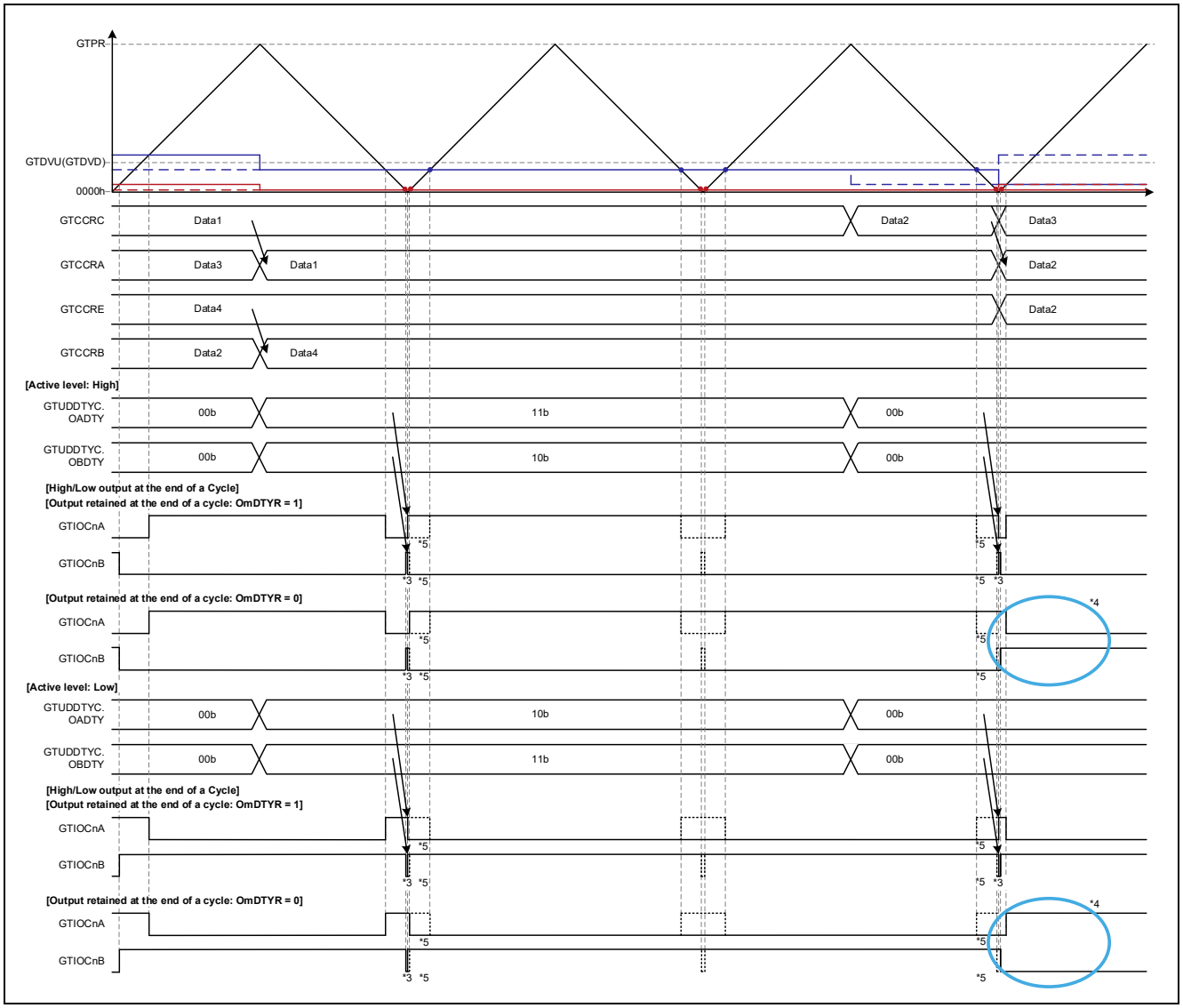


Figure 1.82 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: A → 0%/100% → A)

[Operation example 6] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.83 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.81.

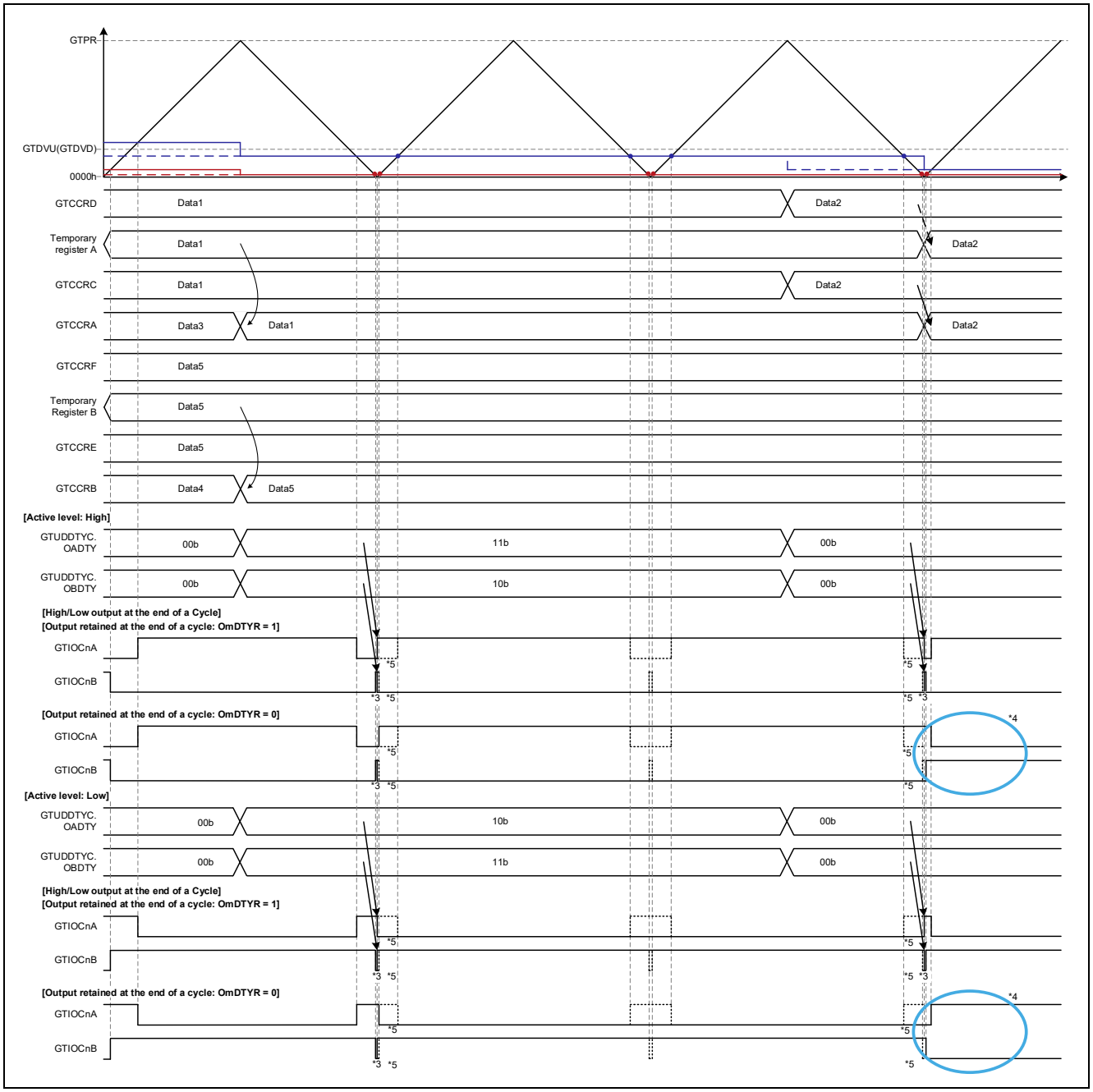


Figure 1.83 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: A → 0%/100% → A)

1.3.2.4 Change from Near 0% to 0% Duty Cycle (F → 0%/100% → F)

Figure 1.84 to Figure 1.89 illustrate the GPTW operating modes and cautions listed in Table 1.10.

- [Operation example 1] Figure 1.84, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4, 5, and 6
- [Operation example 2] Figure 1.85, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4, 5, and 6
- [Operation example 3] Figure 1.86, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled, cautions 4, 5, and 6
- [Operation example 4] Figure 1.87, Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4, 5, and 6
- [Operation example 5] Figure 1.88, Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4, 5, and 6
- [Operation example 6] Figure 1.89, Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled, cautions 4, 5, and 6

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: F → 0%/100% → F
  - F < GTPR, F > GTDVU
- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
  - Dotted black lines for GTIOCnA and GTIOCnB pins: Operation masked by 0% and 100% duty cycle settings
  - Data 1: F
- Cautions
  4. When the value of the GTUDDTYC.OmDTYR bit is 0b and that of the GTIOR.GTIOm[3:2] bits is 00b, after the recovery from 0%/100% duty cycle the output level is inverted relative to the output level before the 0%/100% duty cycle setting. (The inversion locations are indicated by blue circles in the figures.)
  5. Dead time is not maintained in order to produce 0%/100% duty cycle output.
  6. The positive phase becomes minute pulses to the extent that the value of F is close to GTPR.

[Operation example 1] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.84 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Output changes due to compare match with compare register.
(d) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).

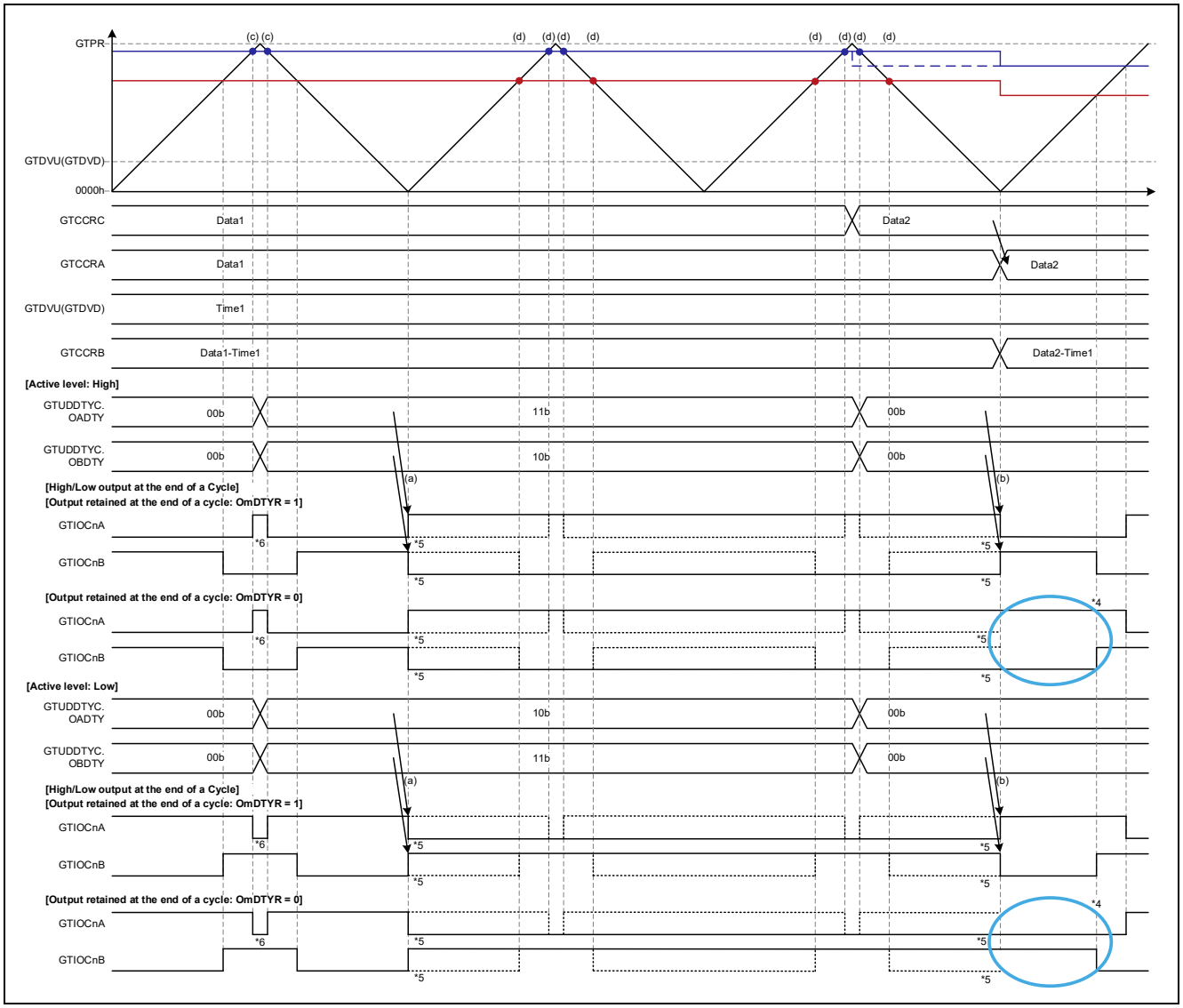


Figure 1.84 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: F → 0%/100% → F)

[Operation example 2] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.85 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.84.

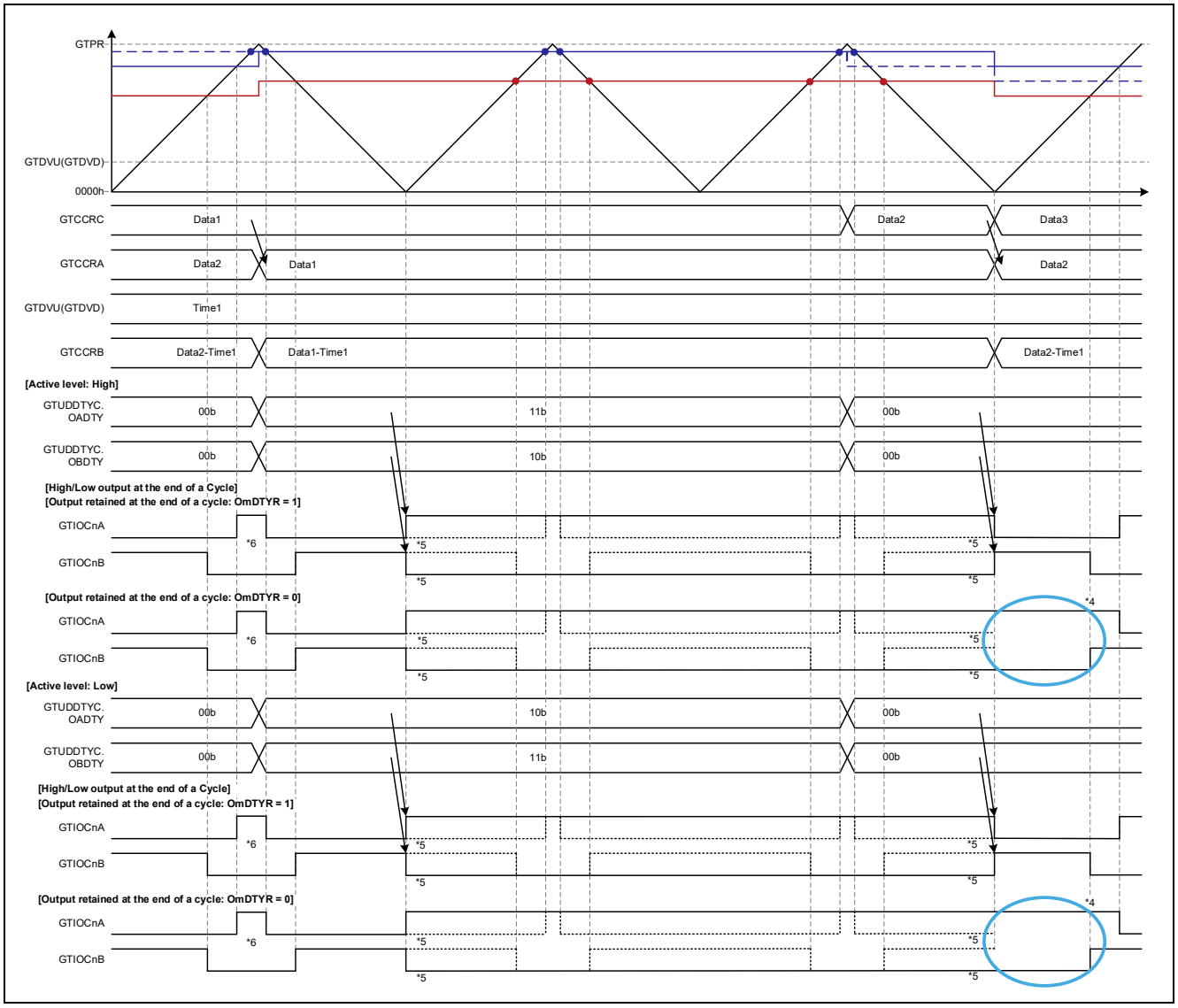


Figure 1.85 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: F → 0%/100% → F)

[Operation example 3] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Enabled

Figure 1.86 shows an operation example with automatic dead time setting function enabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.84.

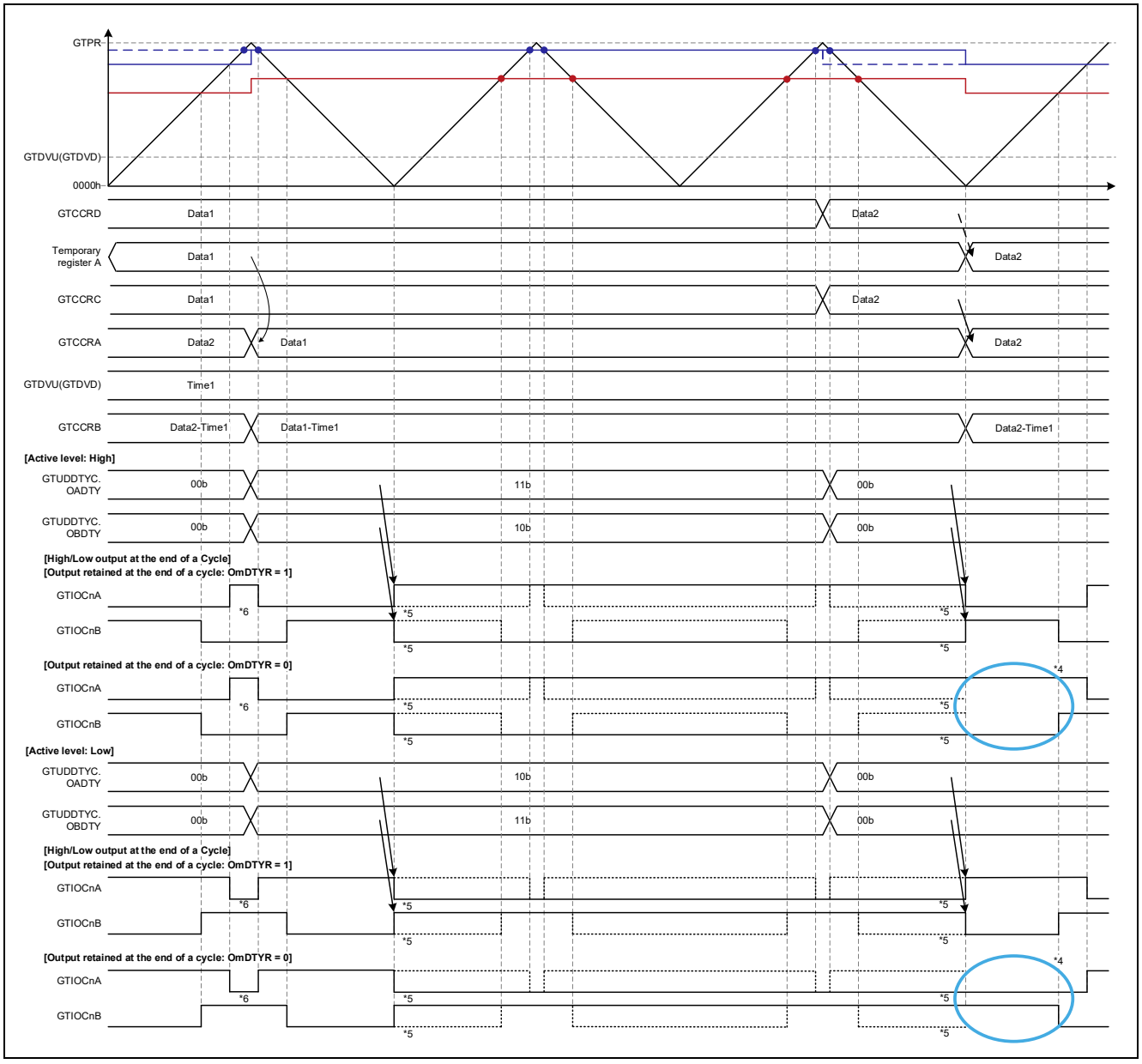


Figure 1.86 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Enabled, Duty: F → 0%/100% → F)

[Operation example 4] Triangle-Wave PWM Mode 1, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.87 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 1.

(a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
(b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
(c) Output changes due to compare match with compare register.
(d) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).

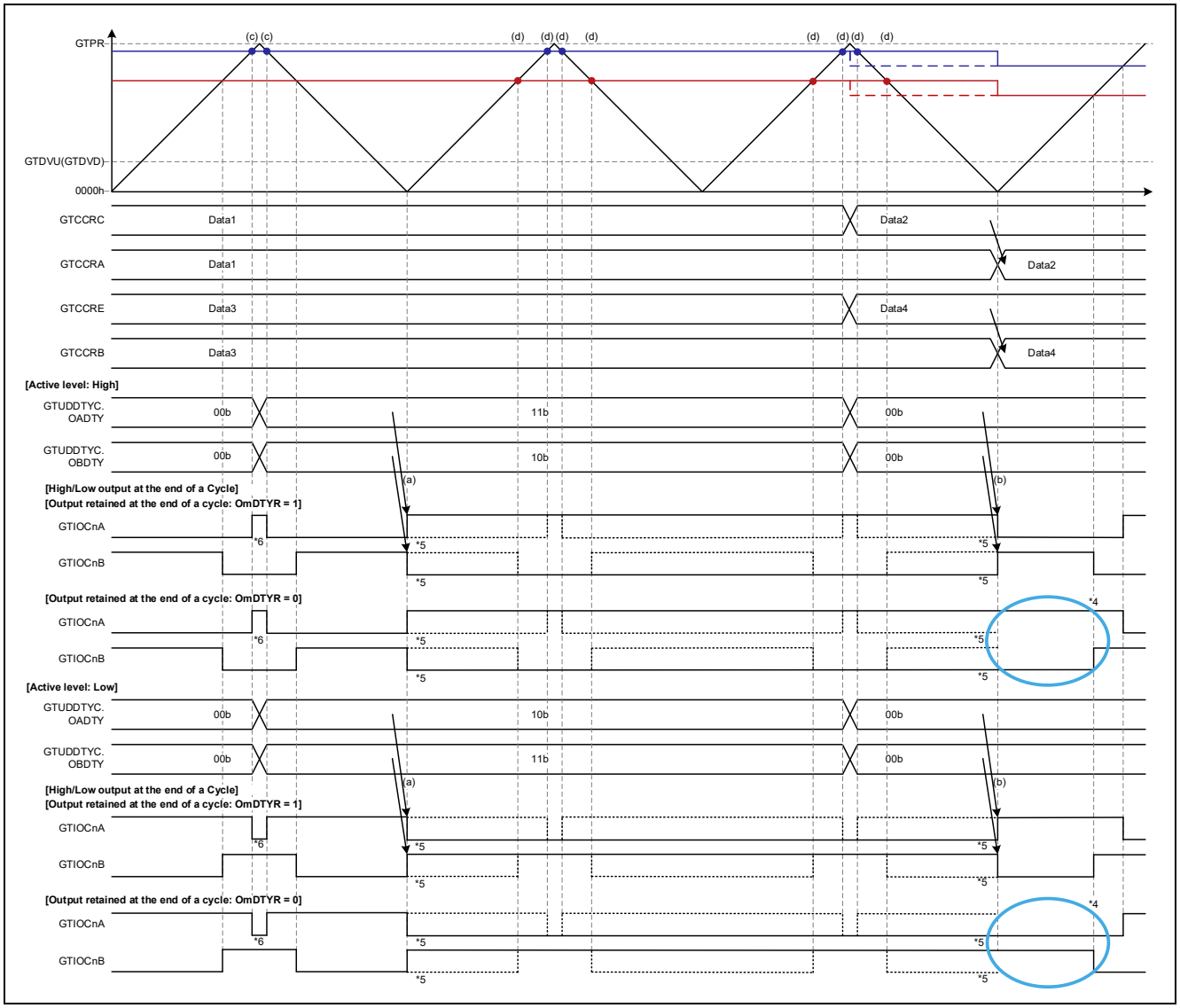


Figure 1.87 Triangle-Wave PWM Mode 1 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: F → 0%/100% → F)

[Operation example 5] Triangle-Wave PWM Mode 2, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.88 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 2. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.87.

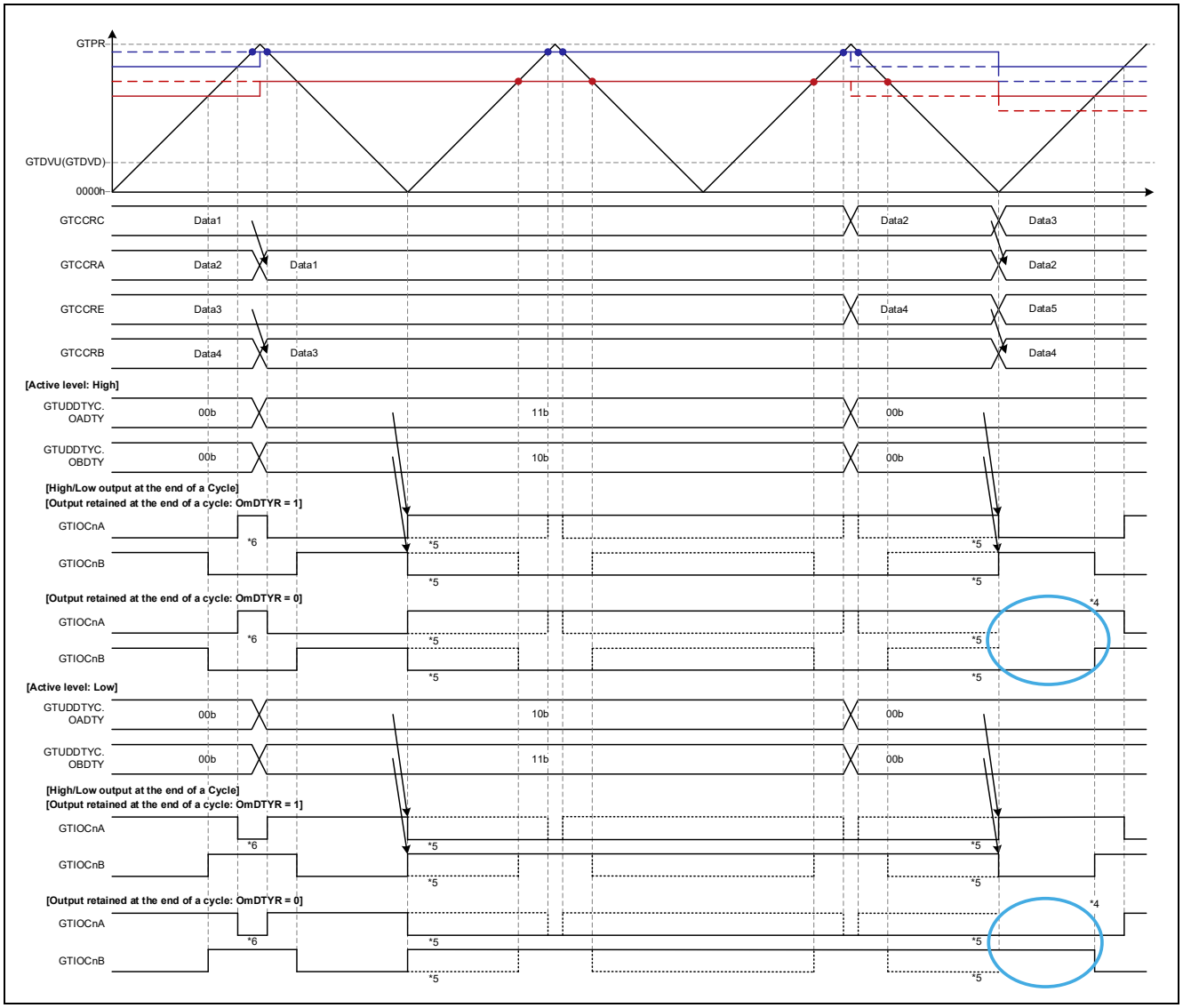


Figure 1.88 Triangle-Wave PWM Mode 2 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: F → 0%/100% → F)

[Operation example 6] Triangle-Wave PWM Mode 3, Output Start: Trough, Automatic Dead Time Setting Disabled

Figure 1.89 shows an operation example with automatic dead time setting function disabled in triangle-wave PWM mode 3. Except for the difference in the buffer operation in the various modes, the operation is the same as that shown in Figure 1.87.

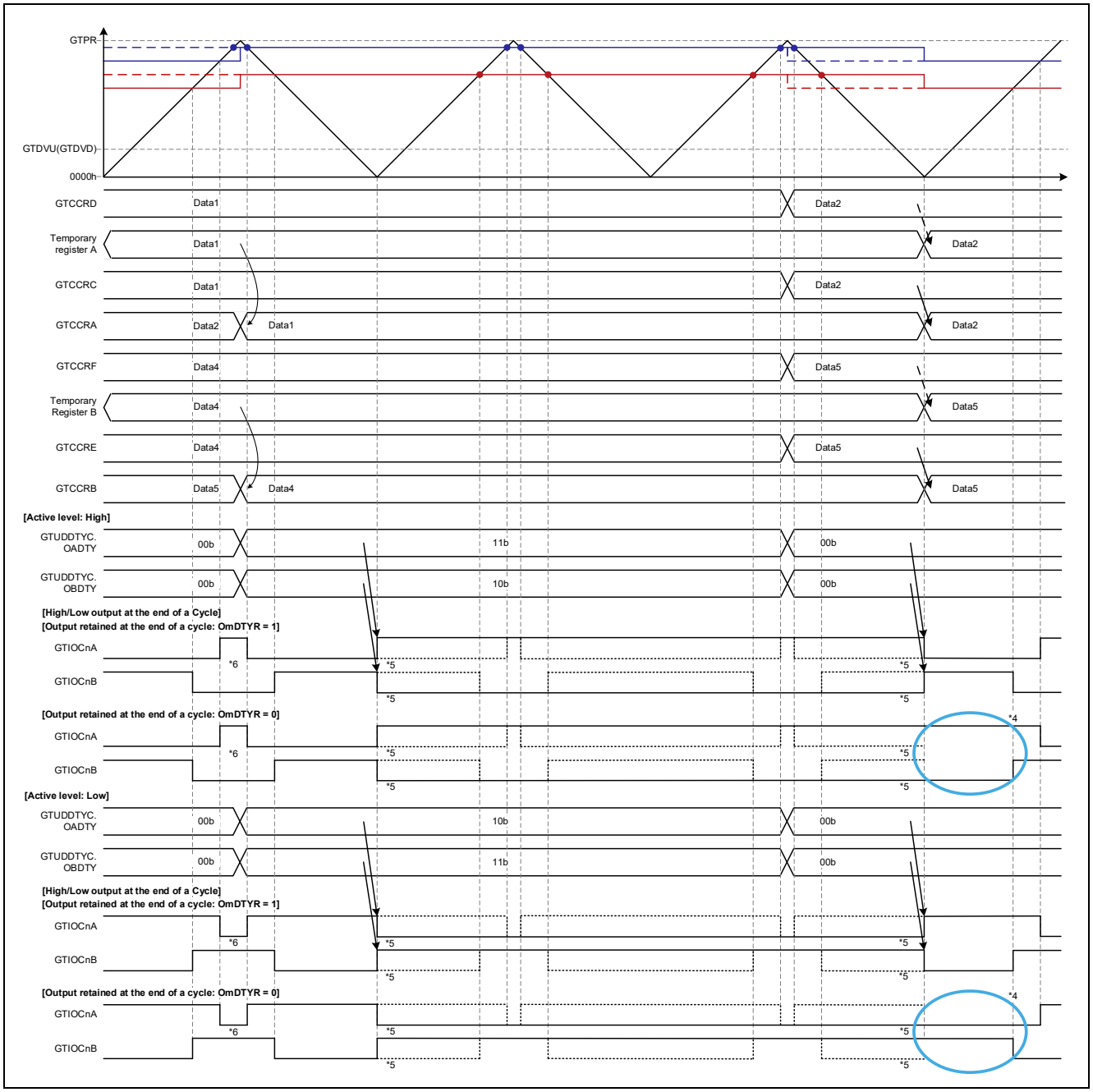


Figure 1.89 Triangle-Wave PWM Mode 3 Operation Example
(Output Start: Trough, Automatic Dead Time Setting Function Disabled, Duty: F → 0%/100% → F)

1.4 Cautions when Using GPTW Output Protection Function

On the GPTW the output protection function can be used to output 0% and 100% duty cycle waveforms. However, there are cautions to be considered regarding setting values when using the output protection function. These cautions are described in this section.

1.4.1 GPTW Output Protection Function

If an abnormal value (0000 0000h or a value exceeding the GTPR register setting value) is set in the GTCCRA register in triangle-wave PWM mode 1, 2, or 3 and automatic dead time setting enabled, the output protection function (disabling function) operates on the GTIOCnm (n = 0 to 9, m = A or B) pins. The protection function does not operate when automatic dead time setting is disabled.

The operating status of the output protection function can be confirmed by reading the GTSOS.SOS[1:0] bits.

For details of the output protection function, refer to 24.8.4, Output Protection Function for GTIOCnm Pin Output, in RX66T Group User's Manual: Hardware.

See the following section for a description of the operation of the output protection function and cautions that apply when the automatic dead time setting is enabled and when it is disabled.

1.4.2 Operation of Output Protection Function and Cautions when Automatic Dead Time Setting Is Enabled

Transitions in the state of the output protection function that occur when the setting value of the GTCCRA register changes are shown below.

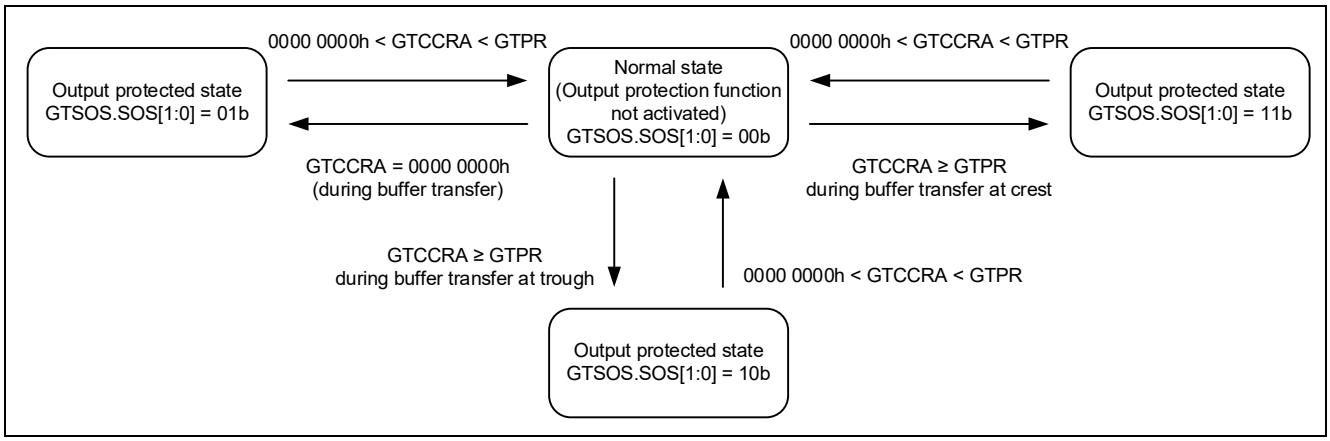


Figure 1.90 Output Protection Function State Transitions Relative to GTCCRA Settings

Intervals called "transition intervals" and "return intervals" occur during transitions between the normal state (output protection function disabled) and the output protected state.

- Transition interval: The interval in which transition from the normal state to the output protected state occurs and during which toggle operation continues
- Return interval: The interval in which return from the output protected state to the normal state occurs

Regarding the output protection function, caution is necessary because output operation in the transition interval and return interval will differ according to the (crest/trough) timing of the transfer to GTCCRA of abnormal values and normal values at return. Note that normal values meet the following condition: 0000 0000h < GTCCRA < GTPR.

Table 1.11, Table 1.12, and Table 1.13 show the conditions under which output protection occurs and the differences in operation in each interval due to the transfer timing of abnormal and normal values in triangle-wave PWM modes 1, 2, and 3.

Table 1.11 Triangle-Wave PWM Mode 1

Output Protection Function Activation Conditions	GTCCRA Transfer Timing		Interval Presence/Absence		Key
	Normal State → Output Protected State	Output Protected State → Normal State	Transition interval	Return interval	
GTCCRA = 000 0000h	Trough	Trough	Present	Present	Figure 1.91
GTCCRA ≥ GTPR	Trough	Trough	Absent	Absent	Figure 1.100

Table 1.12 Triangle-Wave PWM Mode 2

Output Protection Function Activation Conditions	GTCCRA Transfer Timing		Interval Presence/Absence		Key
	Normal State → Output Protected State	Output Protected State → Normal State	Transition interval	Return interval	
GTCCRA = 000 0000h	Trough	Trough	Present	Present	Figure 1.92
	Trough	Crest	Present	Absent	Figure 1.93
	Crest	Trough	Present	Present	Figure 1.94
	Crest	Crest	Present	Absent	Figure 1.95
GTCCRA ≥ GTPR	Trough	Trough	Absent	Absent	Figure 1.101
	Trough	Crest	Absent	Present	Figure 1.102
	Crest	Trough	Absent	Present	Figure 1.103
	Crest	Crest	Absent	Absent	Figure 1.104

Table 1.13 Triangle-Wave PWM Mode 3

Output Protection Function Activation Conditions	GTCCRA Transfer Timing		Interval Presence/Absence		Key
	Normal State → Output Protected State	Output Protected State → Normal State	Transition interval	Return interval	
GTCCRA = 000 0000h	Trough	Trough	Present	Present	Figure 1.96
	Trough	Crest	Present	Absent	Figure 1.97
	Crest	Trough	Present	Present	Figure 1.98
	Crest	Crest	Present	Absent	Figure 1.99
GTCCRA ≥ GTPR	Trough	Trough	Absent	Absent	Figure 1.105
	Trough	Crest	Absent	Present	Figure 1.106
	Crest	Trough	Absent	Present	Figure 1.107
	Crest	Crest	Absent	Absent	Figure 1.108

1.4.2.1 Operation Examples with Abnormal Value (0000 0000h) Setting

Operation examples when an abnormal value (0000 0000h) setting is used as listed in Table 1.11, Table 1.12, and Table 1.13 are shown in Figure 1.91 to Figure 1.99 and applicable cautions are described below.

- Operation Example 1: Figure 1.91 Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 7 and 8
- Operation Example 2: Figure 1.92 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 7 and 8
- Operation Example 3: Figure 1.93 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest), caution 7
- Operation Example 4: Figure 1.94 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough), cautions 2, 7, 8, and 9
- Operation Example 5: Figure 1.95 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest), cautions 2, 7, and 9
- Operation Example 6: Figure 1.96 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 7 and 8
- Operation Example 7: Figure 1.97 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest), caution 7
- Operation Example 8: Figure 1.98 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough), cautions 2, 7, 8, and 9
- Operation Example 9: Figure 1.99 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest), cautions 2, 7, and 9

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → 0000 0000h → D
  - D > GTDVU

- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Solid green line: Positive phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: 0000 0000h

- Key to figures
  2. The correction function causes the negative phase to become minute pulses with a width of 1 count clock cycle.
  7. Transition interval. Output toggle operation continues until next crest.
  8. Return interval. Output maintained until next crest.
  9. GTCCRA = 0000 0000h, but toggle operation continues until next trough.
  10. Transition interval. Output maintained until next trough.

[Operation Example 1] Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.91 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 1

(a) Change point 1 count clock cycle from trough due to correction function, negative phase turns off.
(b) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(c) Output maintained by output protection function.
(d) Compare match occurs, but output maintained due to return interval.
(e) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(f) Change at 1 count clock cycle after trough.

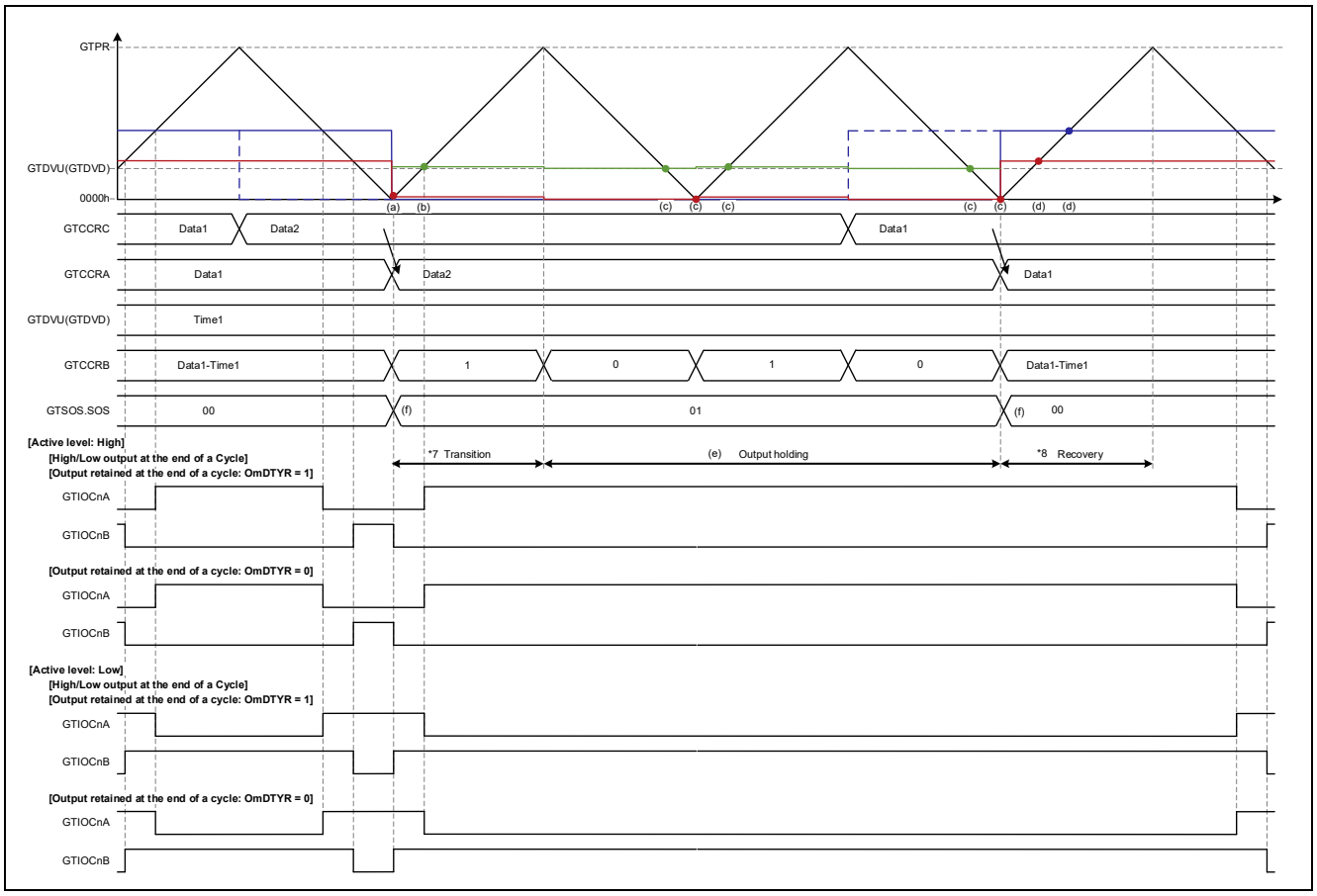


Figure 1.91 Triangle-Wave PWM Mode 1 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 2] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.92 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.91.

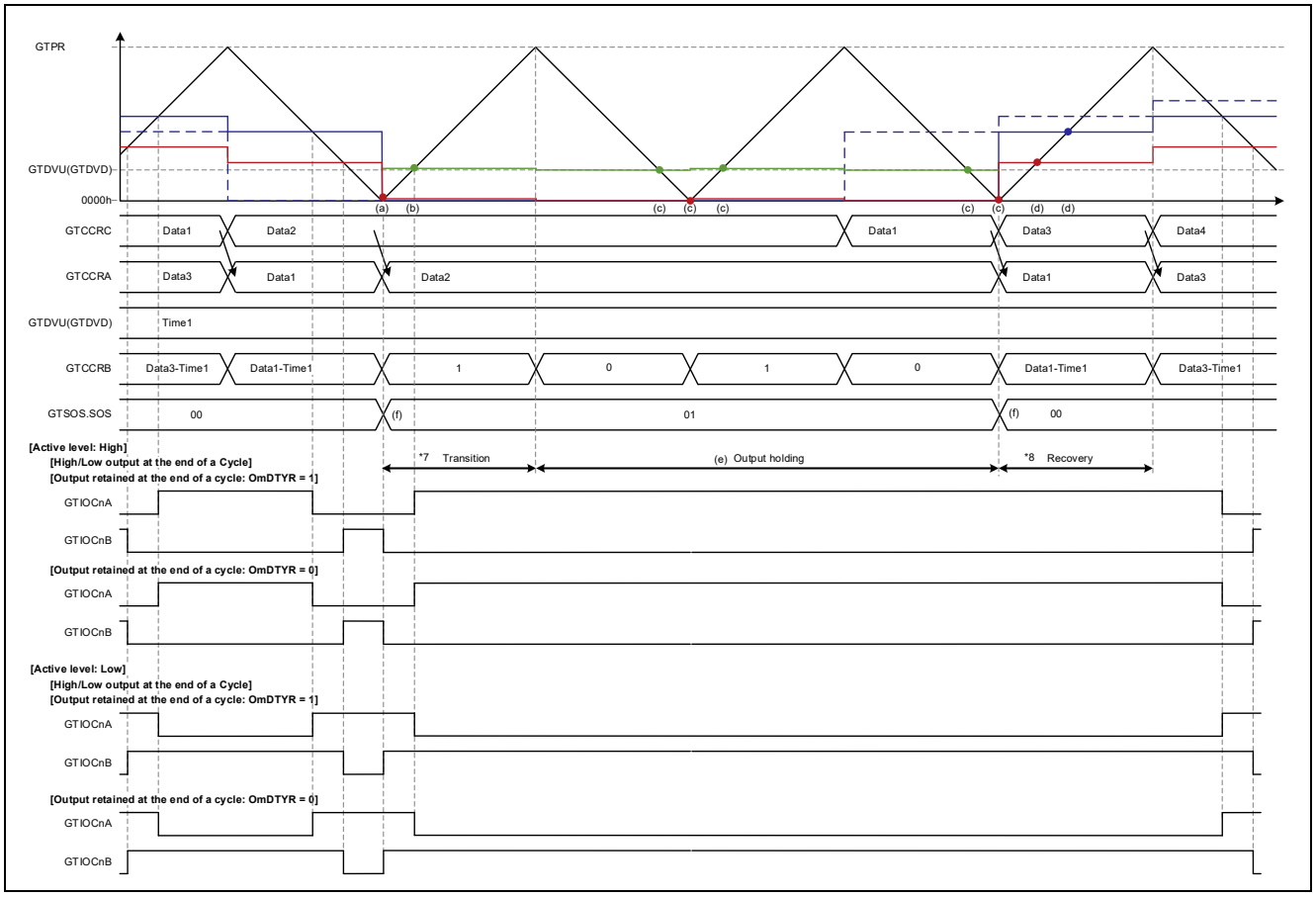


Figure 1.92 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 3] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest)

Figure 1.93 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 2

(a) Change point 1 count clock cycle from trough due to correction function, negative phase turns off.
(b) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(c) Compare match occurs, but output maintained due to return interval.
(d) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(e) Change at 1 count clock cycle after trough.
(f) Change at 1 count clock cycle after crest.

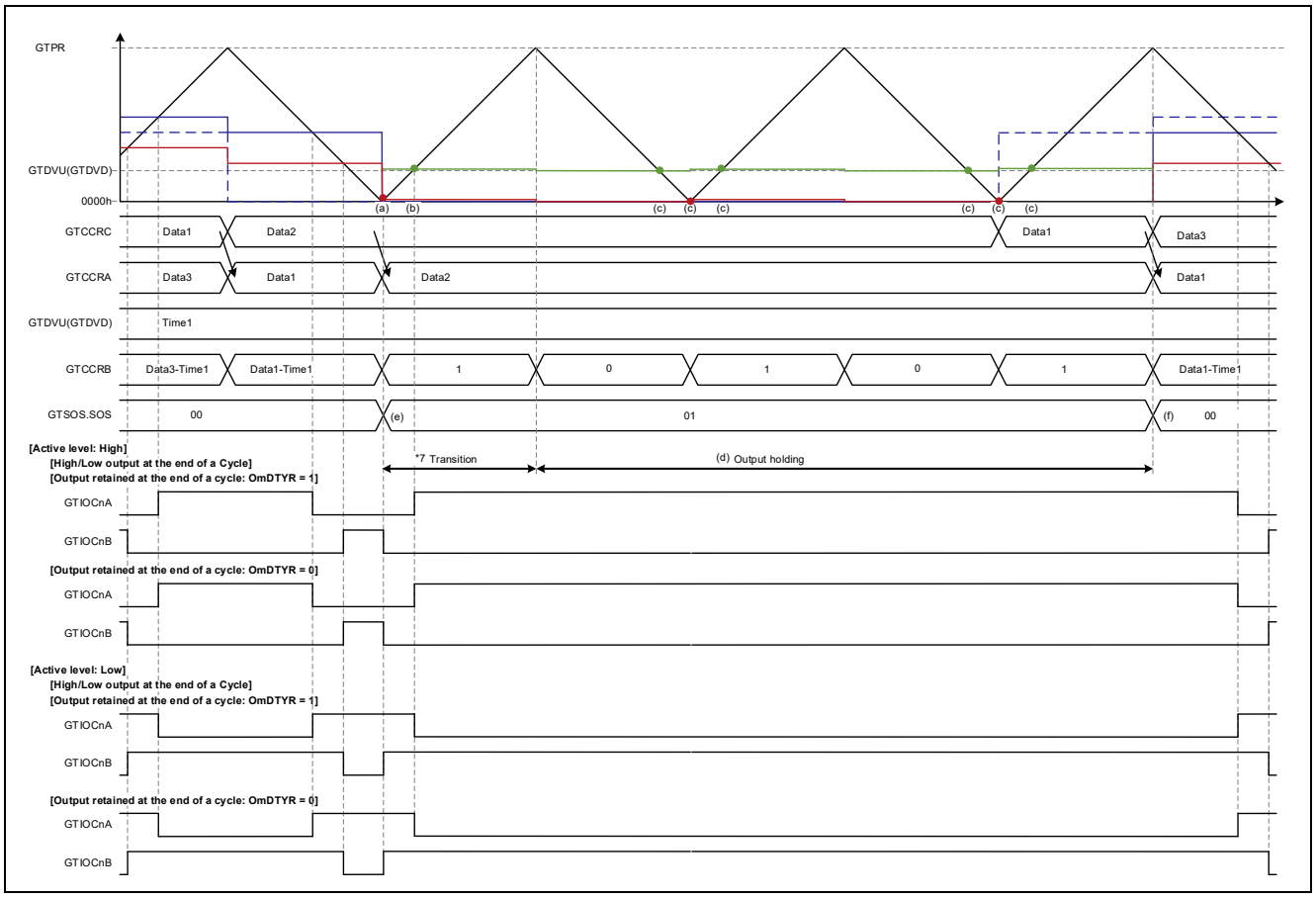


Figure 1.93 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 4] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough)

Figure 1.94 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at crest and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 2

(a) Change point at GTDVU due to correction function, positive phase turns off.
(b) Generation of pulse with width of 1 count clock cycle due to correction function.
(c) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(d) Output maintained by output protection function.
(e) Compare match occurs, but output maintained due to return interval.
(f) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(g) Change at 1 count clock cycle after trough.

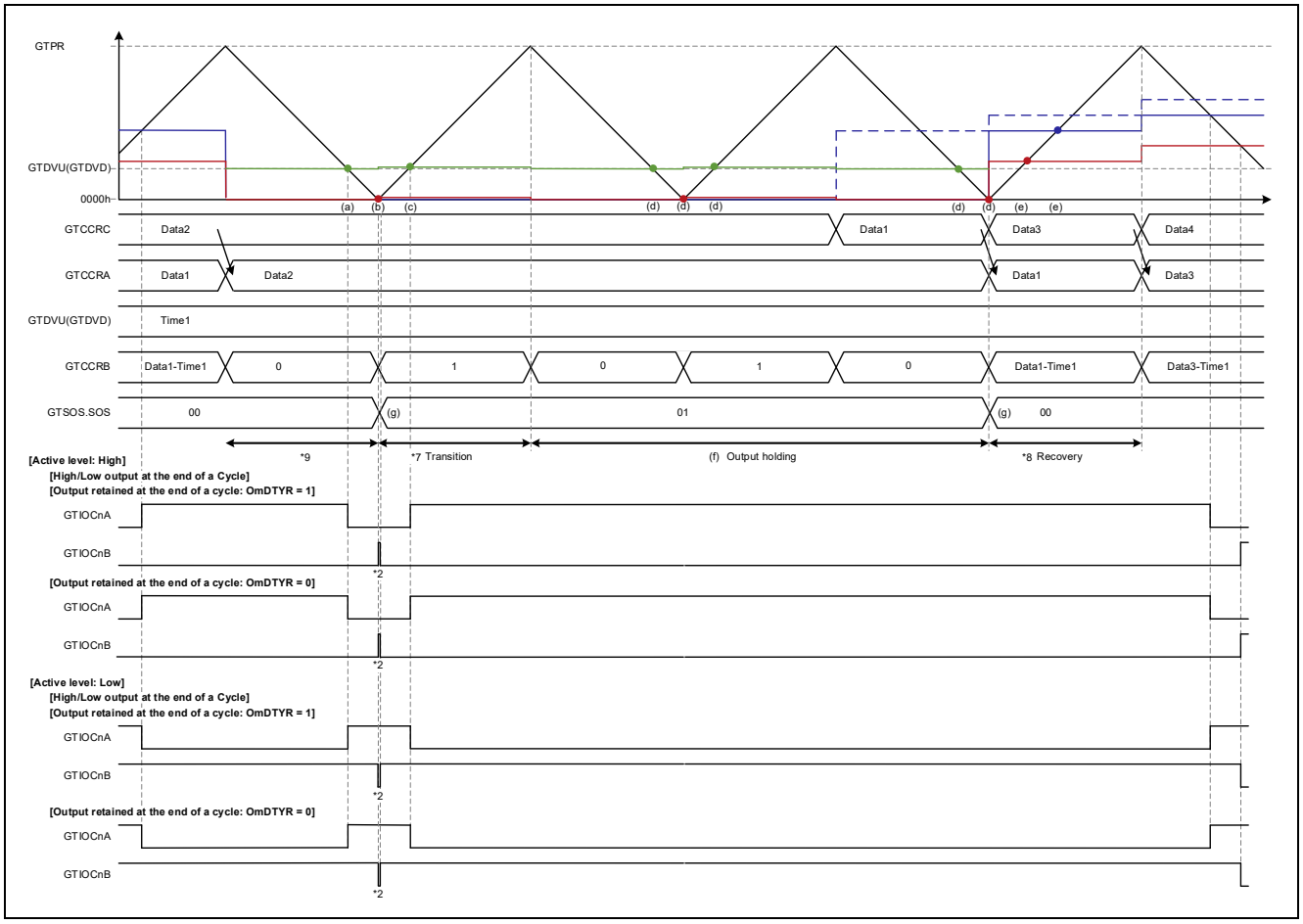


Figure 1.94 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Crest, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 5] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)

Figure 1.95 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at crest and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 2

(a) Change point at GTDVU due to correction function, positive phase turns off.
(b) Generation of pulse with width of 1 count clock cycle due to correction function.
(c) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(d) Output maintained by output protection function.
(e) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(f) Change at 1 count clock cycle after trough.
(g) Change at 1 count clock cycle after crest.

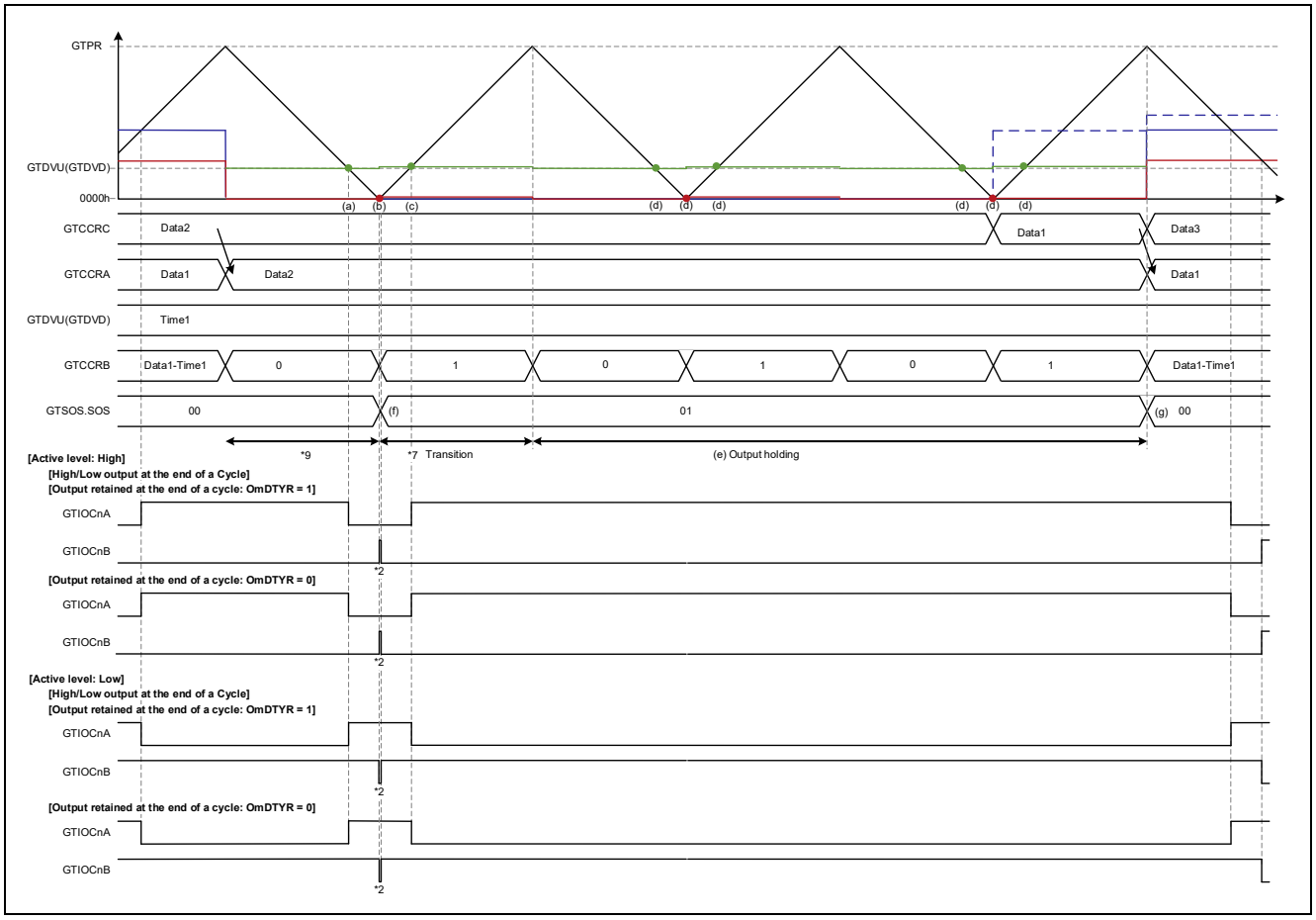


Figure 1.95 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Crest, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 6] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.96 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 3

(a) Change point 1 count clock cycle from trough due to correction function, negative phase turns off.
(b) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(c) Output maintained by output protection function.
(d) Compare match occurs, but output maintained due to return interval.
(e) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(f) Change at 1 count clock cycle after trough.

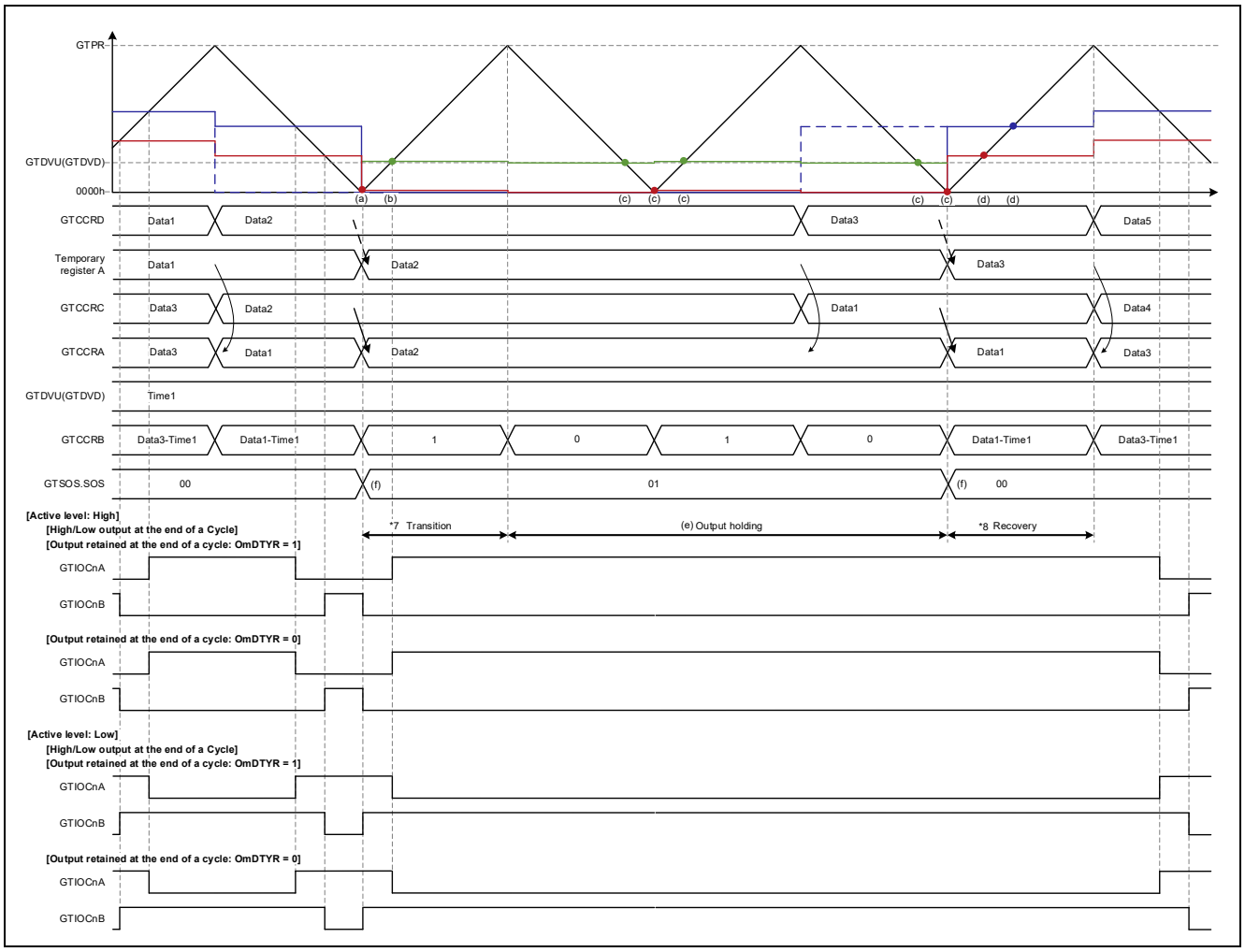


Figure 1.96 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 7] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest)

Figure 1.97 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 3

(a) Change point 1 count clock cycle from trough due to correction function, negative phase turns off.
(b) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(c) Compare match occurs, but output maintained due to return interval.
(d) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(e) Change at 1 count clock cycle after trough.
(f) Change at 1 count clock cycle after crest.

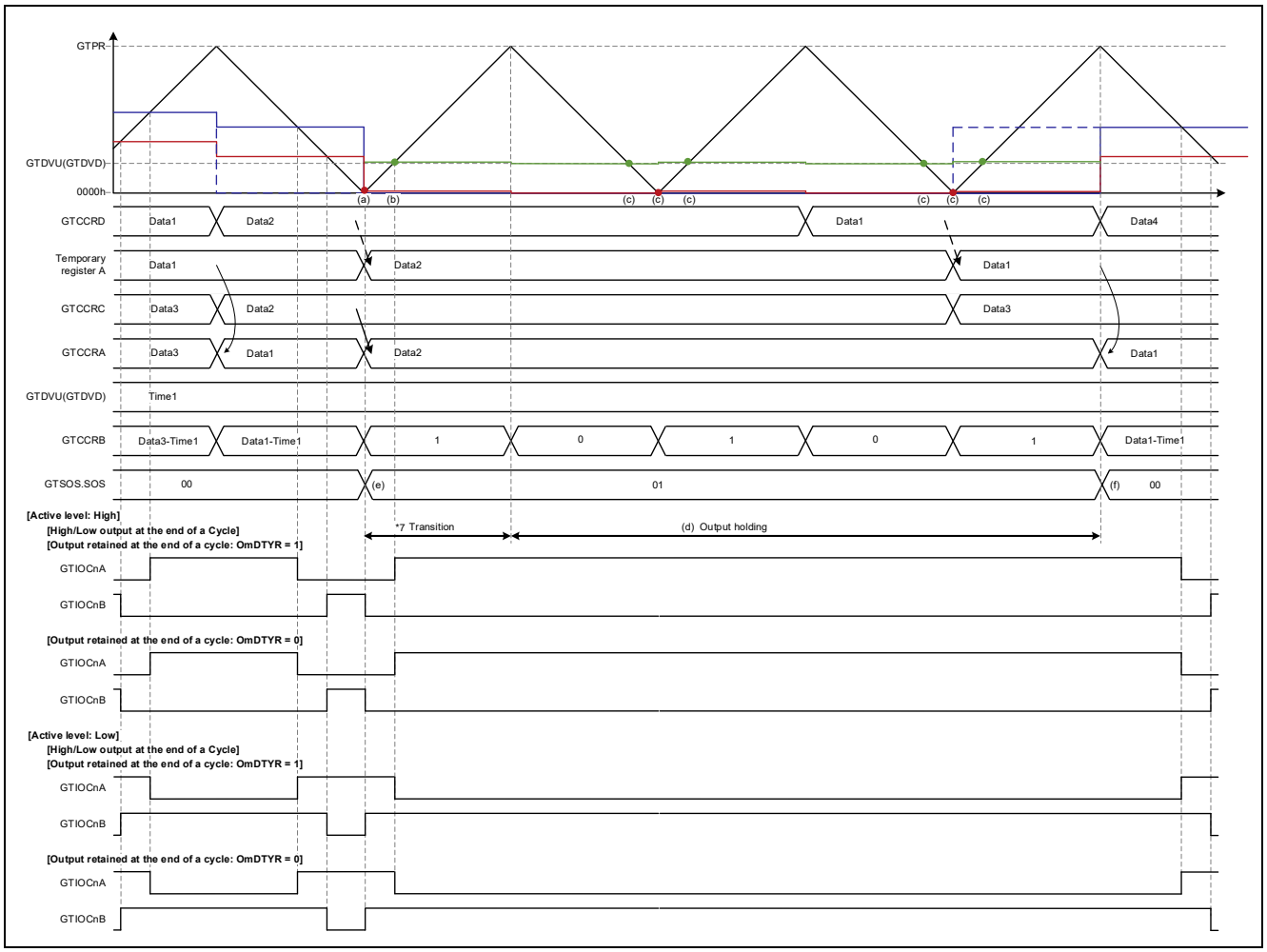


Figure 1.97 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 8] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough)

Figure 1.98 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at crest and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 3

(a) Change point at GTDVU due to correction function, positive phase turns off.
(b) Generation of pulse with width of 1 count clock cycle due to correction function.
(c) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(d) Output maintained by output protection function.
(e) Compare match occurs, but output maintained due to return interval.
(f) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(g) Change at 1 count clock cycle after trough.

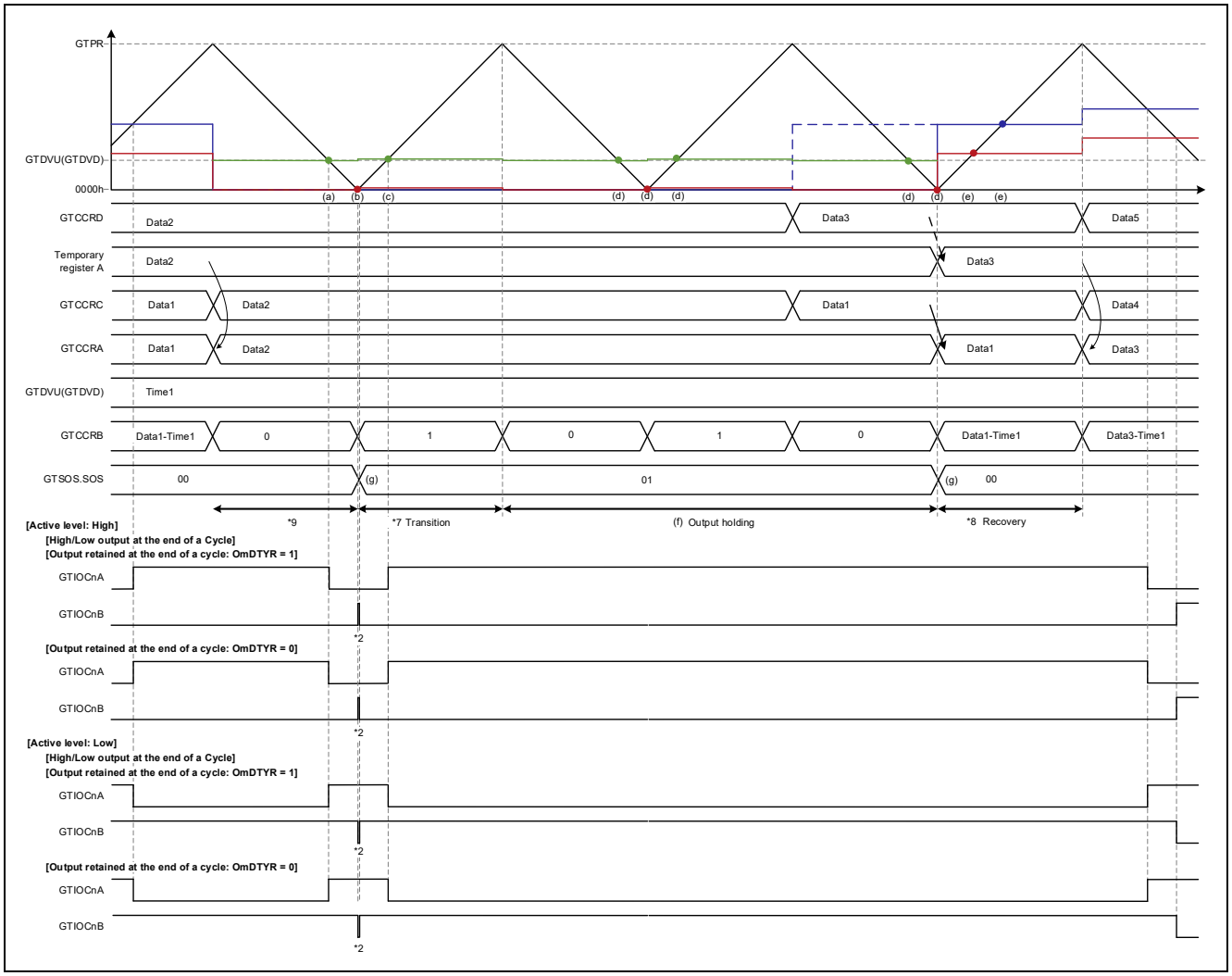


Figure 1.98 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Crest, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 9] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)

Figure 1.99 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at crest and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 3

(a) Change point at GTDVU due to correction function, positive phase turns off.
(b) Generation of pulse with width of 1 count clock cycle due to correction function.
(c) Change point at GTDVU + 1 due to correction function, positive phase turns on.
(d) Output maintained by output protection function.
(e) Output maintained interval. Output maintained while GTCCRA = 0000 0000h.
(f) Change at 1 count clock cycle after trough.
(g) Change at 1 count clock cycle after crest.

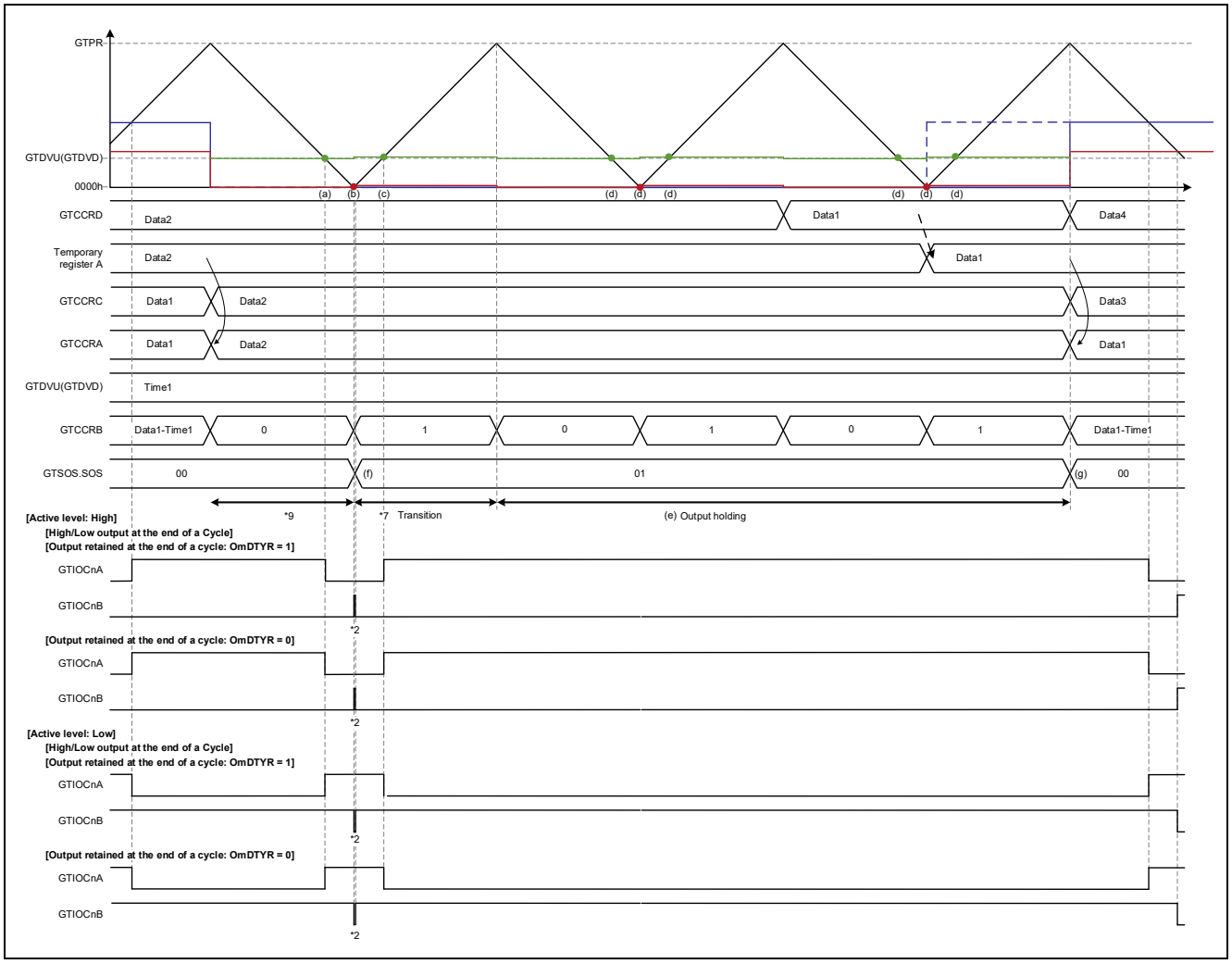


Figure 1.99 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Crest, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Crest)

1.4.2.2 Operation Examples with Abnormal Value (Value Exceeding GTPR Register Setting Value) Setting

Operation examples when an abnormal value (value exceeding GTPR register setting value) setting is used as listed in Table 1.11, Table 1.12, and Table 1.13 are shown in Figure 1.100 to Figure 1.108 and applicable cautions are described below.

- Operation Example 1: Figure 1.100 Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)
- Operation Example 2: Figure 1.101 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)
- Operation Example 3: Figure 1.102 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest), caution 10
- Operation Example 4: Figure 1.103 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough), caution 7
- Operation Example 5: Figure 1.104 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)
- Operation Example 6: Figure 1.105 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)
- Operation Example 7: Figure 1.106 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest), caution 10
- Operation Example 8: Figure 1.107 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough), caution 7
- Operation Example 9: Figure 1.108 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → G → D
  - D > GTDVU
  - G ≥ GTPR

- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: G

- Key to figures
  7. Transition interval. Output toggle operation continues until next crest.
  10. Transition interval. Output maintained until next trough.

[Operation Example 1] Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.100 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 1.

(a) Output maintained by output protection function.
(b) Output maintained by output protection function.

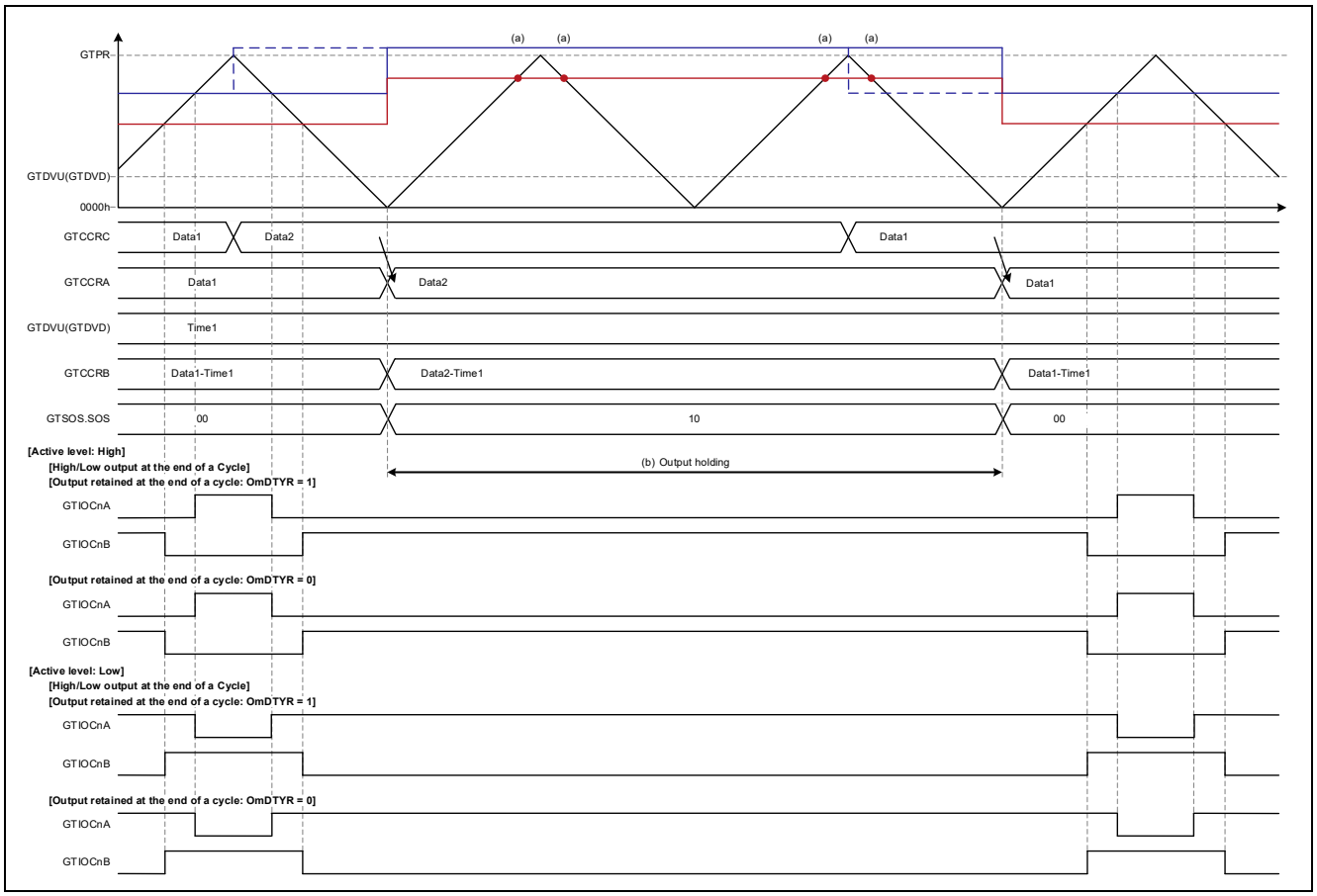


Figure 1.100 Triangle-Wave PWM Mode 1 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 2] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.101 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 2. Except for the difference in the buffer overwrite timing, the operation is the same as that shown in Figure 1.100.

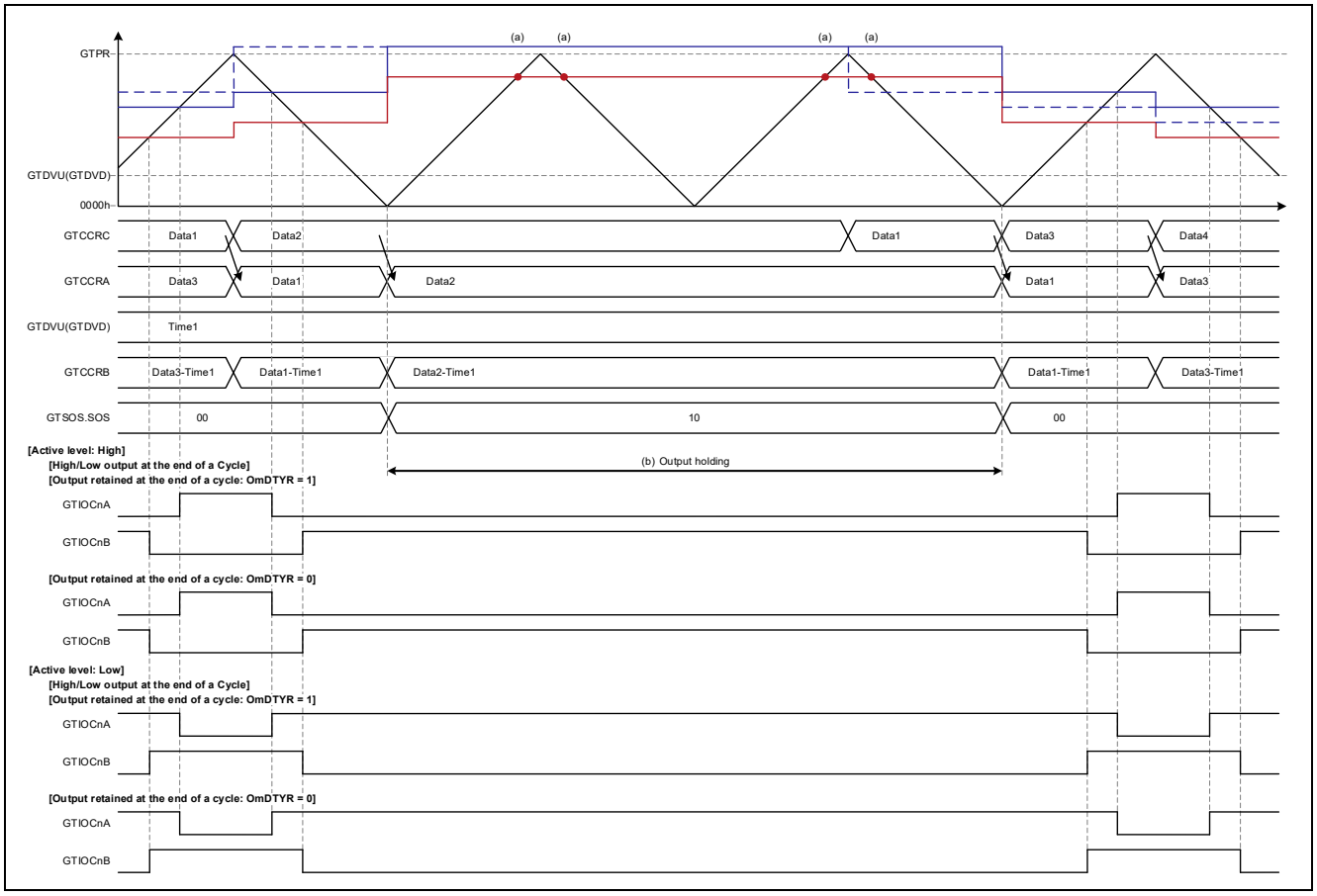


Figure 1.101 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 3] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest)

Figure 1.102 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 2.

(a) Output maintained by output protection function.
(b) Compare match occurs, but output maintained due to return interval.
(c) Output maintained by output protection function.

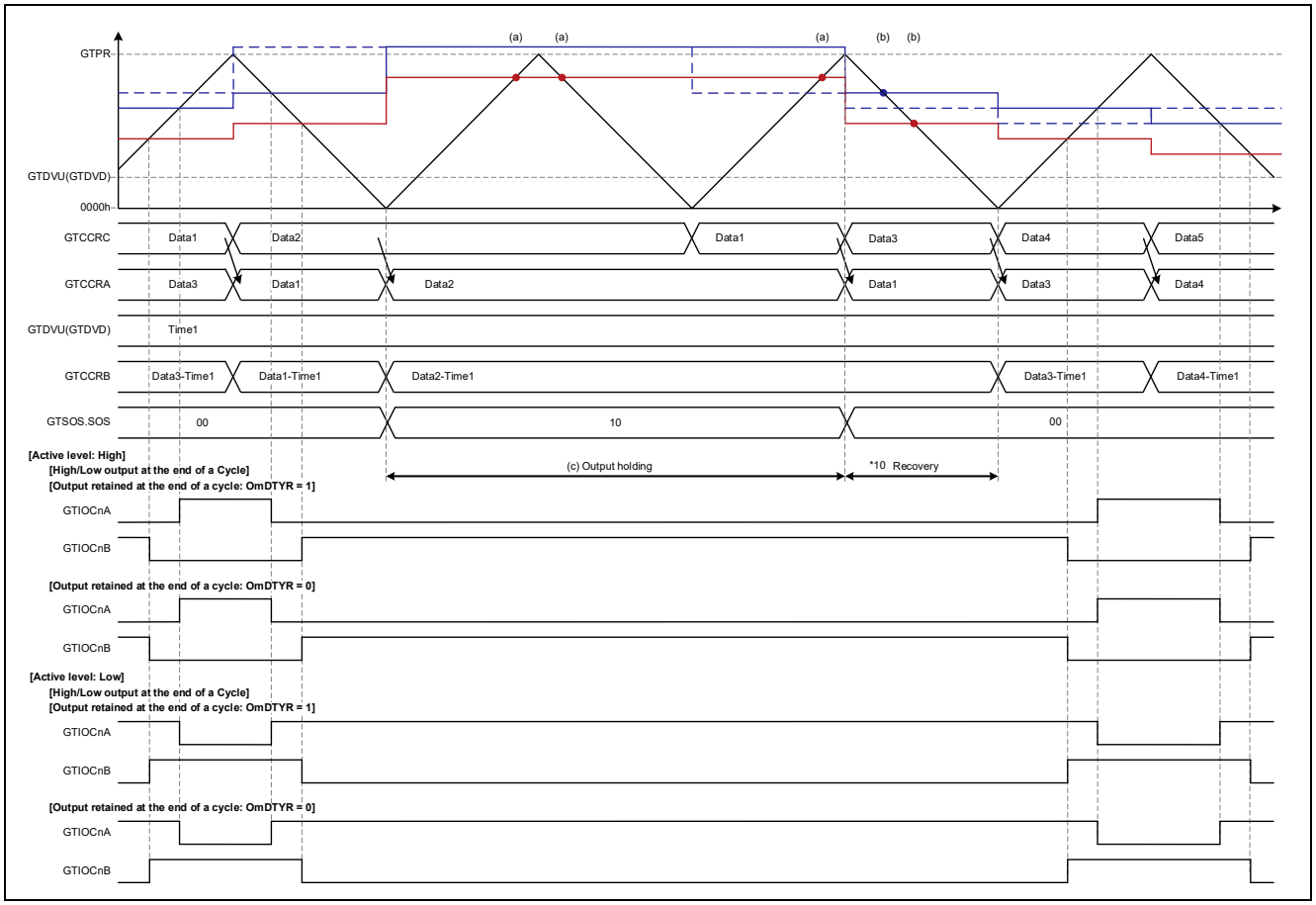


Figure 1.102 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 4] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough)

Figure 1.103 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at crest and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 2.

(a) Output maintained by output protection function.
(b) Compare match occurs, but output maintained due to return interval.
(c) Output maintained by output protection function.

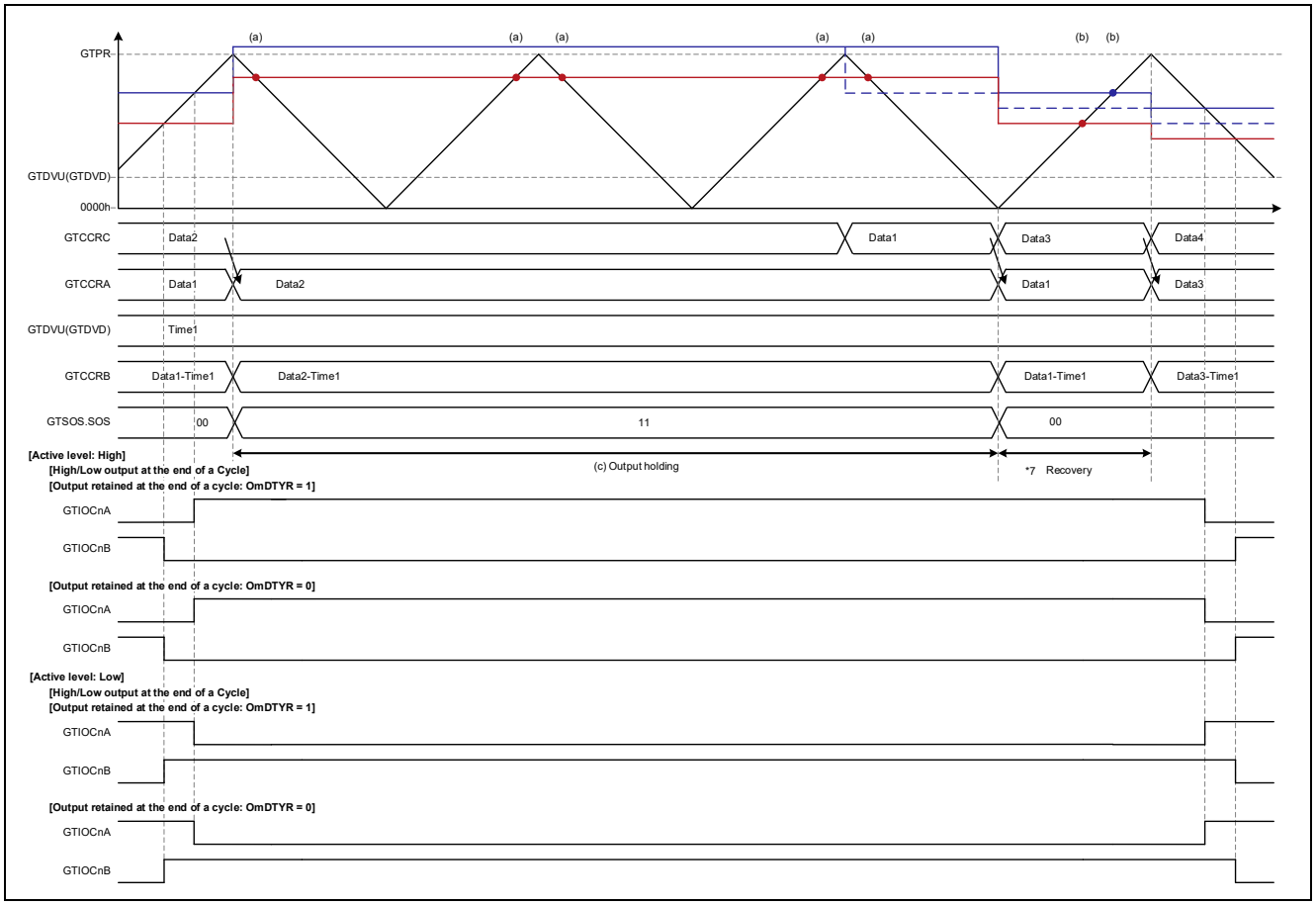


Figure 1.103 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Crest, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 5] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)

Figure 1.104 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at crest and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 2.

(a) Output maintained by output protection function.
(b) Output maintained by output protection function.

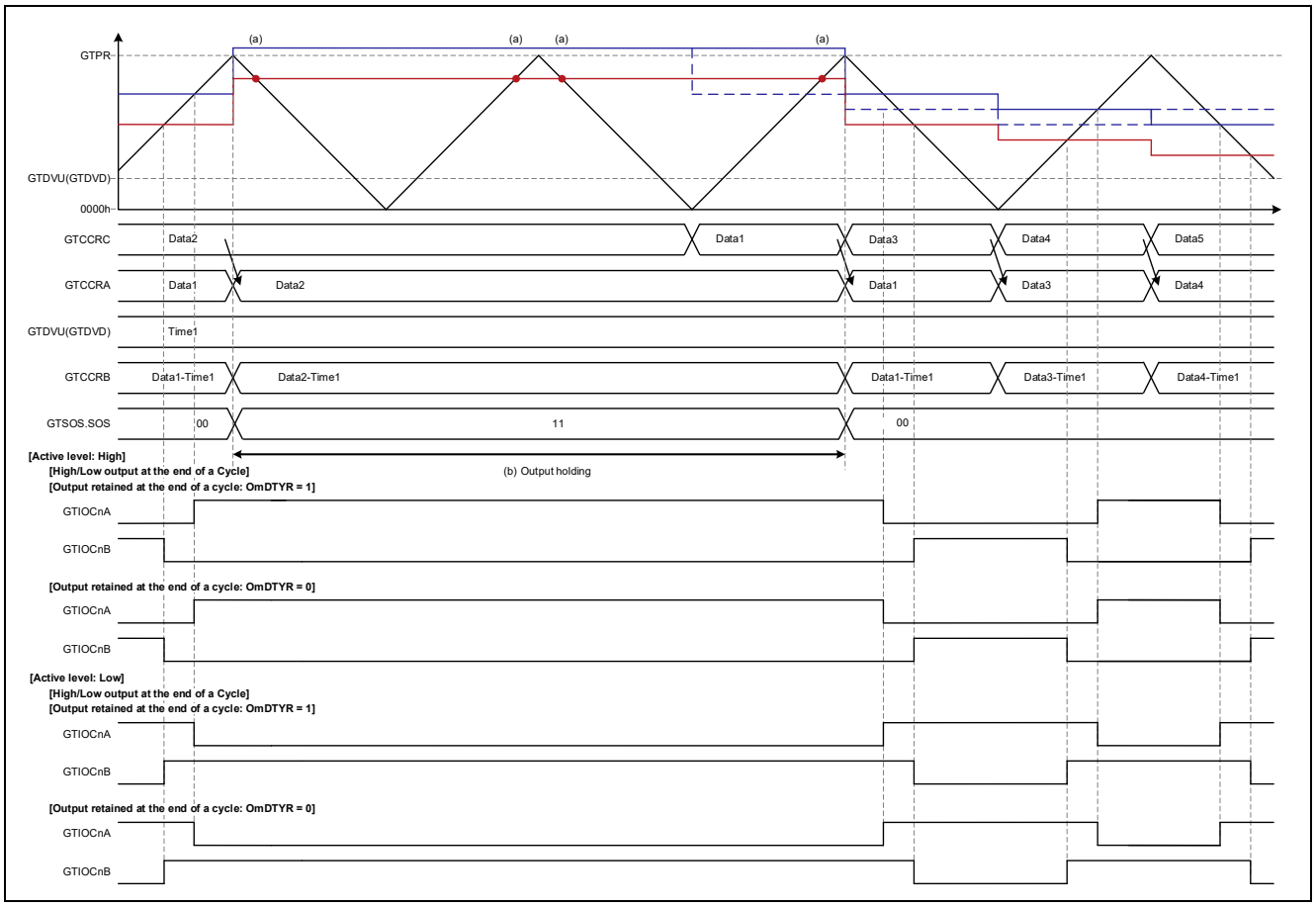


Figure 1.104 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Crest, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 6] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.105 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 3.

(a) Output maintained by output protection function.
(b) Output maintained by output protection function.

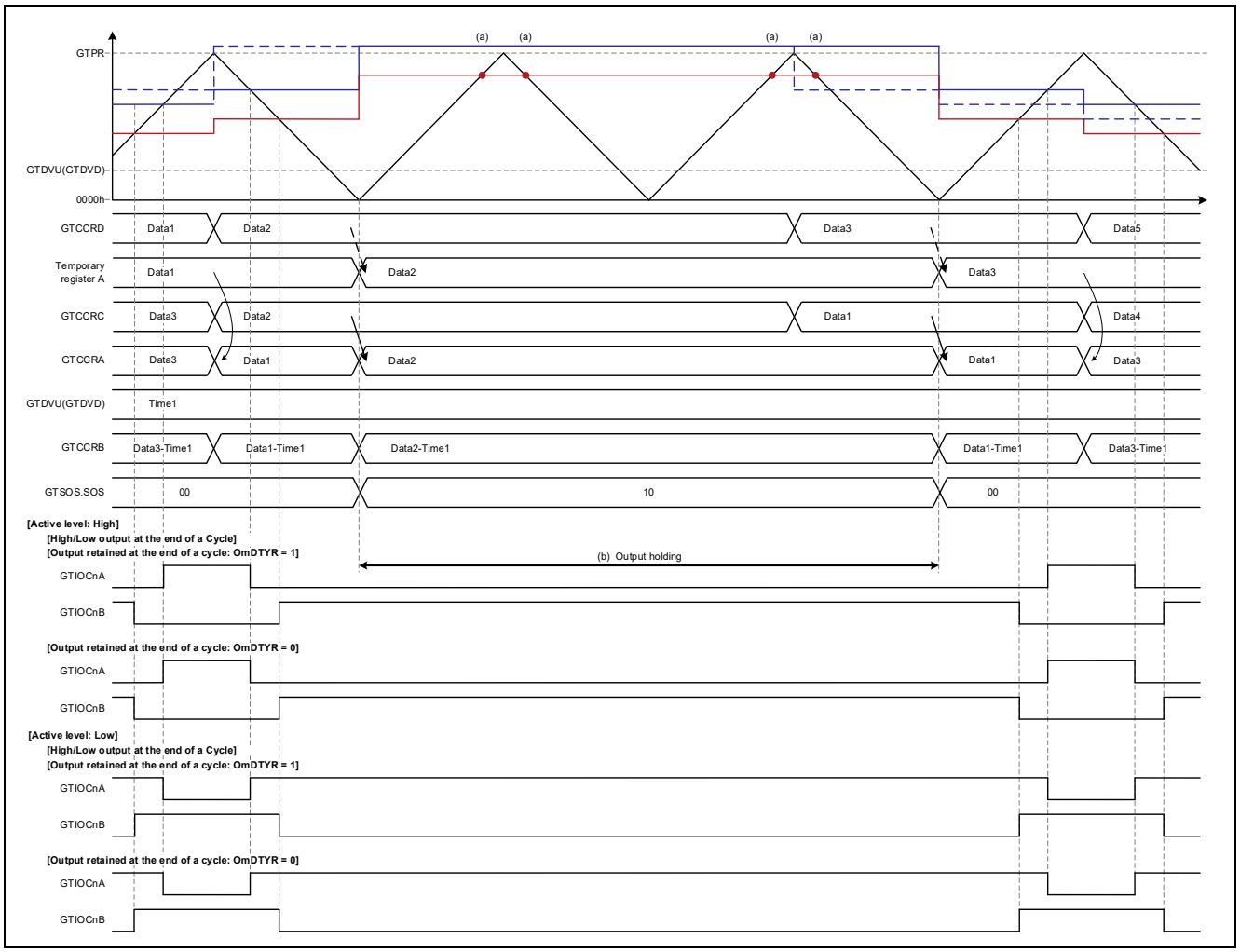


Figure 1.105 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 7] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Crest)

Figure 1.106 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 3.

(a) Output maintained by output protection function.
(b) Compare match occurs, but output maintained due to return interval.
(c) Output maintained by output protection function.

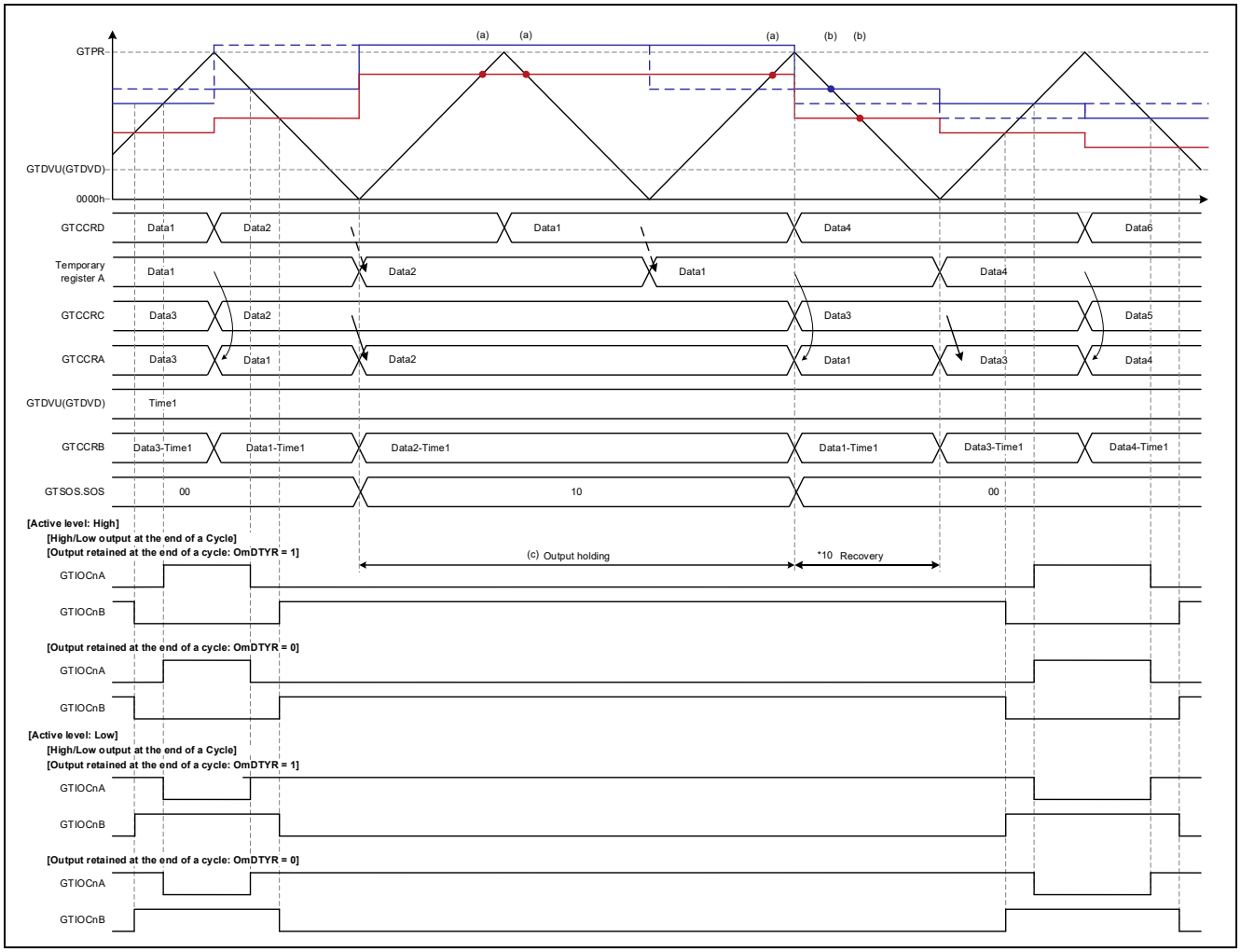


Figure 1.106 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Crest)

[Operation Example 8] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Trough)

Figure 1.107 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at crest and return via buffer transfer at trough of a normal value in triangle-wave PWM mode 3.

(a) Output maintained by output protection function.
(b) Compare match occurs, but output maintained due to return interval.
(c) Output maintained by output protection function.

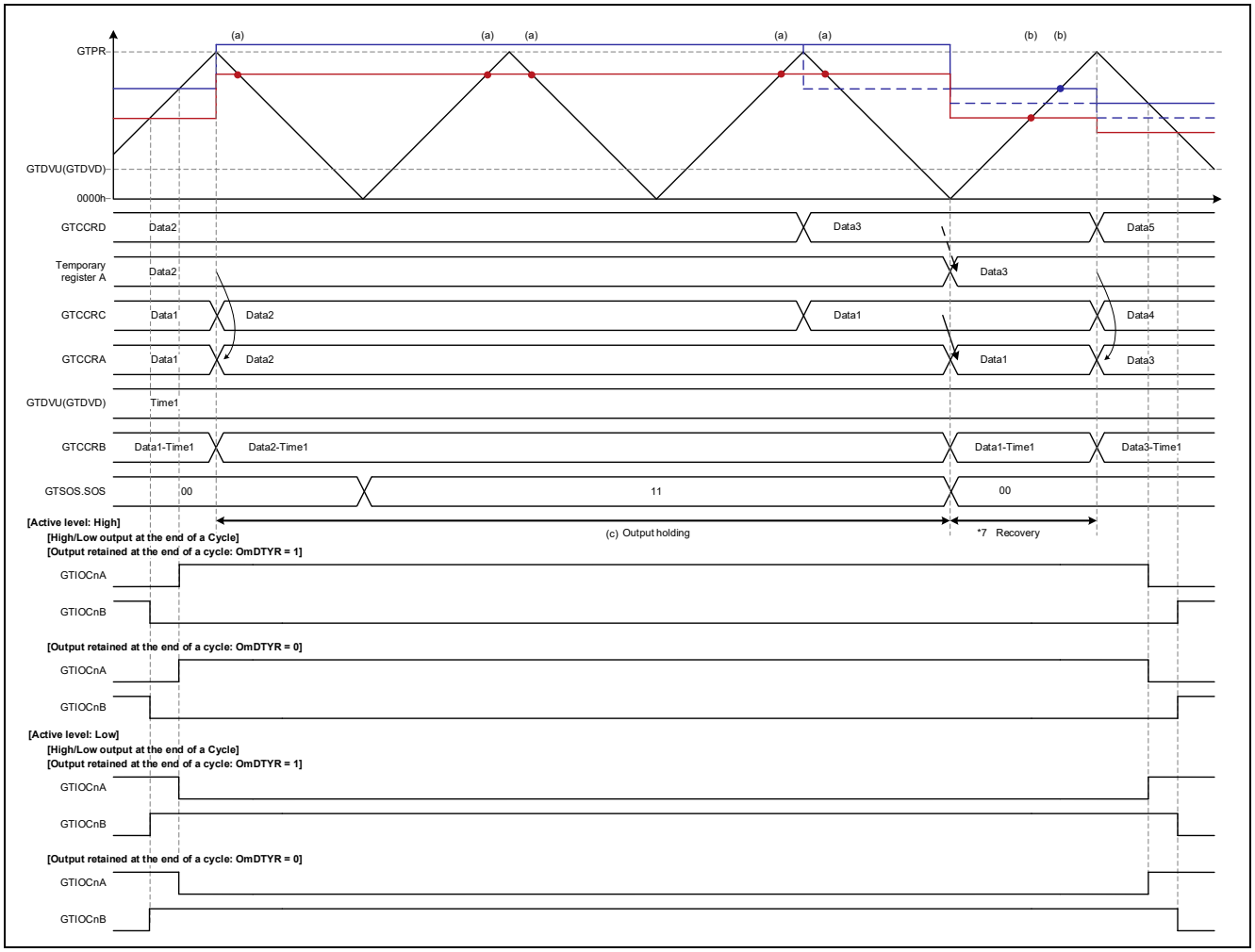


Figure 1.107 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Crest, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 9] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Crest)/Normal Value (Transfer at Crest)

Figure 1.108 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at crest and return via buffer transfer at crest of a normal value in triangle-wave PWM mode 3.

(a) Output maintained by output protection function.
(b) Output maintained by output protection function.

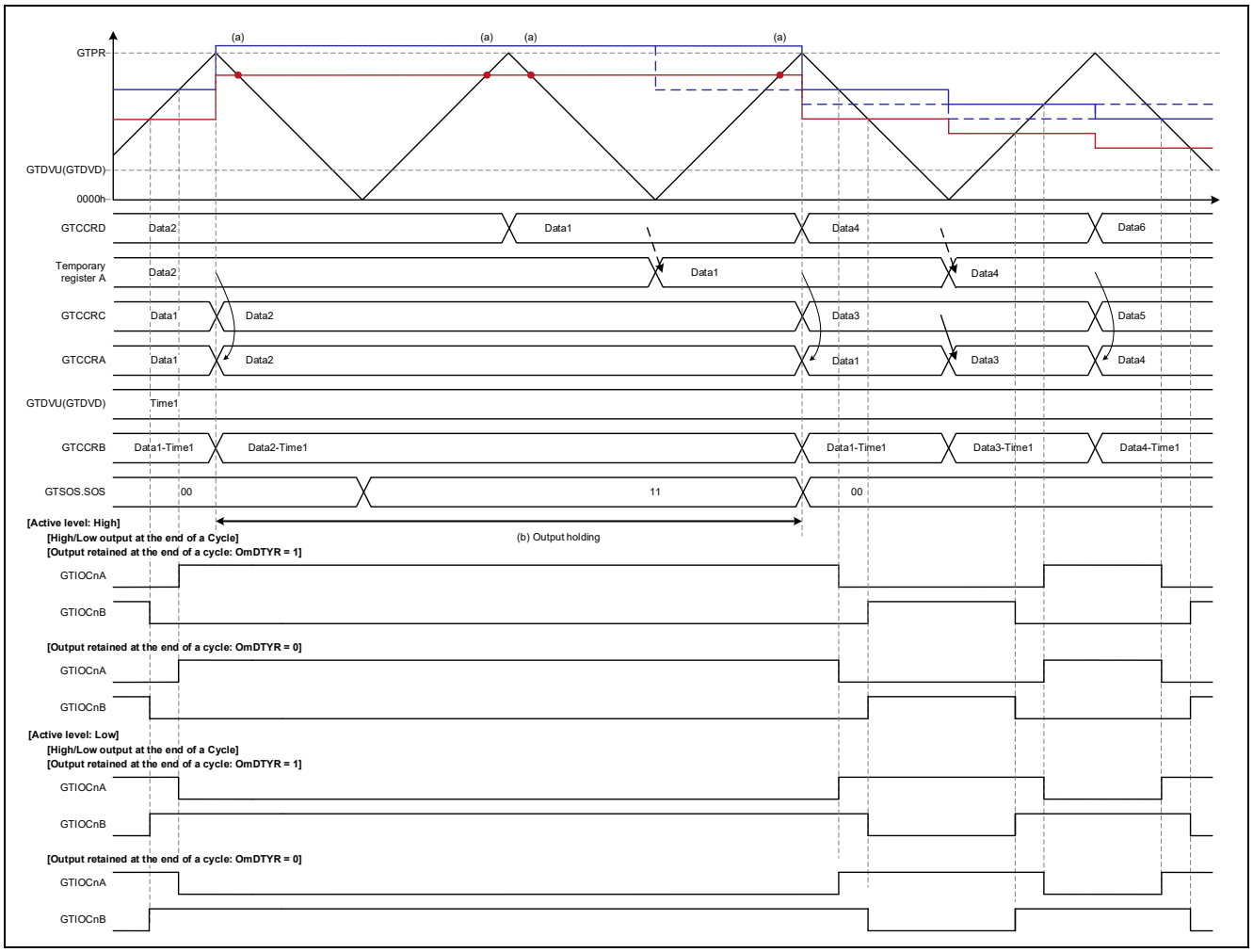


Figure 1.108 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Enabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Crest, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Crest)

1.4.3 Cautions when Automatic Dead Time Setting Is Disabled

The protection function does not operate when the automatic dead time setting is disabled. Operation is as follows when the GTCCRA or GTCCRB register is set to an abnormal value (0000 0000h or a value exceeding the GTPR register setting value).

- 0000 0000h: Only compare matches with 0000 0000h occur during the period.
- Same value as GTPR register: Only compare matches with the value of GTPR occur during the period.
- Value exceeding the GTPR register: No compare matches occur.

Figures showing the output waveforms resulting from these conditions are listed below.

Table 1.14 Figures Showing Output Waveforms

	Abnormal Value		
Operating Mode	**0000 0000h**	**Same Value as GTPR Register**	**Value Exceeding the GTPR Register**
Triangle-Wave PWM mode 1	Figure 1.109	Figure 1.112	Figure 1.115
Triangle-Wave PWM mode 2	Figure 1.110	Figure 1.113	Figure 1.116
Triangle-Wave PWM mode 3	Figure 1.111	Figure 1.114	Figure 1.117

1.4.3.1 Operation Examples with Abnormal Value (0000 0000h) Setting

Operation examples when an abnormal value (0000 0000h) setting is used as listed in Table 1.14, Figures Showing Output Waveforms, are shown in Figure 1.109 to Figure 1.111 and applicable cautions are described below.

- Operation Example 1: Figure 1.109 Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 11
- Operation Example 2: Figure 1.110 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 11
- Operation Example 3: Figure 1.111 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 11

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → 0000 0000h → D
  - D > GTDVU
- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: 0000 0000h
- Cautions
  11. Toggling of positive and negative phases occurs at end of period.

[Operation Example 1] Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.109 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 1.

(a) No change to positive or negative phase because no compare match occurs.
(b) Toggling of positive and negative phases occurs due to compare match with GTCCRB.

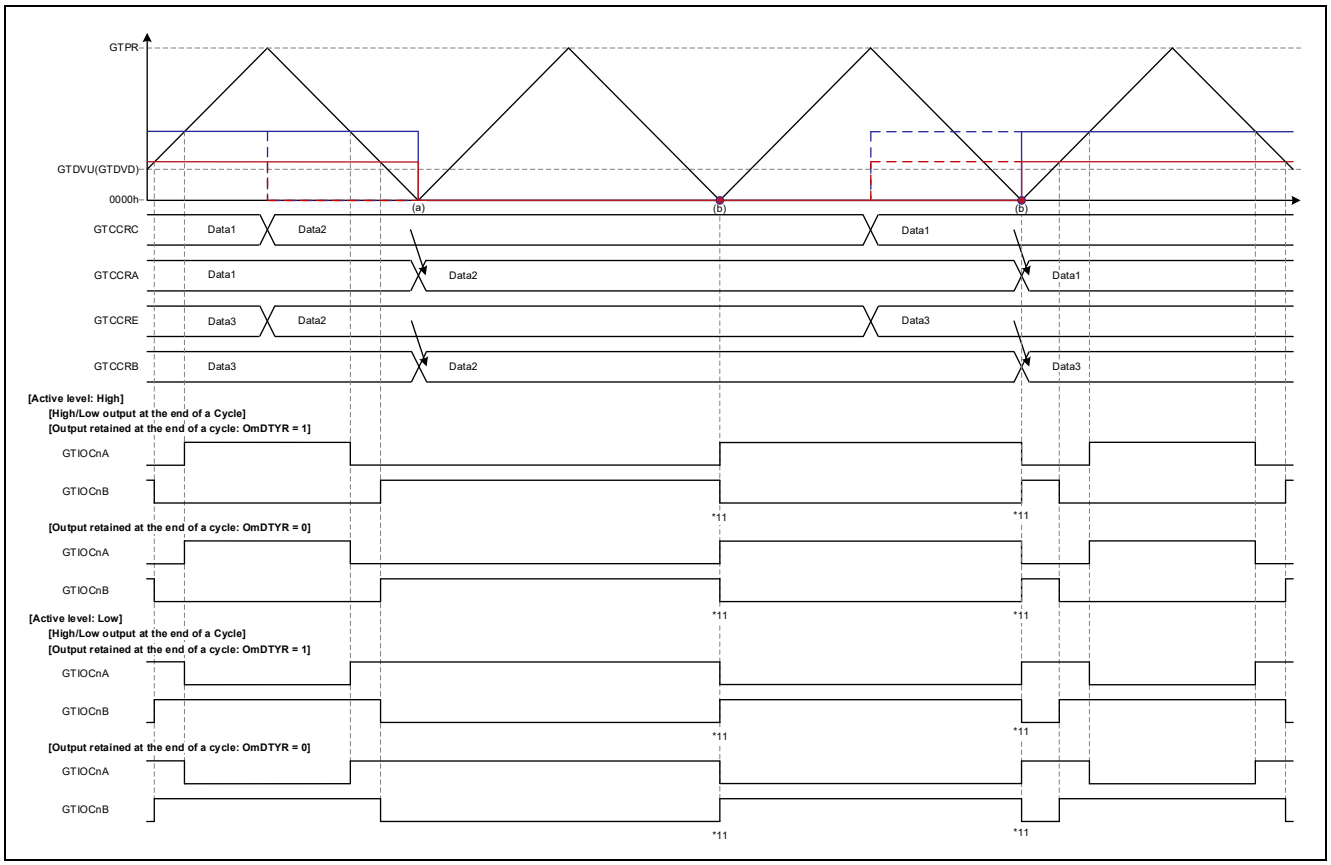


Figure 1.109 Triangle-Wave PWM Mode 1 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 2] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.110 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 2. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.109.

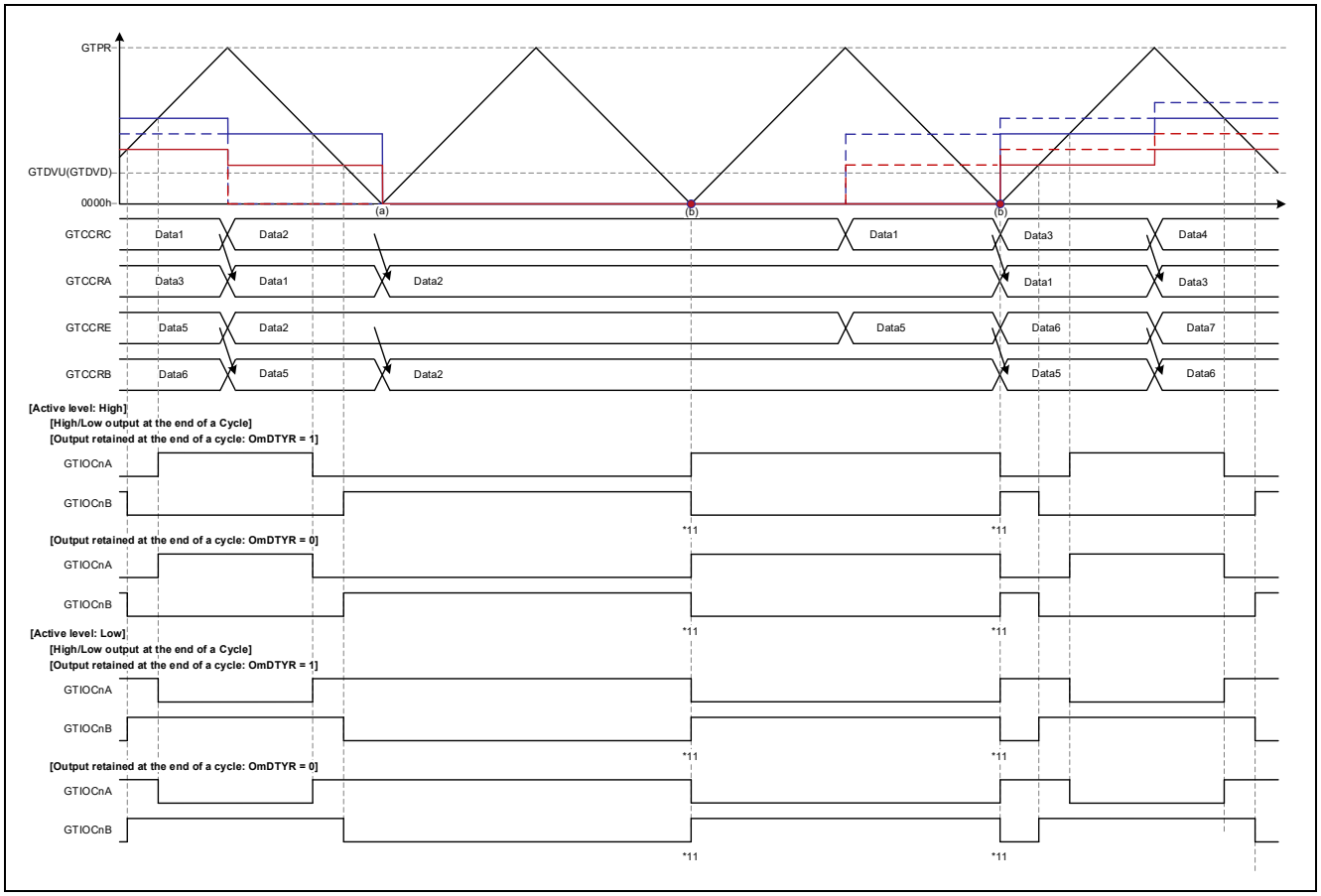


Figure 1.110 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 3] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.111 shows an operation example of transfer of 0000 0000h to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.109.

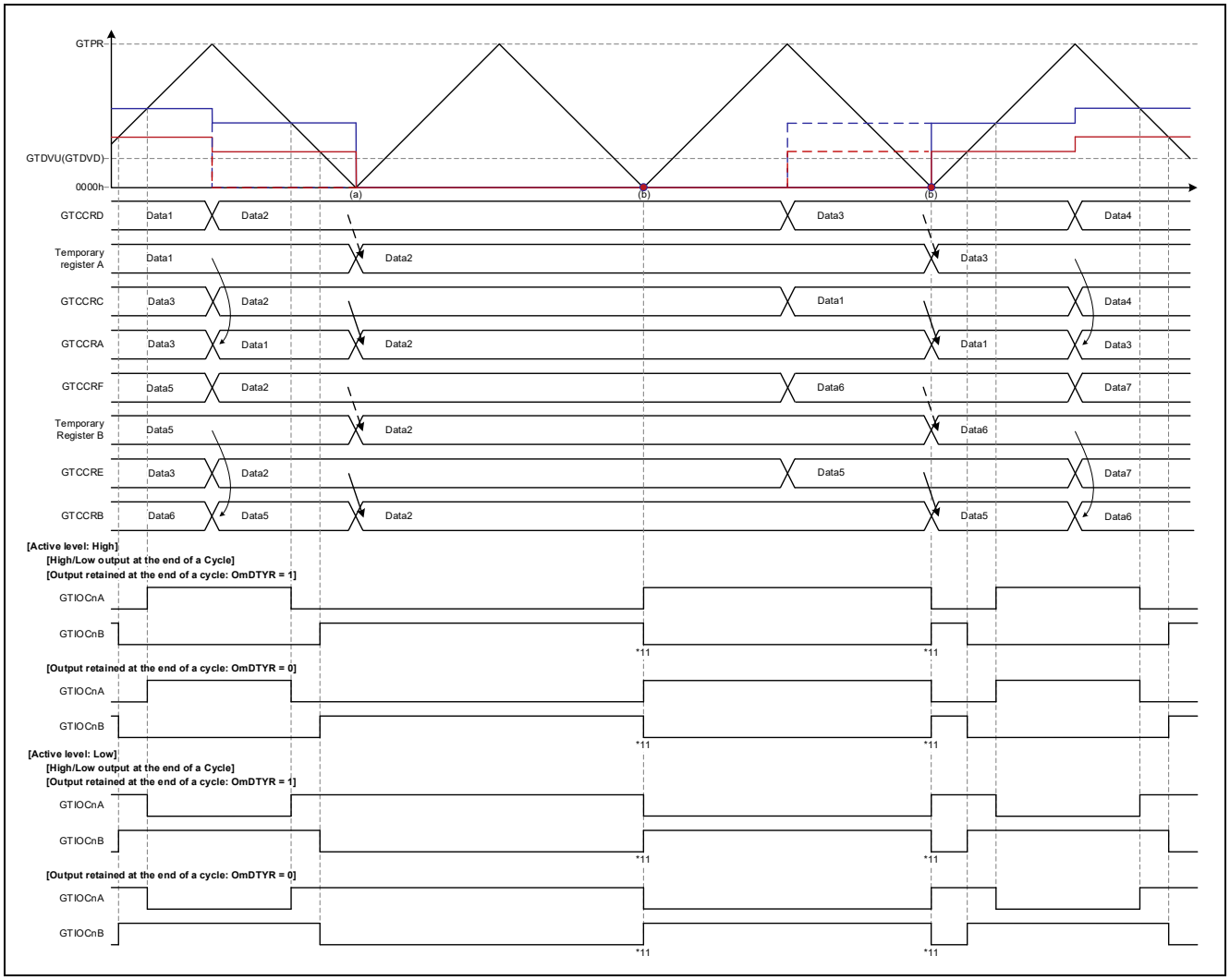


Figure 1.111 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → 0000 0000h (Abnormal Value): Transfer at Trough, 0000 0000h (Abnormal Value) → D (Normal Value): Transfer at Trough)

1.4.3.2 Operation Examples with Abnormal Value (Same as GTPR Register Setting Value) Setting

Operation examples when an abnormal value (same as GTPR register setting value) setting is used as listed in Table 1.14, Figures Showing Output Waveforms, are shown in Figure 1.112 to Figure 1.114 and applicable cautions are described below.

- Operation Example 1: Figure 1.112 Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 12 and 13
- Operation Example 2: Figure 1.113 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 12 and 13
- Operation Example 3: Figure 1.114 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), cautions 12 and 13

- **Key to Figures of Operating Conditions of Operation Examples and Cautions**
  - Duty: D → G → D
  - D > GTDVU
  - G: GTPR

- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: G

- Cautions
  12. The negative phase becomes more minute pulses the closer the value of GTCCRB is to GTPR, relative to G. (The output does not change if the value of GTCCRB is greater than GTPR.)
  13. Toggling of positive and negative phases occurs at the crest timing.

[Operation Example 1] Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.112 shows an operation example of transfer of a value equal to GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 1.

(a) Toggling of positive and negative phases occurs at compare match with GTCCRA.
(b) Negative phase turns off at compare match with GTCCRB.
(c) Negative phase turns on at compare match with GTCCRB.

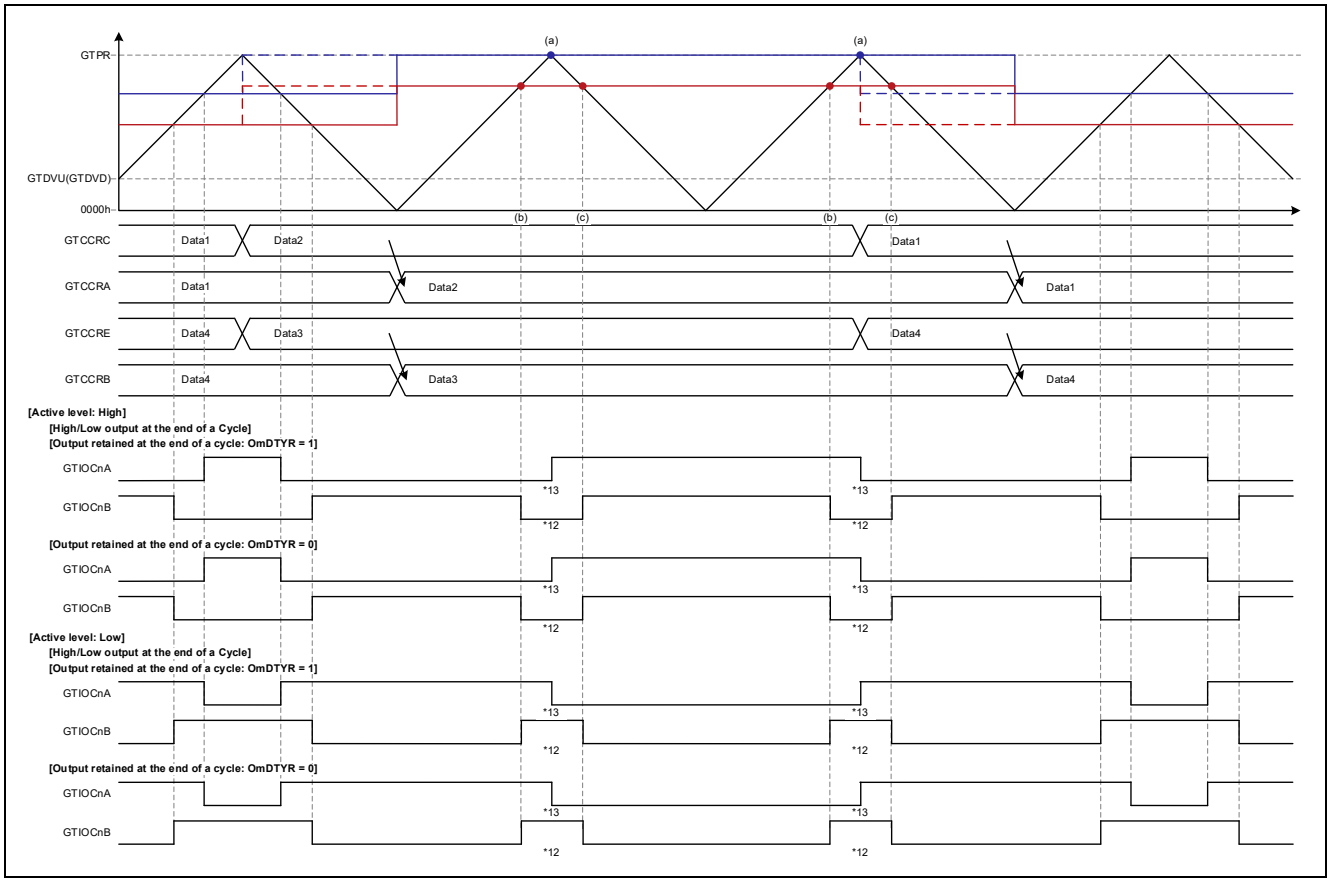


Figure 1.112 Triangle-Wave PWM Mode 1 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → GTPR (Abnormal Value): Transfer at Trough, GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 2] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.113 shows an operation example of transfer of a value equal to GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 2. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.112.

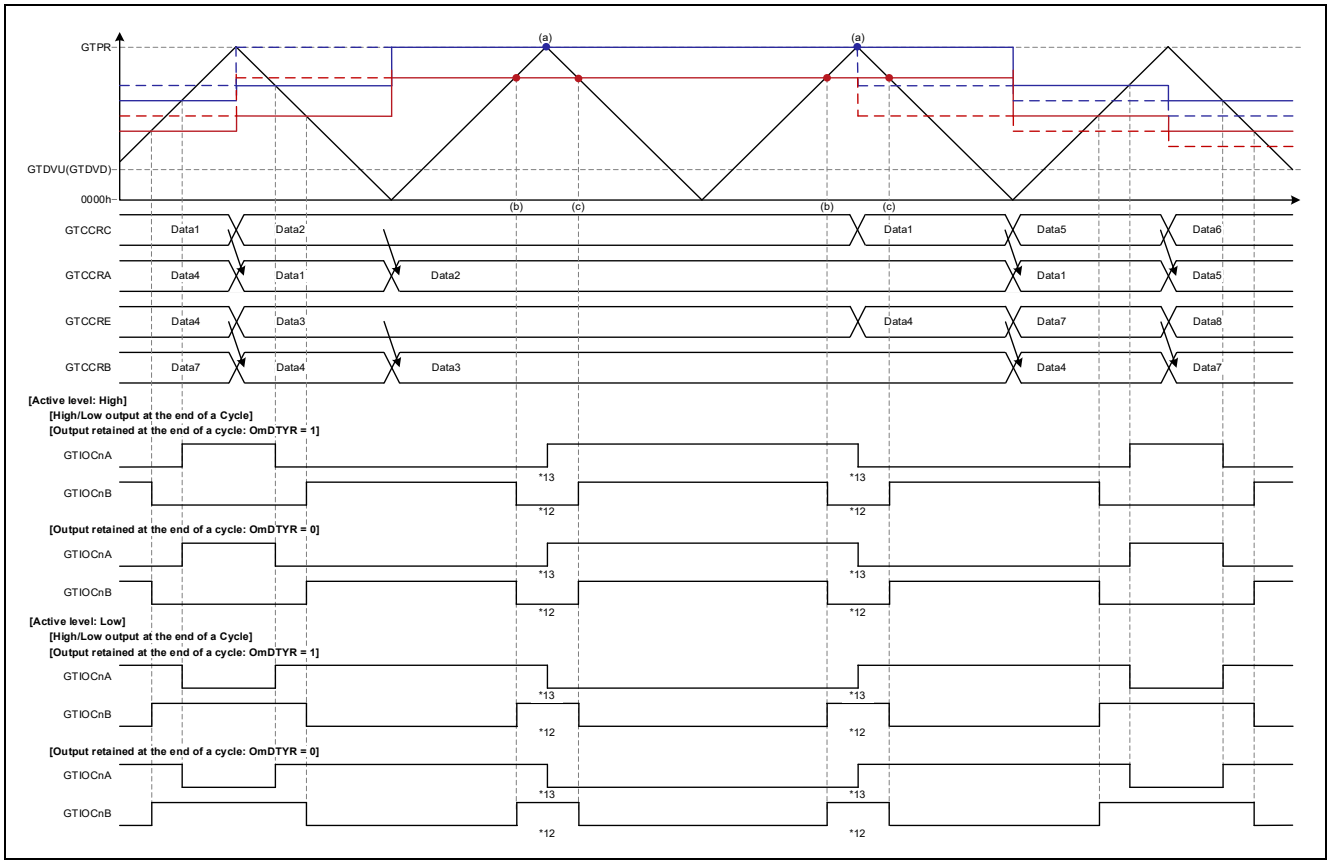


Figure 1.113 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → GTPR (Abnormal Value): Transfer at Trough, GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 3] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.114 shows an operation example of transfer of a value equal to GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.112.

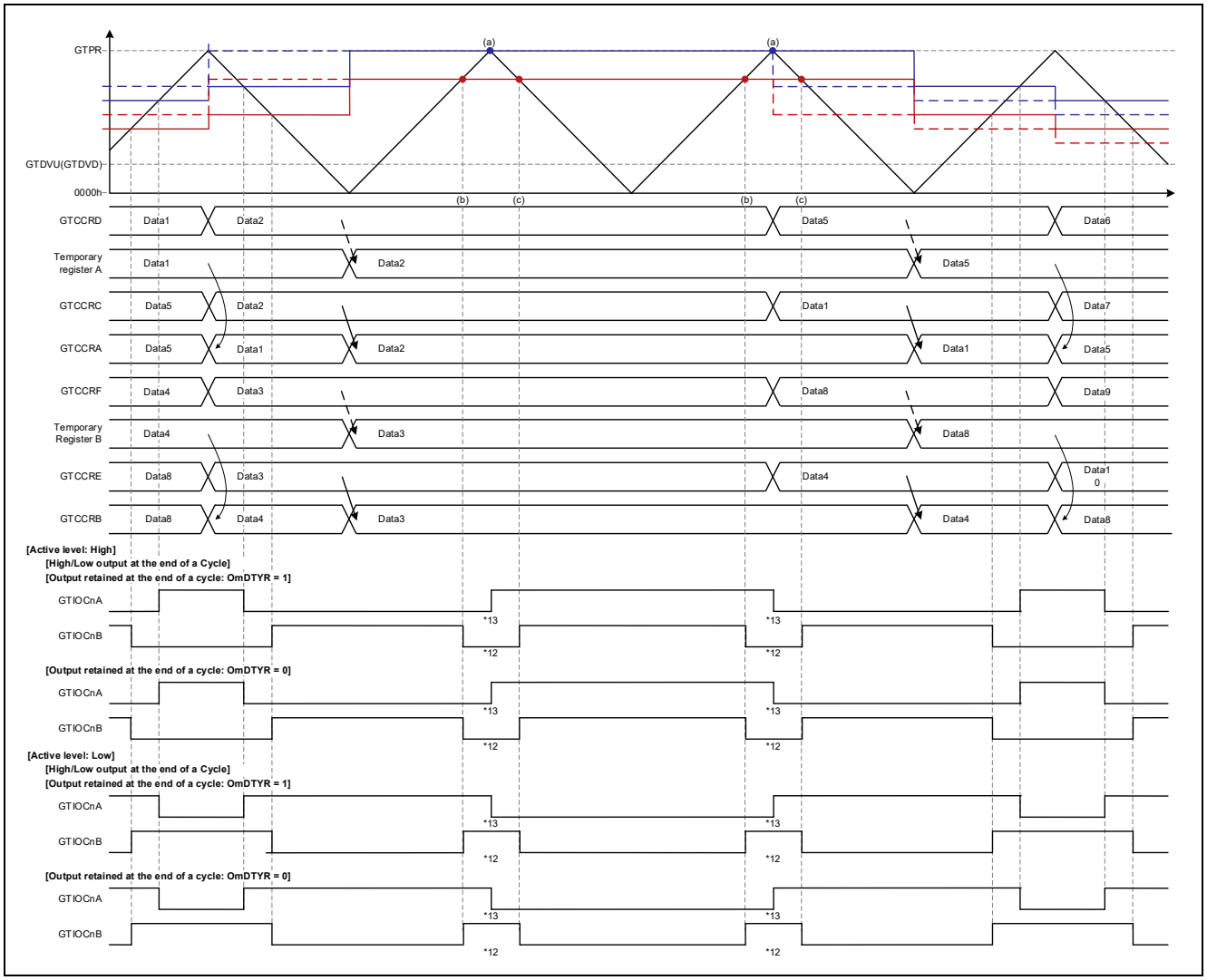


Figure 1.114 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → GTPR (Abnormal Value): Transfer at Trough, GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

1.4.3.3 Operation Examples with Abnormal Value (Value Exceeding GTPR Register Setting Value) Setting

Operation examples when an abnormal value (value exceeding GTPR register setting value) setting is used as listed in Table 1.14, Figures Showing Output Waveforms, are shown in Figure 1.115 to Figure 1.117 and applicable cautions are described below.

- Operation Example 1: Figure 1.115 Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 12
- Operation Example 2: Figure 1.116 Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 12
- Operation Example 3: Figure 1.117 Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough), caution 12

Key to Figures of Operating Conditions of Operation Examples and Cautions

- Duty: D → G → D
  - D > GTDVU
  - G > GTPR
- Key to figures
  - Dashed blue line: Setting timing and value changes of positive phase buffer register (GTCCRC)
  - Solid blue line: Setting timing and value changes of positive phase compare register (GTCCRA)
  - Dashed red line: Setting timing and value changes of negative phase buffer register (GTCCRE)
  - Solid red line: Setting timing and value changes of negative phase compare register (GTCCRB)
    Negative phase waveform change points when dead time errors occur while using the automatic dead time setting function
  - Data 1: D
  - Data 2: G
- Cautions
  12. The negative phase becomes more minute pulses the closer the value of GTCCRB is to GTPR, relative to G. (The output does not change if the value of GTCCRB is greater than GTPR.)

[Operation Example 1] Triangle-Wave PWM Mode 1, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.115 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 1.

(a) Output does not change because value of GTCCRA exceeds GTPR.
(b) GTCCRA has no effect, and negative phase turns off at compare match with GTCCRB.
(c) GTCCRA has no effect, and negative phase turns on at compare match with GTCCRB.

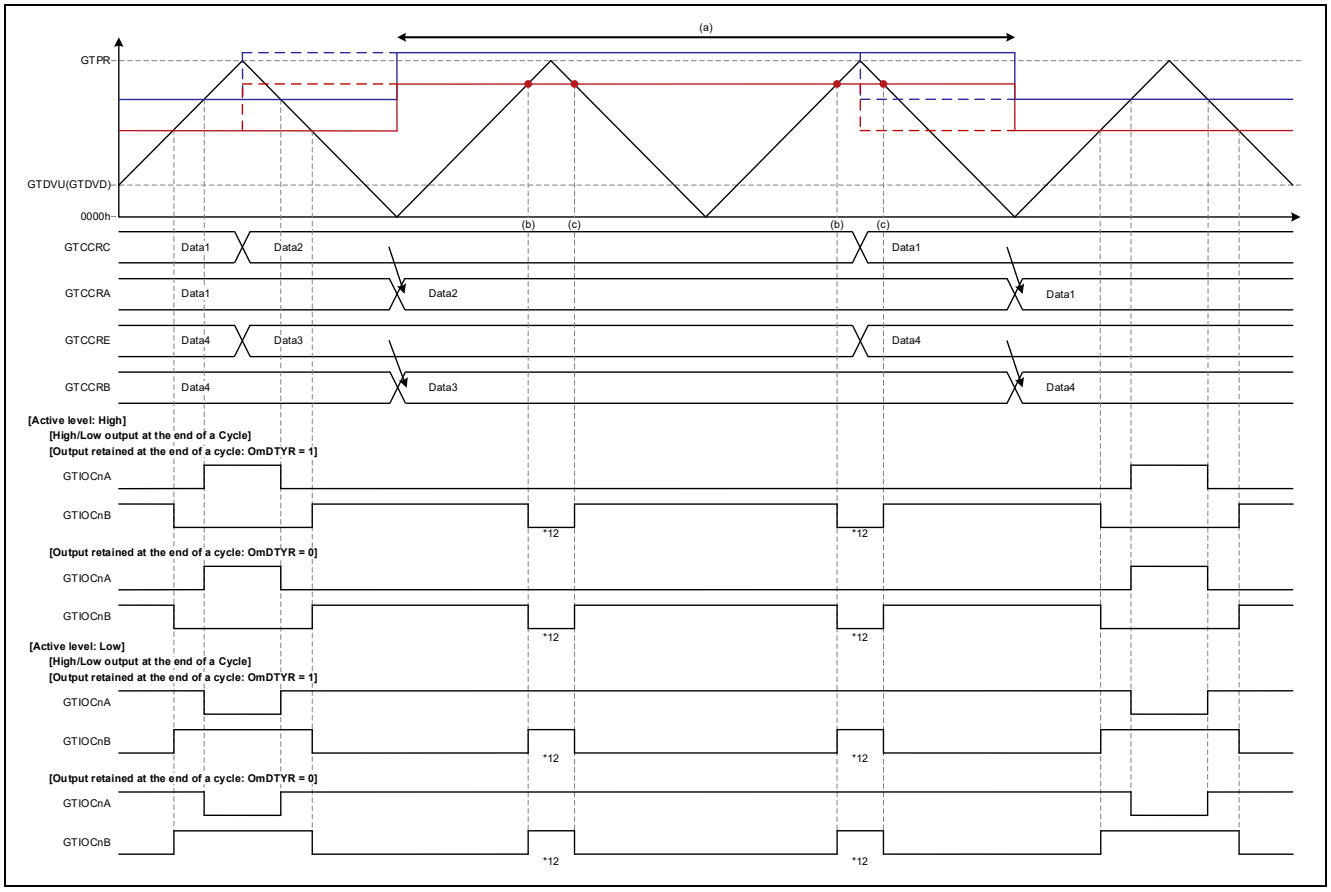


Figure 1.115 Triangle-Wave PWM Mode 1 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 2] Triangle-Wave PWM Mode 2, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.116 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 2. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.115.

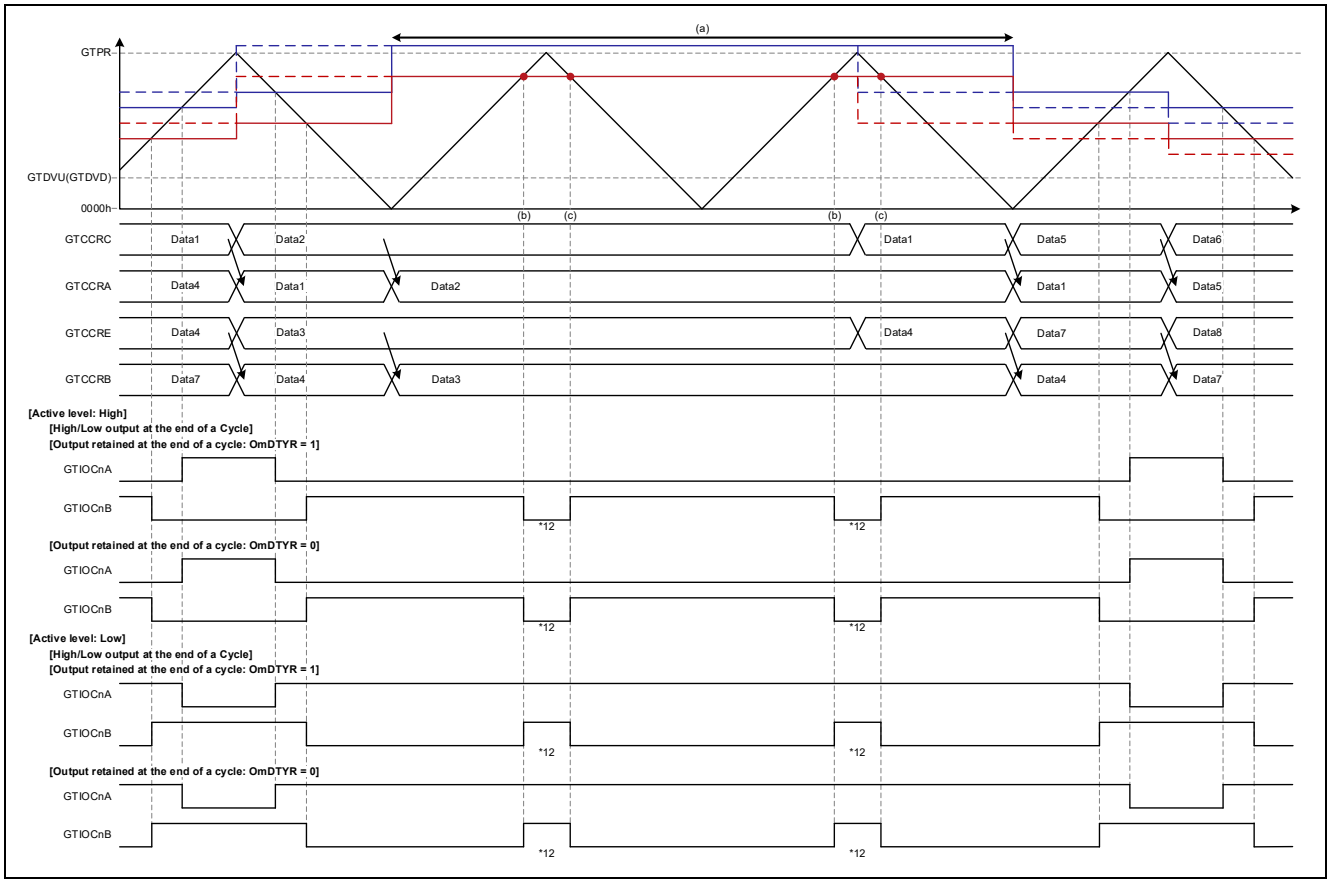


Figure 1.116 Triangle-Wave PWM Mode 2 Operation Example (Transfer at Crest and Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

[Operation Example 3] Triangle-Wave PWM Mode 3, Abnormal Value (Transfer at Trough)/Normal Value (Transfer at Trough)

Figure 1.117 shows an operation example of transfer of a value exceeding GTPR to GTCCRA via buffer transfer at trough in triangle-wave PWM mode 3. Except for the difference in the buffer overwrite timing and transfer timing, the operation is the same as that shown in Figure 1.115.

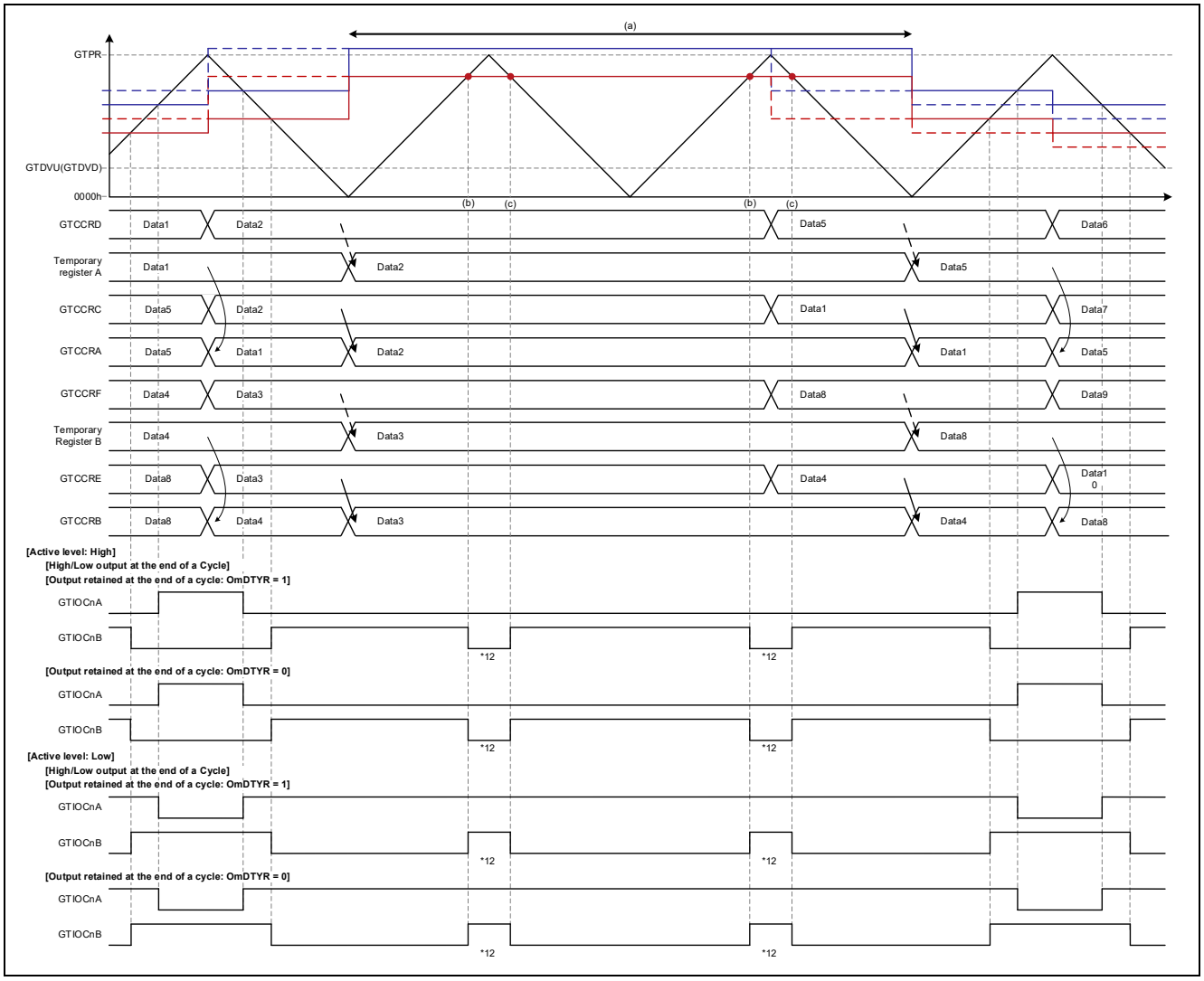


Figure 1.117 Triangle-Wave PWM Mode 3 Operation Example (Transfer at Trough, Automatic Dead Time Setting Function Disabled, D (Normal Value) → Value Exceeding GTPR (Abnormal Value): Transfer at Trough, Value Exceeding GTPR (Abnormal Value) → D (Normal Value): Transfer at Trough)

1.5 Dead Time Due to GPTW 0%/100% Duty Cycle Switching Register

Changing the values of the OADTY[1:0] and OBDTY[1:0] bits in GTUDDTYC causes the GPTW to produce 0% and 100% duty cycle output. The values of the OADTY[1:0] and OBDTY[1:0] bits in GTUDDTYC are applied when an underflow (trough) occurs, causing both the positive and negative phases to change simultaneously. For this reason, there is no dead time when the GPTW is producing 0% and 100% duty cycle output.

Figure 1.118 shows an operation example of 0% and 100% duty cycle output with the GPTW's automatic dead time setting disabled, and Figure 1.119 shows an operation example of the MTU producing 0% and 100% duty cycle output. The yellow shaded areas in the figures represent dead time.

When the GPTW transitions to 100% duty cycle output (Figure 1.118 (a)) and at return (Figure 1.118 (b)), dead time cannot be guaranteed because the positive and negative phases change simultaneously. When the MTU transitions to 100% output (Figure 1.119 (c)) and at return (Figure 1.119 (d)), the negative phase change is ignored and output is fixed low, guaranteeing the dead time.

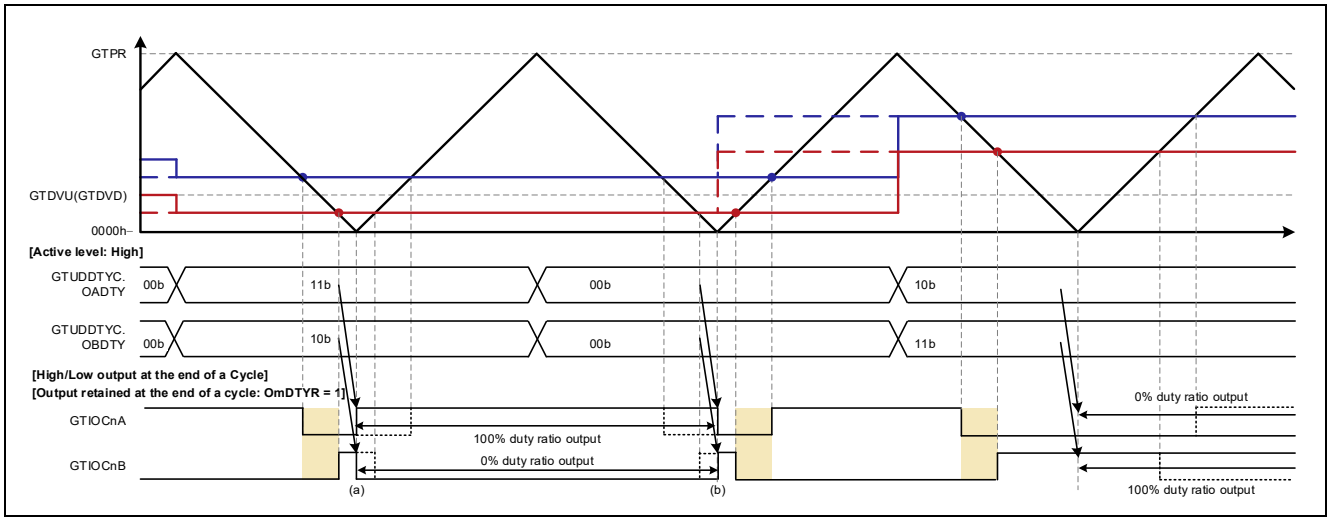


Figure 1.118 GPTW Operation Example

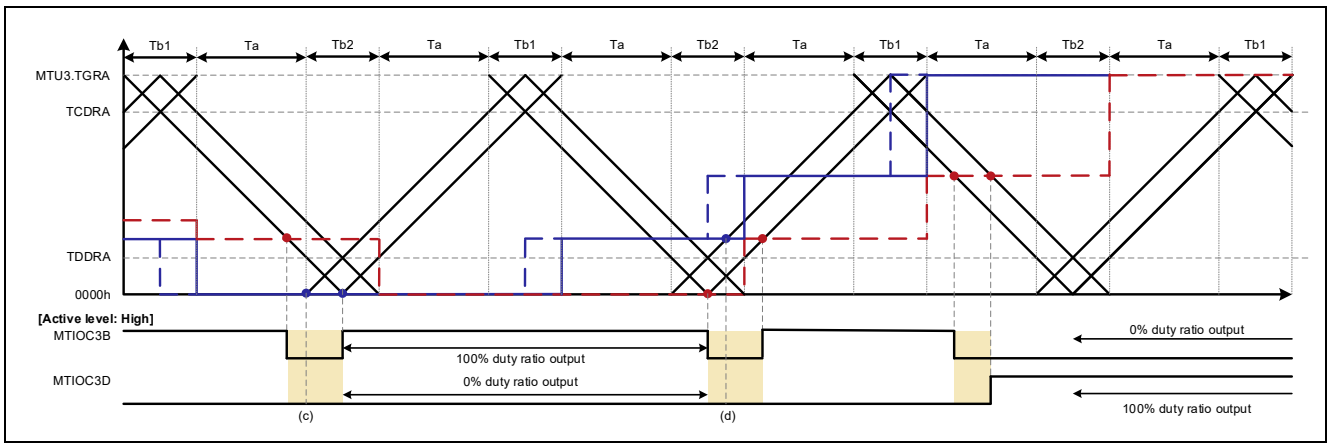


Figure 1.119 MTU Operation Example

2. Operation Confirmation Conditions

The operation of the sample code accompanying this application note has been confirmed under the following operating conditions.

Table 2.1 Operation Confirmation Environment

Item	Description
MCU used	R5F566TEADFP (included in Renesas Starter Kit for RX66T)
Operating frequency	Main clock: 8 MHz PLL: 160 MHz (Main clock × 1/1 × 20) HOCO: stopped LOCO: stopped System clock (ICLK): 160 MHz (PLL × 1/1) Peripheral module clock A (PCLKA): 80 MHz (PLL × 1/2) Peripheral module clock B (PCLKB): 40 MHz (PLL × 1/4) Peripheral module clock C (PCLKC): 160 MHz (PLL × 1/1) Peripheral module clock D (PCLKD): 40 MHz (PLL × 1/4) FlashIF clock (FCLK): 40 MHz (PLL × 1/4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics e² studio Version 2022-07
C compiler*1	Renesas Electronics C/C++ Compiler Package for RX Family V3.04.00
	Compiler option Default settings of integrated development environment
RX Smart Configurator	V2.14.0
Board support package (r_bsp)	V7.20
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	V1.00
Board used	Renesas Starter Kit for RX66T (product No.: RTK50566T0CxxxxxBE)
Emulator	E2-Lite

Note: 1. Import the same version of the toolchain (C compiler) as specified in the original project. If the same toolchain is not located in the import destination, the toolchain cannot be selected, and an error will occur. Check the toolchain selection status on the project settings screen.
Refer to FAQ 3000404 for setting methods.
FAQ 3000404: “Program ‘make’ not found in PATH” error when attempting to build an imported project (e² studio)

3. MCU Sample Code

3.1 Common

3.1.1 Sample Code List

This application note provides the following sample code created with Smart Configurator. Sample code can be downloaded from the Renesas Electronics website.

Table 3.1 MTU Sample Code List

Name	Sample Code Usage Conditions	Reference
Operation near 0% and 100% duty cycles r01an6539_rx66t_mtu3.zip	• Complementary PWM mode 3 (transfer at crest and trough) • Single buffer	3.2

3.1.2 Folder Structure

The main folder structure of the sample code is as follows.

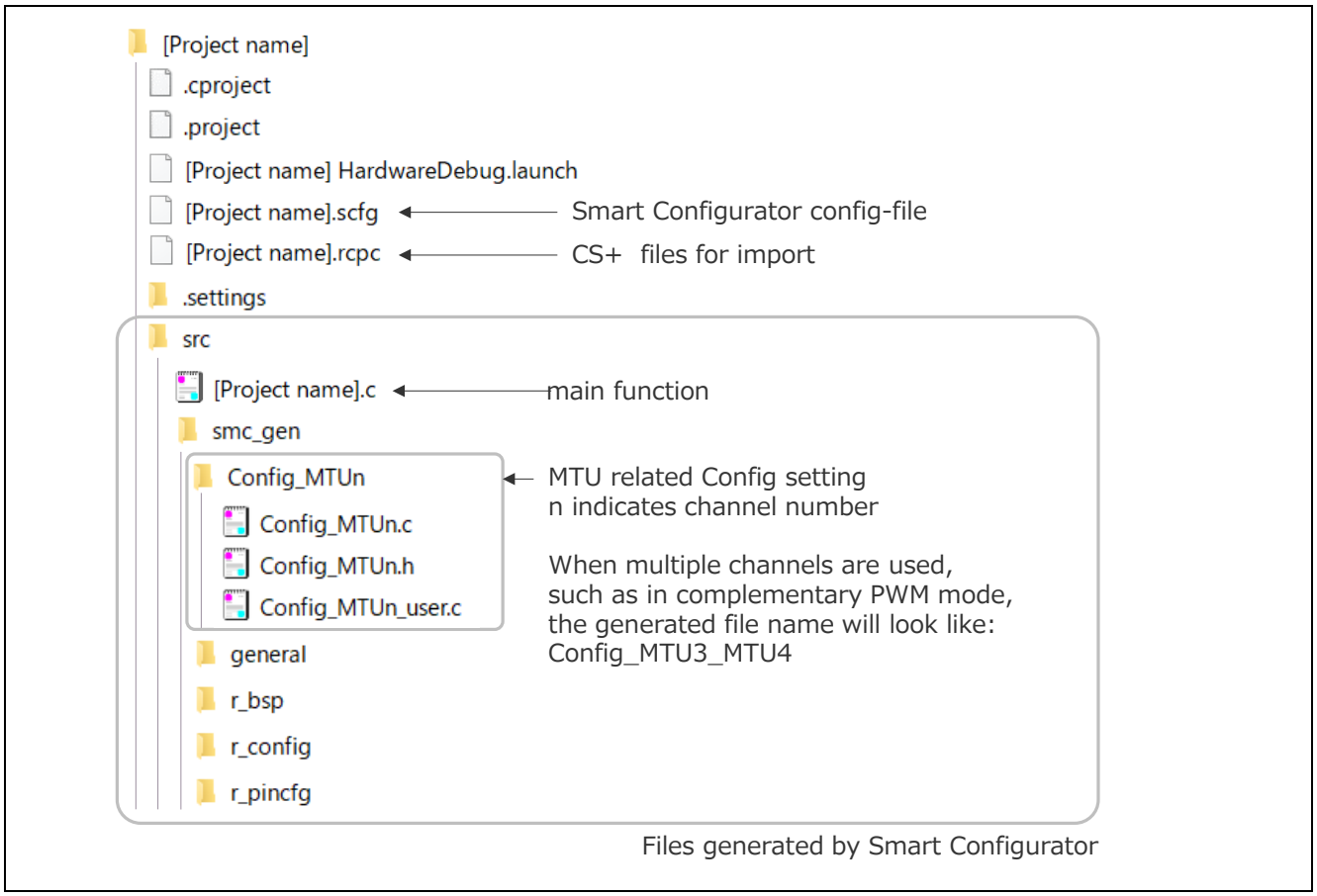


Figure 3.1 MTU Folder Structure

3.1.3 File Structure

The main file structure of the sample code is as follows.

Table 3.2 MTU File Structure

File Name	Description
[project name].c	Main function This is the main function. Smart Configurator generates an empty function. The necessary processing for each code sample is described here.
Config_MTUn.c*1	R_Config_MTUn_Create function This is the MTU's initialization function. Smart Configurator generates this initialization function based on the Smart Configurator settings. Calls by this function are generated by Smart Configurator. This function is called by the R_SystemInit function that runs before the main function.
	R_Config_MTUn_Start function This is the MTU's count stop function. This function is generated by Smart Configurator. This function is called by the main function in the sample code.
	R_Config_MTUn_Stop function This is the MTU's count stop function. This function is generated by Smart Configurator. This function is not used in the sample code.
Config_MTUn_user.c*1	r_Config_MTUn_Create_UserInit function This is a user function used to initialize the MTU. Smart Configurator generates an empty function. The necessary processing for each code sample is described here. This is the last function to be called by the R_Config_MTUn_Create function generated by Smart Configurator.
	r_Config_MTUn_[interrupt name]_interrupt function This is an interrupt handler function. Smart Configurator generates an empty function. The necessary processing for each code sample is described here.
Config_MTUn.h*1	This is the header file that defines MTU related functions. This file is included in the r_smc_entry.h file generated by Smart Configurator. To use MTU related functions, be sure to include the r_smc_entry.h file.

Note: 1. n represents the channel number.

3.1.4 Adding Components

Smart Configurator is used to add MTU functionality to the sample code as described below.

Table 3.3 Adding Components

Item	Description
Component	Reference section for each code sample ((1) in figure below)
Configuration name	Default setting name used in sample code
Operation	Reference section for each code sample ((2) in figure below)
Resources	Reference section for each code sample ((3) in figure below)

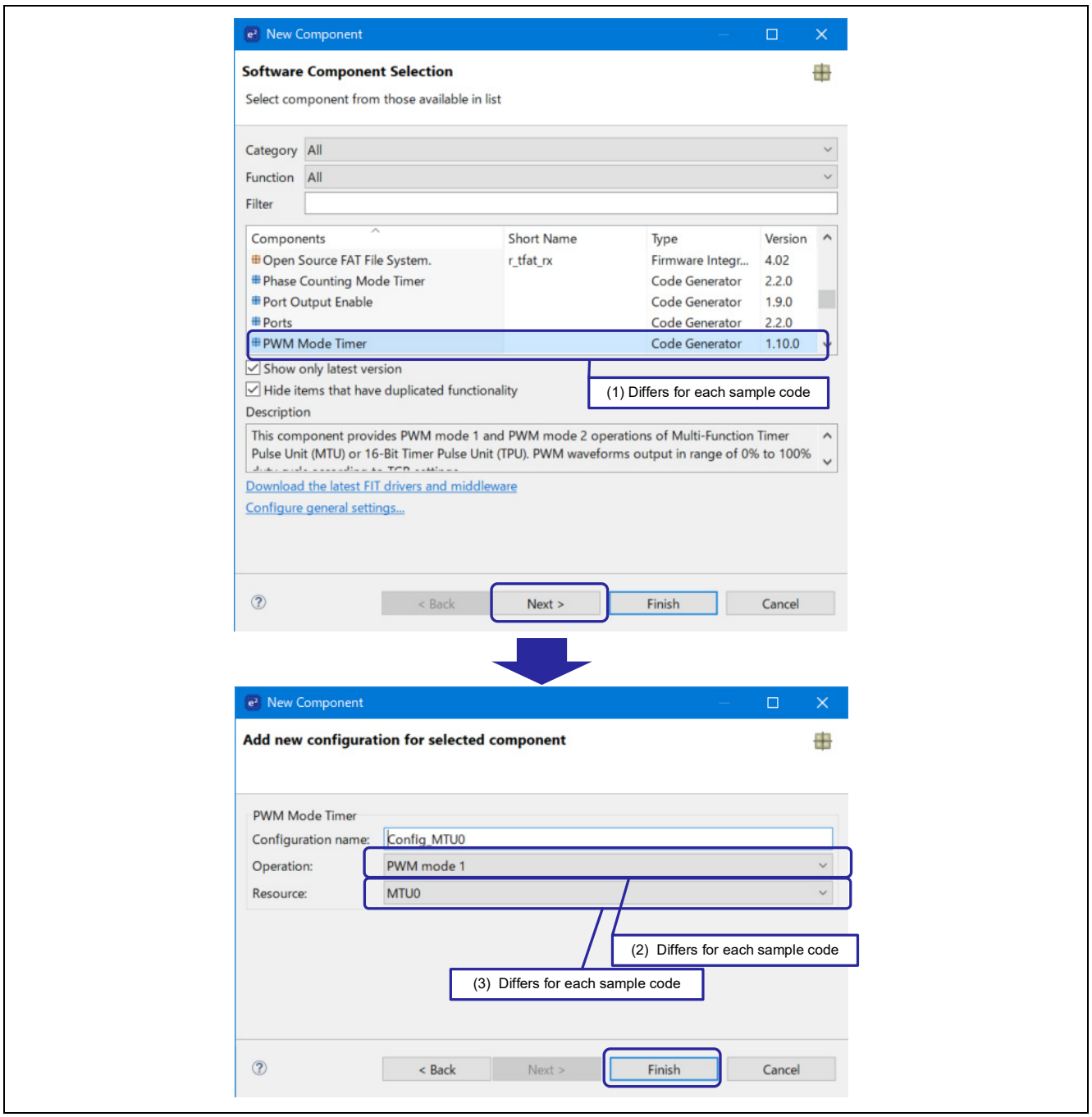


Figure 3.2 Adding Components

3.1.5 Pin Settings

Figure 3.3 shows an example of pin settings in Smart Configurator.

Configure the pins after configuring MTU settings. For MTU settings, refer to the “Smart Configurator Settings” in each code sample.

Pin settings are applied by the R_Config_MTUn_Create function generated by Smart Configurator.

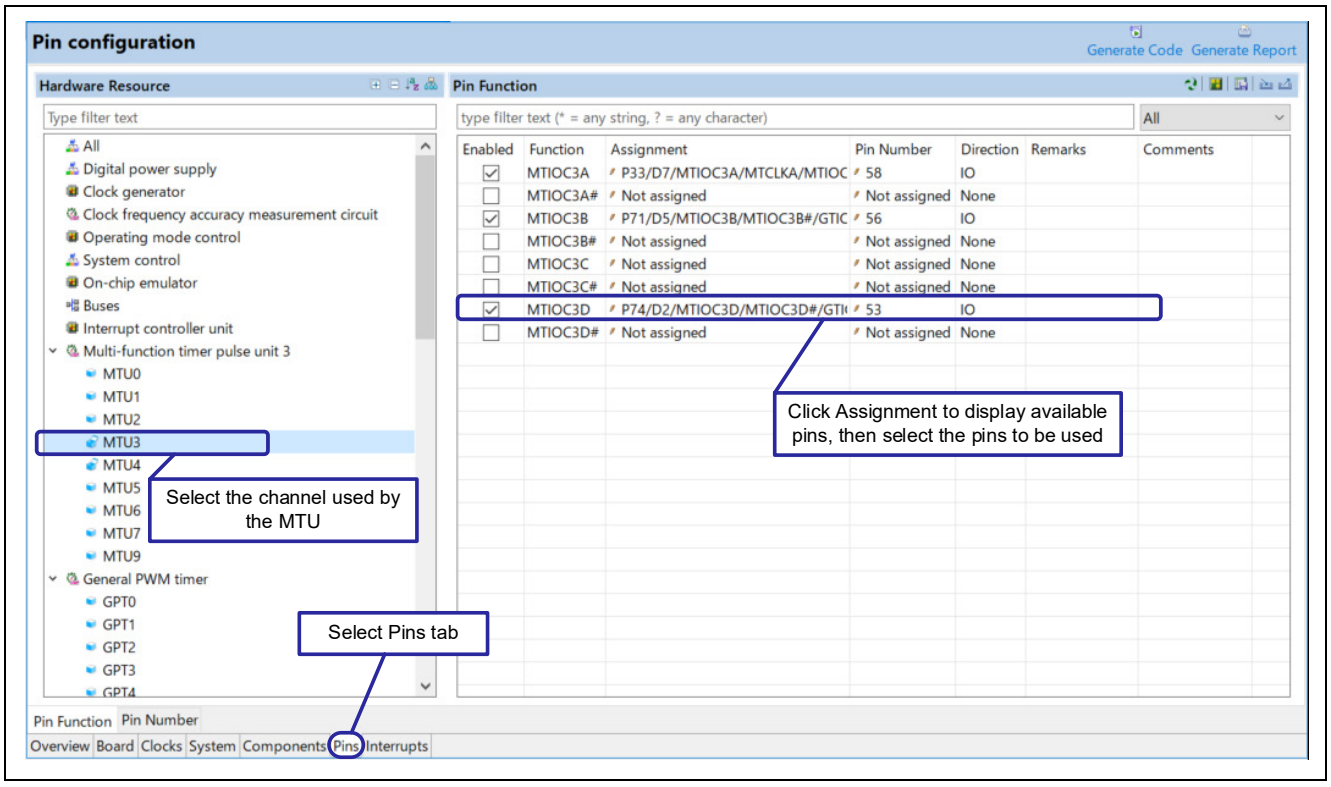


Figure 3.3 Pin Settings

3.1.6 Interrupt Settings

Figure 3.4 shows an example of interrupt settings in Smart Configurator. For details of software configurable interrupt A, refer to 14.4.5.1, Software Configurable Interrupt A, in Renesas RX66T Group User's Manual Hardware.

Configure interrupts after configuring MTU settings. For MTU settings, refer to the "Smart Configurator Settings" in each code sample.

Interrupt settings are applied by the R_Config_MTUn_Create, R_Config_MTUn_Start, and R_Config_MTUn_Stop functions, all of which are generated by Smart Configurator.

The interrupt handler function is created with the name r_Config_MTUn_[interrupt name]_interrupt in the Config_MTUn_user.c file generated by Smart Configurator.

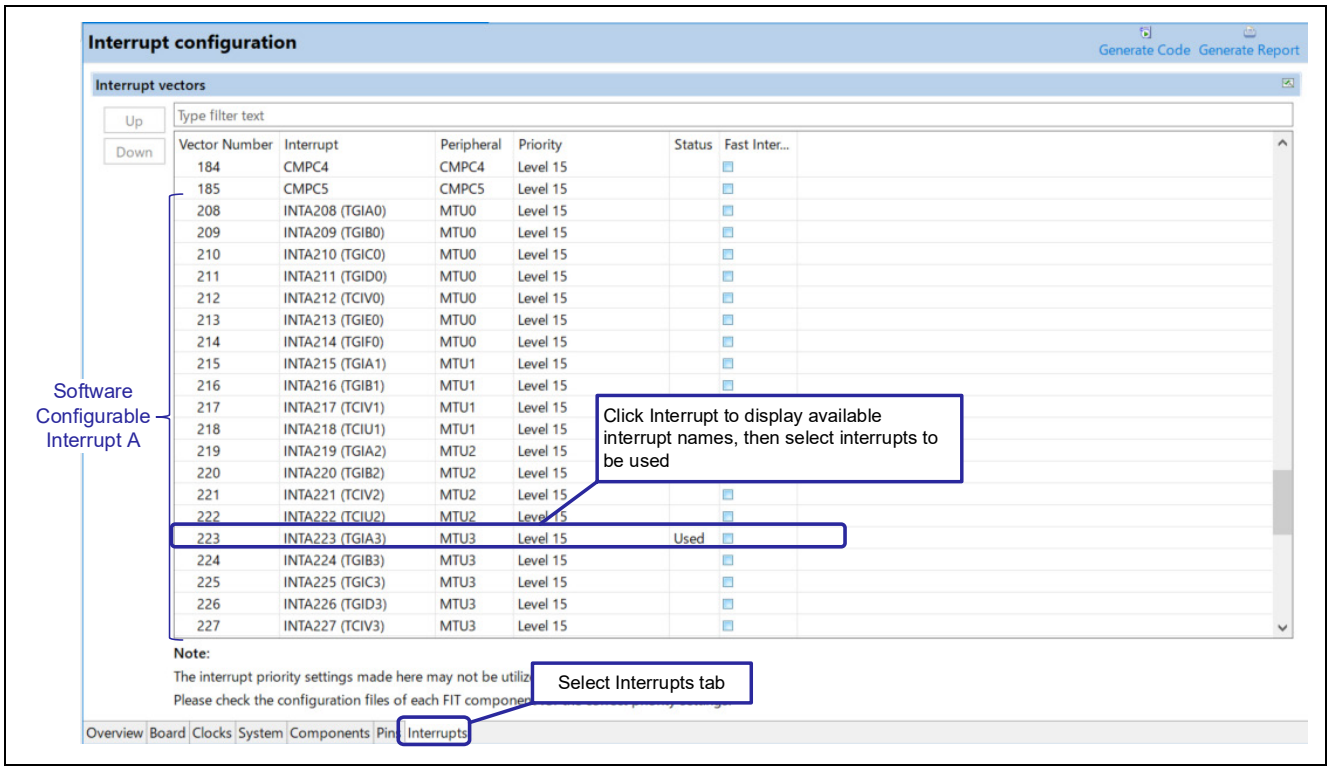


Figure 3.4 Interrupt Settings

3.2 Operation Near 0% and 100% Duly Cycles

Applicable sample code file name: r01an6539_rx66t_mtu3.zip

3.2.1 Overview

This sample code performs operation near 0% and 100% duly cycles on the MTU.

The sample code repeatedly generates waveform output near 0% or 100% duty cycle using the MTU's complementary PWM mode 3 (transfer at crest and trough).

- Near 0% duty cycle: 8% → 4% → 0% → 0% → 4% → 8%
- Near 100% duty cycle: 92% → 96% → 100% → 100% → 96% → 92%

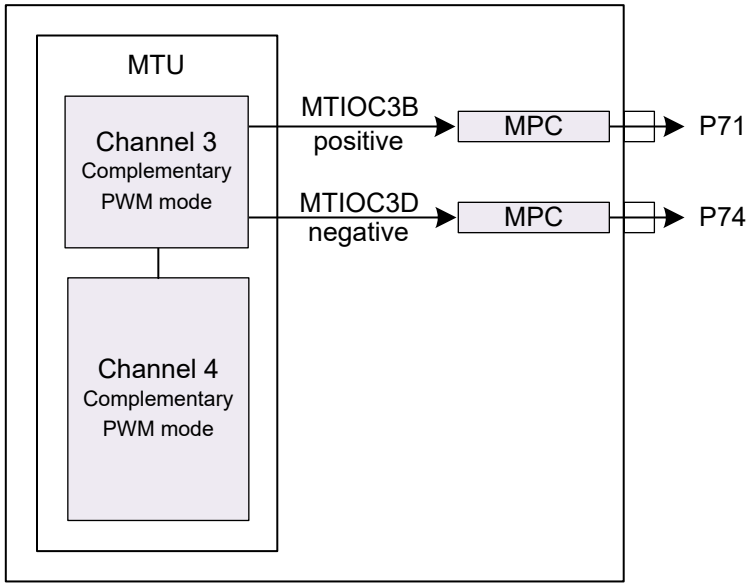
Complementary PWM mode can be used to generate three-phase waveform output (U, V, and W phases), but the sample code generates only single-phase (positive phase and negative phase) waveform output.

The MTU settings used in the sample code are as follows.

- Use complementary PWM mode 3 (transfer at crest and trough).
- Use channel 3 and channel 4.
- The carrier period is 1 ms.
- The dead time is 25 µs.
- The timer count clock frequency is 40 MHz (PCLKC/4).
- MTU3.TGRA sets the upper limit value of MTU3.TCNT (1/2 of carrier period + dead time).
- The buffer transfer timing is set.
  - Transfer at counter crest and trough
- The initial output value is low, and the active level is high.
- MTU3.TGRB is used as the duty cycle register.
  - Positive phase: High output at up-count compare match, low output at down-count compare match
  - Negative phase: Low output at up-count compare match, high output at down-count compare match
- A buffer register is used.
  - MTU3.TGRD is used as the buffer register of MTU3.TGRB.
  - Refer to Figure 3.6 and Figure 3.7 for buffer register initial values.
- The duty cycle changes each period.
  - The duty cycle changes at a MTU3.TGRA compare match interrupt.
  - Refer to Figure 3.6 and Figure 3.7 for duty cycle change timings.

Settings can be configured in Smart Configurator. Refer to section 3.2.3 for instructions.

The structure of the sample code is shown below.



MTU: Generates complementary PWM mode waveforms
MPC: Changes the settings for the pins to be used from general purpose I/O port to peripheral function I/O port

Figure 3.5 Sample Code Structure

3.2.2 Operation Details

The sample code contains settings for near 0% duty cycle (8% → 4% → 0% → 0% → 4% → 8%). To change the settings to near 100% duty cycle (92% → 96% → 100% → 100% → 96% → 92%), change the following values in Config_MTU3_MTU4_user.c as shown.

- Near 0% duty cycle

```
#define PRV_COMPARE_DATA_0          (1)
#define PRV_COMPARE_DATA_100        (0)
```

- Near 100% duty cycle

```
#define PRV_COMPARE_DATA_0          (0)
#define PRV_COMPARE_DATA_100        (1)
```

Operation near 0% duty cycle and operation near 100% duty cycle are shown below.

- Near 0% duty cycle: 8% → 4% → 0% → 0% → 4% → 8%
- Operation
  Buffer overwrite occurs in the Tb1 interval (crest) in complementary PWM mode 3 (Figure 3.6).
  (a) Compare match with temporary register, positive phase remains off.
  (b) Simultaneous compare matches for on (red dots) and off (blue dots), no change in negative phase.
  (c) Compare match for on, but no change in positive phase because (c) off takes precedence.

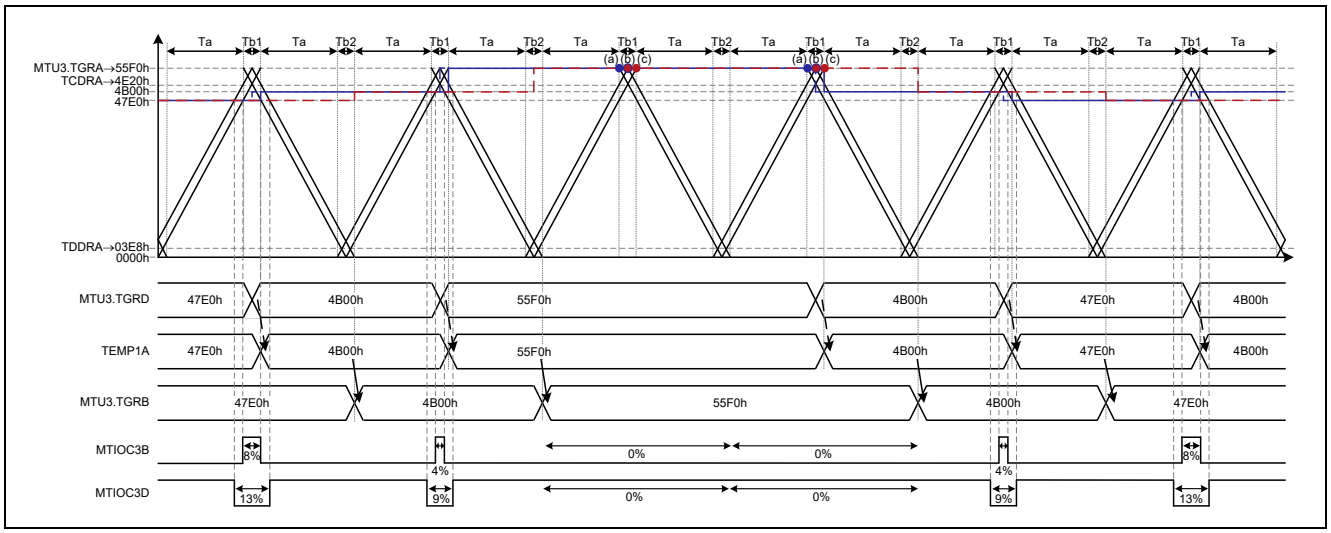


Figure 3.6 Sample Code Operation (Near 0% Duty Cycle: 8% → 4% → 0% → 0% → 4% → 8%)

- Near 100% duty cycle: 92% → 96% → 100% → 100% → 96% → 92%
- Operation
  Buffer overwrite occurs in the Tb1 interval (crest) in complementary PWM mode 3 (Figure 3.7).
  (a) Compare match with compare register, positive phase turns off.
  (b) Compare match with temporary register, positive phase turns on.
  (c) Compare match with temporary register, negative phase remains off.
  (d) Simultaneous compare matches for on (blue dots) and off (red dots), no change in positive phase.
  (e) Compare match for on, but no change in negative positive phase because (c) off takes precedence.
  (f) Compare match with compare register, positive phase turns off.
  (g) Compare match with temporary register, positive phase turns on.

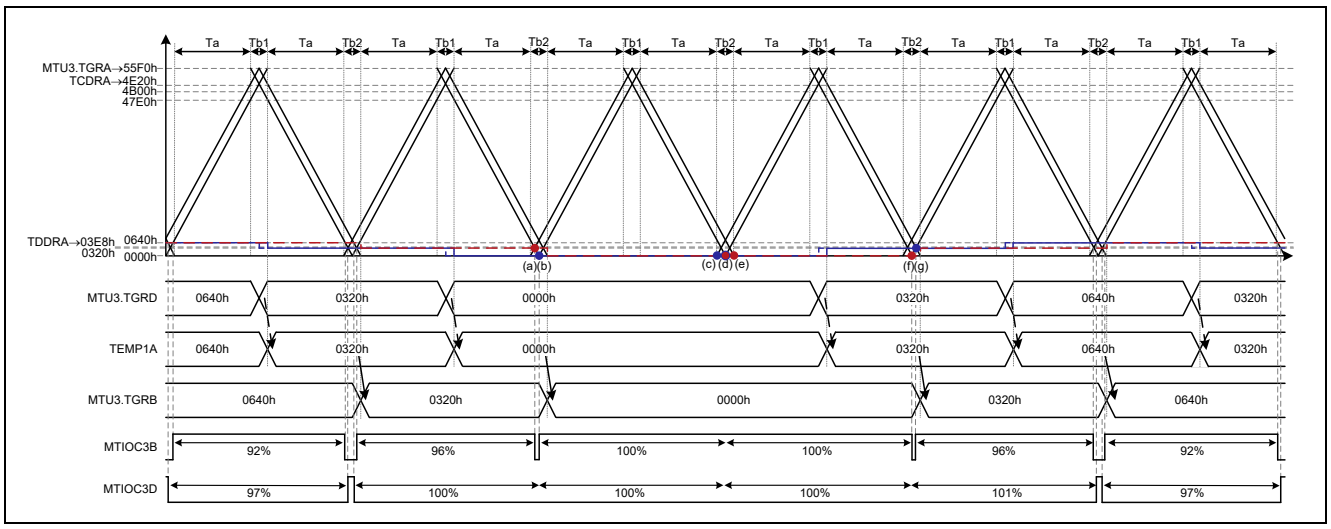


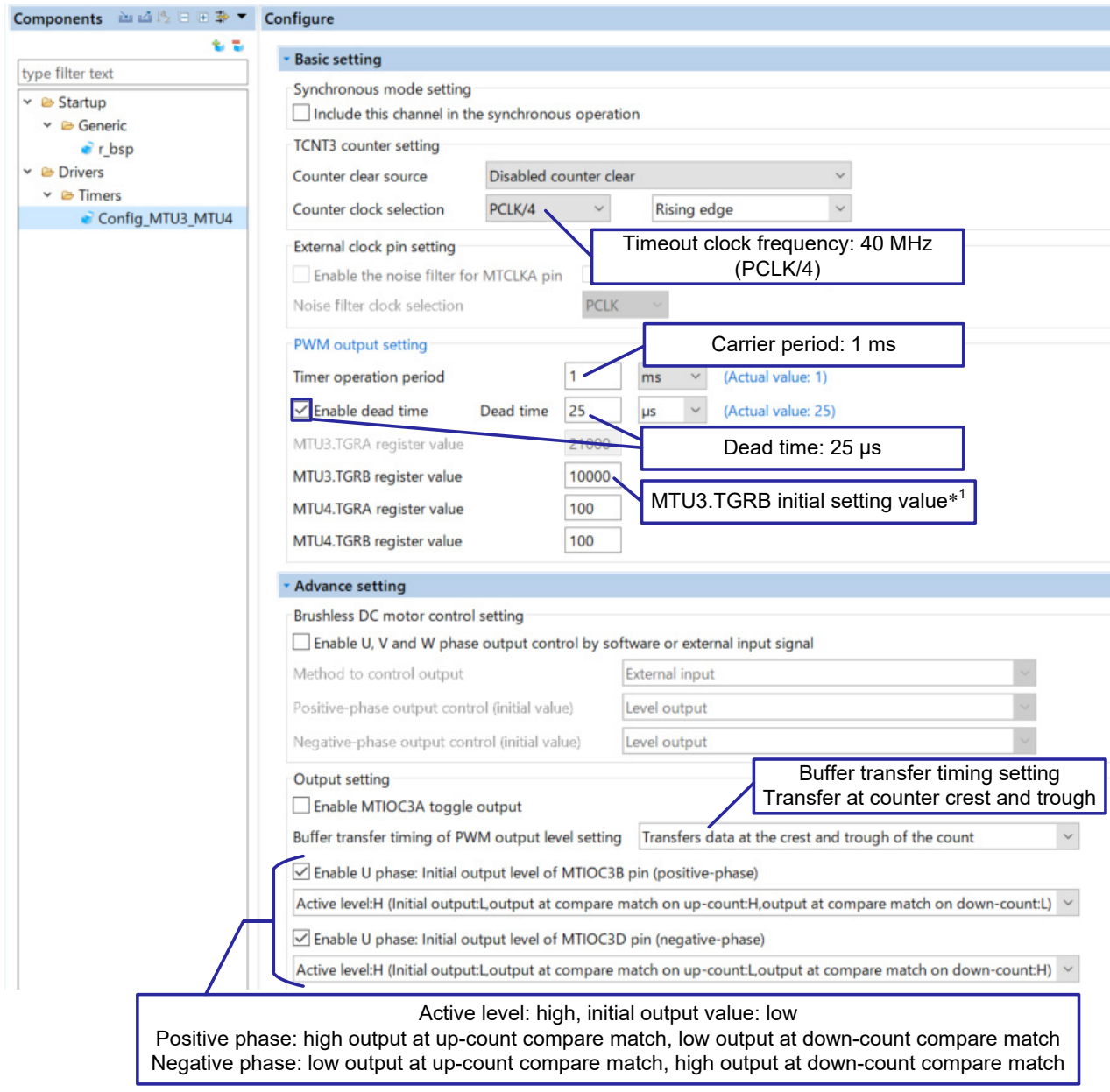
Figure 3.7 Sample Code Operation
(Near 100% Duty Cycle: 92% → 96% → 100% → 100% → 96% → 92%

3.2.3 Smart Configurator Settings

The sample code uses Smart Configurator to add the MTU as described below. For details on how to add components, refer to section 3.1.4, Adding Components.

Table 3.4 Adding Components

Item	Description
Component	Complementary PWM mode timer
Configuration name	Config_MTU3_MTU4
Operation	Complementary PWM mode 3 (transfer at crest and trough)
Resource	MTU3_MTU4



Note: 1. Configuration of the output duty cycle (8% or 92%) compare match register setting is performed by the R_Config_GPT0_Create_UserInit function.

Figure 3.8 MTU3 and MTU4 Settings (1/2)

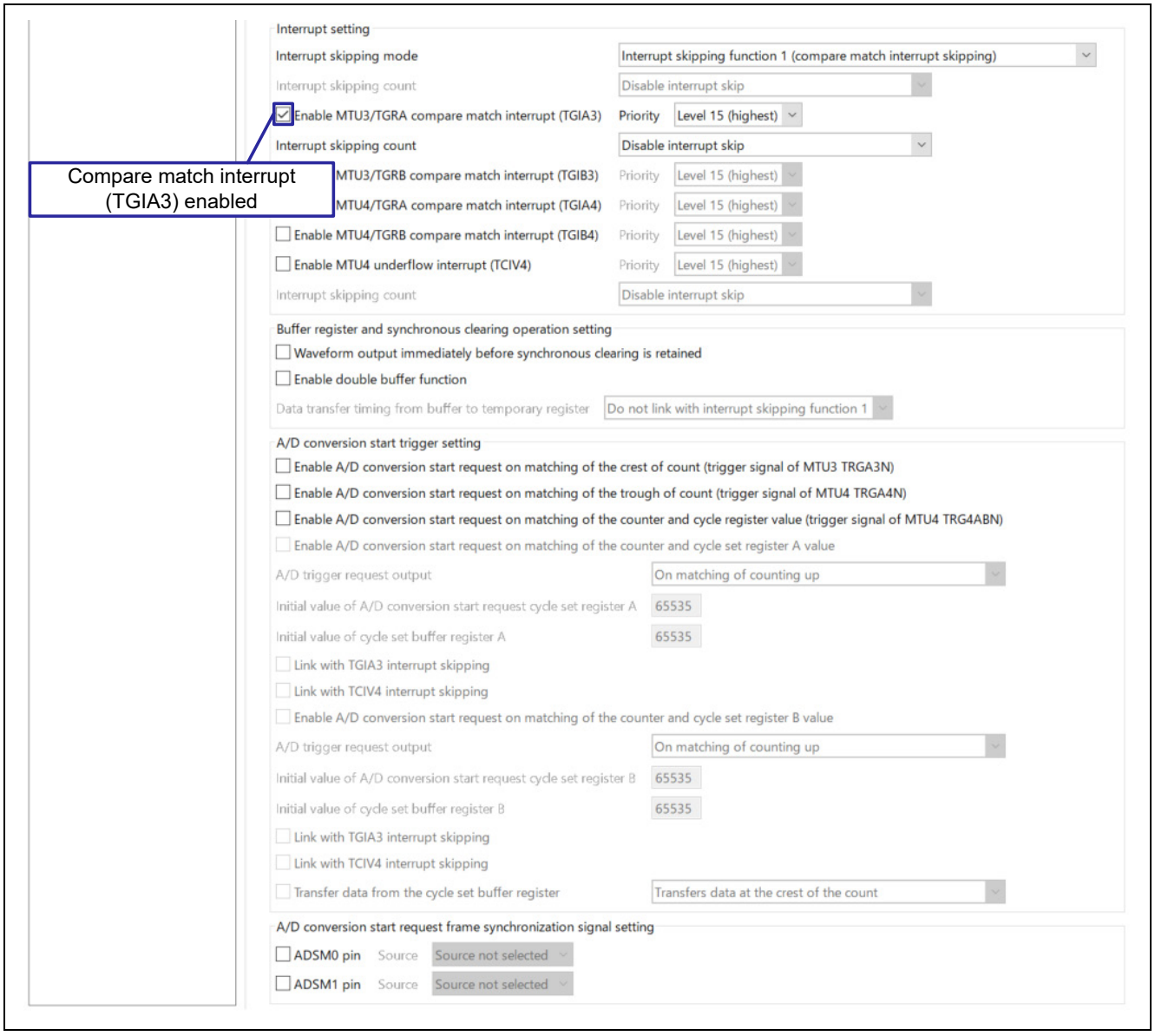


Figure 3.9 MTU3 and MTU4 Settings (2/2)

3.2.4 Flowcharts

Processing by the main function added after code generation by Smart Configurator is shown below. Counting by MTU3.TCNT and MTU4.TCNT is started in the main function.

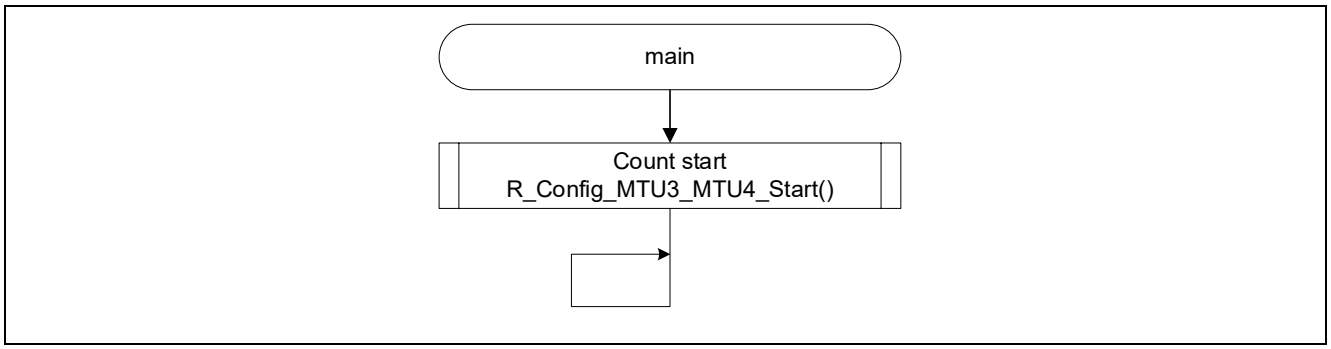


Figure 3.10 main Function

The user initialization function R_Config_MTU3_MTU4_Create_UserInit runs before the main function and initializes variables. This function is called by the R_Config_MTU3_MTU4_Create function.

The following variable, which us used by the sample code, is initialized.

s_duty_list_counter: Counter variable for reading from duty ratio list

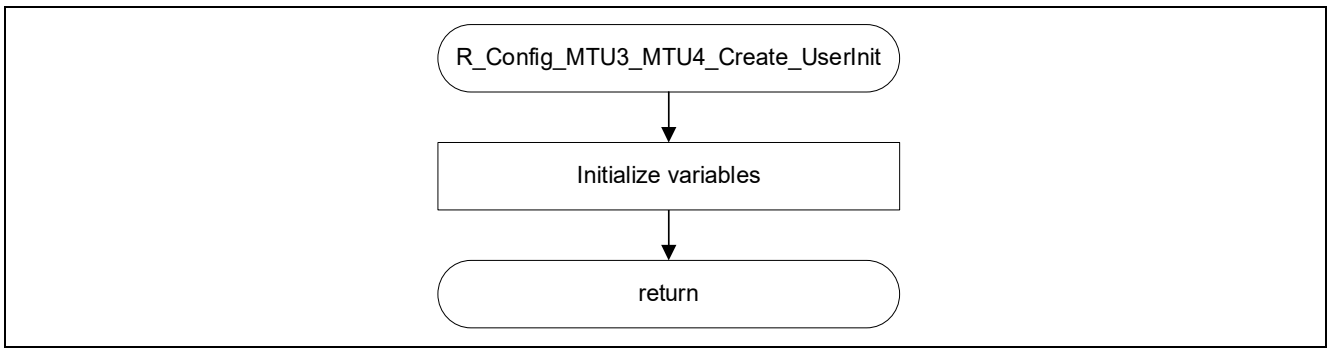


Figure 3.11 User Initialization Function

The TGIA3 interrupt handler function changes the value of the buffer register (MTU3.TGRD) sequentially according to values read from the duty ratio list array.

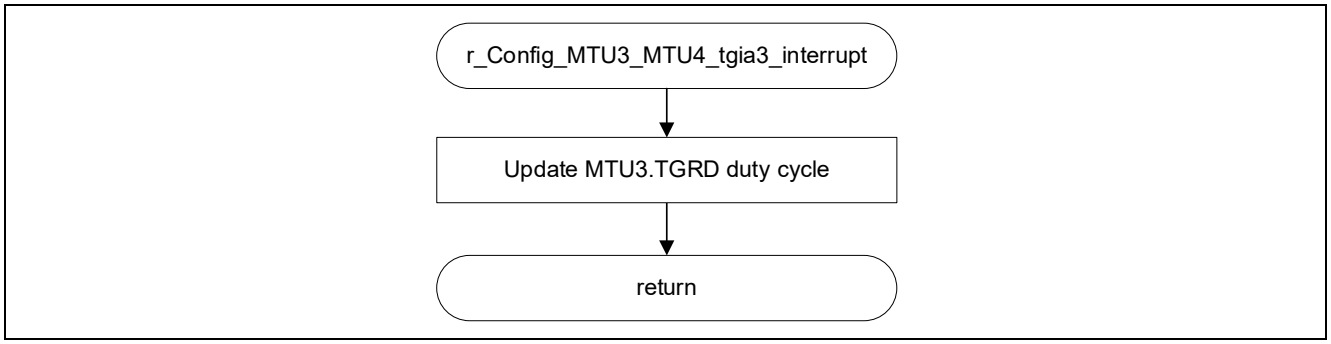


Figure 3.12 TGIA3 Interrupt Handler Function

3.2.5 Usage Notes

3.2.5.1 Pin Settings

Pins MTIOC3C and MTIOC6C cannot be used as timer I/O pins in complementary PWM mode. They must be configured as I/O ports.

For details, refer to Table 22.74, Output Pins in Complementary PWM Mode, under 22.3.8, Complementary PWM Mode, in RX66T Group User's Manual: Hardware.

3.2.5.2 Updating Buffer Register Values

When overwriting data in the buffer register, write to MTU4.TGRD (MTU7.TGRD) as the final step. Data transfer from the buffer register to the temporary register takes place simultaneously for all five registers after data is written to MTU4.TGRD (MTU7.TGRD).

If it is not necessary to update all five registers or it is not necessary to update the data in MTU4.TGRD (MTU7.TGRD), write to MTU4.TGRD (MTU7.TGRD) after writing data to the registers to be updated. At this time, make sure that the data written to MTU4.TGRD (MTU7.TGRD) is that same as the data preceding the write operation.

3.2.5.3 Buffer Operation Settings

Buffer operation should be used to overwrite the PWM period setting registers (MTU3.TGRA and MTU6.TGRA), timer period data registers (TCDRA and TCDRB), and duty cycle setting registers (MTU3.TGRB, MTU4.TGRA, MTU4.TGRB, MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB) in complementary PWM mode.

When the buffer operation bit MTU4.TMDR1.BFA (MTU7.TMDR1.BFA) or MTU4.TMDR1.BFB (MTU7.TMDR1.BFB) is set to 1, waveform output cannot be generated on pin MTIOC4C (MTIOC7C) or MTIOC4D (MTIOC7D). Therefore, the MTU4.TMDR1.BFA (MTU7.TMDR1.BFA) and MTU4.TMDR1.BFB (MTU7.TMDR1.BFB) bits should be cleared to 0.

For details, refer to 22.6.14, Buffer Operation Settings in Complementary PWM Mode in RX66T Group User's Manual: Hardware.

3.2.5.4 Output Level Settings

The output level of the PWM waveforms is set by the TOCR1A.OLSP, TOCR1A.OLSN, TOCR1B.OLSP, and TOCR1B.OLSN bits, as well as the TOCR2A.OLSnP, TOCR2A.OLSnN, TOCR2B.OLSnP, and TOCR2B.OLSnN (n = 0 to 3) bits in complementary PWM mode on the MTU3 and MTU4 (MTU6 and MTU7). The TIOR register should be set to 00h.

When the TDERA.TDER (TDERB.TDER) bit is cleared to 0 (do not generate dead time) in complementary PWM mode, the negative phase output level is the inversion of the positive phase output level set by the TOCR1A.OLSP (TOCR1B.OLSP) and TOCR2A.OLSnP (TOCR2B.OLSnP) (n = 0 to 3) bits, regardless of the settings of the TOCR1A.OLSN (TOCR1B.OLSN) and TOCR2A.OLSnN (TOCR2B.OLSnN) (n = 0 to 3) bits.

For details, refer to 22.2.22, Timer Output Control Register 1 (TOCR1A, TOCR1B), and 22.2.23, Timer Output Control Register 2 (TOCR2A, TOCR2B), in RX66T Group User's Manual: Hardware.

4. GPTW Sample Code

4.1 Common

4.1.1 Sample Code List

This application note provides the following sample code created with Smart Configurator. Sample code can be downloaded from the Renesas Electronics website.

Table 4.1 GPTW Sample Code List

Name	Sample Code Usage Conditions	Reference
Operation near 0% and 100% duty cycles r01an6539_rx66t_gptw.zip	Triangle-wave PWM mode 3 (trough, 64-bit transfer)	4.2

4.1.2 Folder Structure

The main folder structure of the sample code is as follows.

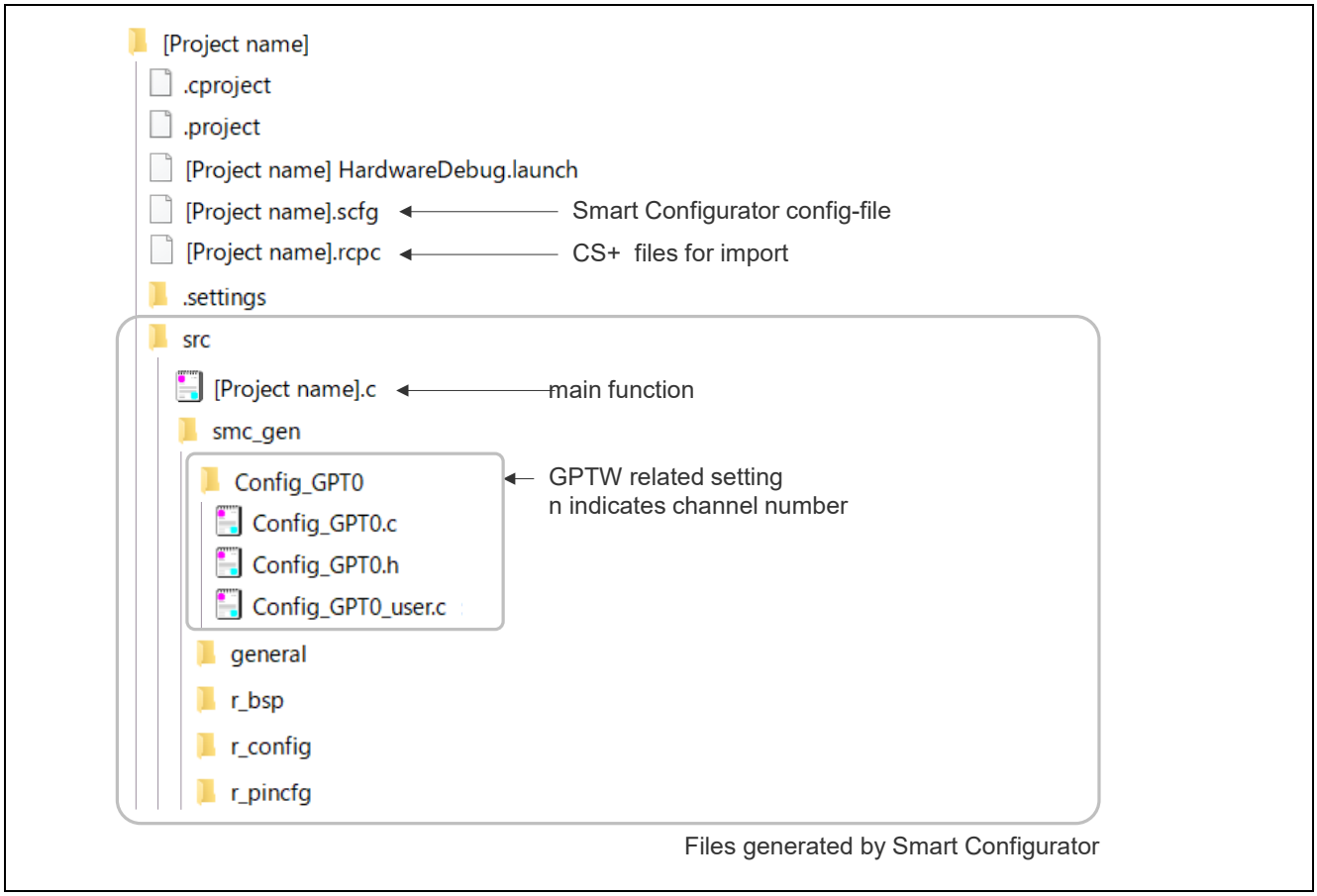


Figure 4.1 GPTW Folder Structure

4.1.3 File Structure

The main file structure of the sample code is as follows.

Table 4.2 GPTW File Structure

File Name	Description
[project name].c	Main function This is the main function. Smart Configurator generates an empty function. The necessary processing for each code sample is described here.
Config_GPTn.c*1	R_Config_GPTn_Create function This is the GPTW's initialization function. Smart Configurator generates this initialization function based on the Smart Configurator settings. Calls by this function are generated by Smart Configurator. This function is called by the R_SystemInit function that runs before the main function.
	R_Config_GPTn_Start function This is the GPTW's count stop function. This function is generated by Smart Configurator. This function is called by the main function in the sample code.
	R_Config_GPTn_Stop function This is the GPTW's count stop function. This function is generated by Smart Configurator. This function is not used in the sample code.
Config_GPTn_user.c*1	r_Config_GPTn_Create_UserInit function This is a user function used to initialize the GPTW. Smart Configurator generates an empty function. The necessary processing for each code sample is described here. This is the last function to be called by the R_Config_GPTn_Create function generated by Smart Configurator.
	r_Config_GPTn_[interrupt name]_interrupt function This is an interrupt handler function. Smart Configurator generates an empty function. The necessary processing for each code sample is described here.
Config_GPTn.h*1	This is the header file that defines GPTW related functions. This file is included in the r_smc_entry.h file generated by Smart Configurator. To use GPTW related functions, be sure to include the r_smc_entry.h file.

Note: 1. n represents the channel number.

4.1.4 Adding Components

Smart Configurator is used to add GPTW functionality to the sample code as described below.

Table 4.3 Adding Components

Item	Description
Component	General-purpose PWM timer ((1) in figure below)
Configuration name	Default setting name used in sample code
Operation	Reference section for each code sample ((2) in figure below)
Resources	Reference section for each code sample ((3) in figure below)

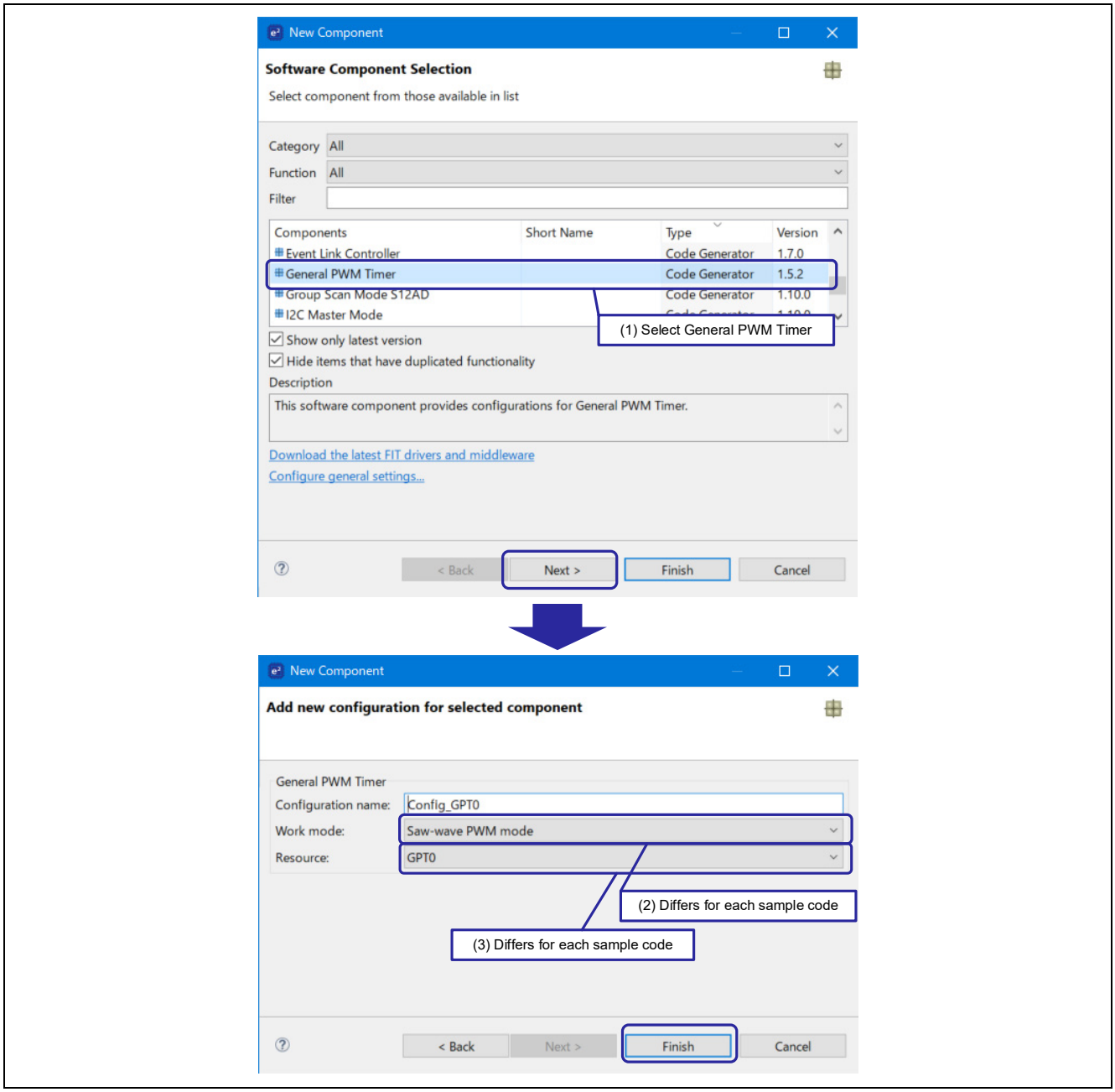


Figure 4.2 Adding Components

4.1.5 Pin Settings

Figure 4.3 shows an example of pin settings in Smart Configurator.

Configure the pins after configuring GPTW settings. For GPTW settings, refer to the “Smart Configurator Settings” in each code sample.

Pin settings are applied by the R_Config_GPTn_Create function generated by Smart Configurator.

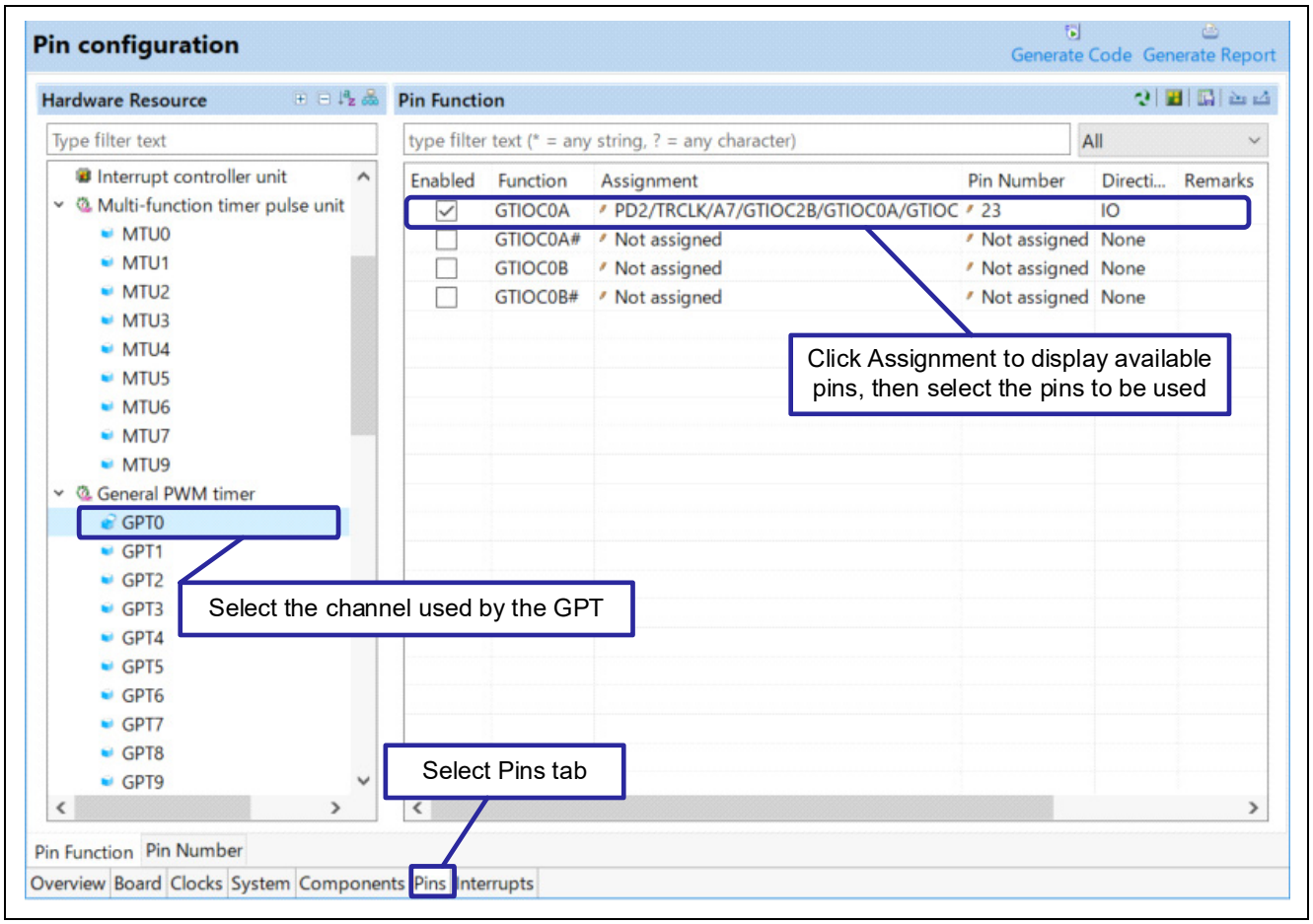


Figure 4.3 Pin Settings

4.1.6 Interrupt Settings

Figure 4.4 shows an example of interrupt settings in Smart Configurator. For details of software configurable interrupt A, refer to 14.4.5.1, Software Configurable Interrupt A, in Renesas RX66T Group User's Manual Hardware.

Configure interrupts after configuring GPTW settings. For GPTW settings, refer to the "Smart Configurator Settings" in each code sample.

Interrupt settings are applied by the R_Config_GPTn_Create, R_Config_GPTn_Start, and R_Config_GPTn_Stop functions, all of which are generated by Smart Configurator.

The interrupt handler function is created with the name r_Config_GPTn_[interrupt name]_interrupt in the Config_GPTn_user.c file generated by Smart Configurator.

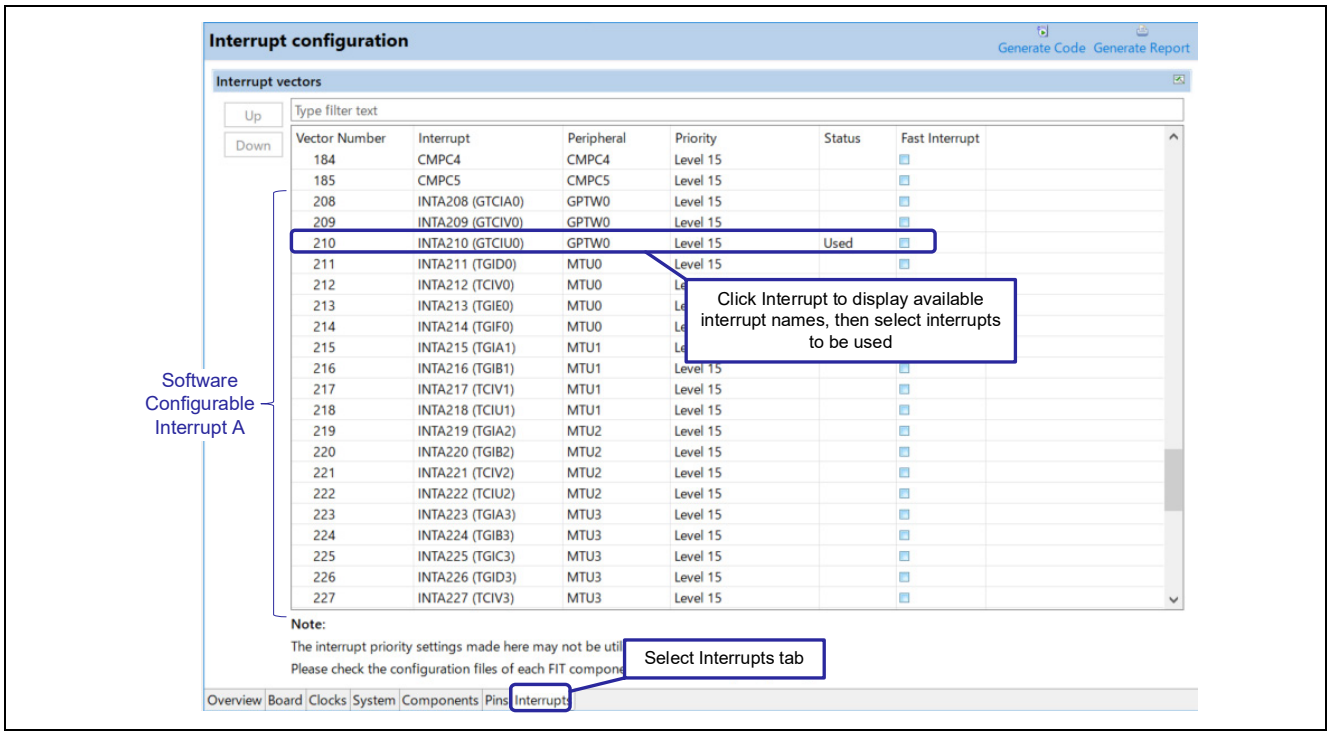


Figure 4.4 Interrupt Settings

In the initial settings on the Interrupt tab of Smart Configurator, only GPTW interrupts GTCIE0, GTCIF0, and GDTE0 are selected. To use interrupts configured on the Component tab, it is necessary to select them on the Interrupt tab. An error message is displayed if the selection below is insufficient.

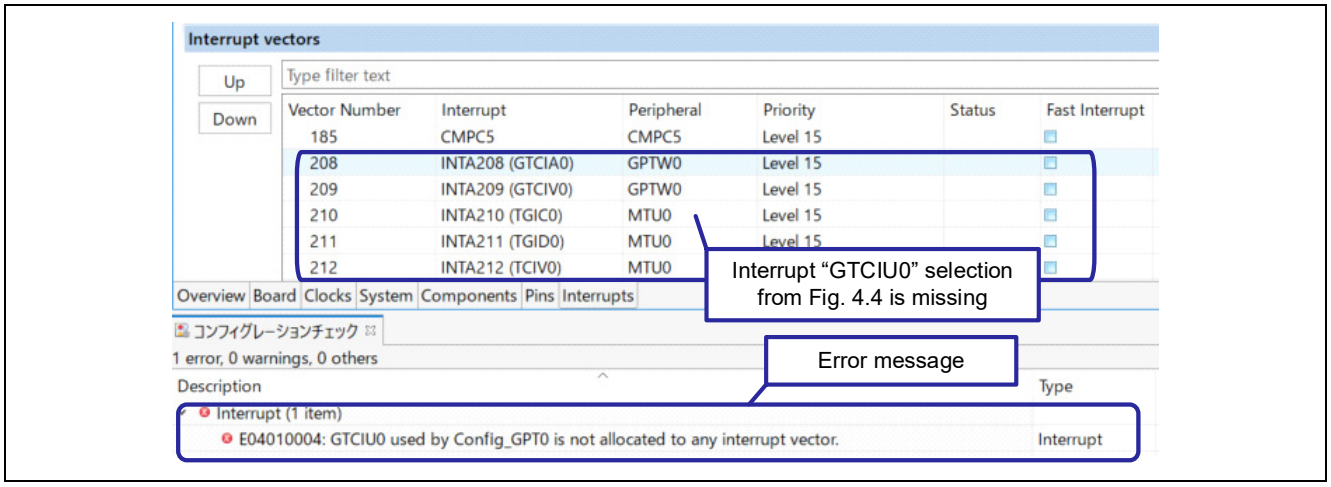


Figure 4.5 Interrupt Settings (Insufficient Interrupt Selection)

4.2 Operation Near 0% and 100% Duly Cycles

Applicable sample code file name: r01an6539_rx66t_gptw.zip

4.2.1 Overview

This sample code performs operation near 0% and 100% duly cycles on the GPTW.

The sample code repeatedly generates waveform output near 0% or 100% duty cycle using the GPTW's triangle-wave PWM mode 3 (trough, 64-bit transfer). The 0% and 100% duty cycle output is produced by overwriting the GTUDDTYC register when the GTCNT counter underflows (trough).

- Near 0% duty cycle: 8% → 4% → 0% → 0% → 4% → 8%
- Near 100% duty cycle: 92% → 96% → 100% → 100% → 96% → 92%

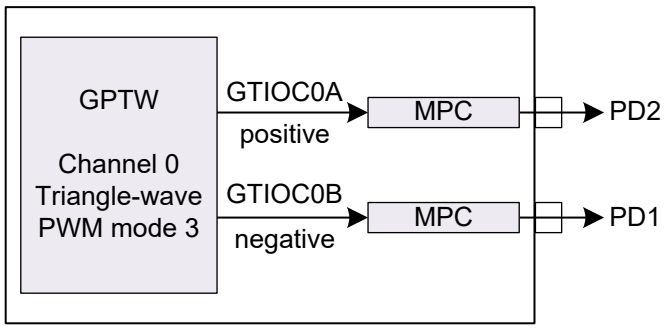
The GPTW settings used in the sample code are as follows.

- Use triangle-wave PWM mode 3.
- Use channel 0.
- The carrier period is 1 ms.
- The timer count clock frequency is 160 MHz (PCLKC/1)
- GTPR is used as the period register.
  - The counter performs up-count operation from an initial value of 0.
- GTCCRA is used for compare matches with the duty cycle output.
  - The GTIOC0A pin is used as a PWM output pin.
  - GTCCRA is used for compare matches.
  - Low output at count start.
  - Toggle output at GTCCRA compare match.
  - Retain output at end of period.
  - Previously masked compare match output values are output after cancellation of 0% and 100% duty cycles.*
- GTCCRB is used for compare matches with the duty cycle output.
  - The GTIOC0B pin is used as a PWM output pin.
  - GTCCRB is used for compare matches.
  - High output at count start.
  - Toggle output at GTCCRB compare match.
  - Retain output at end of period.
  - Previously masked compare match output values are output after cancellation of 0% and 100% duty cycles.*
- Use buffer registers.
  - GTCCRC and GTCCRD are buffer registers for GTCCRA.
- Use automatic dead time generation.
- Software source count start enabled.
- The duty cycle changes each period.
  - The duty cycle changes at a GTCNT counter underflow interrupt.
  - Refer to Figure 4.7 and Figure 4.8 for duty cycle change timings.

Settings can be configured in Smart Configurator. Refer to section 4.2.3 for instructions. (Except items marked with an asterisk (*).)

* Set by user initialization function R_Config_GPT0_Create_UserInit.

The structure of the sample code is shown below.



GPTW: Generates PWM waveform with triangle-wave PWM mode 3
MPC: Changes the settings for the pins to be used from general purpose I/O port to peripheral function I/O port

Figure 4.6 Sample Code Structure

4.2.2 Operation Details

The sample code contains settings for near 0% duty cycle (8% → 4% → 0% → 0% → 4% → 8%). To change the settings to near 100% duty cycle (92% → 96% → 100% → 100% → 96% → 92%), change the following values in Config_GPT0_user.c as shown.

- Near 0% duty cycle

```
#define PRV_COMPARE_DATA_0          (1)
#define PRV_COMPARE_DATA_100        (0)
```

- Near 100% duty cycle

```
#define PRV_COMPARE_DATA_0          (0)
#define PRV_COMPARE_DATA_100        (1)
```

Operation near 0% duty cycle and operation near 100% duty cycle are shown below.

- Near 0% duty cycle: 8% → 4% → 0% → 0% → 4% → 8%
- Operation
  The buffer register and GTUDDTYC register are overwritten at the underflow (trough) in triangle-wave PWM mode 3 (Figure 4.7).
  (a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
  (b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
  (c) Output changes due to compare match with compare register.
  (d) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).

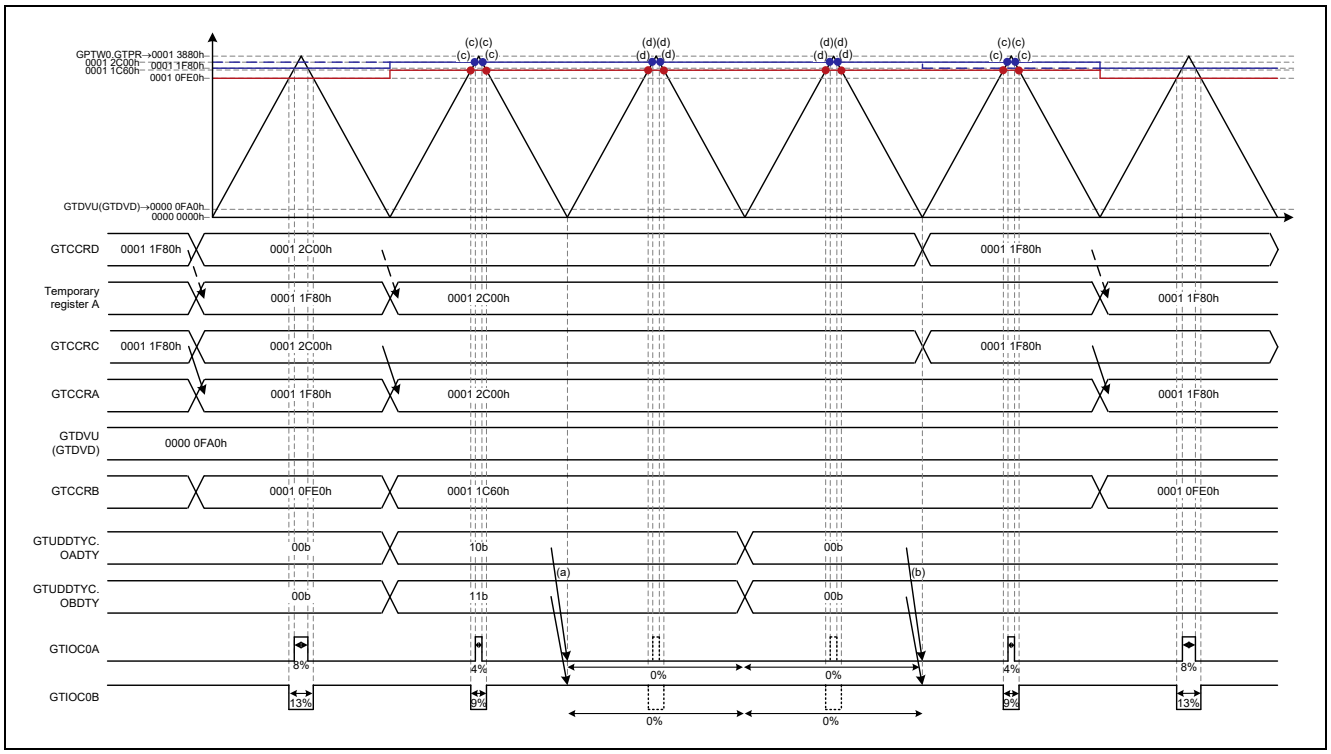


Figure 4.7 Sample Code Operation
(Near 0% Duty Cycle: 8% → 4% → 0% → 0% → 4% → 8%)

- Near 100% duty cycle: 92% → 96% → 100% → 100% → 96% → 92%
- Operation
  The buffer register and GTUDDTYC register are overwritten at the underflow (trough) in triangle-wave PWM mode 3 (Figure 4.8).
  (a) Setting value of OmDTY bits (11b or 10b) applied at underflow (trough), 0%/100% output start.
  (b) Setting value of OmDTY bits (00b) applied at underflow (trough), 0%/100% duty cycle output canceled (change to output control by compare match).
  (c) Change point at GTDVU due to correction function, positive phase turns off.
  (d) Compare match occurs, but output maintained according to setting value of OmDTY bits (11b or 10b).
  (e) Due to cancelling of 0%/100% duty cycle output, output changes according to setting value of GTUDDTYC.OmDTYR bit and GTIOR.GTIOm[3:2] bits.
  (f) When OmDTY bit is set to 1b, correction function causes negative phase to become pulse with width of 1 count clock cycle.
  (g) Change point at GTDVU + 1 due to correction function, positive phase turns on.

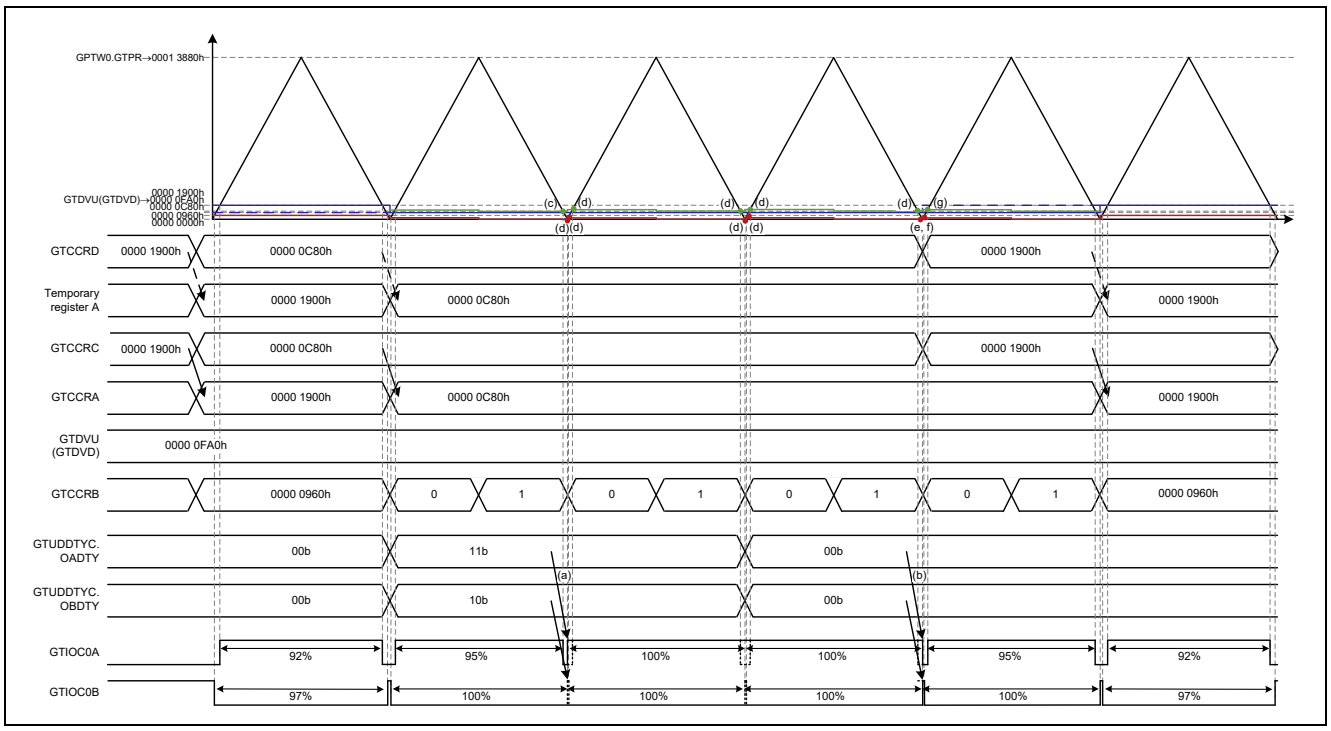


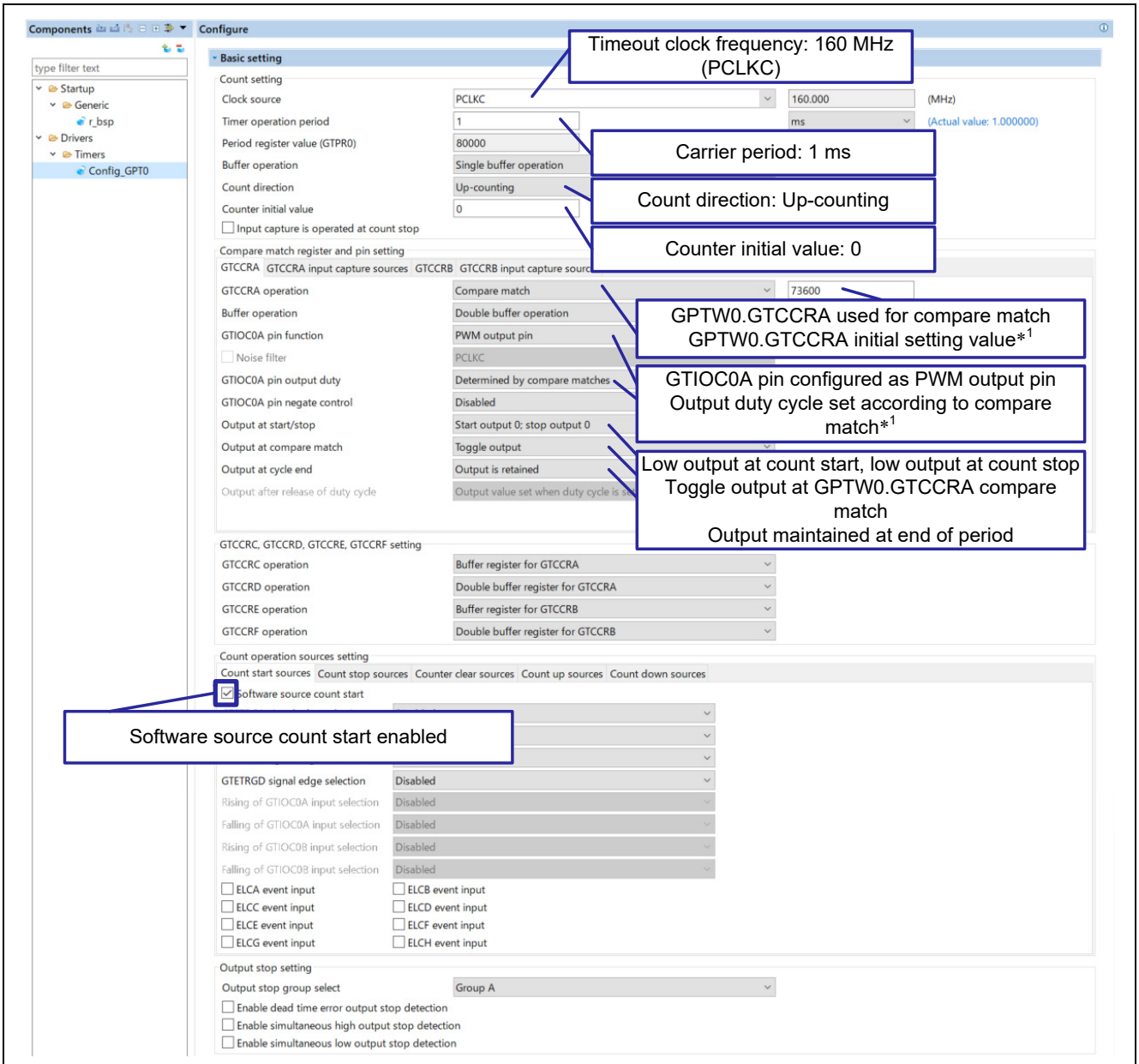
Figure 4.8 Sample Code Operation
(Near 100% Duty Cycle: 92% → 96% → 100% → 100% → 96% → 92%

4.2.3 Smart Configurator Settings

The sample code uses Smart Configurator to add the GPTW as described below. For details on how to add components, refer to section 4.1.4, Adding Components.

Table 4.4 Adding Components

Item	Description
Component	General PWM timer
Configuration name	Config_GPT0
Operation	Triangle-wave PWM mode 3
Resource	GPT0



Note: 1. The compare match register settings for the output duty cycle (8% or 92%) after count start are configured by the R_Config_GPT0_Create_UserInit function.

Figure 4.9 GPT0 Settings (1/3)

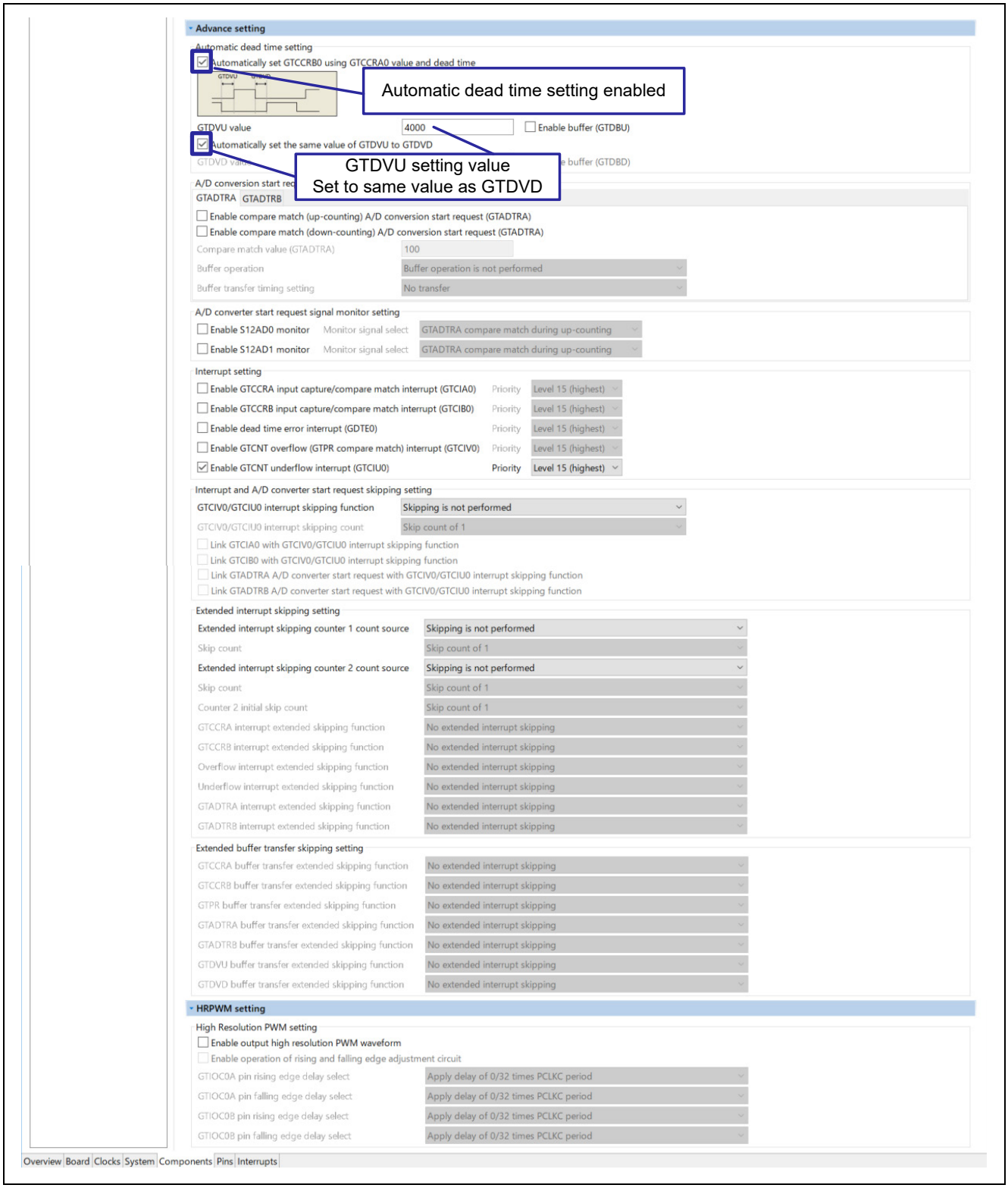


Figure 4.10 GPT0 Settings (2/3)

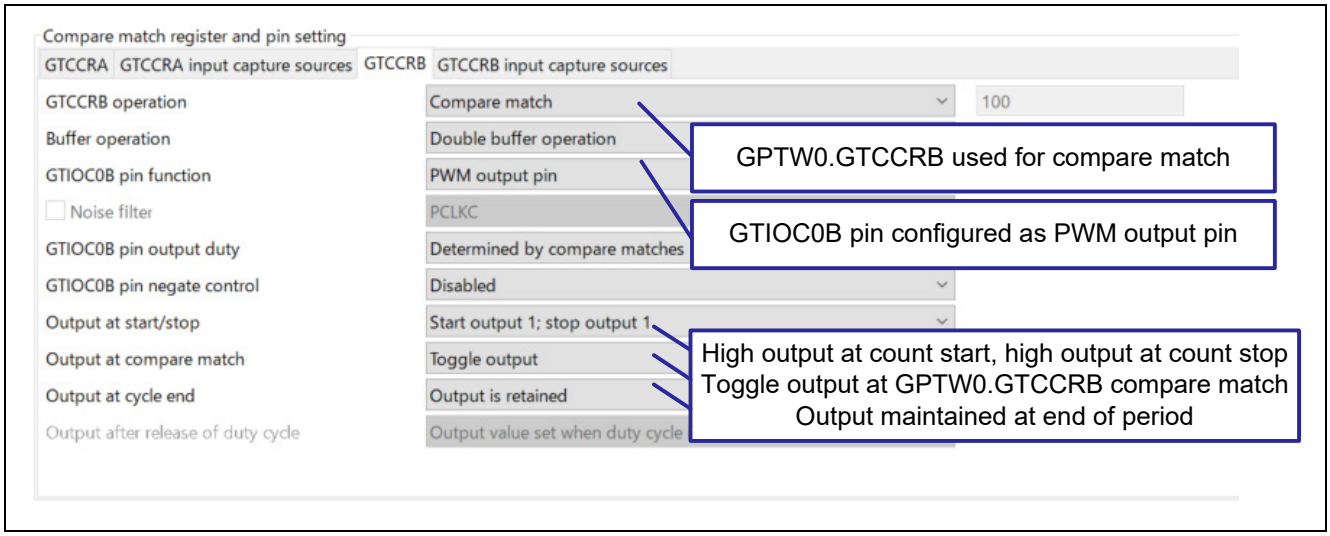


Figure 4.11 GPT0 Settings (3/3)

4.2.4 Flowcharts

Processing by the main function added after code generation by Smart Configurator is shown below. Counting is started within the main function.

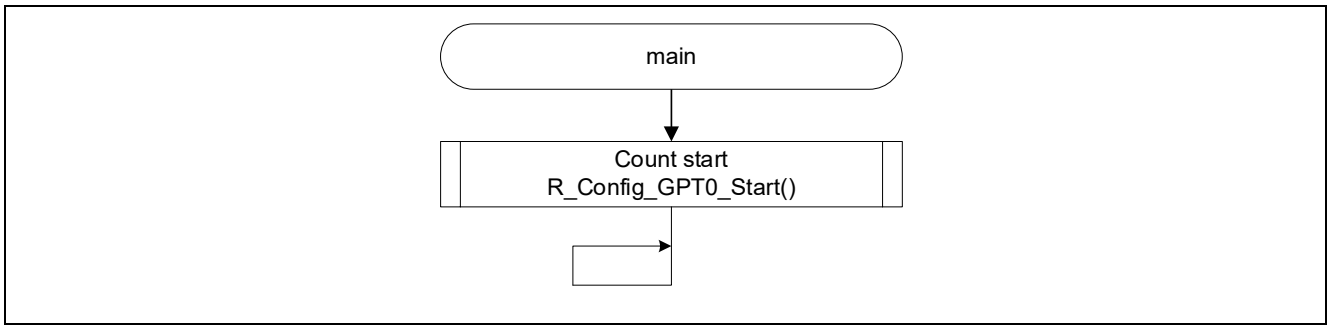


Figure 4.12 main Function

The user initialization function R_Config_GPT0_Create_UserInit runs before the main function and initializes variables, sets the initial value for the buffer register, and configures settings for after 0%/100% duty cycle output is canceled. Since the second compare match register value of the first period is set, a forced buffer transfer occurs after the buffer register value is set and temporary register and compare register values are set. This function is called by the R_Config_GPT0_Create function.

The following variable, which us used by the sample code, is initialized.

s_duty_list_counter: Counter variable for reading from duty ratio list

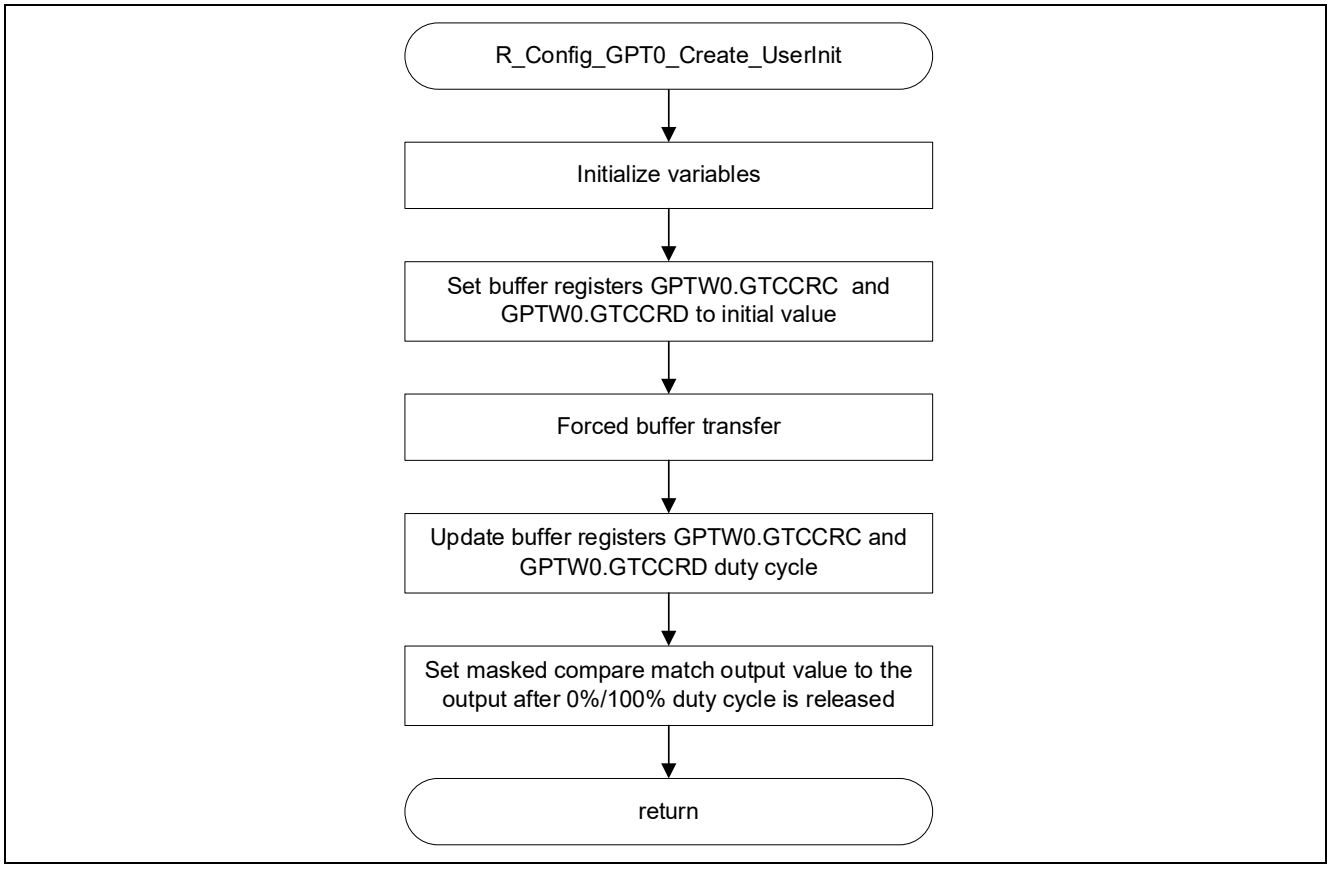


Figure 4.13 User Initialization Function

The GTCIU0 interrupt handler function changes the value of the buffer register and GTUDDTYC register according to the next duty ratio setting.

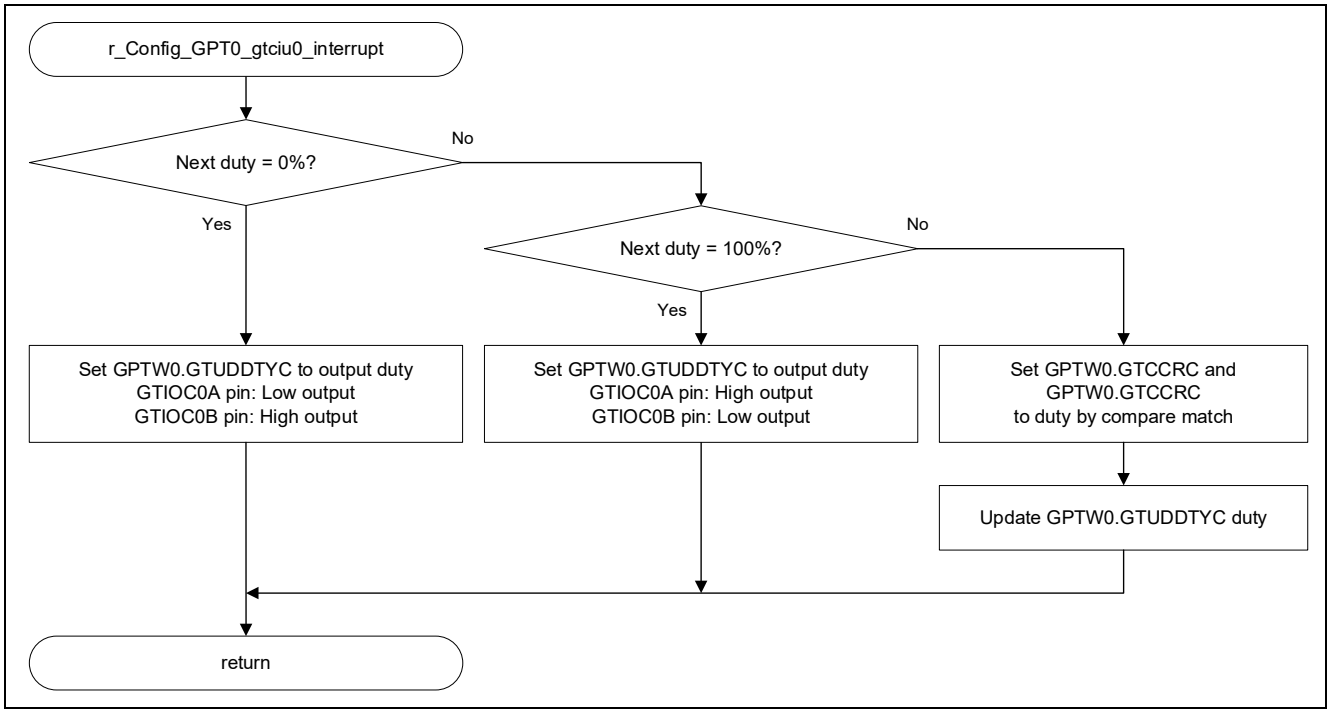


Figure 4.14 GTCIU0 Interrupt Handler Function

4.2.5 Usage Notes

4.2.5.1 Settings of GTCCRm Register during Compare Match Operation (m = A to F)

Automatic dead time setting is enabled in the sample code, and the value of the compare match register for positive phase waveforms (GTCCRA) is used to update the value of the compare match register for negative phase waveforms (GTCCRB).

The setting value of compare register GTCCRA must satisfy the following conditions.

GTCCRA > GTDVU
GTCCRA > GTDVD
GTCCRA < GTPR

The output protection function operates if GTCCRA is set to 0000 0000h or a value equal to or greater than the GTPR setting value during count operation.

However, the function cannot operate normally if the following condition is not satisfied.

Value of GTCCRA is 0000 0001h or greater and less than GTPR setting value.

For details of the output protection function, refer to 24.8.4, Output Protection Function for GTIOCnm Pin Output (n = 0 to 9, m = A or B), in RX66T Group User's Manual: Hardware.

Also, if automatic dead time setting is disabled, GTCCRA (GTCCRB) must be set to a value of 0000 0001h or greater and less than the GTPR register setting value. If set to 0000 0000h or the same value as the GTPR register, a compare match occurs within the period only when the value of GTCCRA (GTCCRB) is 0000 0000h or GTCCRA (GTCCRB) is set to the same value as the GTPR register. If GTCCRA is set to a value that exceeds the setting value of the GTPR register, no compare match occurs.

For details, refer to 1.4, Cautions when Using GPTW Output Protection Function, and 1.5, Dead Time Due to GPTW 0%/100% Duty Cycle Switching Register, in the present document and to (1) When Automatic Dead Time Setting Is Enabled in Triangle-Wave PWM Mode and (2) When Automatic Dead Time Setting Is Disabled in Triangle-Wave PWM Mode, under 24.10.2, Settings of the GTCCRm Register during Compare Match Operation (m = A to F), in RX66T Group User's Manual: Hardware.

4.2.5.2 100% Duty Cycle Output at Compare Match

It is not possible to generate 100% duty cycle output at compare match without changing the value of the GTUDDTYC register. To generate 100% duty cycle output, set the GTUDDTYC.OADTY bits to 11b and the GTUDDTYC.OBDTY bits to 10b.

If the GTCCRA and GTCCRB registers are set to 0 in the settings used in the sample code, 100% duty cycle output cannot be generated because output is generated for one clock cycle after a GTCNT counter overflow occurs.

If the GTCCRA and GTCCRB registers are set to the same value as GTPR and GTCNT counter underflow and a compare match occur at the same time, 100% duty cycle output cannot be generated because the output settings applying to compare match occurrence take precedence and toggling occurs.

For details on waveform output when a GTCNT counter underflow and compare match occur at the same time on the GPTW, refer to the notes accompanying Table 24.4 under 24.2.14, General PWM Timer I/O Control Register (GTIOR) in RX66T Group User's Manual: Hardware.

4.2.5.3 Compare Match Operation during 0% Duty Cycle and 100% Duty Cycle Output

In the sample code, output with 0% and 100% duty cycles is produced based on the setting value of the GTUDDTYC.OADTY bits. Even when the duty cycle is set to either 0% or 100%, compare match operation continues in the GPTW, and interrupt output and buffer transfer operation take place.

The sample code does not use compare match interrupts, so exercise caution if you need to use compare match interrupts during 0% and 100% duty cycle output.

4.2.5.4 Switching from 0% or 100% Duty Cycle

The output value at the end of a period in which a switch from an output duty cycle setting of 0% or 100% to output generated by compare matches is determined by the values of the GTIOR.GTIOA[3:2] bits and the GTUDDTYC.OADTYR bit.

The settings used in the sample code are listed below. Note that if the initial hardware value of the GTUDDTYC.OADTYR bit is 0, the same operation as that of the sample code cannot be performed. The same applies for the GTIOC0B pin.

GTIOR.GTIOA[3:2] = 00b: Output maintained at end of period.

GTUDDTYC.OADTYR = 1: After the 0% or 100% duty cycle setting is canceled, apply the function of the GTIOA[3:2] bits to the previously masked compare match output value.

For details, refer to 24.3.6, Duty Cycle 0%/100% Output Function, in RX66T Group User's Manual: Hardware.

5. How to Import the Project

The sample code is provided in the format of an e² studio project. This chapter describes how to import a project into e² studio and CS+. After the import is complete, confirm the build and debugger settings.

5.1 Importing with e² studio

When using the sample code in e² studio, import it into e² studio using the following steps.

(The actual screen may vary according to the version of e² studio you are using.)

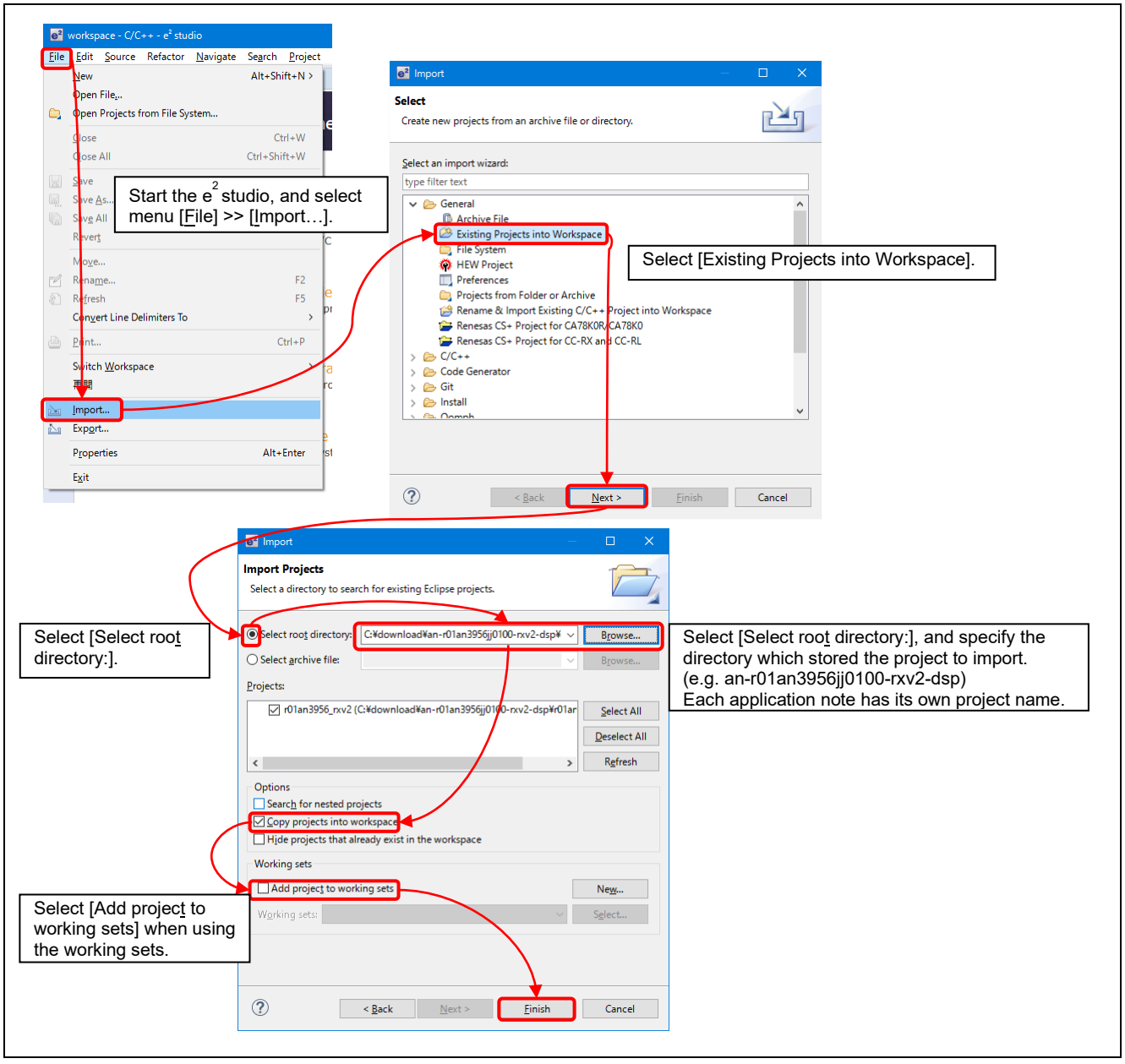


Figure 5.1 How to Import a Project into e² studio

5.2 Importing with CS+

When using the sample code with CS+, import the code to CS+ using the following steps.

(The actual screen may vary according to the version of CS+ you are using.)

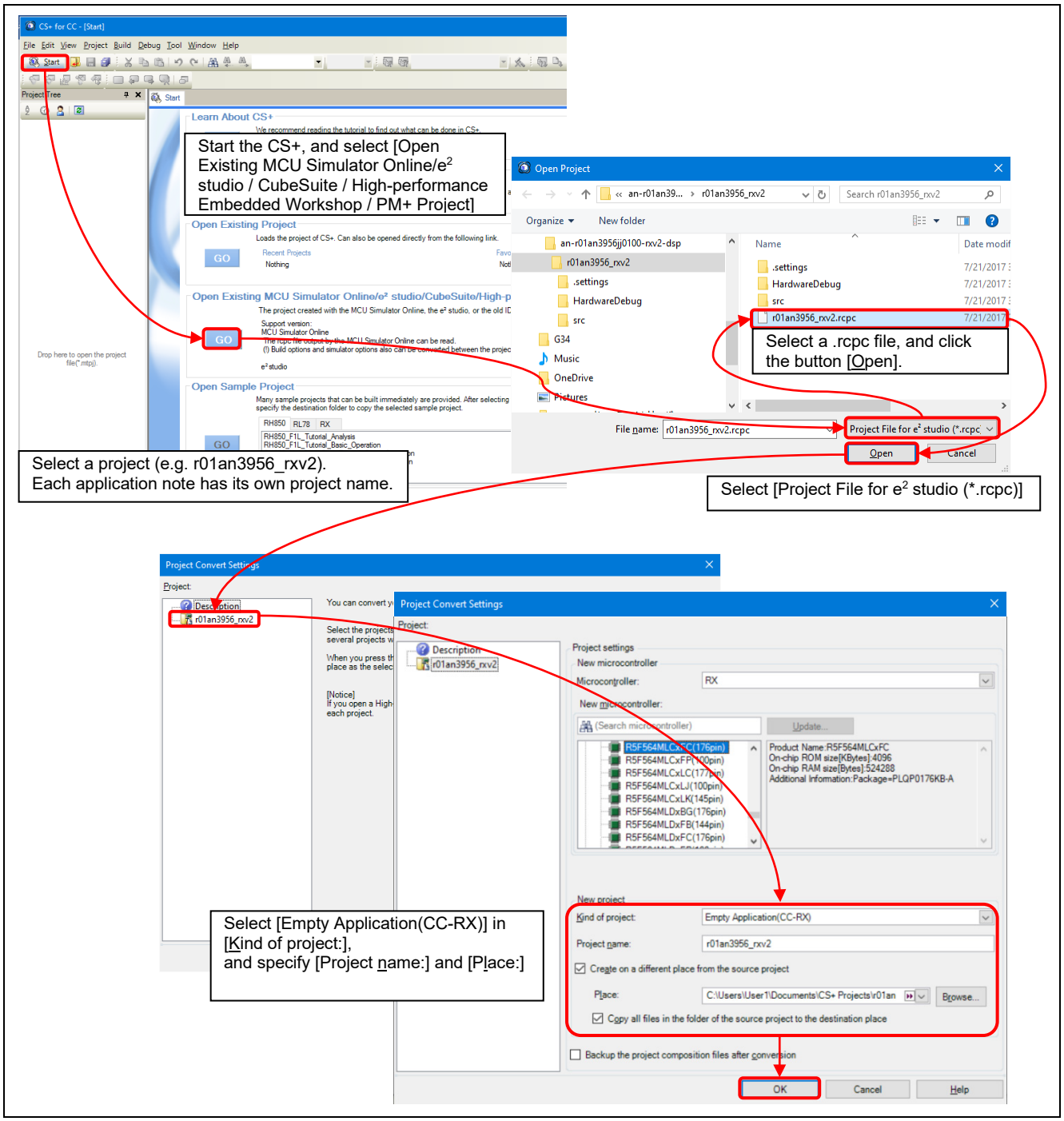


Figure 5.2 How to Import a Project into CS+

6. Reference Documents

- User's Manual: Hardware
  RX66T Group User's Manual: Hardware (R01UH0749)
  (The latest version can be downloaded from the Renesas Electronics website.)
- Technical Updates/Technical News
  (The latest version can be downloaded from the Renesas Electronics website.)
- User's Manual: Development Environment
  RX Family CC-RX Compiler User's Manual (R20UT3248)
  (The latest version can be downloaded from the Renesas Electronics website.)
- User's Manual: Development Environment
  RX66T Group Renesas Starter Kit User's Manual (R20UT4150)
  (The latest version can be downloaded from the Renesas Electronics website.)
- Application Note
  RX Family PWM Output Methods Using MTU3/GPTW (R01AN5995)
  (The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 16, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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