RX Family

Changes to Reset Status Registers when Resets Occur

Introduction

Multiple reset sources are defined on RX Family MCUs. When a reset occurs, the values of the reset status registers change according to the source. This application note describes the effect on the values of the reset status registers when multiple reset sources are generated at approximately the same time.

Unless otherwise specified, the descriptions in this application note apply to the RX65N-2MB.

Target Device

RX65N-2MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Overview

Multiple reset sources are defined on RX Family MCUs. When a reset occurs, the values of the reset status registers change according to the source.

This application note describes what happens when the following resets occur.

- Occurrence of power-on reset and RES# pin reset
- Occurrence of voltage-monitoring 0 reset
- Occurrence of voltage-monitoring 0 reset and power-on reset
- Occurrence of voltage-monitoring 0 reset and RES# pin reset
- Occurrence of watchdog timer reset and voltage-monitoring 0 reset
- Occurrence of watchdog timer reset and power-on reset
- Occurrence of watchdog timer reset and RES# pin reset

2. Operation Confirmation Environment

The operation described in this application note has been confirmed under the following conditions.

Table 2.1 Operation Confirmation Environment

Item	Description
MCU used	R5F565NEDDFC (RX65N Group)
Operating frequencies	• Main clock: 24 MHz • PLL: 240 MHz (main clock divided by 1 and multiplied by 10) • System clock (ICLK): 120 MHz (PLL divided by 2) • Peripheral module clock A (PCLKA): 120 MHz (PLL divided by 2) • Peripheral module clock B (PCLKB): 60 MHz (PLL divided by 4) • Peripheral module clock C (PCLKC): 60 MHz (PLL divided by 4) • Peripheral module clock D (PCLKD): 60 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics e^2 studio 2021-01
C compiler	Renesas Electronics C/C++ Compiler Package for RX Family V.3.03
	Compile option Default settings of integrated development environment
iodefine.h version	Version 2.30
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit+ for RX65N-2MB (product No.: RTK50565N2S80000BE)

3. Reset Status Registers when Resets Occur

The values of the reset status registers after resets in the seven cases listed in section 1. Overview, are described below.

3.1 Occurrence of Power-on Reset and RES# Pin Reset

3.1.1 Values of the registers

An example of occurrence of a power-on reset and RES# pin reset is shown in Figure 3.1.

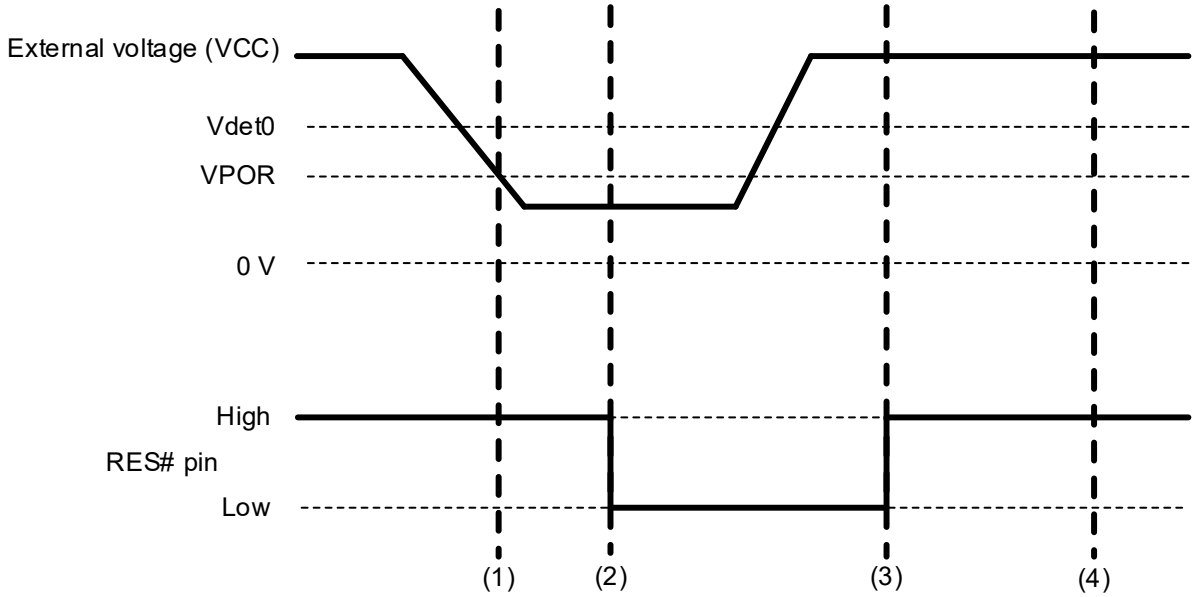

Figure 3.1 Example of Occurrence of Power-on Reset and RES# Pin Reset

(1) Power-on reset generation
(2) RES# pin low-level
(3) RES# pin high-level
(4) Reset release

Table 3.1 shows the values of the reset status registers following reset release (4).

Table 3.1 Register Values after Occurrence of Power-on Reset and RES# Pin Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	0
	LVD0RF	0
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	0
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.1.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.2 shows the list of targets to be initialized by power-on reset and RES# pin reset, excerpted from Table 6.2. of the user’s manual.

Table 3.2 Targets to be initialized by Power-on Reset and RES# Pin Reset

Targets to be Initialized	Reset Source	
	RES# Pin Reset	Power-On Reset
Power-on reset detect flag (RSTSR0.PORF)	✓	—
Cold start/warm start determination flag (RSTSR1.CWSF)	—	✓

✓: To be initialized. —: Not to be initialized.

When power-on reset and RES# pin reset occurred, Table 3.2 should be read as follows.

- RSTSR0.PORF a flag to detect power-on reset, is set to "0" due to initialization by RES# pin reset occurrence.
- RSTSR1.CWSF a flag to determine whether cold or warm start, is set to "0" due to initialization by power-on reset occurrence.

3.1.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When power-on reset and RES# pin reset occurred, the reset source is determined as shown in the Figure 3.2.

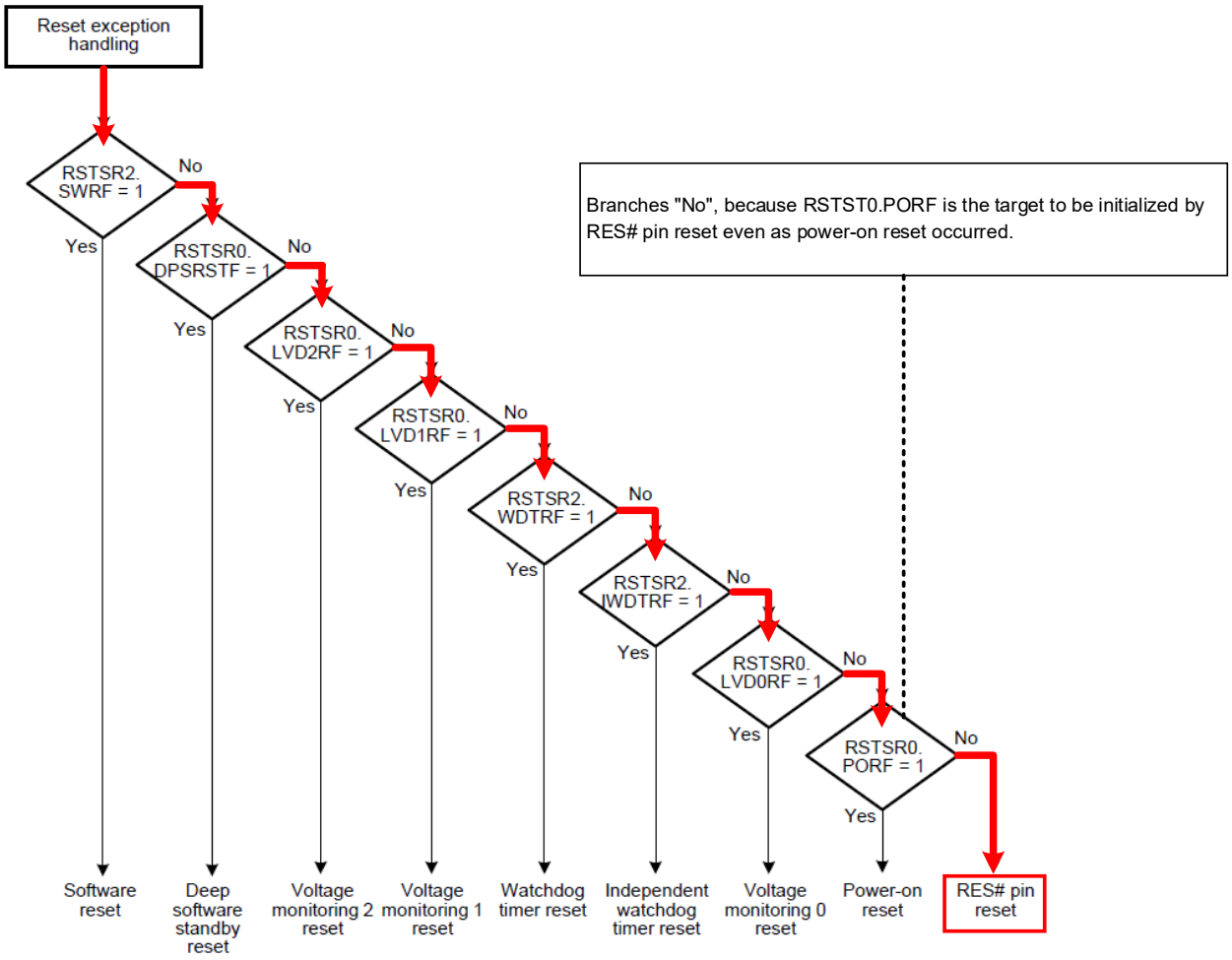

Figure 3.2 Reset Determination Flow when Power-on Reset and RES# Pin Reset Occurred

3.2 Occurrence of Voltage-Monitoring 0 Reset

3.2.1 Values of the registers

An example of occurrence of a voltage-monitoring 0 reset is shown in Figure 3.3.

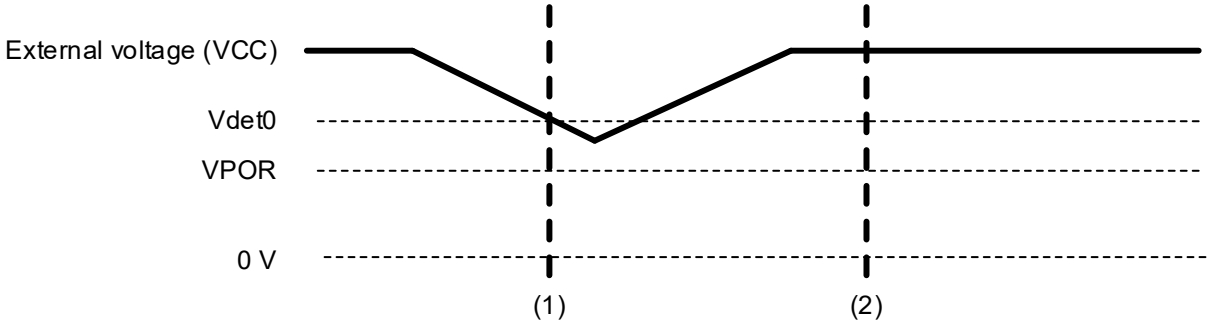

Figure 3.3 Example of Occurrence of Voltage-Monitoring 0 Reset

(1) Voltage-monitoring 0 reset generation
(2) Reset release

Table 3.3 shows the values of the reset status registers following reset release (2).

Table 3.3 Register Values after Occurrence of Voltage-Monitoring 0 Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	The value before the reset occurred.
	LVD0RF	1
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	The value before the reset occurred.
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.2.2 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When voltage-monitoring 0 reset occurred, the reset source is determined as shown in the Figure 3.4.

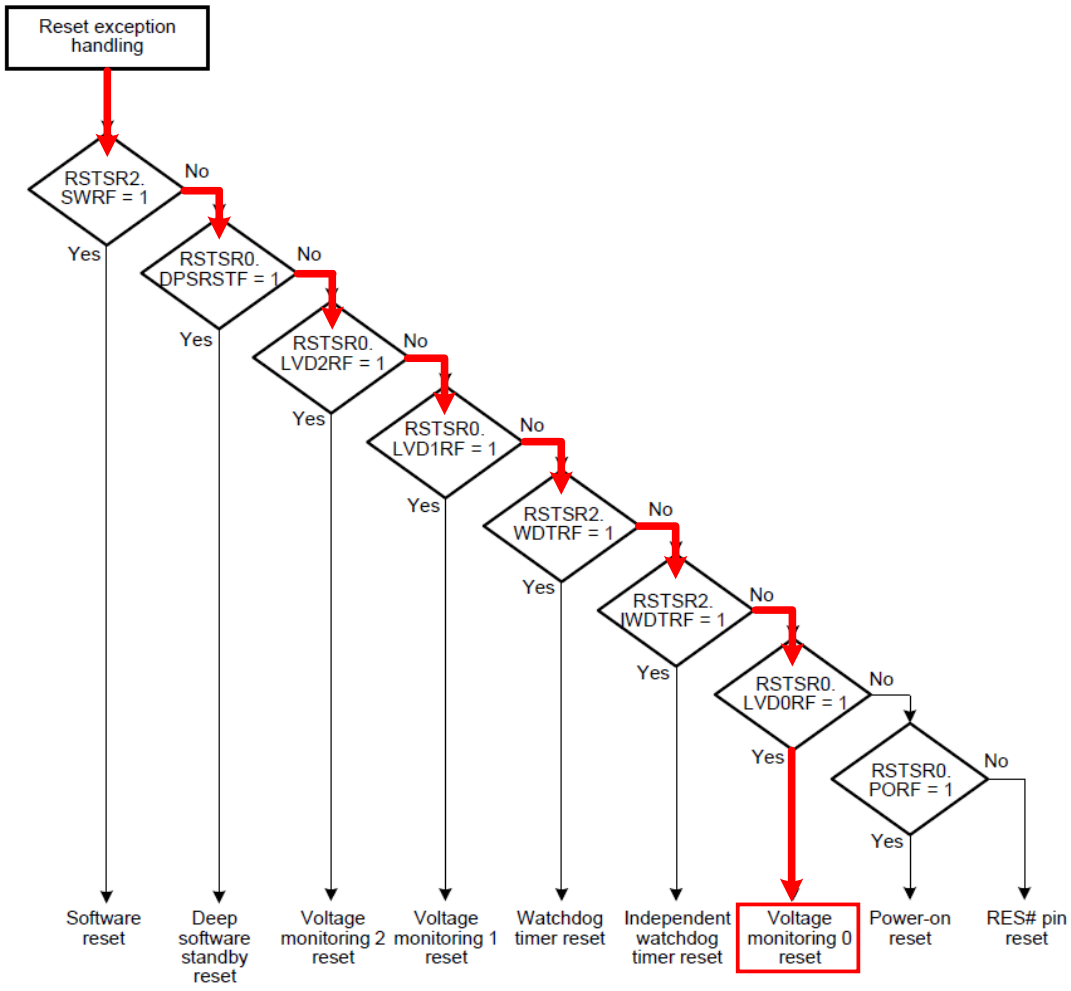

Figure 3.4 Reset Determination Flow when Voltage-Monitoring 0 Occurred

3.3 Occurrence of Voltage-Monitoring 0 Reset and Power-on Reset

3.3.1 Values of the registers

An example of occurrence of a voltage-monitoring 0 reset and power-on reset is shown in Figure 3.5.

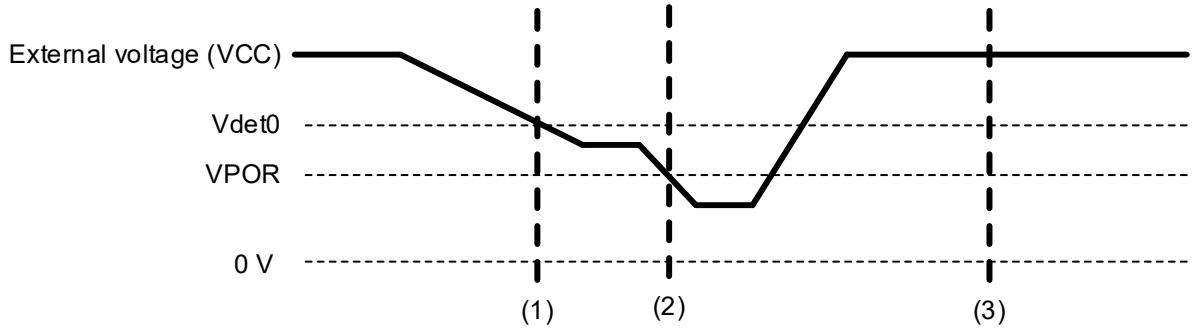

Figure 3.5 Example of Occurrence of Voltage-Monitoring 0 Reset and Power-on Reset

(1) Voltage-monitoring 0 reset generation
(2) Power-on reset generation
(3) Reset release

Table 3.4 shows the values of the reset status registers following reset release (3).

Table 3.4 Register Values after Occurrence of Voltage-Monitoring 0 Reset and Power-on Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	1
	LVD0RF	0
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	0
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.3.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.5 shows the list of targets to be initialized by voltage-monitoring 0 and power-on reset, excerpted from Table 6.2. of the user’s manual.

Table 3.5 Target to be initialized by Voltage-Monitoring 0 Reset and Power-on Reset

Targets to be Initialized	Reset Source	
	Power-On Reset	Voltage-Monitoring 0 Reset
Power-on reset detect flag (RSTSR0.PORF)	—	—
Voltage-monitoring 0 reset detect flag (RSTSR0.LVD0RF)	✓	—

✓: To be initialized. —: Not to be initialized.

When voltage-monitoring 0 reset and power-on reset occurred, Table 3.5 should be read as follows.

- RSTSR0.PORF is set to 1 due to power-on reset occurrence, not affected by voltage-monitoring 0 reset.
- RSTSR0.LVD0RF a flag to detect voltage-monitoring 0 reset, is set to 0 due to initialization by power-on reset occurrence.

3.3.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When voltage-monitoring 0 reset and power-on reset occurred, the reset source is determined as shown in the Figure 3.6.

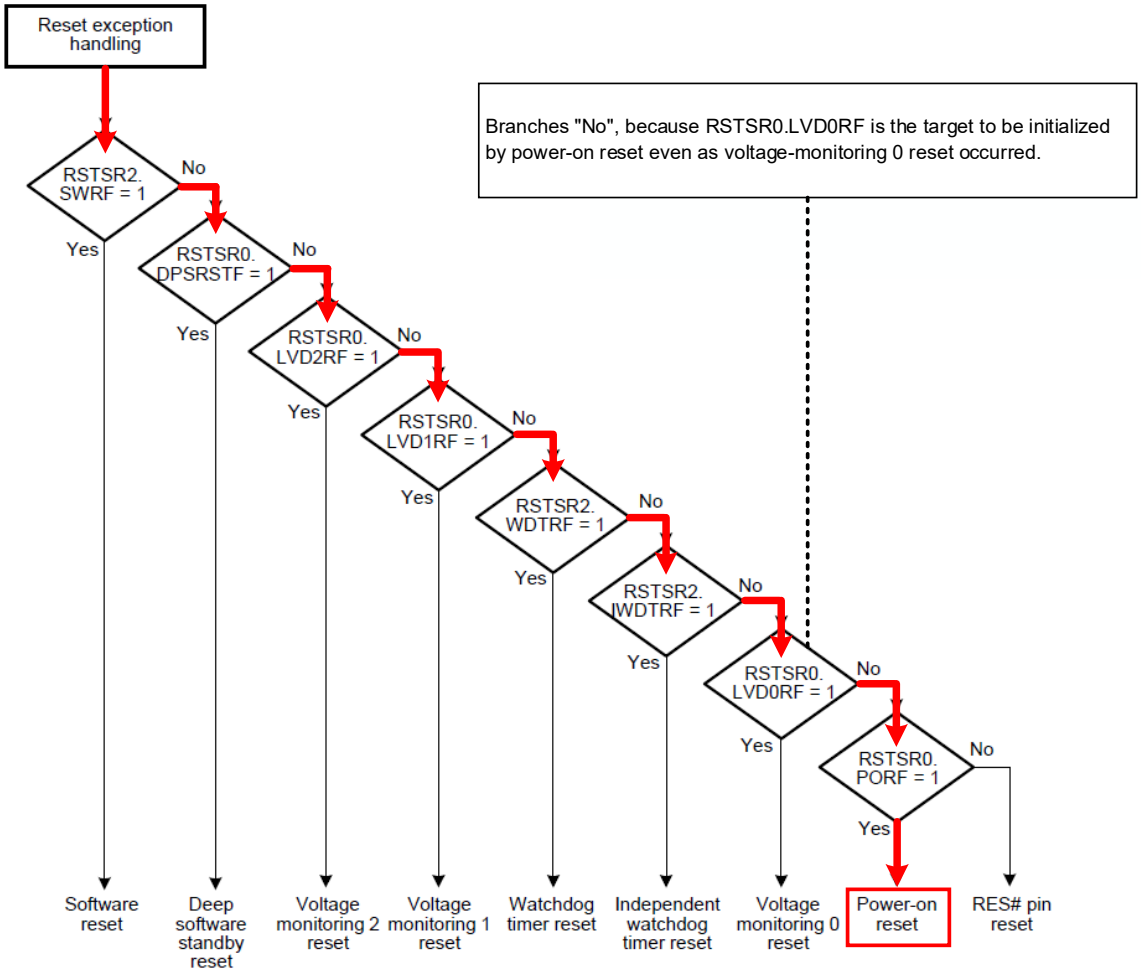

Figure 3.6 Reset Determination Flow when Voltage-Monitoring 0 Reset and Power-on Reset Occurred

3.4 Occurrence of Voltage-Monitoring 0 Reset and RES# Pin Reset

3.4.1 Values of the registers

An example of occurrence of a voltage-monitoring 0 reset and RES# pin reset is shown in Figure 3.7.

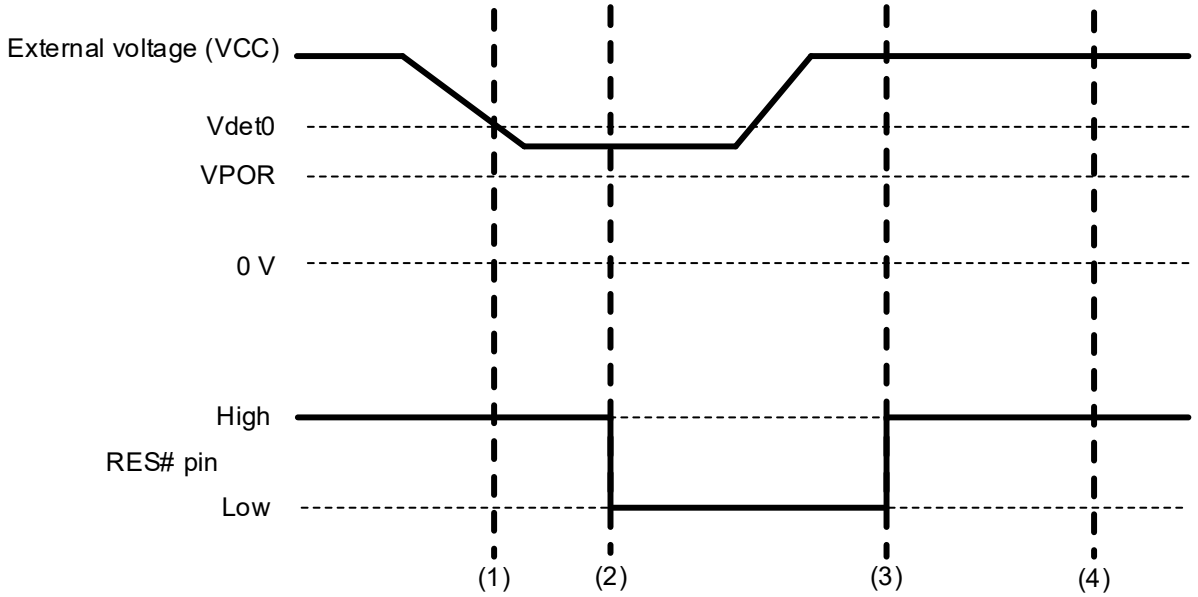

Figure 3.7 Example of Occurrence of Voltage-Monitoring 0 Reset and RES# Pin Reset

(1) Voltage-monitoring 0 reset generation
(2) RES# pin low-level
(3) RES# pin high-level
(4) Reset release

Table 3.6 shows the values of the reset status registers following reset release (4).

Table 3.6 Register Values after Occurrence of Voltage-Monitoring 0 Reset and RES# Pin Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	0
	LVD0RF	0
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	The value before the reset occurred.
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.4.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.7 shows the list of targets to be initialized by voltage-monitoring 0 reset and RES# pin reset, excerpted from Table 6.2 of the user’s manual.

Table 3.7 Targets to be initialized by Voltage-Monitoring 0 Reset and RES# Pin Reset

Targets to be Initialized	Reset Source	
	RES# Pin Reset	Voltage-Monitoring 0 Reset
Cold start/warm start determination flag (RSTSR1.CWSF)	—	—
Voltage-monitoring 0 reset detect flag (RSTSR0.LVD0RF)	✓	—

✓: To be initialized. —: Not to be initialized.

When voltage-monitoring 0 reset and RES# pin reset occurred, Table 3.7 should be read as follows.

- RSTSR1.CWSF keeps the value before the resets occurred, not affected by RES# pin reset and voltage-monitoring 0 reset.
- RSTSR0.LVD0RF a flag to detect voltage-monitoring 0, is set to 0 due to initialization by RES# pin reset occurrence.

3.4.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When voltage-monitoring 0 reset and RES# pin reset occurred, the reset source is determined as shown in the Figure 3.8.

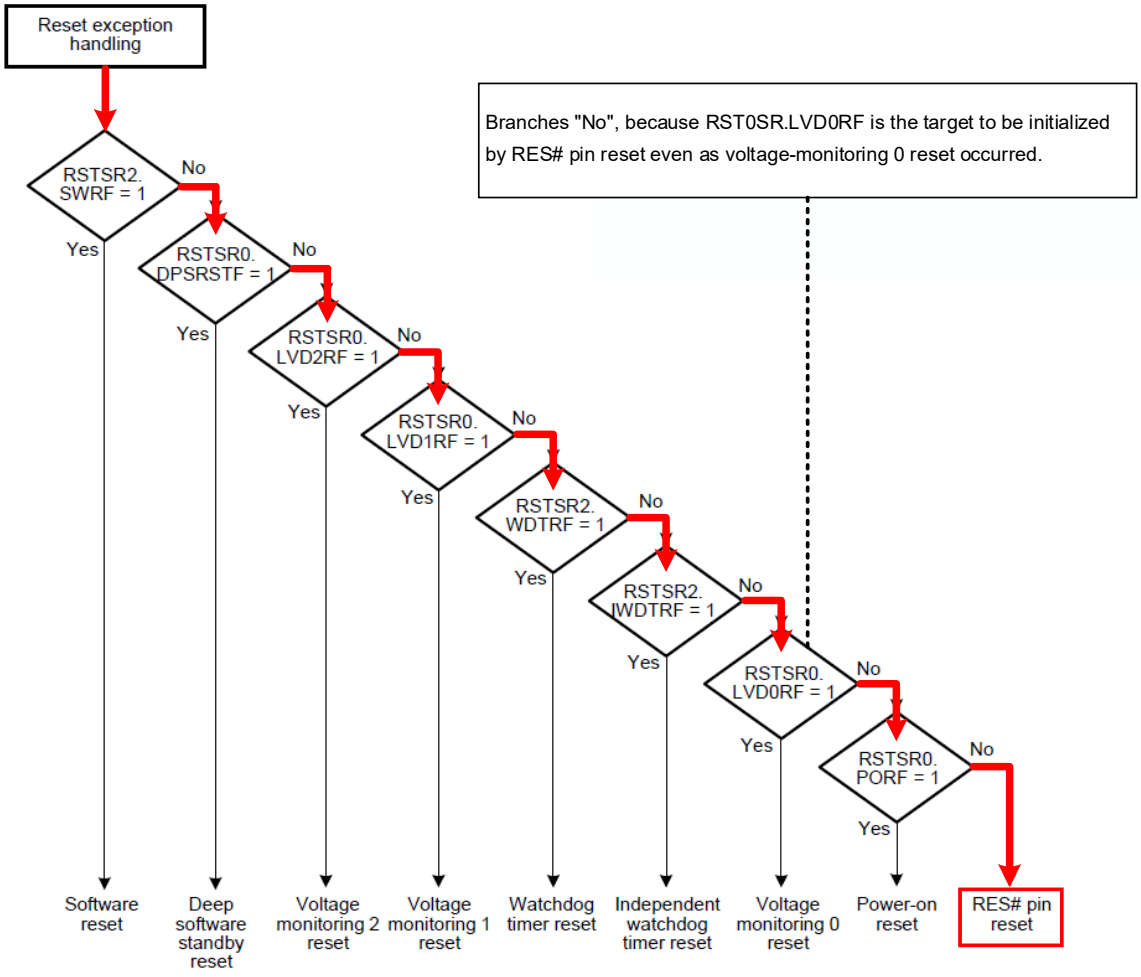

Figure 3.8 Reset Determination Flow when Voltage-Monitoring 0 Reset and RES# Pin Reset Occurred

3.5 Occurrence of Watchdog Timer Reset and Voltage-Monitoring 0 Reset

3.5.1 Values of the registers

An example of occurrence of a watchdog timer reset and voltage-monitoring 0 reset is shown in Figure 3.9.

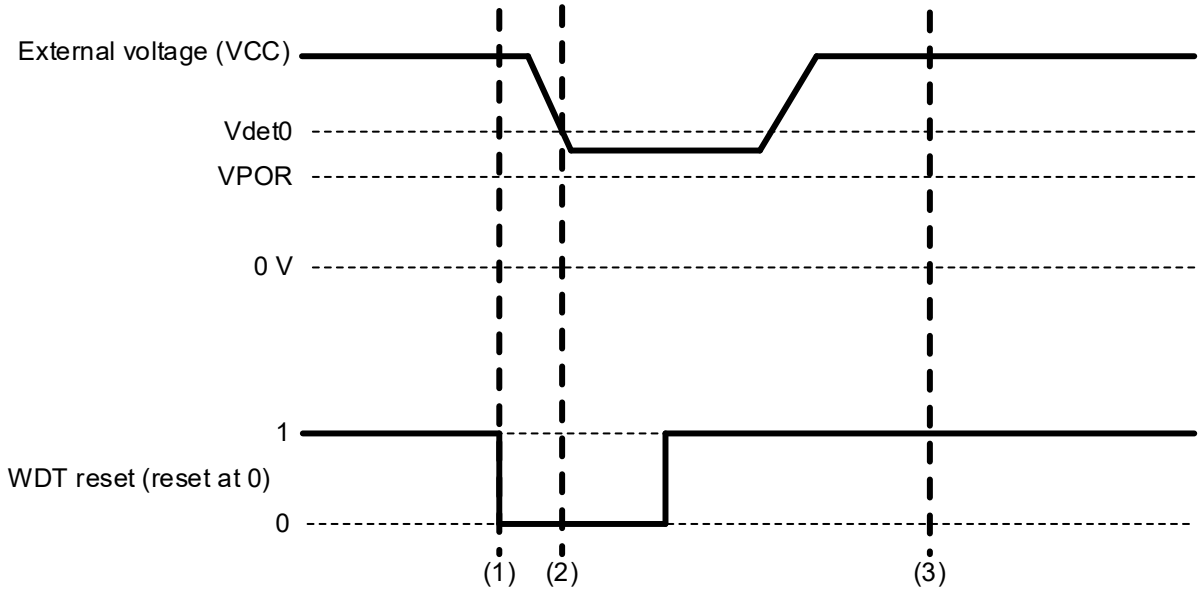

Figure 3.9 Example of Occurrence of Watchdog Timer Reset and Voltage-Monitoring 0 Reset

(1) Watchdog timer reset generation
(2) Voltage-monitoring 0 reset generation
(3) Reset release

Table 3.8 shows the values of the reset status registers following reset release (3).

Table 3.8 Register Values after Occurrence of Watchdog Timer Reset and Voltage-Monitoring 0 Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	The value before the reset occurred.
	LVD0RF	1
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	The value before the reset occurred.
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.5.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.9 shows the list of targets to be initialized by watchdog timer reset and voltage-monitoring 0 reset, excerpted from Table 6.2. of the user’s manual.

Table 3.9 Target to be initialized by Watchdog Timer Reset and Voltage-Monitoring 0 Reset

Targets to be Initialized	Reset Source	
	Voltage-Monitoring 0 Reset	Watchdog Timer Reset
Voltage-monitoring 0 reset detect flag (RSTSR0.LVD0RF)	—	—
Watchdog timer reset detect flag (RSTSR2.WDTRF)	✓	—

✓: To be initialized. —: Not to be initialized.

When watchdog timer reset and voltage-monitoring 0 reset occurred, Table 3.9 should be read as follows.

- RSTSR0.LVD0RF is set to 1 due to voltage-monitoring 0 reset occurrence, not affected by watchdog timer reset.
- RSTSR2.WDTRF a flag to detect watchdog timer reset, is set to 0 due to the initialization by voltage-monitoring 0 reset occurrence.

3.5.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When watchdog timer reset and voltage-monitoring 0 reset occurred, the reset source is determined as shown in the Figure 3.10.

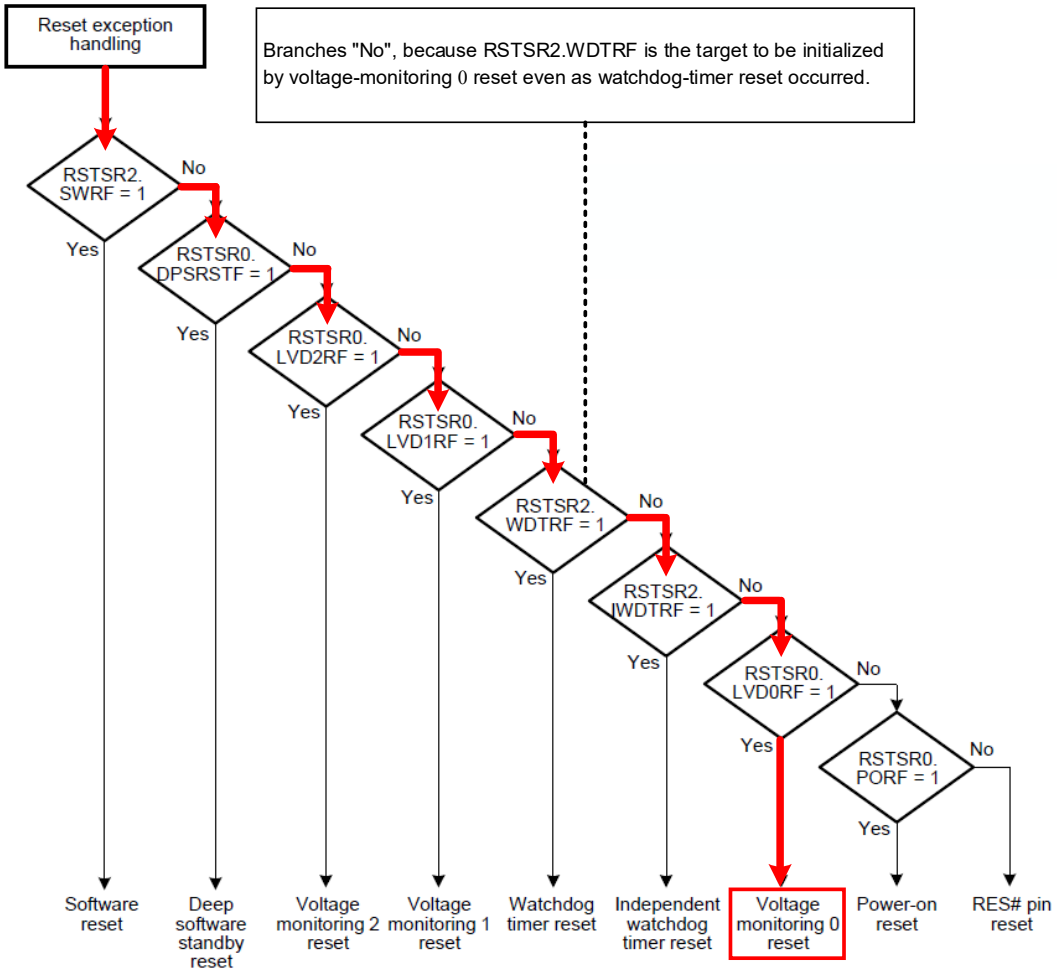

Figure 3.10 Reset Determination Flow when Watchdog Timer Reset and Voltage-Monitoring 0 Reset Occurred

3.6 Occurrence of Watchdog Timer Reset and Power-on Reset

3.6.1 Values of the registers

An example of occurrence of a watchdog timer reset and power-on reset is shown in Figure 3.11.

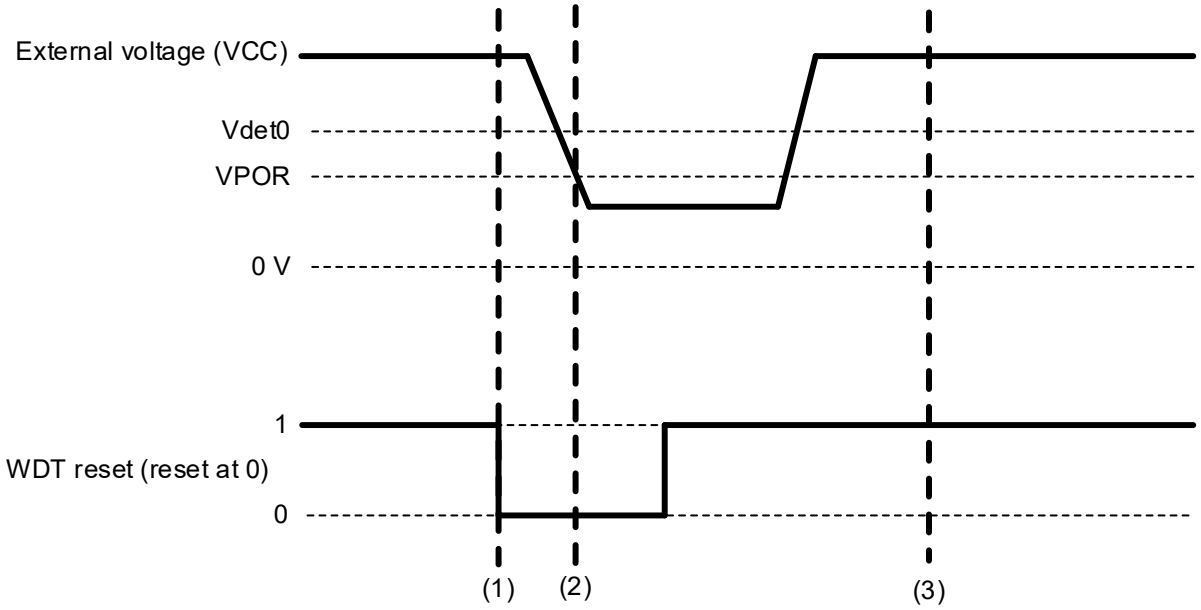

Figure 3.11 Example of Occurrence of Watchdog Timer Reset and Power-on Reset

(1) Watchdog timer reset generation
(2) Power-on reset generation
(3) Reset release

Table 3.10 shows the values of the reset status registers following reset release (3).

Table 3.10 Register Values after Occurrence of Watchdog Timer Reset and Power-on Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	1
	LVD0RF	0
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	0
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.6.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.11 shows the list of targets to be initialized by watchdog timer reset and power-on reset, excerpted from Table 6.2 of the user’s manual.

Table 3.11 Target to be initialized by Watchdog Timer Reset and Power-on Reset

Targets to be Initialized	Reset Source	
	Power-On Reset	Watchdog Timer Reset
Power-on reset detect flag (RSTSR0.PORF)	—	—
Watchdog timer reset detect flag (RSTSR2.WDTRF)	✓	—

✓: To be initialized. —: Not to be initialized.

When watchdog timer reset and power-on reset occurred, Table 3.11 should be read as follows.

- RSTSR0.PORF is set to 1 due to power-on reset occurrence, not affected by watchdog timer reset.
- RSTSR2.WDTRF a flag to detect watchdog timer reset, is set to 0 due to initialization by power-on reset.

3.6.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When watchdog timer reset and power-on reset occurred, the reset source is determined as shown in the Figure 3.12.

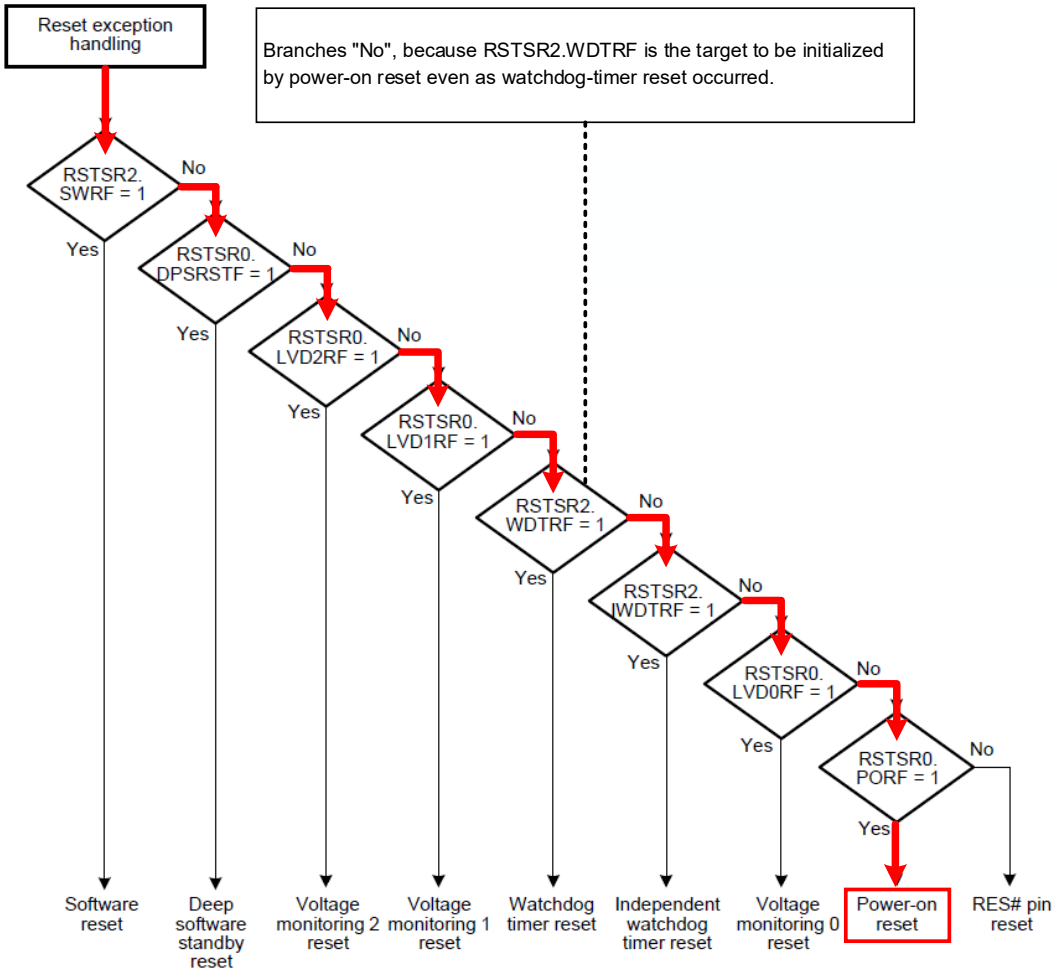

Figure 3.12 Reset Determination Flow when Watchdog Timer Reset and Power-on Reset Occurred

3.7 Occurrence of Watchdog Timer Reset and RES# Pin Reset

3.7.1 Values of the registers

An example of occurrence of a watchdog timer reset and RES# pin reset is shown in Figure 3.13.

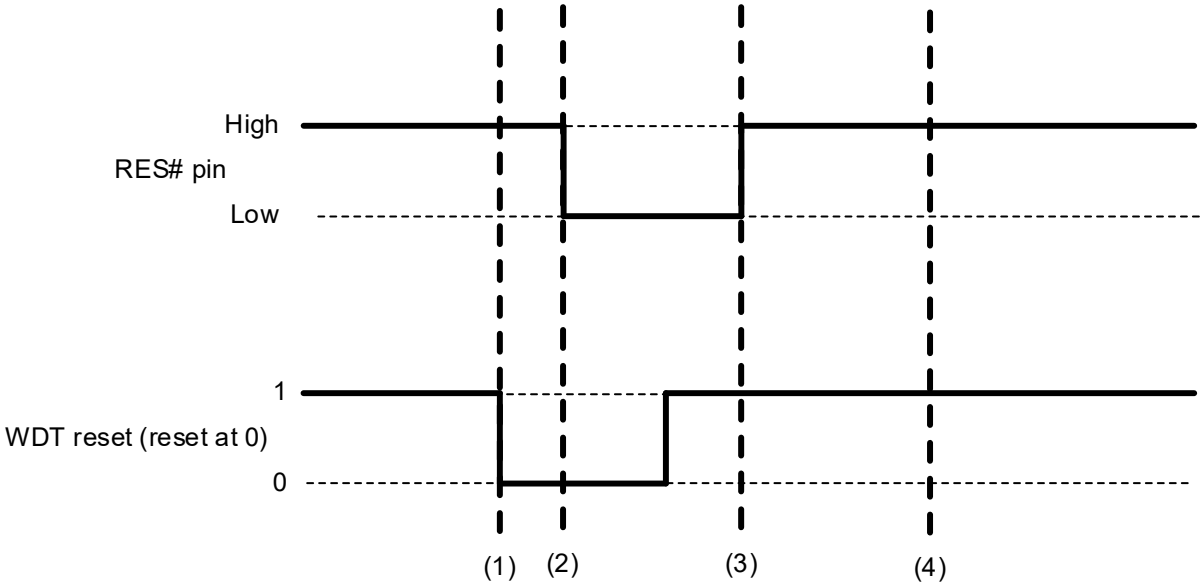

Figure 3.13 Example of Occurrence of Watchdog Timer Reset and RES# Pin Reset

(1) Watchdog timer reset generation
(2) RES# pin low-level
(3) RES# pin high-level
(4) Reset release

Table 3.12 shows the values of the reset status registers following reset release (4).

Table 3.12 Register Values after Occurrence of Watchdog Timer Reset and RES# Pin Reset

Register Name	Symbol Name	Bit Value
RSTSR0	PORF	0
	LVD0RF	0
	LVD1RF	0
	LVD2RF	0
	DPSRSTF	0
RSTSR1	CWSF	The value before the reset occurred.
RSTSR2	IWDTRF	0
	WDTRF	0
	SWRF	0

3.7.2 Description of changes of register values

This part describes changes of register values in reference to “Table 6.2 Targets to be Initialized by Each Reset Source” in from RX65N Group, RX651 Group User’s Manual: Hardware.

Table 3.13 shows the list of targets to be initialized by watchdog timer reset and RES# pin reset, excerpted from Table 6.2 of the user’s manual.

Table 3.13 Target to be initialized by Watchdog Timer Reset and RES# Pin Reset

Targets to be Initialized	Reset Source	
	RES# Pin Reset	Watchdog Timer Reset
Cold start/warm start determination flag (RSTSR1.CWSF)	—	—
Watchdog timer reset detect flag (RSTSR2.WDTRF)	✓	—

✓: To be initialized. —: Not to be initialized.

When watchdog timer reset and RES# pin reset occurred, Table 3.13 should be read as follows.

- RSTSR1.CWSF keeps the value before the resets occurred, not affected by RES# pin reset and watchdog timer reset.
- RSTSR2.WDTRF a flag to detect watchdog timer reset, is set to 0 due to initialization by RES# pin reset occurrence.

3.7.3 Determination of Reset Source

Reset source can be determined in reference to "Figure 6.4 Example of Reset Generation Source Determination Flow" in RX65N Group, RX651 Group User's Manual: Hardware.

When watchdog timer reset and RES# pin reset occurred, the reset source is determined as shown in the Figure 3.14.

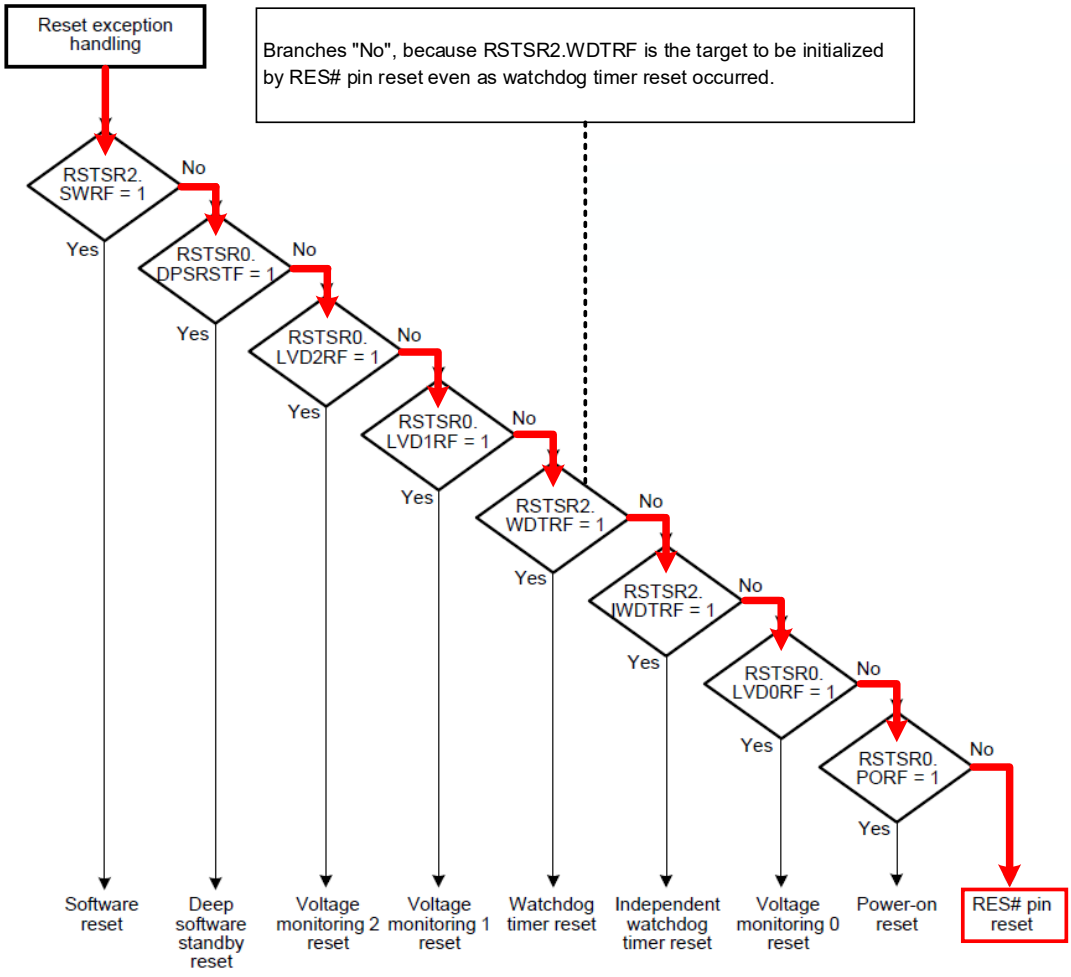

Figure 3.14 Reset Determination Flow when Watchdog Timer Reset and RES# Pin Reset Occurred

4. Reference Documents

User's Manual: Hardware
RX65N Group, RX651 Group User's Manual: Hardware (R01UH0590)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

User's Manual: Development environment
RX Family CC-RX Compiler User's Manual (R20UT3248)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 20, 2021	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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