RL78/L13

Low power consumption of LCD drive Using Voltage Detector (LVD)

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Abstract

Some battery-driven portable devices employ the internal voltage boosting method for generation of the LCD drive voltage in order to maintain the LCD quality. However, this method consumes larger power than the capacitor split method does, which is a problem to be solved.

This application note describes the method to achieve the excellent LCD quality and low power consumption of the system at the same time. In this method, the constant-period interrupt for updating the clock display and LVD are used to select the optimum LCD drive voltage generation method.

Products

RL78/L13

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

With this application, the value of the voltage detection flag LVIF is checked every second to select the optimum LCD drive voltage generation method. To generate an interrupt every second, the constant-period interrupt (INTRTC) of the real-time clock 2 (RTC2) is used.

When LVIF = 0 (supply voltage (V_{DD}) ≥ LVD detection voltage (V_{LVD})), the capacity split method is selected.

When LVIF = 1 (supply voltage (V_{DD}) < LVD detection voltage (V_{LVD})), the internal voltage boosting method is selected.

Table 1.1, figure 1.1, and figure 1.2 show the peripheral functions used and their applications, comparison of power consumption of LCD drive voltage generation methods, and timing of switching the LCD drive voltage generation method by supply voltage VDD, respectively.

Table 1.1 Peripheral Function and Their Applications

Peripheral Function	Application
Voltage Detector	Detection of power supply voltage (VDD)
Real-time Clock 2（RTC2） Note	• Counts the time • Generates periodic interrupt once per second
LCD controller/driver	Controls the LCD panel
12-bit interval timer (IT) Note	• Generates a 10 ms wait time to prevent switch chattering • Generates a 100 ms wait time for LCD drive voltage stabilization
External interrupt INTP0 Note	Detects input from the UP switch and increments the hours and minutes displayed on the LCD
External interrupt INTP7 Note	Detects input from the SET switch and enters hour setting mode or minute setting mode

Note For details on peripheral function settings, refer to the relevant application note and user's manual.

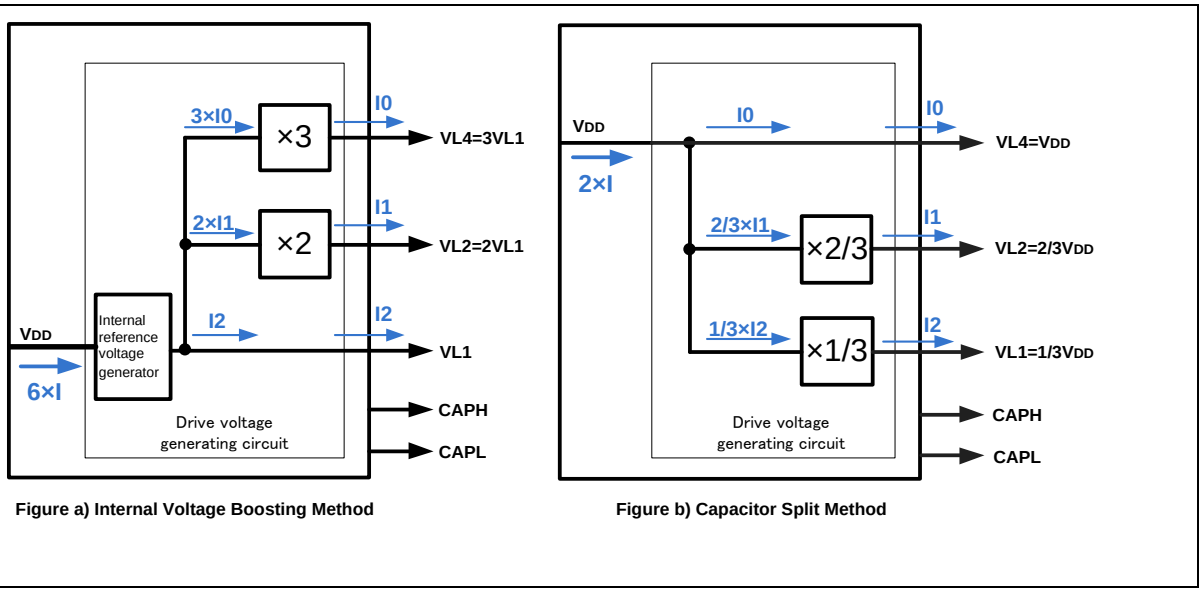

Figure a) Internal Voltage Boosting Method

Figure b) Capacitor Split Method

Figure 1.1 Comparison of power consumption of LCD drive voltage generation method

Assuming that the current flowing through the LCD panel is expressed as I0 = I1 = I2 = I (μA), the operating current of the drive voltage generation circuit in reference to the supply voltage VDD is expressed as follows:

a) Internal Voltage Boosting Method：$I\Sigma = 3\times I + 2\times I + I = 6I$

b) Capacitor Split Method：$I\Sigma = I + 2/3\times I + 1/3\times I = 2I$

In conclusion, the operating current for the internal voltage boosting method is three times that for the capacitor split method.

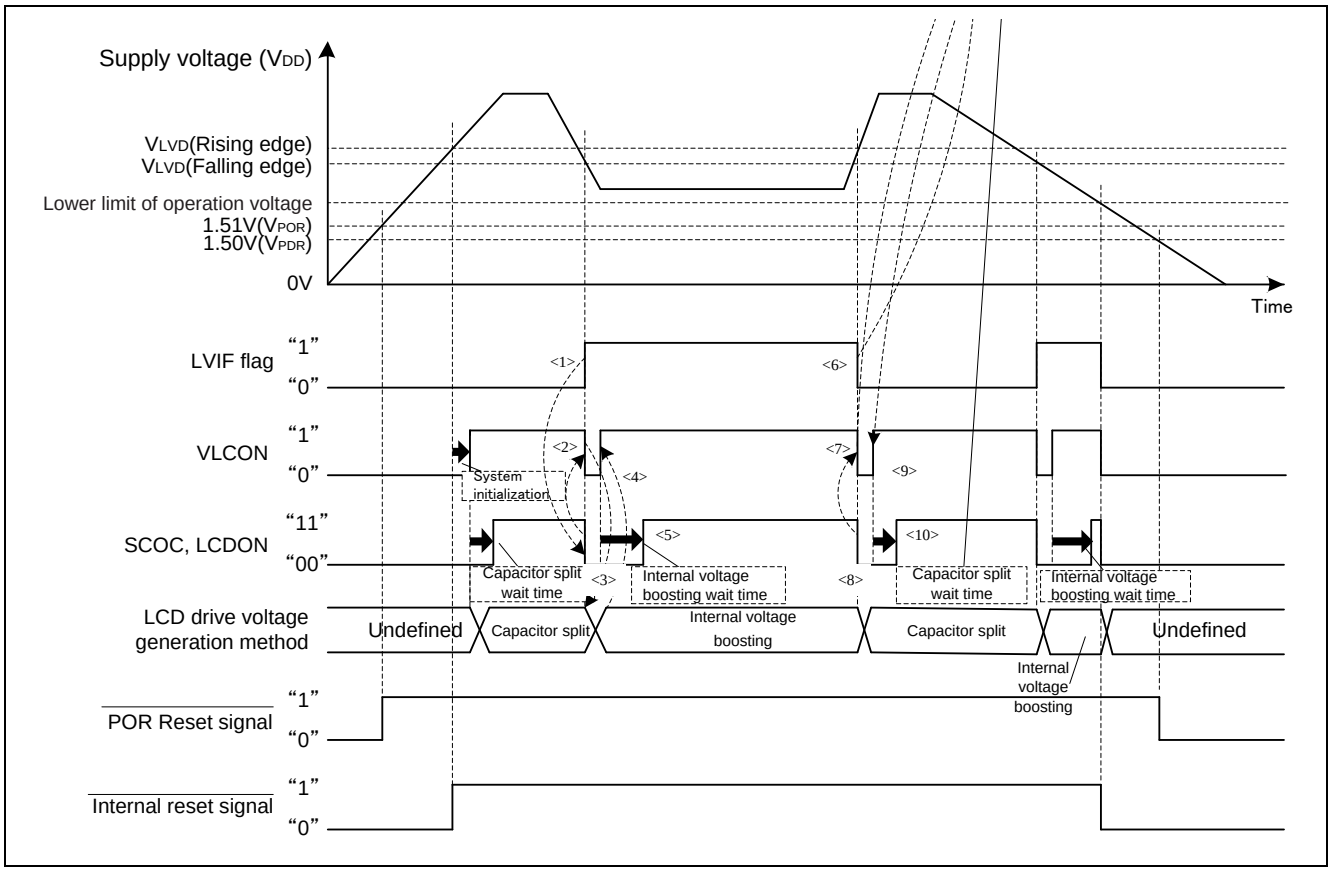

Figure 1.2 Timing of switching the LCD drive voltage generation method by supply voltage VDD

<1> When the supply voltage (V_{DD}) drops below the detection voltage (V_{LVD}), the voltage detection flag LVIF is automatically set to 1, and the ground level is output to the segment/common pins (SCOC = 0, LCDON = 0).

<2> Setting the VLCON bit to 0 stops the operation of the drive voltage generator of the capacitor split method.

<3> The LCD drive voltage generation method is switched from the capacitor split method to the internal voltage boosting method.

<4> Setting the VLCON bit to 1 enables the operation of the internal voltage boost circuit and the suitable drive voltage for the LCD display is generated (the internal reference voltage is assumed to have been stabilized here).

<5> After waiting for 500-ms (wait time after the start of boosting by the internal voltage boosting method until the display operation becomes possible) or longer delay time, setting SCOC and LCDON to 1 enables LCD display.

<6> When the supply voltage (V_{DD}) rises to or above the detection voltage (V_{LVD}), the voltage detection flag LVIF is automatically set to 0, and the ground level is output to the segment/common pins (SCOC = 0, LCDON = 0).

<7> Setting the VLCON bit to 0 stops the operation of the drive voltage generator of the internal voltage boosting method.

<8> The LCD drive voltage generation method is switched from the internal voltage boosting method to the capacitor split method.

<9> Setting the VLCON bit to 1 enables the operation of the capacitor split circuit and the suitable drive voltage for the LCD display is generated.

<10> After waiting for 100-ms (wait time after the start of stepping down the voltage by the capacitor split method until the display operation becomes possible) or longer delay time, setting SCOC and LCDON to 1 enables LCD display.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/L13（R5F10WMGA）
Operating frequencies	• High-speed on-chip oscillator clock (f_{HOCO}) : 4MHz • CPU/peripheral hardware clock (f_{CLK}):1MHz • RTC/IT/LCD operating clock (f_{SUB}):32.768kHz
Operating voltage	1.6V~3.0V（operation possible from 1.6V～5.5V） LVD operation (V_{LVD}) in Interrupt Mode is 2.50V at the rising edge or 2.45V at the falling edge.
Integrated development environment(CS+)	CS+ for CC V6.01.00 from Renesas Electronics Corp.
C compiler(CS+)	CC-RL V1.06.00 from Renesas Electronics Corp.
Integrated development environment(e^2studio)	e2studio V5.4.0.018 from Renesas Electronics Corp.
C compiler(e^2studio)	CC-RL V1.06.00 from Renesas Electronics Corp.
RL78/L13 code library	RL78/L13 code library V1.04.01.02 from Renesas Electronics Corp.
Board used	Original

3. Related application notes

- 24-Hour Clock Displayed on an LCD CC-RL（R01AN3135J）Application note

4. Hardware

4.1 Hardware Example

Figure 4.1 shows the hardware configuration used in this application note.

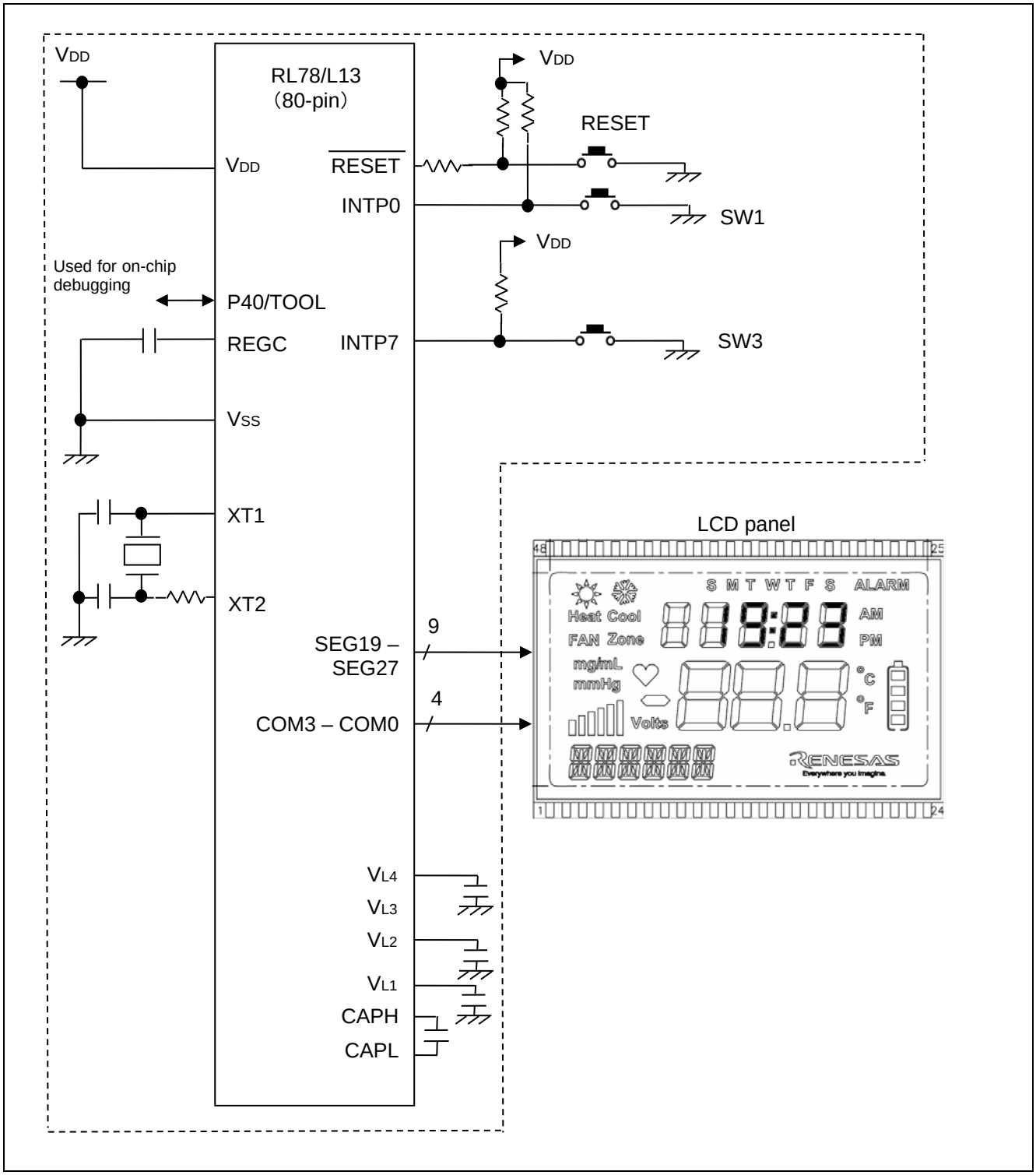

Figure 4.1 Hardware Configuration

Notes 1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either VDD or VSS via resistors).

2. Make sure to set VDD greater than the detection voltage (VLVD) specified by the LVD.

4.2 Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P137/INTP0	Input	Detects input from the UP switch and increments hours and minutes displayed on the LCD
P02/INTP7		Detects input from the SET switch and enters hour setting mode or minute setting mode
P30/SEG20	Output	LCD controller/driver segment signals
P31/SEG21		
P32/SEG22		
P33/SEG23		
P34/SEG24		
P35/SEG25		
P46/SEG26		
P47/SEG27		
P77/SEG19		
COM0	Output	LCD controller/driver common signals
COM1		
COM2		
COM3		

5. Software

5.1 Operation Overview

This section describes the sample code attached to this application note.

The sample code makes the following initial settings.

- Voltage detector
- Real-time clock 2 (RTC2)
- 12-bit interval timer
- LCD controller/driver
- External interrupts INTP0 and INTP7

After completion of the initial settings, the RTC2 is started and the system enters STOP mode. The system returns from STOP mode upon occurrence of the constant-period interrupt generated every second. The LVIF flag is checked and either internal boosting method or capacitor split method is selected.

The sample code is described in detail below.

1. Makes the initial settings for the voltage detector.
<Conditions for setting>

- At power-on or after reset release, sets the option bytes to set the LVD to interrupt mode.
- To maintain the LCD display quality, sets the rising edge detection voltage to 2.50 V and falling edge detection voltage to 2.45 V.

2. Makes the initial settings for the real-time clock 2 (RTC2).
<Conditions for setting>

- Selects the subsystem clock (f_{SUB}) as the operation clock for the RTC2.
- Selects the 24-hour system.
- Selects “once per second” for the constant-period interrupt.
- Makes the initial setting for the time to year 2018, month 1, day 1, hour 00, minute 00, and second 00.
- Enables the INTRTC interrupt.

3. Makes the initial settings for the 12-bit interval timer.
<Conditions for setting>

- Selects the subsystem clock (f_{SUB}) as the operation clock for the 12-bit interval timer.
- Disables the INTIT interrupt.
- Sets the interval time:

Interval time	Function
10ms	Generates a 10 ms wait time to prevent switch chattering
100ms	Generates a 100 ms wait time for LCD drive voltage stabilization

4. Makes the initial settings for the LCD controller/driver.
   <Conditions for setting>
   - Selects the capacitor split method for the LCD drive voltage generator.
   - Sets the LCD display mode to 4-time slice, 1/3 bias method, and waveform A.
   - Sets the LCD display data area control mode in which A-pattern and B-pattern area data are alternately displayed.
   - Sets the LCD clock frequency to 256 Hz, resulting in 64-Hz LCD frame frequency.
   - Sets the LCD reference voltage to1.00 V.

5. Makes the initial settings for the external interrupts INTP0 and INTP7.
   <Conditions for setting>
   - Enables the falling edge.
   - Enables the INTP7 interrupt.

6. After completion of the initial settings, the MCU enters STOP mode, and waits for the RTC constant-period interrupt or external interrupt INTP7 to occur.

7. After releasing STOP mode, identifies the interrupt source and performs the appropriate process according to the interrupt.
   When the interrupt source is the RTC, reads the LVIF flag and the currently selected LCD drive voltage generation method and selects the appropriate LCD drive voltage generation method. Then changes the time display on the LCD panel, and shifts to STOP mode.
   When the interrupt source is the INTP7, enters hour and minute setting mode.
   In the time setting mode, advances the time every time the INTP0 interrupt occurs, and shifts to STOP mode after that.

Caution: For details of the clock operation, refer to the application note, 24-Hour Clock Displayed on an LCD CC-RL （R01AN3135J）

5.2 Option Byte Settings

Table 5.1 lists the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	01101110B	Stops the watchdog timer (counting is stopped when a reset is released)
000C1H/010C1H	01011101B	Sets the LVD in reset mode • V_{LVD}（ rising edge ） ：2.50V • V_{LVD}（ falling edge ） ：2.45V
000C2H/010C2H	00101011B	Sets the high-speed on-chip oscillator clock to 4MHz in LV (low voltage main) mode
000C3H/010C3H	10000100B	Enables on-chip debugging

5.3 Constants

Table 5.2 lists the constants used in the sample code.

Table 5.2 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
LCD_POSITION_HOUR_HIGH _ABCD_SYMBOL	&SEG26	LCD display data address (tens place of hours symbol A,B,C,D)
LCD_POSITION_HOUR_HIGH _EFG_SYMBOL	&SEG27	LCD display data address (tens place of hours symbol E,F,G)
LCD_POSITION_HOUR_LOW _ABCD_SYMBOL	&SEG24	LCD display data address (ones place of hours symbol A,B,C,D)
LCD_POSITION_HOUR_LOW _EFG_SYMBOL	&SEG25	LCD display data address (ones place of hours symbol E,F,G)
LCD_POSITION_COLON	&SEG23	LCD display data address (colon)
LCD_POSITION_MINUTE_HIGH _ABCD_SYMBOL	&SEG21	LCD display data address (tens place of minutes symbol A,B,C,D)
LCD_POSITION_MINUTE_HIGH _EFG_SYMBOL	&SEG22	LCD display data address (tens place of minutes symbol E,F,G)
LCD_POSITION_MINUTE_LOW _ABCD_SYMBOL	&SEG19	LCD display data address (ones place of minutes symbol A,B,C,D)
LCD_POSITION_MINUTE_LOW _EFG_SYMBOL	&SEG20	LCD display data address (ones place of minutes symbol E,F,G)
LCD_DATA_0	0x0A0F	LCD display data (0)
LCD_DATA_1	0x0006	LCD display data (1)
LCD_DATA_2	0x060D	LCD display data (2)
LCD_DATA_3	0x040F	LCD display data (3)
LCD_DATA_4	0x0C06	LCD display data (4)
LCD_DATA_5	0x0C0B	LCD display data (5)
LCD_DATA_6	0x0E0B	LCD display data (6)
LCD_DATA_7	0x080E	LCD display data (7)
LCD_DATA_8	0x0E0F	LCD display data (8)
LCD_DATA_9	0x0C0F	LCD display data (9)
LCD_DATA_COLON	0x02	LCD display data (colon)
LCD_DATA_NONE	0x0000	LCD display data ( ) no display data
INTERRUPT_OFF	0x00	Interrupt request is not generated
INTRC_ON	0x01	RTC constant-period interrupt request is generated
INTPN_ON	0x02	External interrupt (INTPn: n = 0, 7) request is generated
LCD_NUM_DATA_SIZE	0x02	Byte size of the LCD numeric data
LCD_COLON_DATA_SIZE	0x01	Byte size of colon data
LCD_NUM_DATA_FONT_COUNT	0x0C	Number of fonts of LCD numeric data, “, (comma)” and “: (colon)” in total: 12
LCD_DATA_NONE_INDEX	0x0A	LCD data ‘ (space)’ g_FontData index
LCD_DATA_COLON_INDEX	0x0B	LCD data ‘: (colon)’ g_FontData index
WATCH_DISPLAY	0x00	Clock display mode
HOUR_ADJUST	0x01	Hour setting mode
MINUTE_ADJUST	0x02	Minute setting mode
SET_SWITCH_ON	0x01	SET switch is ON
UP_SWITCH_ON	0x02	UP switch is ON
SWITCH_ALL_OFF	0x00	Switches are OFF
LCD_DISPLAY_NORMAL	0x00	LCD display mode (normal mode)

LCD_DISPLAY_BLINK	0x01	LCD display mode (blinking)
_0147_ITMCMP_VALUE_10MS	0x0147U	For setting 10-ms interval time
_0CCC_ITMCMP_VALUE_100MS	0x0CCCU	For setting 100-ms interval time
_5_INTERNAL_VOLTAGE_BOOST_WAIT	0x05U	For setting the internal voltage boost circuit stabilization wait time (0x05U*100 ms)
_1_CAPACITOR_SPLIT_WAIT	0x01U	For setting the capacitor split circuit stabilization wait time (0x01U*100 ms)

5.4 Variables

Table 5.3 lists the static variables.

Table 5.3 static Variables

Type	Variable Name	Contents	Function Used
uint16_t	g_font_data[LCD_NUM_DATA_FONT_COUNT]	LCD font data • Array index is numeric data • g_font_data[10] is ‘ (space)’ data g_font_data[11] is ‘: (colon)’ data	r_main_lcd_hour_blink、 r_main_lcd_minute_blink、 r_main_lcd_display_normal
uint8_t	g_watch_status	Clock status variable	R_MAIN_UserInit、 r_main_set_switch_process、 r_main_up_switch_process、 r_main_lcd_display_time
uint8_t	g_hour	Clock hour data	main、 R_MAIN_UserInit、 r_main_set_switch_process、 r_main_up_switch_process、 r_main_lcd_hour_blink、 r_main_lcd_minute_blink、 r_main_lcd_display_normal
uint8_t	g_minute	Clock minute data	main、 R_MAIN_UserInit、 r_main_set_switch_process、 r_main_up_switch_process、 r_main_lcd_hour_blink、 r_main_lcd_minute_blink、 r_main_lcd_display_normal
uint8_t	g_lcd_blink	LCD display status variable	R_MAIN_UserInit、 r_main_set_switch_process、 r_main_lcd_display_time

5.5 Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Outline
R_MAIN_UserInit[Note]	User application initialization
R_LCD_Stop[Note]	LCD display stop processing
R_LCD_Voltage_Off[Note]	Output ground level to segment/common pin
R_LCD_Voltage_On[Note]	LCD voltage boost circuit operation start processing
r_it_operation_start	IT operation start processing
r_it_operation_stop	IT operation stop processing
R_INTCn_Start[Note]	INTPn operation start processing (n = 0, 7)
R_RTC_Get_CounterValue[Note]	RTC read (SEC to YEAR)
r_main_analyze_switch	Switch analysis
r_main_command_analyze	Command analysis
r_main_lcd_display_time	LCD time display
r_main_lcd_hour_blink	Set hour blinking data in the LCD display data register
r_main_lcd_minute_blink	Set minute blinking data in the LCD display data register
r_main_lcd_display_normal	Set normal display data in the LCD display data register
R_LCD_Start[Note]	LCD display start processing
R_RTC_Set_ConstPeriodInterruptOn[Note]	RTC constant-period interrupt enable
r_rtc_operation_start	RTC operation start processing
R_RTC_Start[Note]	RTC counter operation start processing
r_main_get_interrupt	Interrupt source retrieval
r_main_get_switch_status	Switch status retrieval
r_main_set_switch_process	Processing when pressing the SET switch
r_main_up_switch_process	Processing when pressing the UP switch
R_INTCn_Stop[Note]	NTPn operation stop processing (n = 0, 7)
R_RTC_Set_CounterValue[Note]	RTC write (SEC to YEAR)
r_main_bcd_inc	Addition processing of BCD data
r_rtc_set_counter_value_hour_min	Write minute and hour data to the RTC
R_IT_Start[Note]	IT counter operation start processing
R_IT_Stop[Note]	IT counter operation stop processing
r_main_seg_data_set	Set display data in the LCD display data register

Note These functions are automatically generated by the integrated development environment.

5.6 Function Specifications

The following tables list the sample code function specifications.

R_MAIN_UserInit

Outline	User application initialization	
Header	None	
Declaration	void R_MAIN_UserInit(void)	
Description	Initializes the peripheral functions necessary for using application.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_LCD_Stop

Outline	LCD display start processing (all segment outputs are deselected.)	
Header	r_cg_lcd.h	
Declaration	void R_LCD_Stop(void)	
Description	LCD display disable（LCDON = 0）	
Arguments	None	
Return Value	None	
Remarks	None	

R_LCD_Voltage_Off

Outline	LCD voltage boost circuit operation start processing (Output ground level to segment/common pin)	
Header	r_cg_lcd.h	
Declaration	void R_LCD_Voltage_Off(void)	
Description	LCD display stop processing(VLCON = 0, SCOC=0)	
Arguments	None	None
Return Value	None	
Remarks	None	

R_LCD_Voltage_On

Outline	LCD voltage boost circuit operation start processing	
Header	r_cg_lcd.h	
Declaration	void R_LCD_Voltage_On(void)	
Description	Starts the LCD voltage boost circuit operation (VLCON bit = 1).	
Arguments	None	None
Return Value	None	
Remarks	None	

R_LCD_Start

Outline	LCD display start processing	
Header	r_cg_lcd.h	
Declaration	void R_LCD_Start(void)	
Description	Enables the LCD display (LCDON bit = 1).	
Arguments	None	None
Return Value	None	
Remarks	None	

R_INTCn_Start (n=0,7)

Outline	INTPn operation start processing (n = 0, 7)	
Header	r_cg_intc_h	
Declaration	void R_INTCn_Start(void) (n = 0, 7)	
Description	Clears the INTPn interrupt request flag before enabling the interrupt.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_RTC_Set_ConstPeriodInterruptOn

Outline	RTC constant-period interrupt enable	
Header	r_cg_rtc.h	
Declaration	MD_STATUS R_RTC_Set_ConstPeriodInterruptOn(rtc_int_period_t period)	
Description	Enables the interrupt after setting the RTC constant-period interrupt.	
Arguments	rtc_int_period_t period	rtc_int_period_t period
Return Value	MD_OK: Normal end	
	MD_ARGERROR: Specified argument is invalid	
Remarks	None	

r_rtc_operation_start

Outline	RTC operation start processing	
Header	r_cg_rtc.h	
Declaration	void r_rtc_operation_start(void)	
Description	After the RTC starts counter operation, the program performs processing to enter STOP mode after the RTC is started.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_RTC_Start

Outline	RTC counter operation start processing	
Header	r_cg_rtc.h	
Declaration	void R_RTC_Start(void)	
Description	Clears the interrupt request flag, enables the interrupt, and starts the RTC counter operation and waits until the RTC starts.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_get_interrupt

Outline	Interrupt source retrieval	
Header	r_cg_userdefine.h	
Declaration	uint8_t r_main_get_interrupt (void)	
Description	Returns an interrupt with an interrupt request flag.	
Arguments	None	None
Return Value	INTERRUPT_OFF: Interrupt request is not generated	
	INTRC_ON: RTC constant-period interrupt request is generated	
	INTPN_ON: External interrupt (INTPn: n = 0, 7) request is generated	
Remarks	None	

R_RTC_Get_CounterValue

Outline	RTC read (SEC to YEAR)	
Header	r_cg_rtc.h	
Declaration	MD_STATUS R_RTC_Get_CounterValue(rtc_counter_value_t *const counter_read_val)	
Description	Reads the RTC counter values (SEC to YEAR).	
Arguments	rtc_counter_value_t* const counter_read_val	rtc_counter_value_t* const counter_read_val
Return Value	● MD_OK: Normal end ● MD_BUSY1: Executing the count processing (before reading) ● MD_BUSY2: Executing the count processing (after reading)	
Remarks	None	

r_main_analyze_switch

Outline	Switch analysis	
Header	r_cg_userdefine.h	
Declaration	void r_main_analyze_switch(void)	
Description	Waits to prevent switch chattering and retrieves the status of the switch. When the program detects that a switch has been pressed, the program jumps to each switch processing.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_get_switch_status

Outline	Switch status retrieval
Header	r_cg_userdefine.h
Declaration	uint8_t r_main_get_switch_status(void)
Description	Retrieves the status of the switch which has been pressed.
Arguments	None
Return Value	SWITCH_ALL_OFF: Switches are OFF SET_SWITCH_ON: SET switch is ON UP_SWITCH_ON: UP switch is ON
Remarks	This function ignores the case when the switch is pressed multiple times.

r_main_command_analyze

Outline	Command analysis	
Header	r_cg_userdefine.h	
Declaration	void r_main_command_analyze(uint8_t t_switch)	
Description	Calls the processing of the switch which has been pressed.	
Arguments	uint8_t t_switch	SET_SWITCH_ON: Set this when the SET switch is pressed UP_SWITCH_ON: Set this when the UP switch is pressed
Return Value	None	
Remarks	None	

r_main_set_switch_process

Outline	Processing when pressing the SET switch
Header	r_cg_userdefine.h
Declaration	void r_main_set_switch_process(void)
Description	Performs the SET switch processing. Processing depends on the clock mode. (a) When in clock display mode 1. Enable the UP switch. 2. Enter hour setting mode. 3. Set the LCD display mode to blinking. 4. Set the RTC constant-period interval to 0.5 seconds. 5. Enable LCD blinking. (b) When in hour setting mode 1. Enter minute setting mode. (c) When in minute setting mode 1. Disable the UP switch. 2. Set the LCD display mode to normal mode. 3. Set the RTC constant-period interrupt interval to 1 minute. 4. Disable the LCD blinking. 5. Set the seconds to 00 to update the RTC counter. 6. Enter clock display mode.
Arguments	None
Return Value	None
Remarks	None

r_it_operation_start

Outline	IT operation start processing	
Header	r_cg_it.h	
Declaration	void r_it_operation_start(void)	
Description	Starts the IT and clears the interrupt request flag.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT_Start

Outline	ITcounter operation start processing	
Header	r_cg_it.h	
Declaration	void R_IT_Start(void)	
Description	Starts the IT counter operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_it_operation_stop

Outline	IT operation stop processing	
Header	r_cg_it.h	
Declaration	void r_it_operation_stop(void)	
Description	Clears the interrupt request flag and stops the IT counter operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_IT_Stop

Outline	IT counter operation stop processing	
Header	r_cg_it.h	
Declaration	void R_IT_Stop(void)	
Description	Stops the IT counter operation.	
Arguments	None	None
Return Value	None	
Remarks	None	

R_RTC_Set_CounterValue

Outline	RTC write (SEC to YEAR)	
Header	r_cg_rtc.h	
Declaration	MD_STATUS R_RTC_Set_CounterValue(rtc_counter_value_t counter_write_val)	
Description	Sets the counter values (SEC to YEAR) to the RTC.	
Arguments	rtc_counter_value_t counter_write_val	rtc_counter_value_t counter_write_val
Return Value	● MD_OK: Normal end ● MD_BUSY1: Executing the count processing (before changing the setting) ● MD_BUSY2: Executing the count processing (after changing the setting)	
Remarks	None	

r_main_up_switch_process

Outline	Processing when pressing the UP switch	
Header	r_cg_userdefine.h	
Declaration	void r_main_up_switch_process(void)	
Description	Performs the UP switch processing. Processing depends on the clock mode status. (a) When in hour setting mode 1: Hour data is incremented by 1 to set the clock data to the RTC. (b) When in minute setting mode 1. 1: Minute data is incremented by 1 to set the clock data to the RTC.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_rtc_set_counter_value_hour_min

Outline	Write minute and hour data to the RTC	
Header	r_cg_rtc.h	
Declaration	MD_STATUS r_rtc_set_counter_value_hour_min(uint8_t hour, uint8_t minute)	
Description	Sets the counter values (MIN, HOUR) to the RTC.	
Arguments	uint8_t hour	: Counter value (hour)
Return Value	unit8_minute	: Counter value (minute)
Remarks	● MD_OK: Normal end ● MD_BUSY1: Executing the counter processing (before changing the setting) ● MD_BUSY2: Executing the counter processing (after changing the setting)	
Outline	None	

r_main_lcd_display_time

Outline	LCD time display	
Header	r_cg_userdefine.h	
Declaration	void r_main_lcd_display_time(void)	
Description	Depending on the LCD display mode (normal or blinking), clock mode (clock display mode, hour setting mode, minute setting mode), the program branches to the processing to set each data to the LCD display data address.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_lcd_hour_blink

Outline	Set hour blinking data in the LCD display data register	
Header	r_cg_userdefine.h	
Declaration	void r_main_lcd_hour_blink(void)	
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the hour on LCD. Write the same minute data both in A-pattern area and B-pattern area so only the hour data blinks.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_lcd_minute_blink

Outline	Set minute blinking data in the LCD display data register	
Header	r_cg_userdefine.h	
Declaration	void r_main_lcd_minute_blink(void)	
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the minutes on LCD. Write the same hour data both in A-pattern area and B-pattern area so only the minute data blinks.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_lcd_display_normal

Outline	Set normal display data in the LCD display data register	
Header	r_cg_userdefine.h	
Declaration	void r_main_lcd_display_normal(void)	
Description	Writes the font data of the current time in SEG19 to SEG27 in the LCD display data register to display the data on LCD.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_seg_data_set

Outline	Set display data in the LCD display data register	
Header	r_cg_userdefine.h	
Declaration	void r_main_seg_data_set(void)	
Description	Set the display data to LCD display data register.	
Arguments	None	None
Return Value	None	
Remarks	None	

r_main_bcd_inc

Outline	Addition processing of BCD data	
Header	r_cg_userdefine.h	
Declaration	void r_main_bcd_inc(void)	
Description	BCD data convert to the decimal. Add the value to decimal, and converted to BCD data.	
Arguments	None	None
Return Value	None	
Remarks	None	

5.7 Flowcharts

Figure 5.1 Overall Flow shows the overall flow of the sample code.

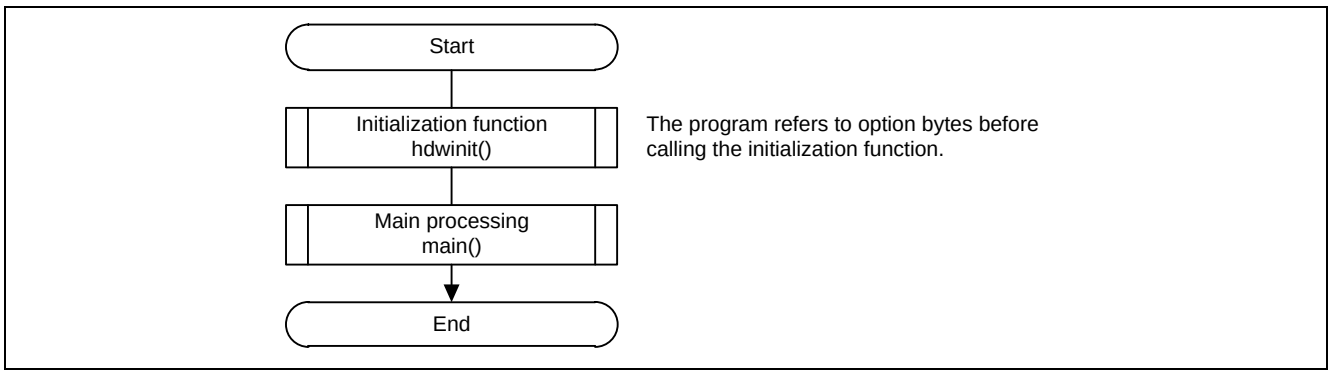

Figure 5.1 Overall Flow

Option byte setting overview:

RL78/L13 option bytes consist of user option bytes (000C0H to 000C2H) and on-chip debug option bytes (000C3H). At power-on or when a reset is released, RL78/L13 automatically refers to the option bytes to set the function specified.

User option bytes:

- Settings associated with the WDT (000C0H)
- Settings associated with the LVD (000C1H)
- HOCO and flash memory operation (000C2H)
- On-chip debug option bytes (000C3H)

Option bytes can also be specified in the [Device] category of the [Link Options] tab. As link options setting is prior to settings in the program, select [No] in the [Set user option byte] property.

Note: To learn more on how to set Link Options in CS+, refer to the CS+ Tutorial manual.

(1) 000C0H (WDT settings)

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON
0	**1**	**1**	**0**	**1**	**1**	**1**	**0**

Bit 7

WDTINT bit	Use of interval interrupt of watchdog timer
0	Interval interrupt is not used
1	Interval interrupt is generated when 75% of the overflow time is reached

Bits 6-5

Bits WINDOW1 and WINDOW0	Watchdog timer window open period
0	Setting prohibited
1	50%
10	75%
11	100%

Bit 4

WDTON bit	Operation control of watchdog timer counter
0	Counter operation disabled (counting stopped after reset)
1	Counter operation enabled (counting started after reset)

Bits 3-1

Bits WDCS2 to WDCS0	Watchdog timer overflow time
000	$26/f_{IL}$
001	$27/f_{IL}$
010	$28/f_{IL}$
011	$29/f_{IL}$
100	$211/f_{IL}$
101	$213/f_{IL}$
110	$214/f_{IL}$
111	$216/f_{IL}$

Bit 0

WDSTBYON bit	Operation control of watchdog timer counter
0	Counter operation stopped in HALT/STOP mode
1	Counter operation enabled in HALT/STOP mode

（2）000C1H(LVD settings)

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0
0	**1**	**0**	1	**1**	**1**	**0**	**1**

- Setting in interrupt & reset mode

Detection Voltage			Option Byte Setting Value						
V_{LVDH}		V_{LVDL}	Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	Falling edge	LVIMDS1	LVIMDS0					
1.77 V	1.73 V	1.63 V	1	0	0	0	0	1	0
1.88 V	1.84 V							0	1
2.92 V	2.86 V							0	0
1.98 V	1.94 V	1.84 V				0	1	1	0
2.09 V	2.04 V							0	1
3.13 V	3.06 V							0	0
2.61 V	2.55 V	2.45 V				1	0	1	0
2.71 V	2.65 V							0	1
3.75 V	3.67 V							0	0
2.92 V	2.86 V	2.75 V				1	1	1	0
3.02 V	2.96 V							0	1
4.06 V	3.98 V							0	0
Other than above			Setting prohibited						

- Setting in reset mode

Detection Voltage		Option Byte Setting Value						
V_{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	1	1	0	0	0	1	1
1.77 V	1.73 V				0	0	1	0
1.88 V	1.84 V				0	1	1	1
1.98 V	1.94 V				0	1	1	0
2.09 V	2.04 V				0	1	0	1
2.50 V	2.45 V				1	0	1	1
2.61 V	2.55 V				1	0	1	0
2.71 V	2.65 V				1	0	0	1
2.81 V	2.75 V				1	1	1	1
2.92 V	2.86 V				1	1	1	0
3.02 V	2.96 V				1	1	0	1
3.13 V	3.06 V				0	1	0	0
3.75 V	3.67 V				1	0	0	0
4.06 V	3.98 V				1	1	0	0
Other than above		Setting prohibited						

Setting in interrupt mode

Detection Voltage		Option Byte Setting Value						
VLVD		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
1.67 V	1.63 V	0	1	0	0	1	1	1
1.77 V	1.73 V				0	0	1	0
1.88 V	1.84 V				0	1	1	1
1.98 V	1.94 V				0	1	1	0
2.09 V	2.04 V				0	1	0	1
2.50 V	2.45 V				1	0	1	1
2.61 V	2.55 V				1	0	1	0
2.71 V	2.65 V				1	0	0	1
2.81 V	2.75 V				1	1	1	1
2.92 V	2.86 V				1	1	1	0
3.02 V	2.96 V				1	1	0	1
3.13 V	3.06 V				0	1	0	0
3.75 V	3.67 V				1	0	0	0
4.06 V	3.98 V				1	1	0	0
Other than above		Setting prohibited						

- Setting when LVD is off

Detection Voltage		Option Byte Setting Value						
V_{LVD}		Mode setting		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	LVIMDS1	LVIMDS0					
–	–	×	1	1	×	×	×	×
Other than above		Setting prohibited						

Note: ×: don't care

（3） 000C2H (HOCO and flash operation mode settings)

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0
0	**0**	1	**0**	**1**	**0**	**1**	**1**

Bits 7－6

CMODE 1 bit	CMODE 0 bit	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low-voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low-speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high-speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

Bits 4－0

FRQSEL 4 bit	FRQSEL 3 bit	FRQSEL 2 bit	FRQSEL 1 bit	FRQSEL 0 bit	Frequency of the high-speed on-chip oscillator clock	
					f_{HOCO}	f_{IH}
1	0	0	0	0	48 MHz	24 MHz
0	0	0	0	0	24 MHz	24 MHz
0	1	0	0	1	16 MHz	16 MHz
0	0	0	0	1	12 MHz	12 MHz
0	1	0	1	0	8 MHz	8 MHz
0	1	0	1	1	4 MHz	4 MHz
0	1	1	0	1	1 MHz	1 MHz
Other than above					Setting prohibited	

（4） 000C3H (On-chip debug option byte)

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD
1	0	0	0	0	1	0	**0**

Bit 7,0

OCDENSET bit	OCDERSD bit	Control of on-chip debug operation
0	0	Disables on-chip debug operation
0	1	Setting prohibited
1	0	Enables on-chip debugging.
.1	1	Erases data of flash memory in case of failures in authenticating on-chip debug security ID

5.7.1 Initialization

Figure 5.2 Initialization shows the initialization.

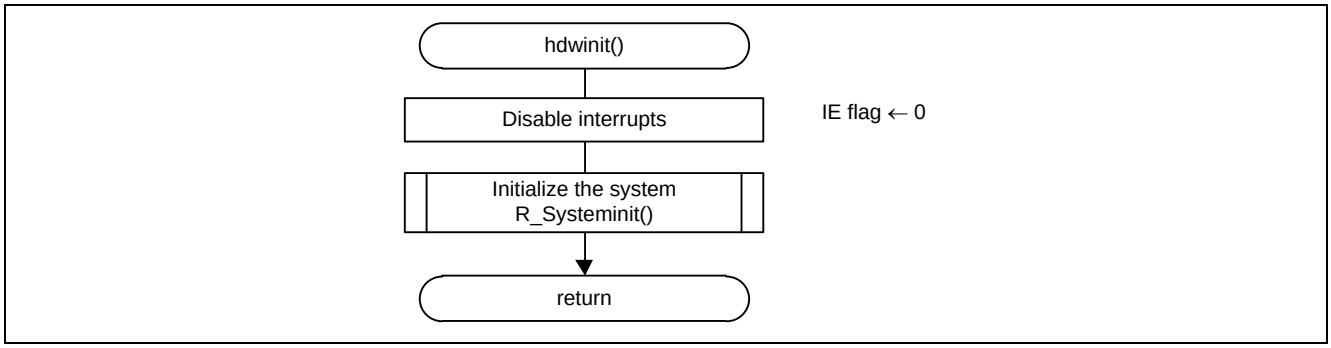

Figure 5.2 Initialization

5.7.2 System Initialization

Figure 5.3 shows the system initialization.

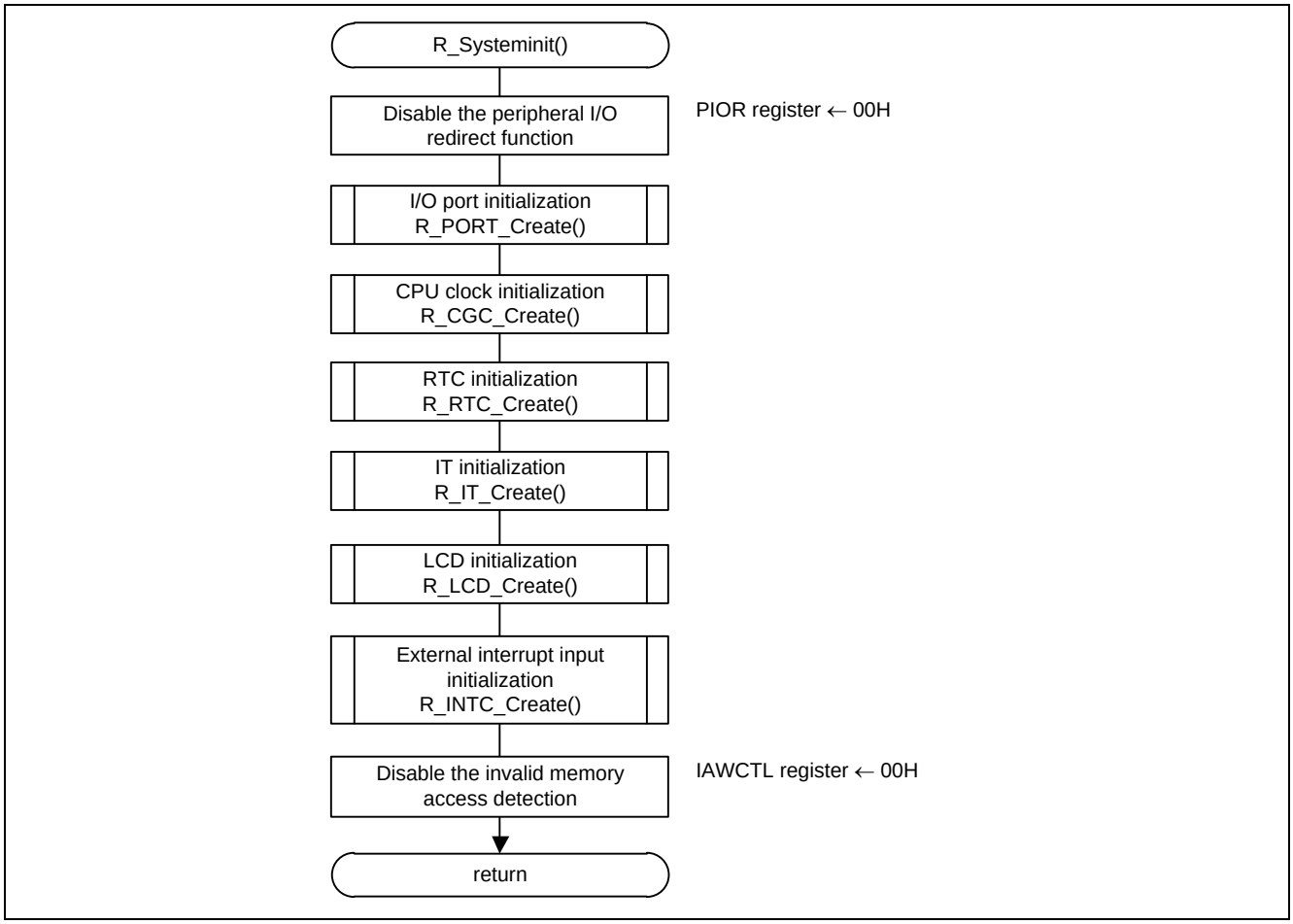

Figure 5.3 System Initialization

5.7.3 CPU Clock Setting

Figure 5.4 shows the CPU clock setting.

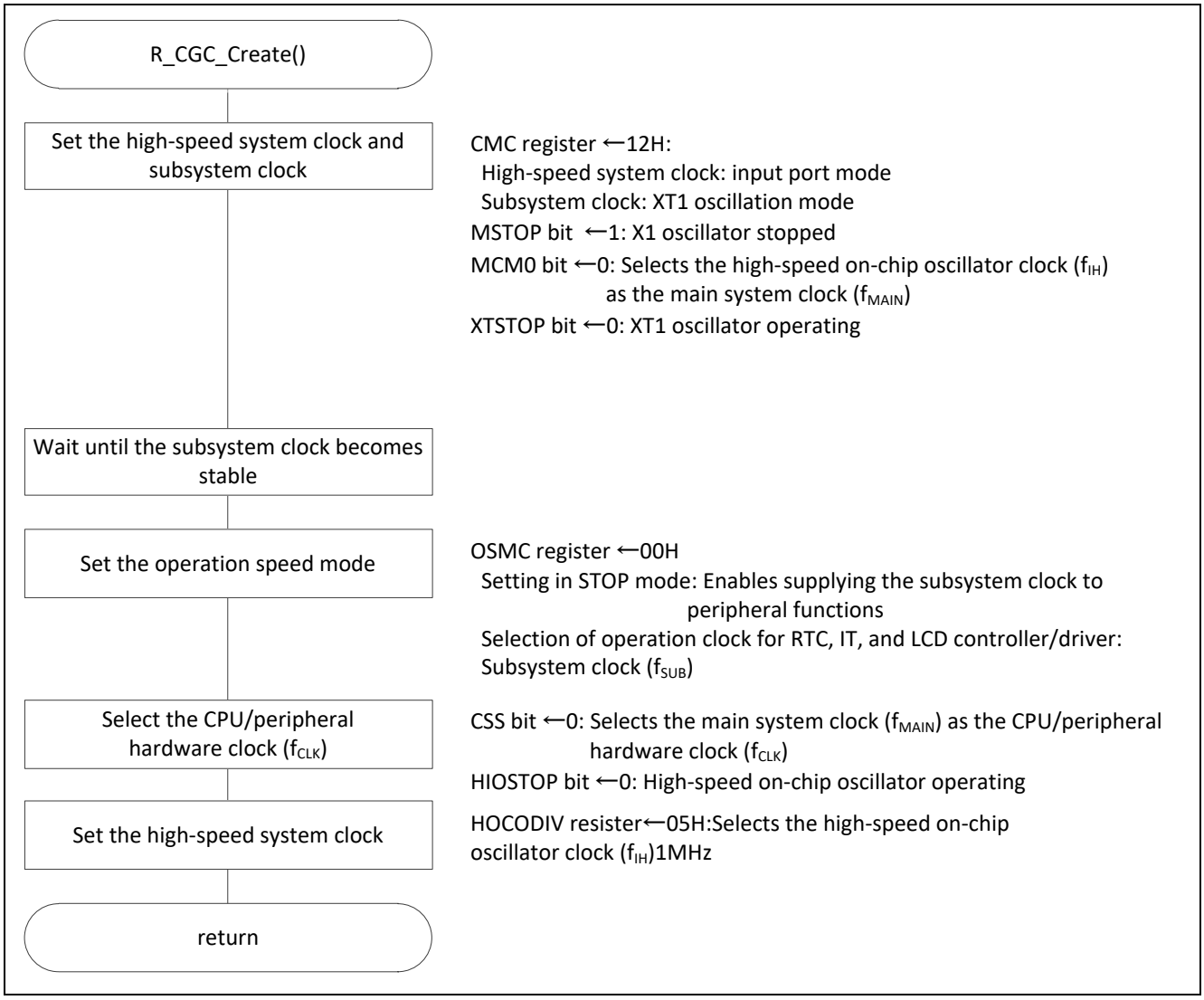

Figure 5.4 CPU clock setting

5.7.4 RTC2 setting

Figure 5.5 shows the RTC2 setting.

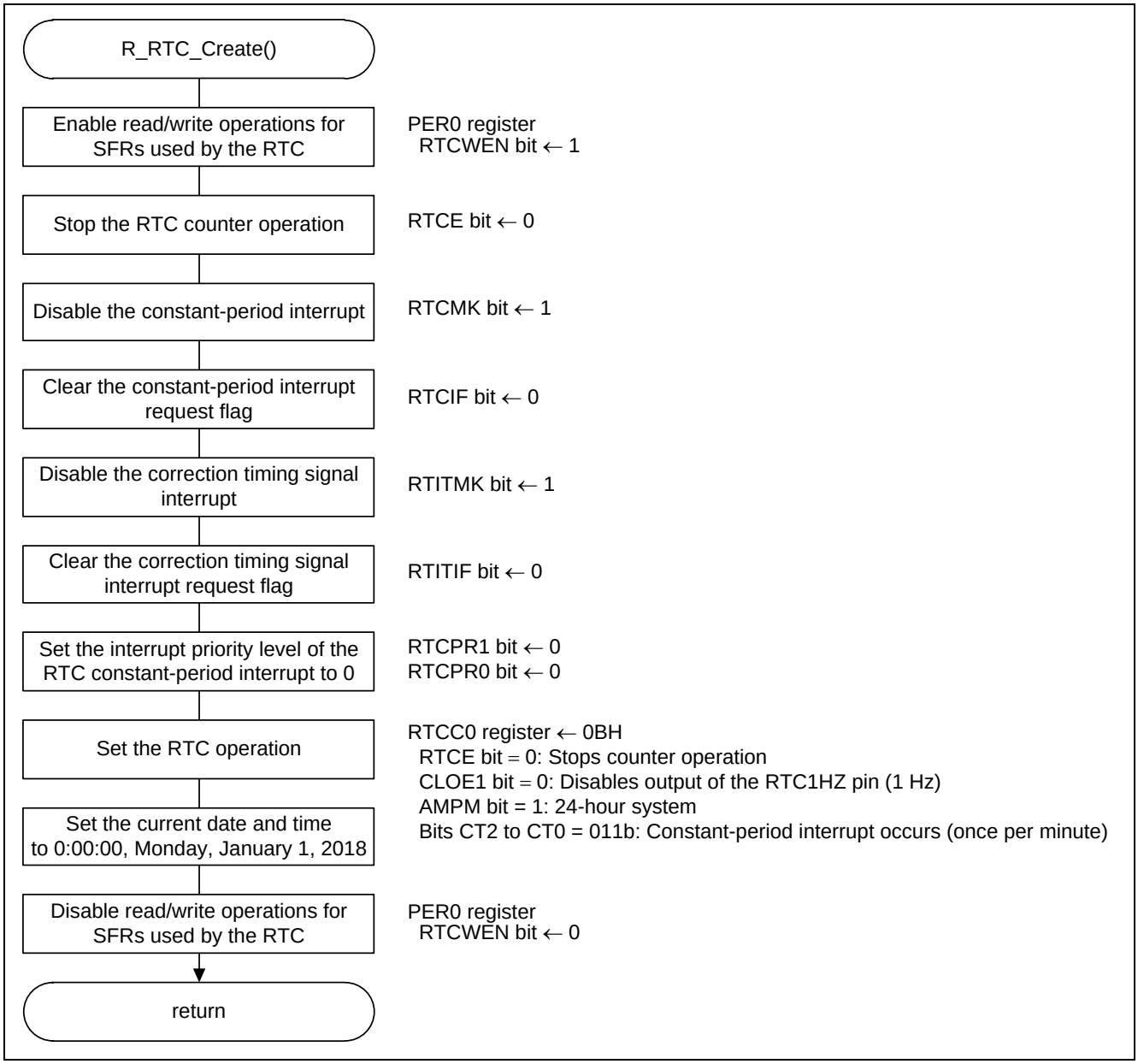

Figure 5.5 RTC2 setting

5.7.5 12-bit Interval Timer setting

Figure 5.6 shows the 12-bit Interval Timer setting.

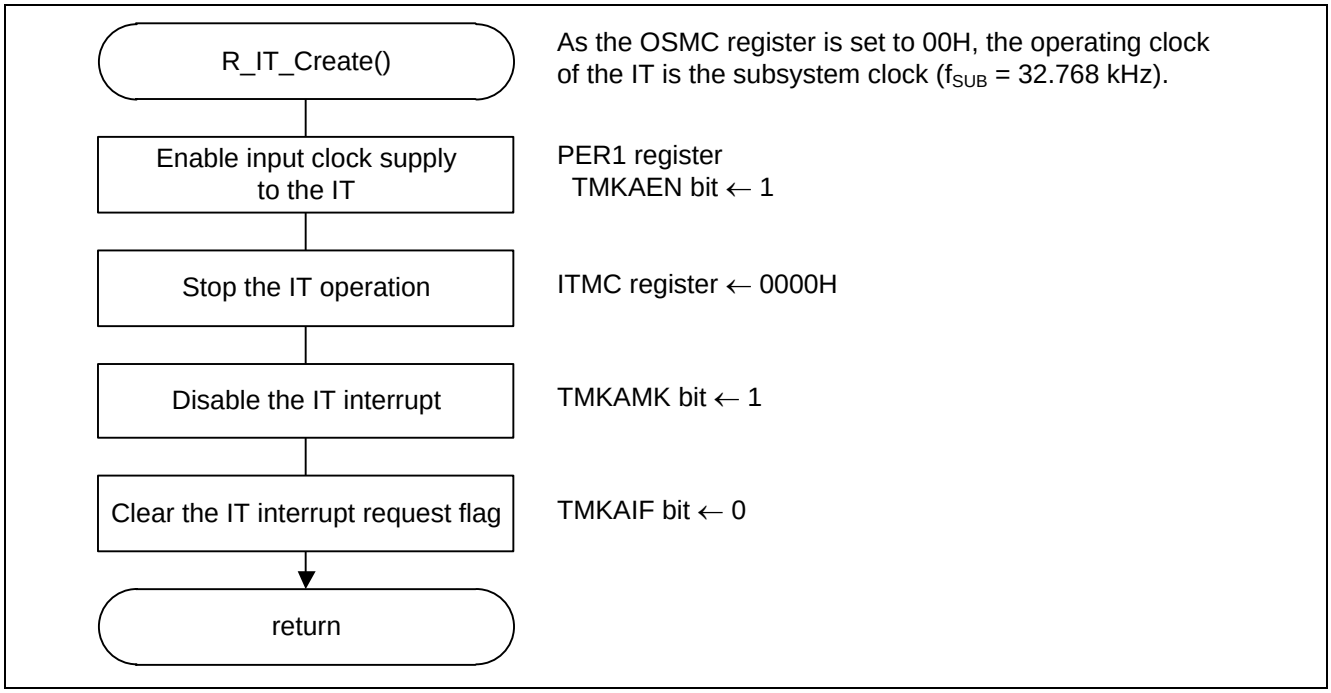

Figure 5.6 12-bit Interval Timer setting

5.7.6 LCD Controller/Driver Setting

Figure 5.7 and Figure 5.8 show the LCD controller/driver setting.

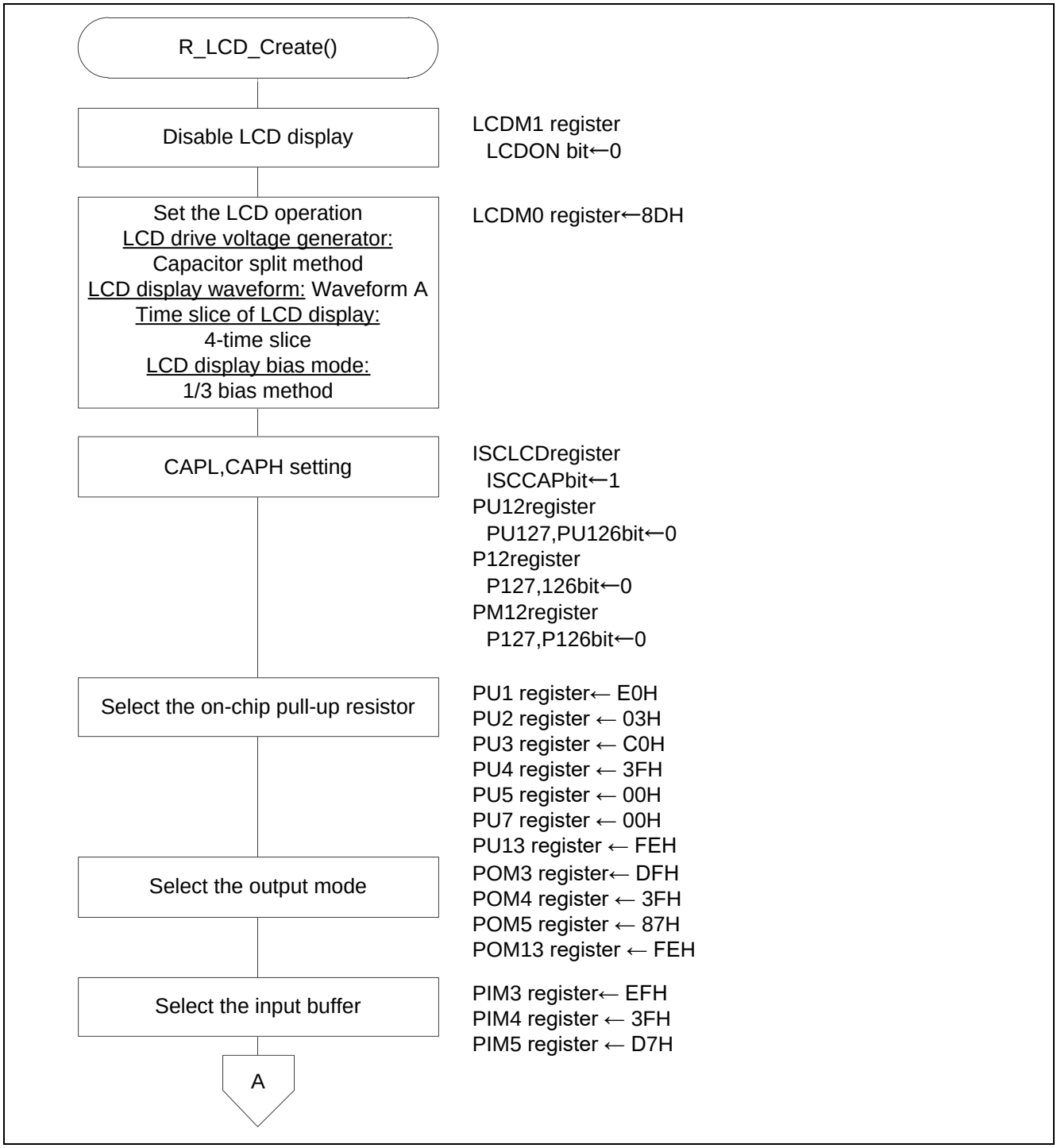

Figure 5.7 LCD Controller/Driver Setting (1/2)

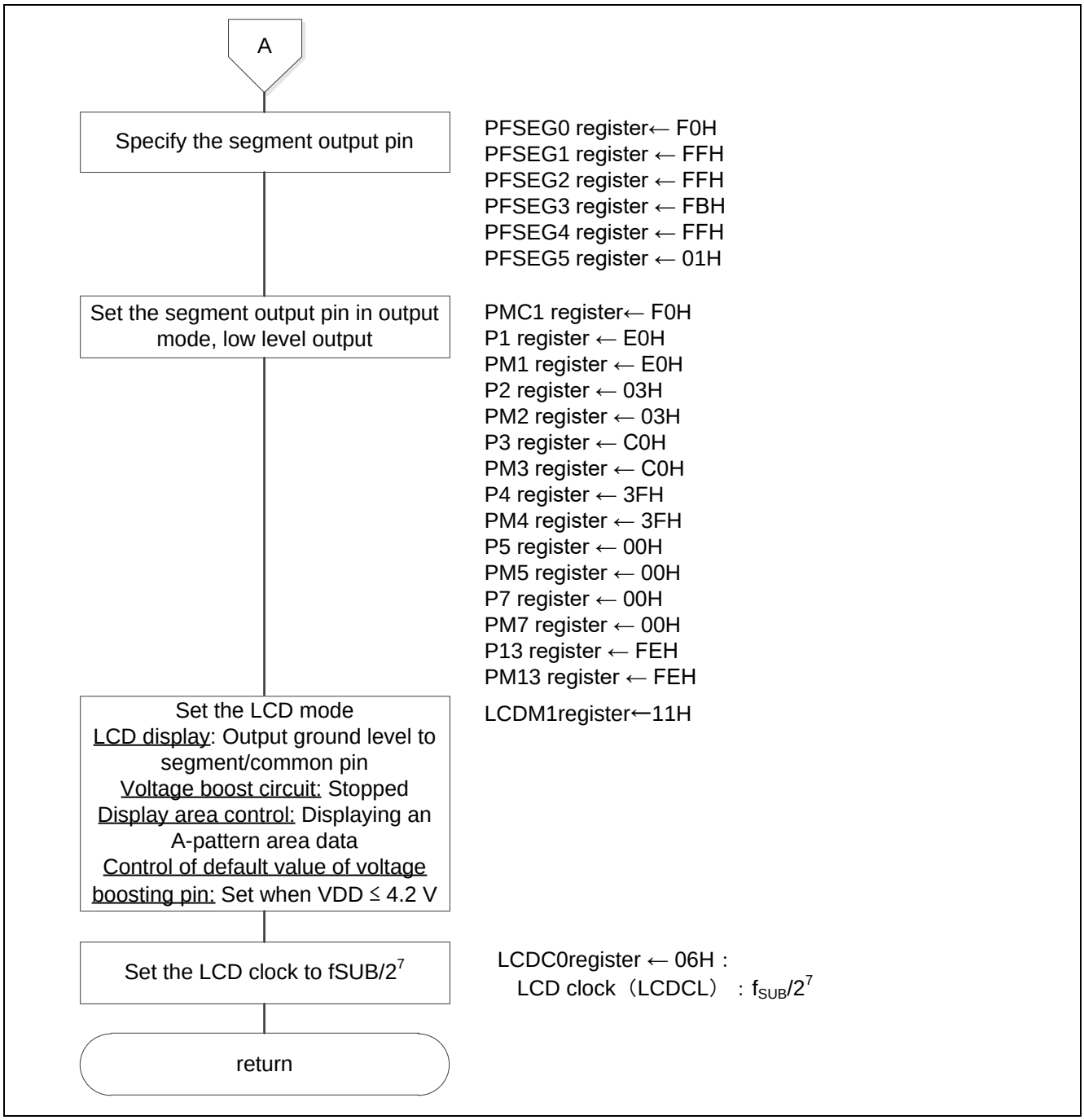

Figure 5.8 LCD Controller/Driver Setting (2/2)

Setting the LCD mode

- LCD mode register 1 (LCDM1)
- Outputs ground level to segment/common pin
- Stops voltage boost circuit or capacitor split circuit operation
- Alternately displaying A-pattern and B-pattern area data
- Sets the default value of the voltage boosting pin when VDD ≤ 4.2 V

Symbol：LCDM1

7	6	5	4	3	2	1	0
LCDON	SCOC	VLCON	BLON	LCDSEL	0	0	LCDVLM
0	**0**	**0**	**1**	**0**	0	0	**1**

Bits 7－6

SCOC	LCDON	LCD display enable/disable
0	**0**	Output ground level to segment/common pin
0	1	
1	0	Display off (all segment outputs are deselected)
1	1	Display on

Bit 5

VLCON	Voltage boost circuit or capacitor split circuit operation enable/disable
0	Stops voltage boost circuit or capacitor split circuit operation
1	Enables voltage boost circuit or capacitor split circuit operation

Bits 4－3

BLON[Note1]	LCDSEL	Display data area control
0	0	Displaying an A-pattern area data (lower four bits of LCD display data register)
0	1	Displaying a B-pattern area data (higher four bits of LCD display data register)
1	**0**	Alternately displaying A-pattern and B-pattern area data (blinking display corresponding to the constant-period interrupt (INTRTC) timing of the high-accuracy real-time clock (RTC))
1	1	

Bit 0

LCDVLM bit [Note 2]	Control of default value of voltage boosting pin
0	Set when V_{DD} ≥ 2.7V
1	Set when V_{DD} ≤ 4.2V

Note 1. When f_{IL} is selected as the LCD source clock (f_{LCD}), be sure to set the BLON bit to “0”.

Note 2. This function is used to shorten the boost stabilization time by setting the VLX pin to the default status when the voltage boost circuit is used. If the VDD voltage is 2.7V or higher when boosting is started, set the LCDVLM bit to “0”; if the VDD voltage is 4.2V or less, set the LCDVLM bit to “1”. However, when 2.7V ≤ VDD ≤ 4.2V, operation is possible with LCDVLM = 0 or LCDVLM = 1.

Caution: For details on register setting, refer to the RL78/L13 User’s Manual: Hardware.

Setting the LCD operation

LCD mode register 0 (LCDM0)
LCD drive voltage generator: : Capacitor split method
LCD display waveform : A
Time slice of LCD display : 4-time slice
LCD display bias mode : 1/3 bias method

Symbol：LCDM0

7	6	5	4	3	2	1	0
MDSET1	MDSET0	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0
1	**0**	**0**	**0**	**1**	**1**	**0**	**1**

Bits 7－6

MDSET1	MDSET0	LCD drive voltage generator selection
0	0	External resistance division method
0	1	Internal voltage boosting method
1	**0**	Capacitor split method
1	1	Setting prohibited

Bit 5

MLCDEN	LWAVE	LCD display waveform selection
0	**0**	Waveform A
0	1	Waveform B

Bits 4－2

LDTY2	LDTY1	LDTY0	Selection of time slice of LCD display
0	0	0	Static
0	0	1	2-time slice
0	1	0	3-time slice
0	**1**	**1**	4-time slice
1	0	1	8-time slice
Other than above			Setting prohibited

Bits 1－0

LBAS1	LBAS0	LCD display bias mode selection
0	0	1/2 bias method
0	**1**	1/3 bias method
1	0	1/4 bias method
1	1	Setting prohibited

Caution: For details on register setting, refer to the RL78/L13 User’s Manual: Hardware.

Controlling the Schmitt trigger buffer

LCD input switch control register (ISCLCD)
Input to the Schmitt trigger: Input invalid

Symbol：ISCLCD

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ISCVL3	ISCCAP
0	0	0	0	0	0	0	**1**

Bit 0

ISCCAP	CAPL/P126, CAPH/P127 pins Schmitt trigger buffer control
0	Input invalid
1	Input valid

The functions of the CAPL/P126, and CAPH/P127 pins can be selected by using the LCD input switch control register (ISCLCD), LCD mode register 0 (LCDM0), and port mode register 12 (PM12).

CAPL/P126, CAPH/P127 Pin Function Settings:

LCD Drive Voltage Generator	ISCCAP Bit in the ISCLCD Register	Bits PM126 and PM127 in the PM12 Register	Pin Function	Initial Status
External resistance division	0	1	Digital input invalid mode	○
	1	0	Digital output mode	—
	1	1	Digital input mode	—
Internal voltage boosting or capacitor split	**0**	**1**	CAPL/CAPH function mode	**—**
Other than above			Setting prohibited	

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Selecting the on-chip pull-up resistor

Pull-up resistor option registers (PU3 to PU7)
On-chip pull-up resistor: Not connected

Symbol：PU1

7	6	5	4	3	2	1	0
PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10
0	0	0	**0**	**0**	**0**	**0**	**0**

Bits 4-0

PUmn	Pmn pin on-chip pull-up resistor selection (m = 1, n = 0 to 4)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU2

7	6	5	4	3	2	1	0
PU27	PU26	PU25	PU24	PU23	PU22	0	0
0	**0**	**0**	**0**	**0**	**0**	0	0

Bits 7-2

PUmn	Pmn pin on-chip pull-up resistor selection (m = 2, n = 2 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU3

7	6	5	4	3	2	1	0
0	0	PU35	PU34	PU33	PU32	PU31	PU30
0	0	**0**	**0**	**0**	**0**	**0**	**0**

Bits 5-0

PUmn	Pmn pin on-chip pull-up resistor selection (m = 3, n = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU4

7	6	5	4	3	2	1	0
PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40
0	**0**	0	0	0	0	0	0

Bits 7-6

PUmn	Pmn pin on-chip pull-up resistor selection (m = 4, n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU5

7	6	5	4	3	2	1	0
PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7-0

PUmn	Pmn pin on-chip pull-up resistor selection (m = 5, n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU7

7	6	5	4	3	2	1	0
PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 7-0

PUmn	Pmn pin on-chip pull-up resistor selection (m = 7, n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Symbol：PU13

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PU130
0	0	0	0	0	0	0	**0**

Bit 0

PUmn	Pmn pin on-chip pull-up resistor selection (m = 3, n = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Specifying the segment output pin

LCD port function registers 2 and 3 (PFSEG2, PFSEG3)
P30 to P35, P46, P47, and P77: Used as the segment output

Symbol：PFSEG2

7	6	5	4	3	2	1	0
PFSEG23	PFSEG22	PFSEG21	PFSEG20	PFSEG19	PFSEG18	PFSEG17	PFSEG16
1	**1**	**1**	**1**	**1**	1	1	1

Bits 7-3

Bits PFSEG23 to PFSEG19	Port (other than segment output)/segment outputs specification of Pmn pins, mn=77, 30 to 33
0	Used the Pmn pin as port (other than segment output)
1	Used the Pmn pin as segment output

Symbol：PFSEG3

7	6	5	4	3	2	1	0
PFSEG30	PFSEG29	PFSEG28	PFSEG27	PFSEG26	PFDEG	PFSEG25	PFSEG24
1	1	1	**1**	**1**	0	**1**	**1**

Bits 4-3、1-0

Bits PFSEG24 to PFSEG27	Port (other than segment output)/segment outputs specification of Pmn pins, mn=34, 35, 46, 47
0	Used the Pmn pin as port (other than segment output)
1	Used the Pmn pin as segment output

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Setting the LCD clock

LCD clock control register 0 (LCDC0)
Sets the LCD clock to $f_{SUB}/2^7$.

Symbol：LCDC0

7	6	5	4	3	2	1	0
0	0	LCDC05	LCDC04	LCDC03	LCDC02	LCDC01	LCDC00
0	0	**0**	**0**	**0**	**1**	**1**	**0**

Bits 5-0

LCDC05	LCDC04	LCDC03	LCDC02	LCDC01	LCDC00	LCD クロック（LCDCL）
0	0	0	1	0	0	$f_{SUB}/2^5$ or $f_{IL}/2^5$
0	0	0	1	0	1	$f_{SUB}/2^6$ or $f_{IL}/2^6$
0	**0**	**0**	**1**	**1**	**0**	**$f_{SUB}/2^7$ or $f_{IL}/2^7$**
0	0	0	1	1	1	$f_{SUB}/2^8$ or $f_{IL}/2^8$
0	0	1	0	0	0	$f_{SUB}/2^9$ or $f_{IL}/2^9$
0	0	1	0	0	1	$f_{SUB}/2^{10}$
0	1	0	0	1	1	$f_{MAIN}/2^{10}$
0	1	0	1	0	0	$f_{MAIN}/2^{11}$
0	1	0	1	0	1	$f_{MAIN}/2^{12}$
0	1	0	1	1	0	$f_{MAIN}/2^{13}$
0	1	0	1	1	1	$f_{MAIN}/2^{14}$
0	1	1	0	0	0	$f_{MAIN}/2^{15}$
0	1	1	0	0	1	$f_{MAIN}/2^{16}$
0	1	1	0	1	0	$f_{MAIN}/2^{17}$
0	1	1	0	1	1	$f_{MAIN}/2^{18}$
1	0	1	0	1	1	$f_{MAIN}/2^{19}$
Other than above						Setting prohibited

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

Setting the reference voltage of the voltage boost circuit

LCD boost level control register (VLCD)

Sets the reference voltage to 1.00V (V_{L4} = 3.00V).

Symbol：VLCD

7	6	5	4	3	2	1	0
0	0	0	VLCD4	VLCD3	VLCD2	VLCD1	VLCD0
0	0	0	**0**	**0**	**1**	**0**	**0**

Bits 4－0

VLCD4	VLCD3	VLCD2	VLCD1	VLCD0	Reference voltage selection (contrast adjustment)	V_{L4} voltage	
						1/3 bias method	1/4 bias method
0	**0**	**1**	**0**	**0**	**1.00V** (default)	**3.00V**	4.00V
0	0	1	0	1	1.05V	3.15V	4.20V
0	0	1	1	0	1.10V	3.30V	4.40V
0	0	1	1	1	1.15V	3.45V	4.60V
0	1	0	0	0	1.20V	3.60V	4.80V
0	1	0	0	1	1.25V	3.75V	5.00V
0	1	0	1	0	1.30V	3.90V	5.20V
0	1	0	1	1	1.35V	4.05V	Setting prohibited
0	1	1	0	0	1.40V	4.20V	
0	1	1	0	1	1.45V	4.35V	
0	1	1	1	0	1.50V	4.50V	
0	1	1	1	1	1.55V	4.65V	
1	0	0	0	0	1.60V	4.80V	
1	0	0	0	1	1.65V	4.95V	
1	0	0	1	0	1.70V	5.10V	
1	0	0	1	1	1.75V	5.25V	
Other than above					Setting prohibited		

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

5.7.7 Main Processing

Figure 5.9 shows the main processing.

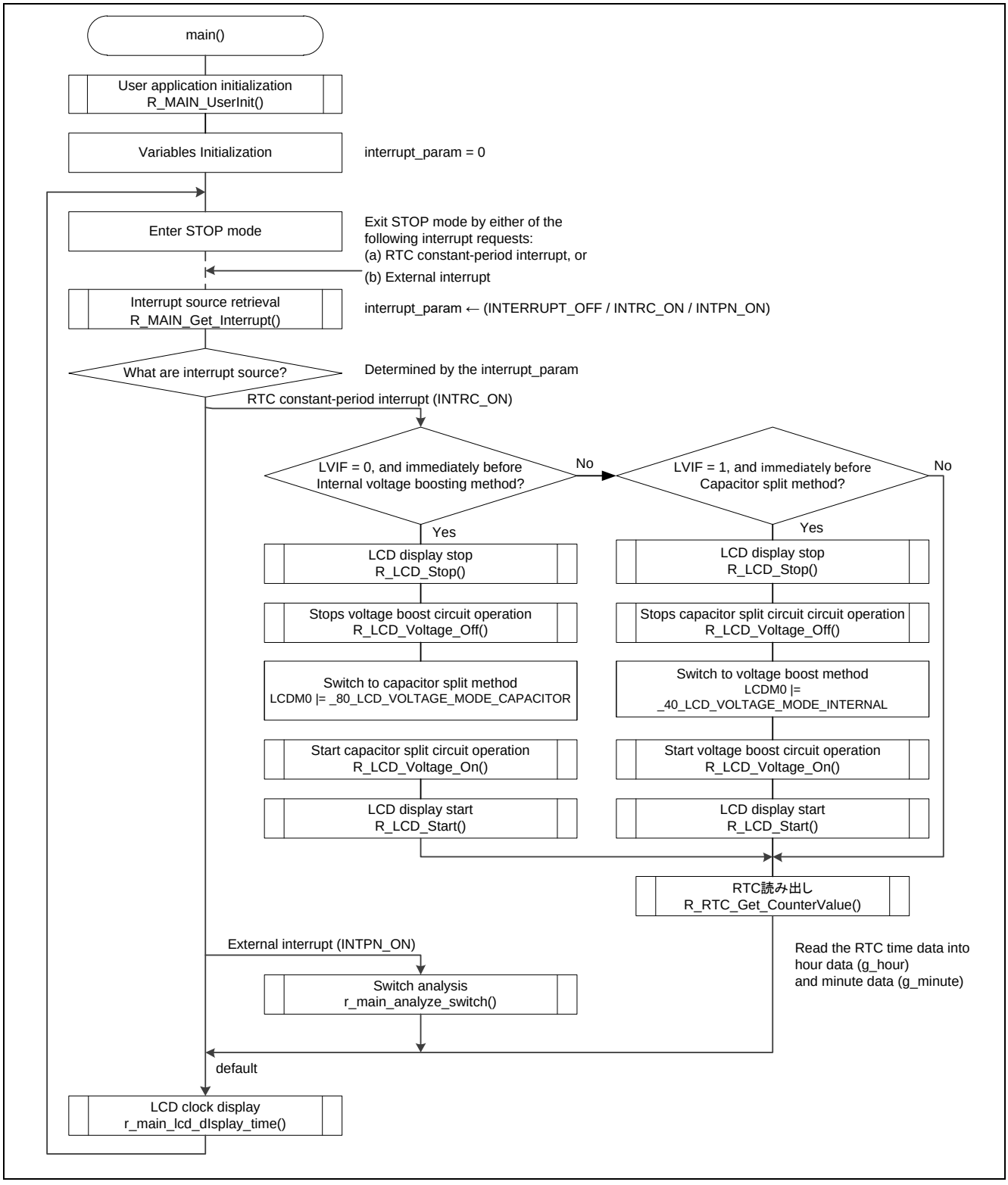

Figure 5.9 Main Processing

5.7.8 User Application Initialization

Figure 5.10 shows the user application initialization.

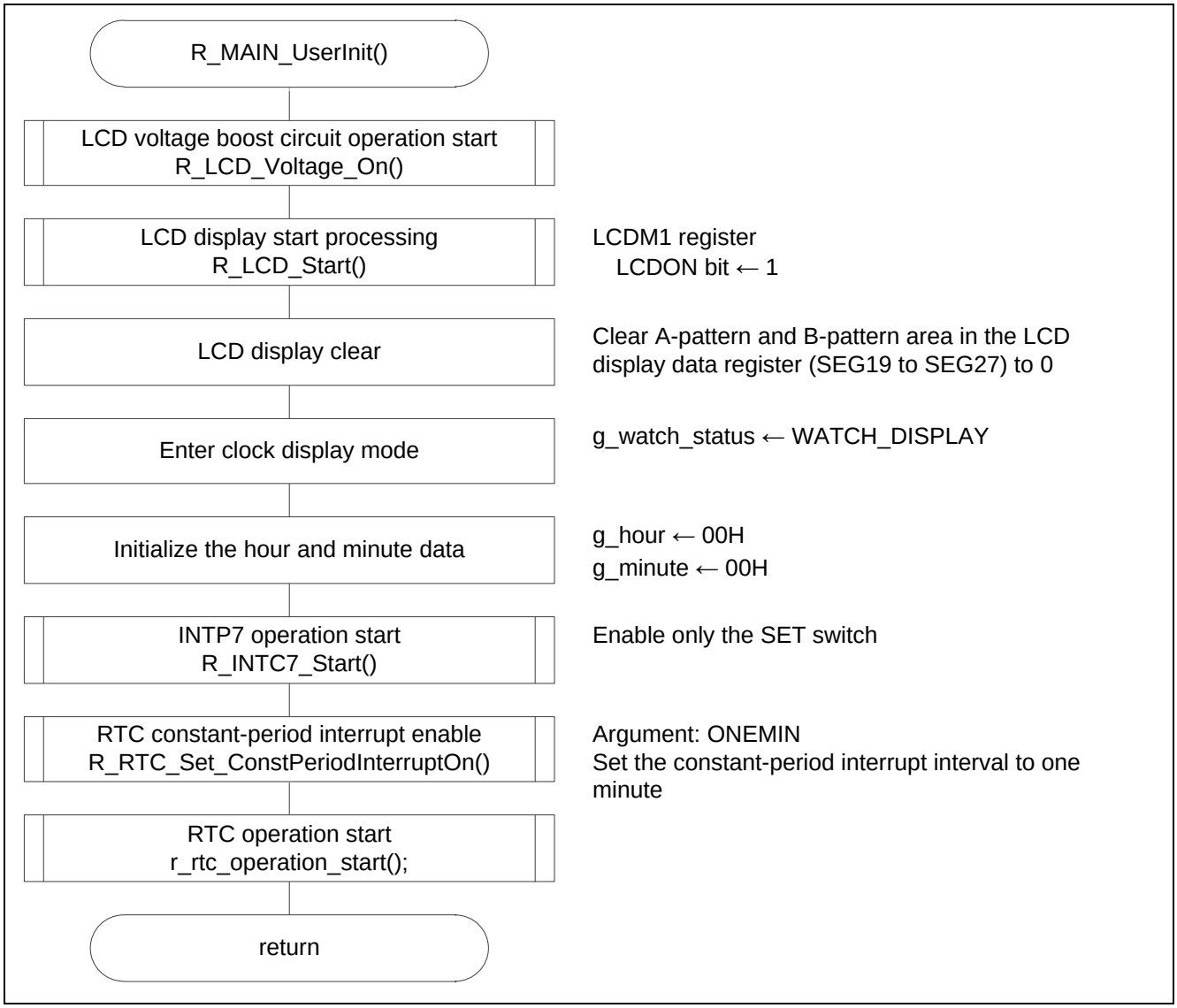

Figure 5.10 User Application Initialization

5.7.9 LCD Voltage Boost and Capacitor Split Circuit Operation Start Setting

Figure 5.11 shows the LCD Voltage Boost and Capacitor Split Circuit Operation Start Setting

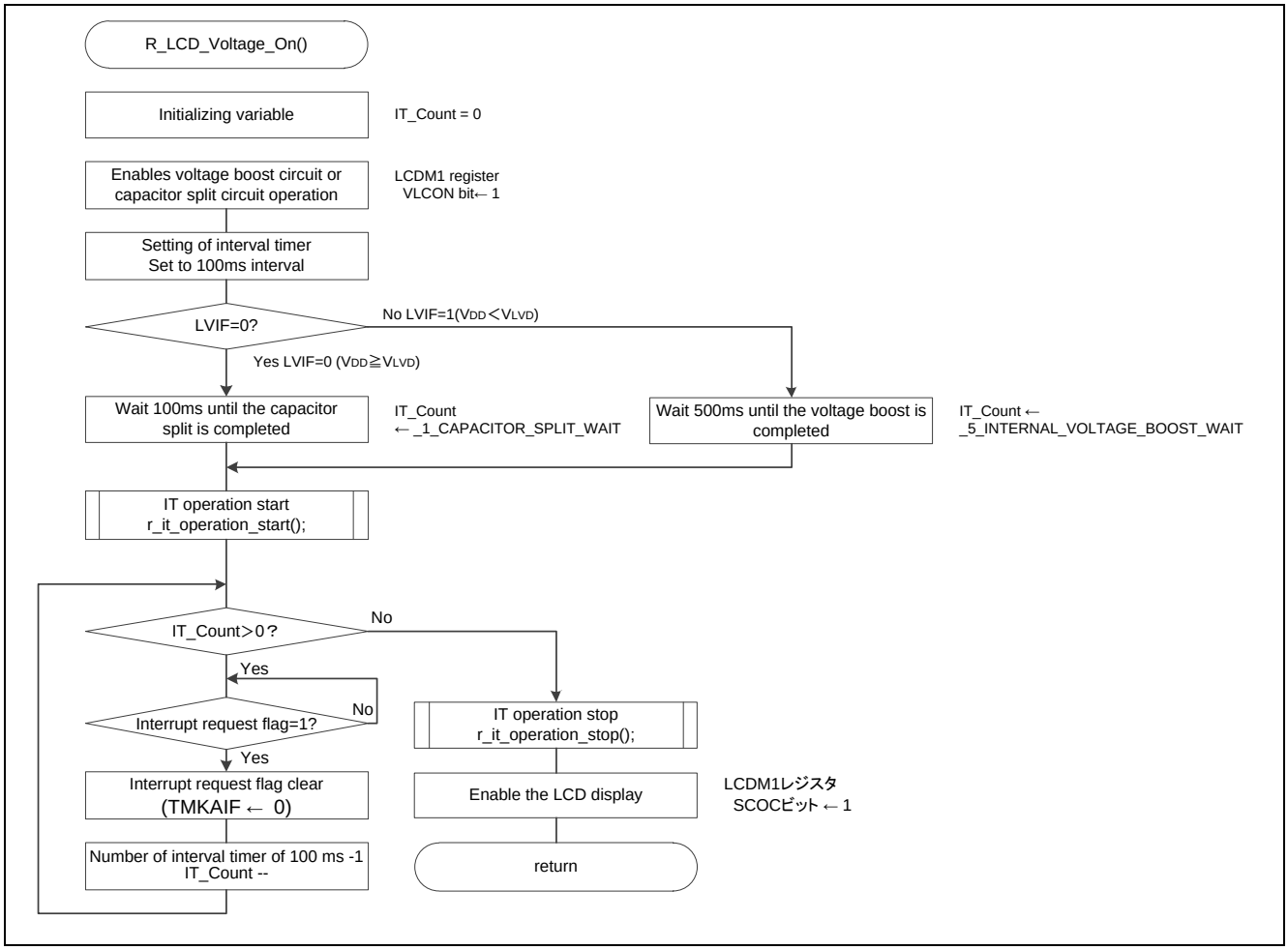

Figure 5.11 LCD Voltage Boost and Capacitor Split Circuit Operation Start Setting

Caution: For details on register setting, refer to the RL78/L13 User's Manual: Hardware.

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User's Manual: Hardware

RL78/L13 User's Manual: Hardware Rev.1.00

RL78 Family User's Manual: Software Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/L13 Low power consumption of LCD drive Using Voltage Detector (LVD)

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 27, 2018	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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