RL78/G24

TIMER WINDOW Output using Timer RD2, Timer Array Unit and Comparator

Introduction

This application note explains the TIMER WINDOW output function based on the combined use of the RL78/G24 timer RD2, timer array unit (TAU), and comparator (CMP).

TIMER WINDOW output is a function that sets CMP output to a low level when TAU output (TO02) is at a low level. This means that the TIMER WINDOW output enables voltage detection by the CMP only when TAU output (TO02) is at a high level.

The RL78/G24 allows users to set the valid edge (rising, falling, or both edges) of timer RD2 output (TRDIOxx; xx = B0, C0, D0, A1, B1, C1, D1) as the TAU0 channel 0 start trigger. Thus, when PWM output is performed by timer RD2, the CMP voltage detection period can be set in conjunction with the timer RD2 output.

Target Device

RL78/G24

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Specification overview

This section describes the specifications of this application. Timer RD2 is set to the PWM function and outputs PWM from the TRDIOB0 pin with a 30% duty cycle for a period of 300us. TAU is used to execute the one-shot pulse output function with the rising edge of TRDIOB0 as the start trigger. In this application, the delay is set to 10us and the pulse width to 100us.

The comparator (CMP) outputs the comparison results of the IVCOMP1 input voltage and the D/A converter-1 (DAC1) for internal comparator reference voltage as the timer window output through the VCOUT1 pin. The D/A converter output is VDD x 512/1024.

Table 1-1 provides a list of the peripheral functions used and their purposes, and Figure 1-1 shows the system configuration of the CMP output with the TIMER WINDOW output function.

During the TO02 pulse output period, the VCOUT1 output indicated by the dotted circles is not output because the CMP output is masked.

Table 1-1 Peripheral Functions and Their Usage

Peripheral	Usage
Timer RD2 (TRD20)	PWM output
Timer Array Unit (TAU)	CMP1 output enable signal output
Comparator (CMP)	Comparator output
D/A Converter 1 (DAC1)	D/A Conversion

Figure 1-1 System Configuration of CMP Output with the TIMER WINDOW Output Function

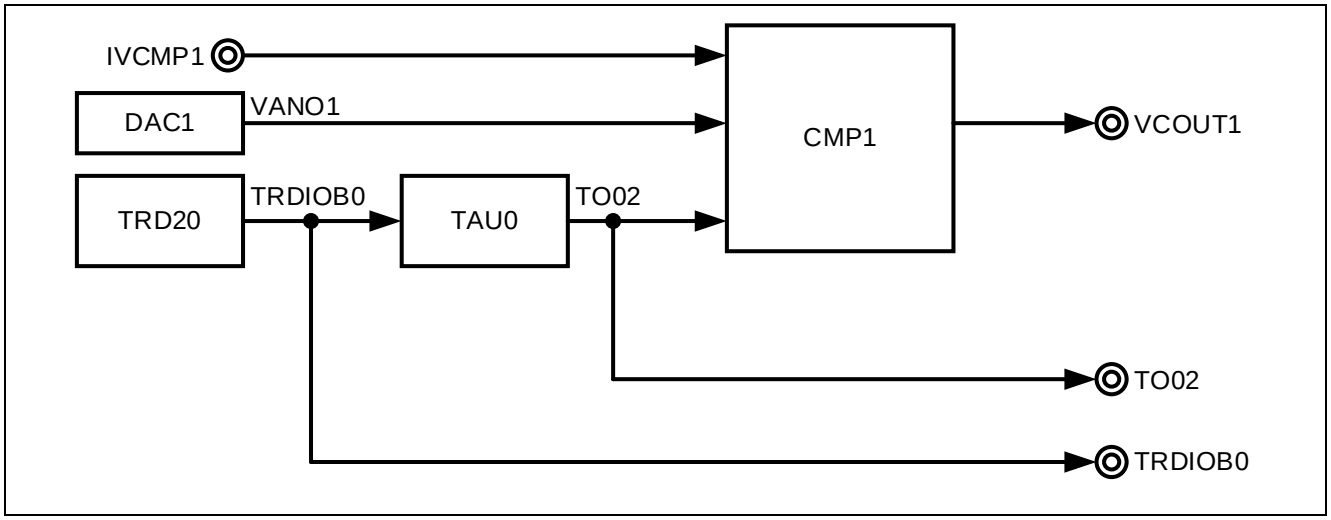

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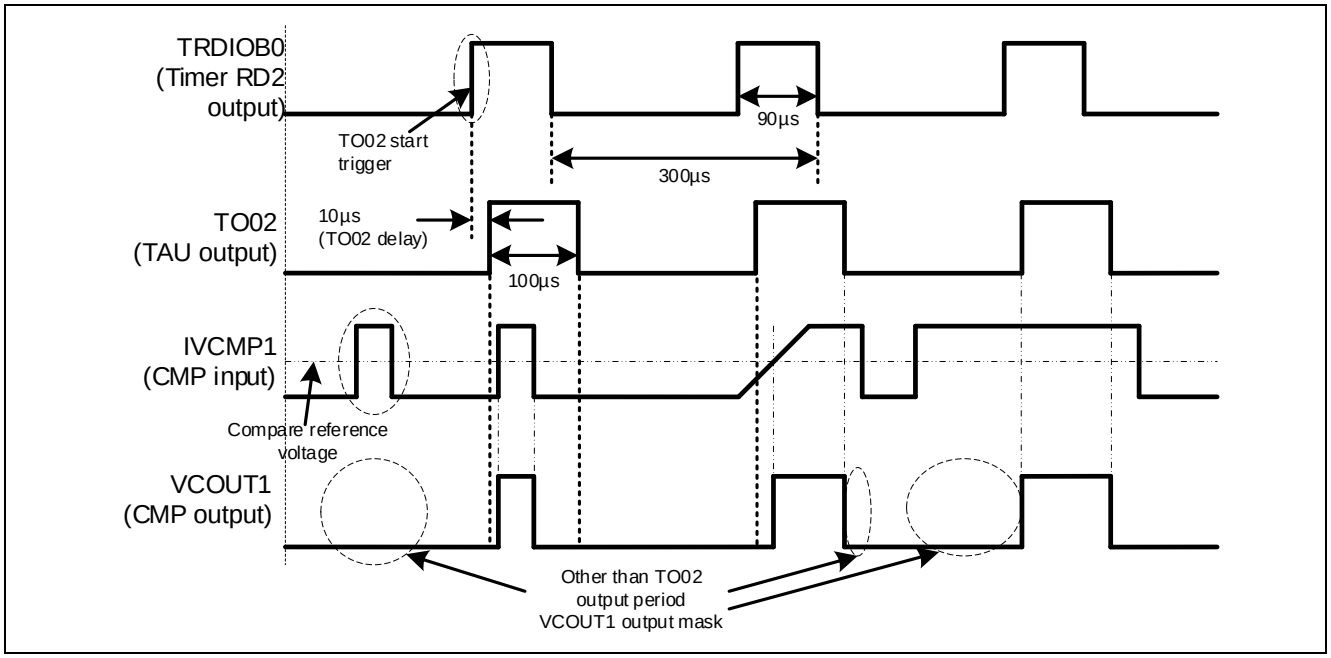
Figure 1-2 shows an example of CMP output using the TIMER WINDOW output.

Figure 1-2 Output waveform of CMP using TIMER WINDOW Ooutput



1.2 Operation overview

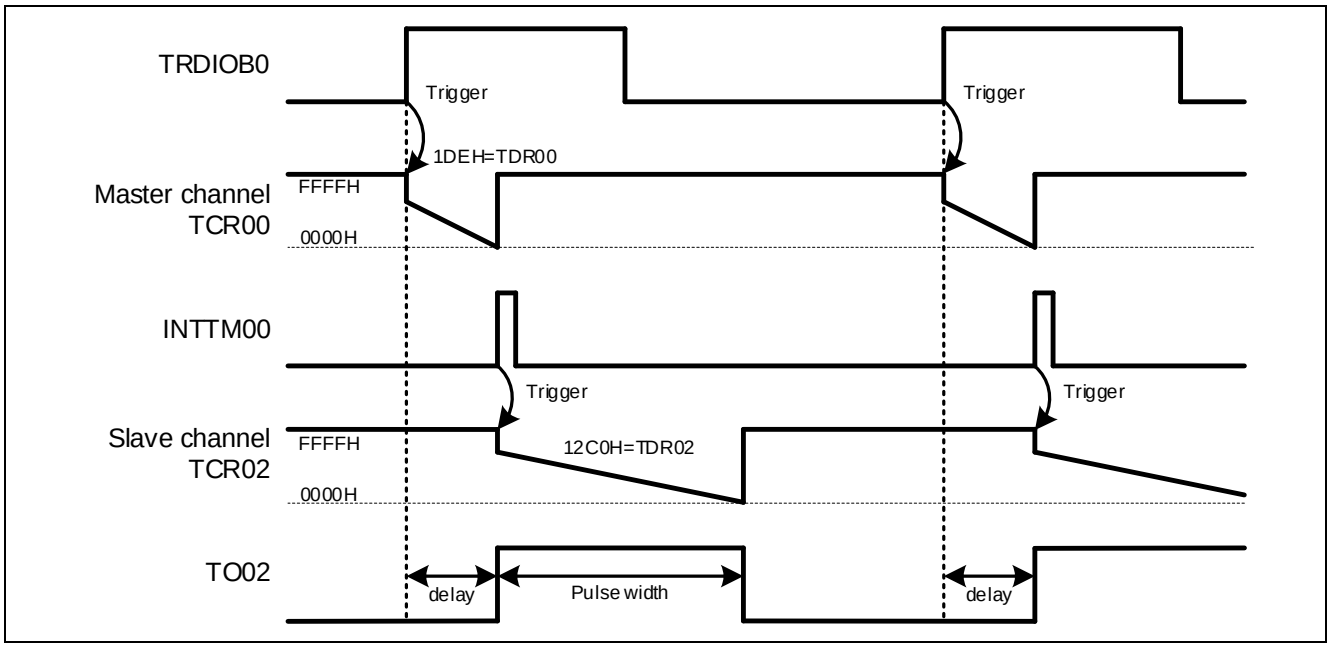
To enable the TIMER WINDOW output, initialization of the TAU, DAC, CMP, and timer RD2 is necessary, and then executing the corresponding operations in the same sequence.

The TAU is set to the one-shot pulse output function. It is triggered by the rising edge of TRDIOB0 with a delay of 10µs and a pulse width setting of 100µs.

<TAU Initialization>
· Set TAU0_0 to one-shot pulse output.
· For clock settings, set operating clock to CK00 and clock source to fCLK (48MHz).
· Set the one-shot trigger to external trigger and the rising edge of TRDIOB0.
· Set the one-shot delay to 10µs.
· No interrupt is used.
· Set channel 2 as a slave channel.
· Set the one-shot pulse width to 100µs.
· For output settings, set the initial output value to 0 and output level to active high.
· No interrupt is used.

Figure 1-3 shows the timing of the TAU one-shot pulse output function based on these settings.

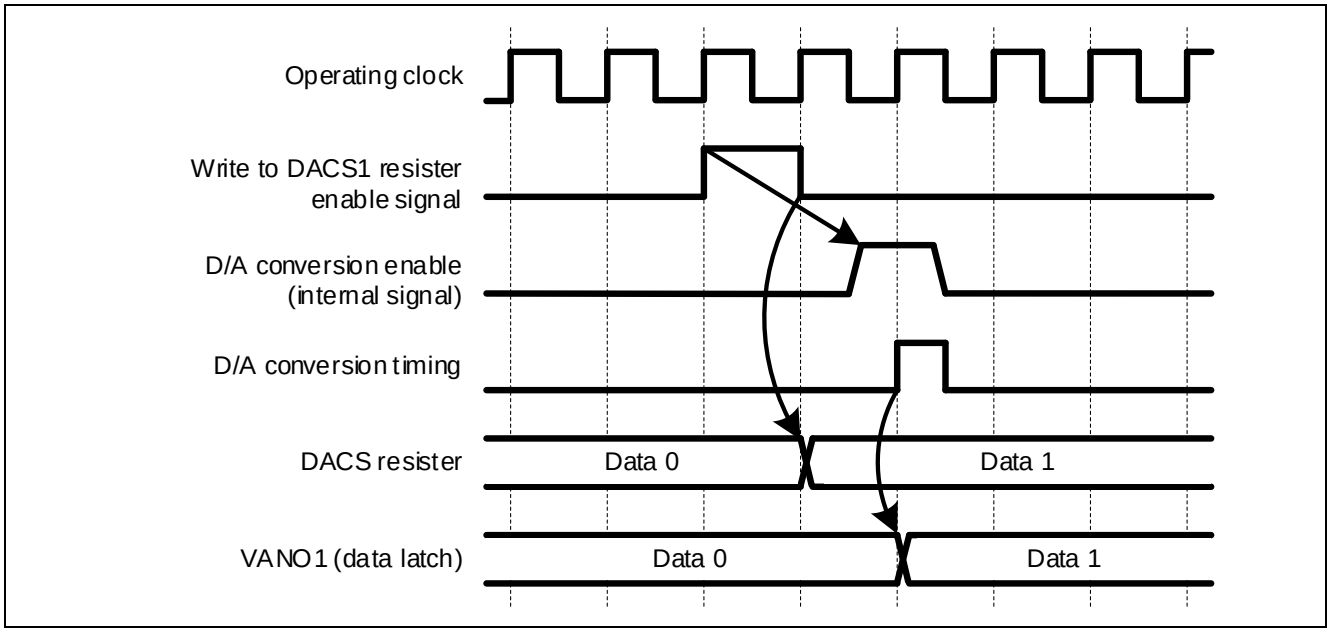
Figure 1-3 Timing of TAU's one-shot pulse output function.



The D/A converter uses D/A converter 1, which allows selection of 10-bit resolution.
＜DAC Initialization＞
· Set analog output to disabled.
· Set the D/A converter resolution to 10 bits.
· Set the D/A converter operation mode to normal mode.
· Set the conversion value to 512 (50%).

Figure 1-4 shows the output timing of the D/A converter based on these settings.

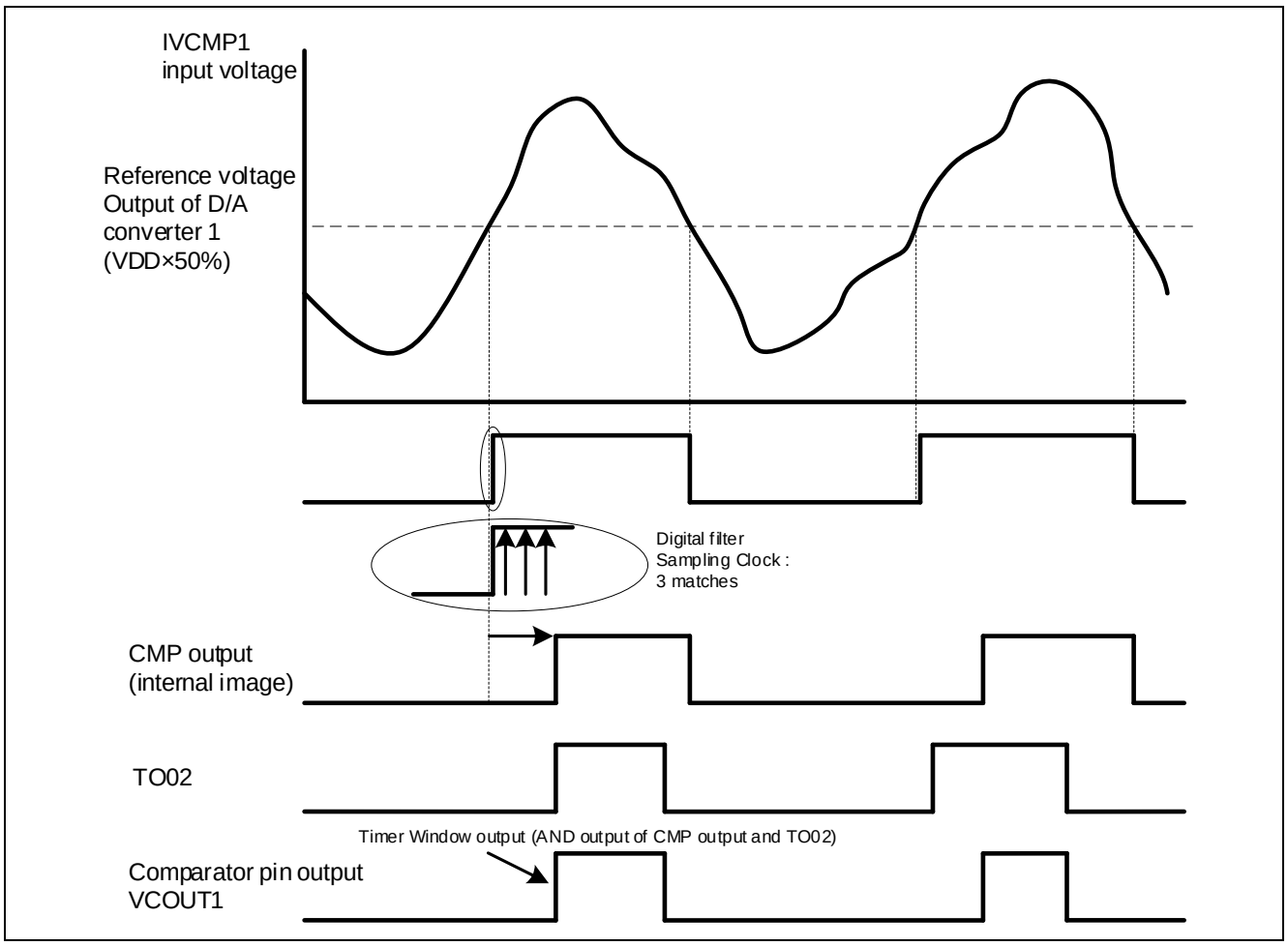
Figure 1-4 D/A Converter Output Timing.



The comparator uses Comparator 1.
<CMP Initialization>
· Set the reference voltage to the output of D/A Converter 1. (Refer to the previous page for details).
· Set the edge to rising.
· Set the digital filter to fCLK, fPLL, or fHOCO.
· Enable output from VCOUT1 in TIMER WINDOW output mode.
· No interrupt settings are made.

Figure 1-5 shows the output timing of the comparator based on these settings.

Figure 1-5 Comparator Output Timing.



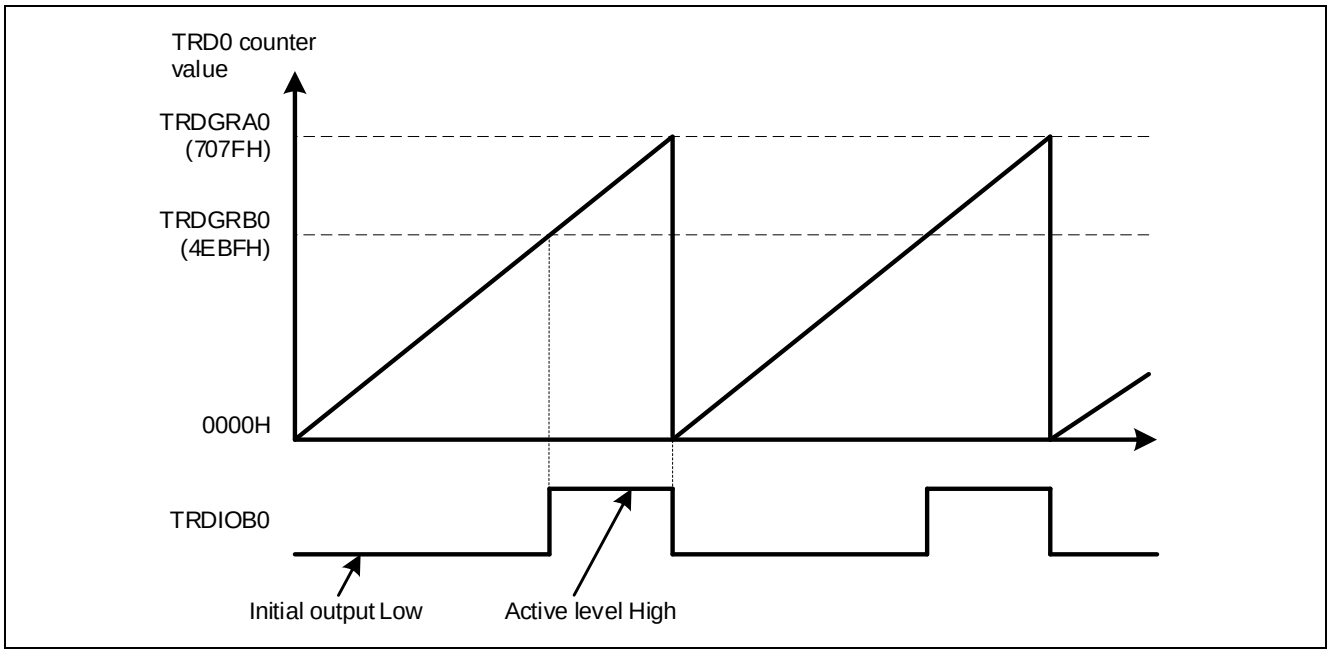
The Timer RD2 is used with the PWM function. It outputs a positive phase with a cycle of 300µs and a duty of 30% from the TRDIOB0 terminal.

＜Timer RD2 Initialization＞

- Set TRD20 for PWM output.
- Set the count source to fTRD (96MHz).
- Set the counter to continue counting even after matching TRDGRA0.
- Register function settings are set to general registers for both TRDGRD0 and TRDGRC0.
- PWM output settings are configured with a cycle of 300µs and a duty of 30%.
- The initial output of the TRDIOB0 pin is set to inactive level, and the output level is set to H active.
- No settings are made for pulse output force cutoff or interrupts.

Figure 1-6 shows the timing of the PWM output function of Timer RD2 based on these settings.

Figure 1-6 Timing of the Timer RD2 PWM Output Function.



2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

Table 2-1 Operation Confirmation Conditions

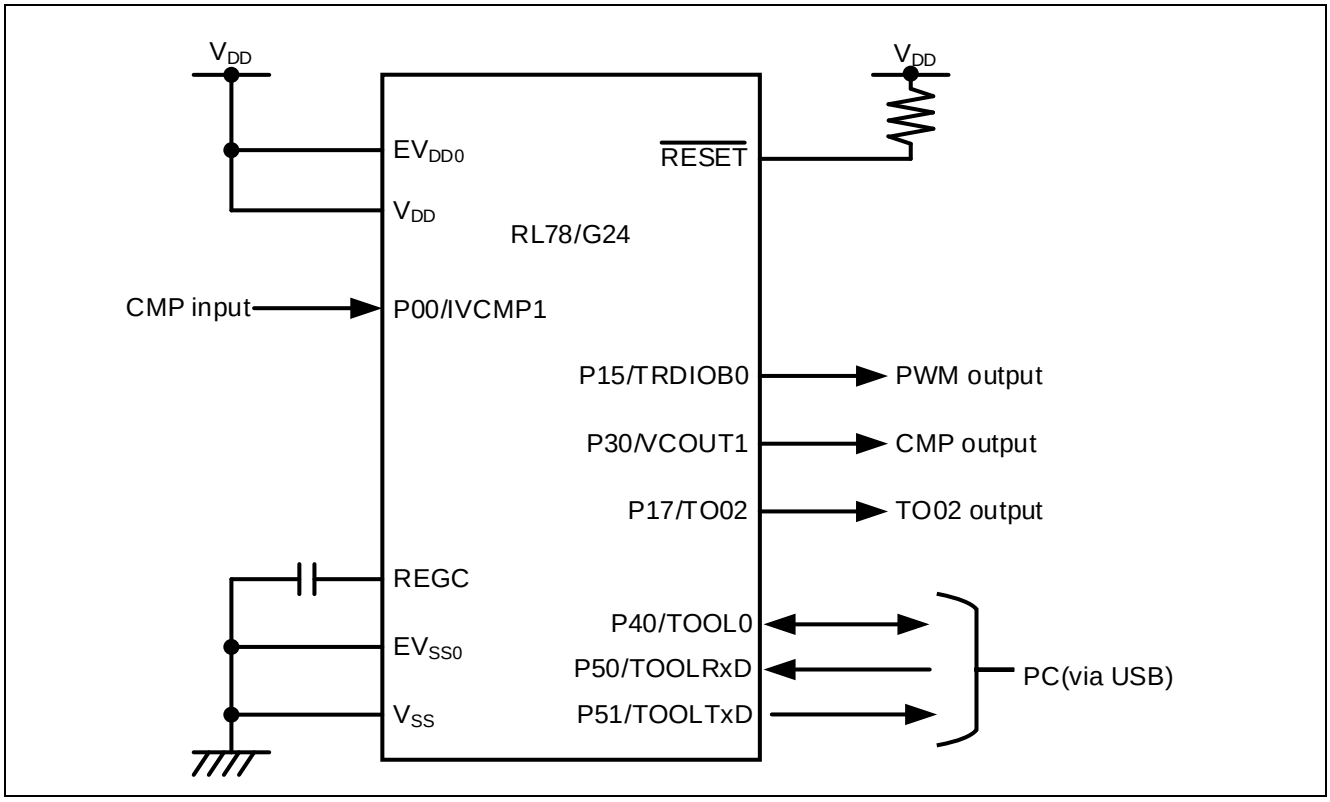
Item	Description
MCU used	RL78/G24 (R7F101GLG)
Operating frequency	· High-Speed On-Chip Oscillator Clock (fHOCO): 8MHz · PLL Oscillator Circuit Output (fPLL): 96MHz · CPU/Peripheral Hardware Clock (fCLK): 48MHz
Operating voltage	· 3.3V (Can operate between 2.7V to 5.5V) · LVD0 Operation (VLVD0): Reset Mode Rising edge = 2.97V Falling edge = 2.91V
Integrated development environment (CS+)	CS+ for CC V8.10.00 Manufactured by Renesas Electronics
C compiler (CS+)	CC-RL V1.12.01 Manufactured by Renesas Electronics
Integrated development environment (e^2 studio)	e^2 studio 2023-07 (23.7.0) Manufactured by Renesas Electronics
C compiler (e^2 studio)	CC-RL V1.12.00 Manufactured by Renesas Electronics
Integrated development Environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 Manufactured by IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.7.0
Board Support Package (r_bsp)	V.1.60
Emulator	CS+, e^2 studio: COM port IAR: E2 Emulator Lite
Board used	RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ)

3. Hardware Description

3.1 Example of Hardware Configuration

Figure 3-1 shows the hardware configuration example used in the sample code for this application.

Figure 3-1 Example of Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of used Pins

Table 3-1 shows the pins used and their functions.

Table 3-1 Pins Used and Their Functions

Pin name	I/O	Function
P15/TRDIOB0	Output	PWM output
P00/IVCMP1	Input	Comparator 1 positive side input
P30/VCOUT1	Output	Comparator 1 comparison result output
P17/TO02	Output	TO02 output

Caution: In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Description

4.1 Smart Configurator Settings

This section presents the settings of the Smart Configurator used in this sample program. The items and settings in each table for the Smart Configurator are described as they appear in the configuration screen.

4.1.1 System Configuration

The system configuration used in this sample program are shown below.

Note that the system settings used in this sample program are the same for the integrated development environments e2 studio and CS+, but different for IAR. Please adjust the settings appropriately according to the environment you are using.

Firstly, Figure 4-1 shows the system configuration used in this sample program (for e2 studio and CS+).

If you are conducting a COM port debug on the RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ), it is necessary to set the integrated development environments (e2 studio and CS+) appropriately. For details, please refer to the "RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)", specifically "7.1 Using COM Port Debugging with the e^2 studio" and "7.2 Using COM Port Debugging in CS+".

Figure 4-1 System Configuration (e^2 studio, CS+)

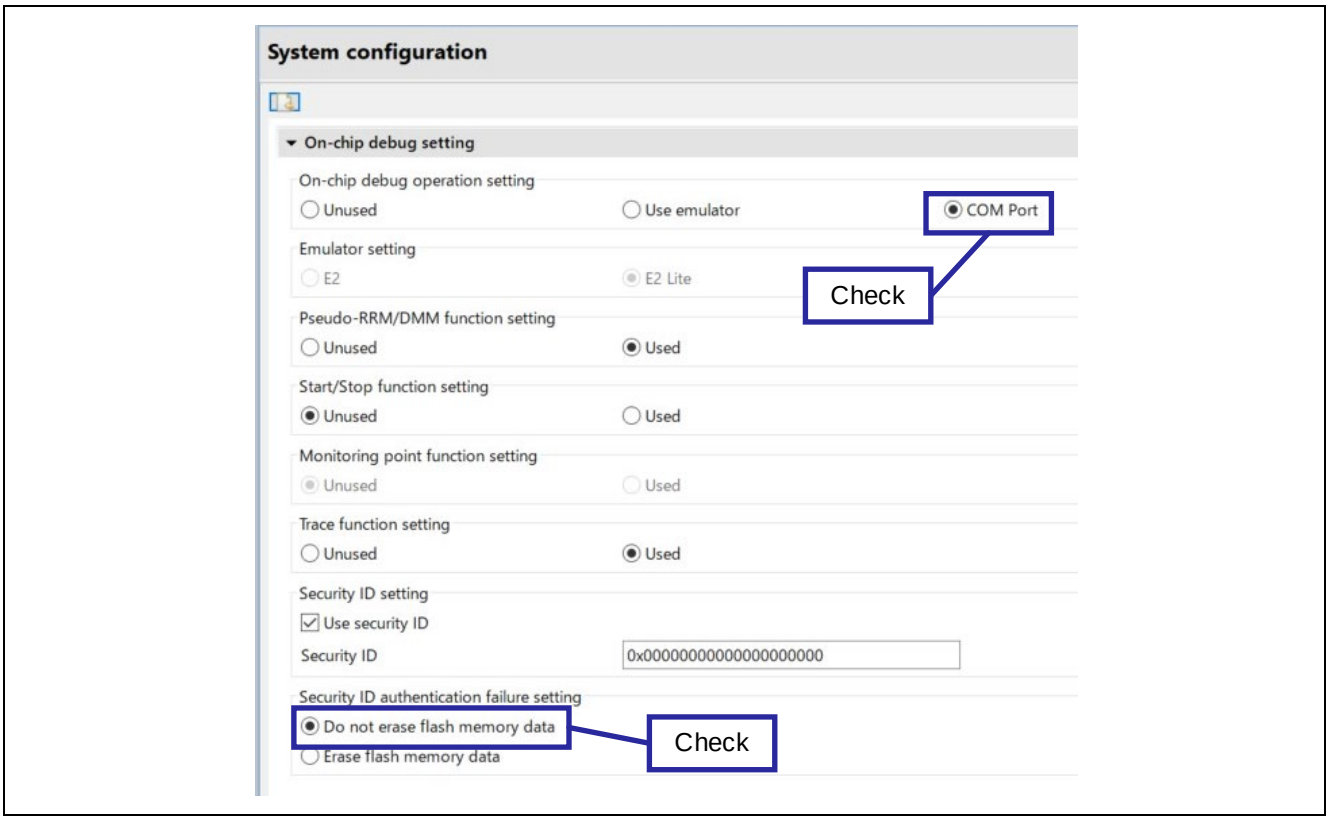
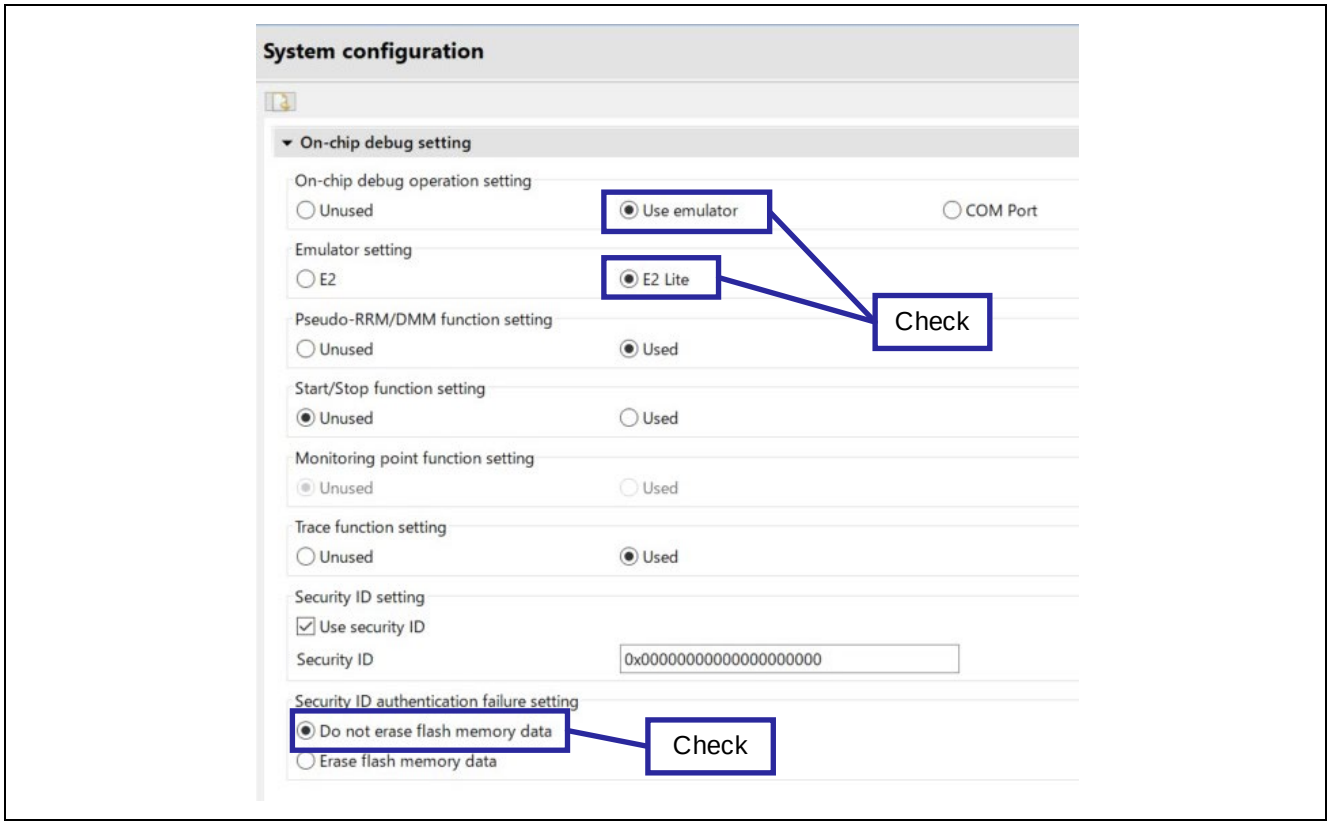


Figure 4-2 shows the system configurations used in this sample program for IAR.

Figure 4-2 System Configurations (IAR)



4.1.2 Component Configurations

This section presents the component configurations used in this sample program.

Table 4-1 Component Configurations (TAU)

Item	Content
Component	One-shot Pulse Output
Configuration Name	Config_TAU0_0
Resource	TAU0_0

Figure 4-3 Configuration of TAU0_0

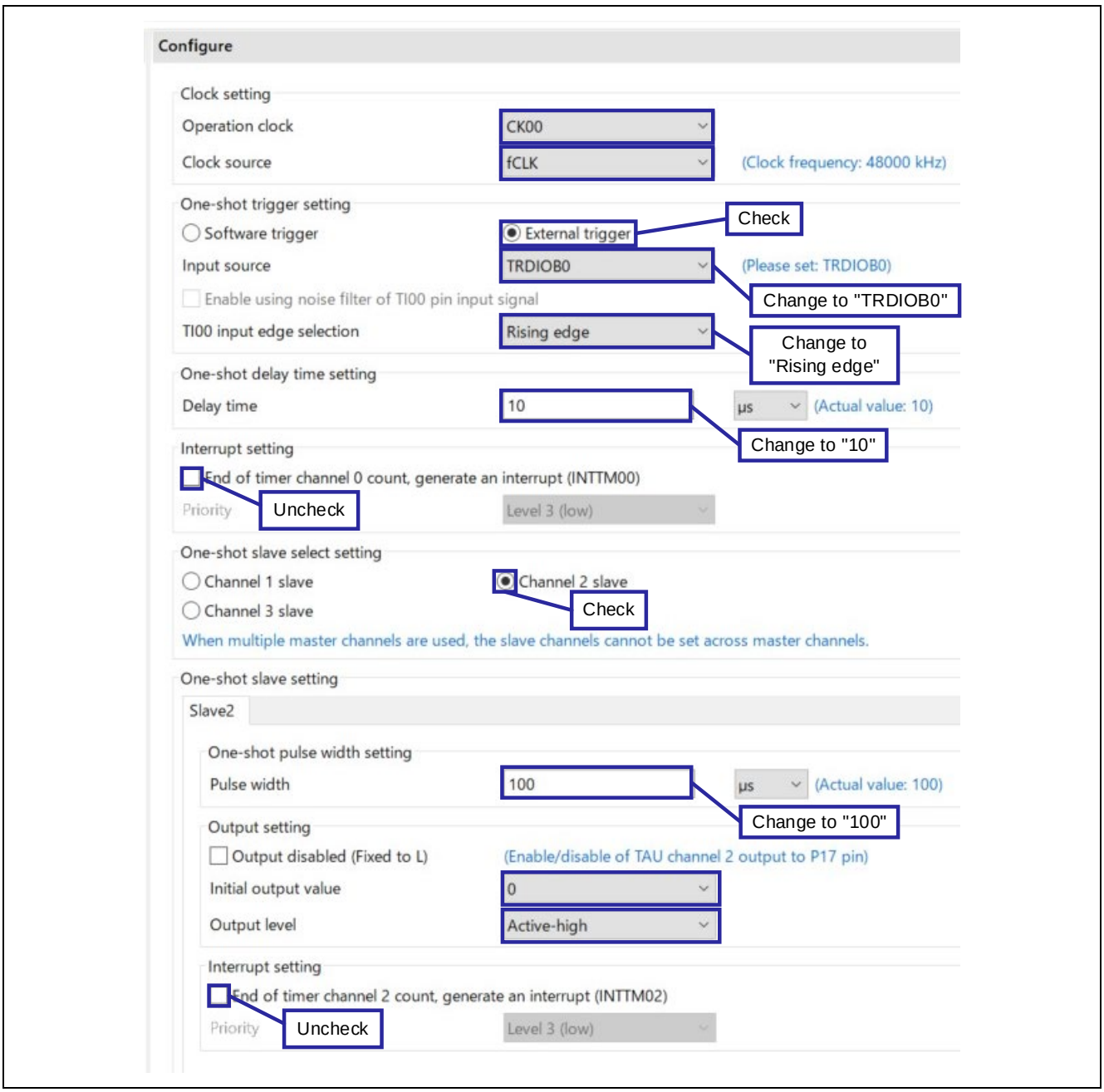


Table 4-2 Component Configurations (D/A Converter)

Item	Content
Component	D/A Converter
Configuration Name	Config_DAC1
Resource	DAC1

Figure 4-4 Configuration of D/A Converter

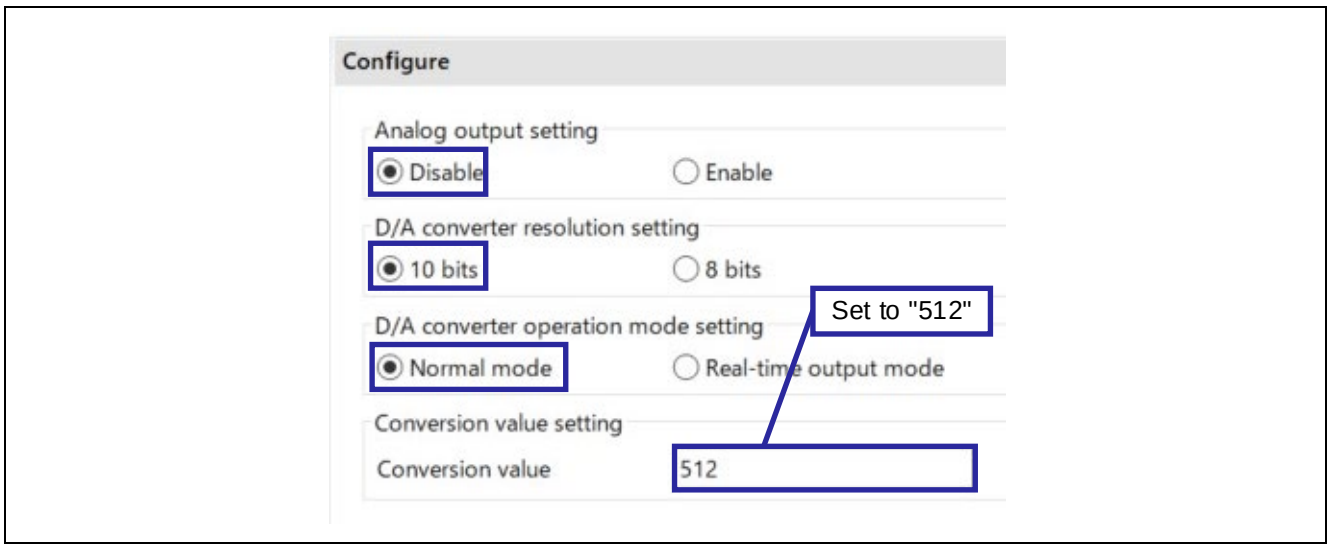


Table 4-3 Component Configurations（Comparator）

Item	Content
Component	Comparator
Configuration Name	Config_COMP1
Resource	COMP1

Figure 4-5 Configuration of COMP1

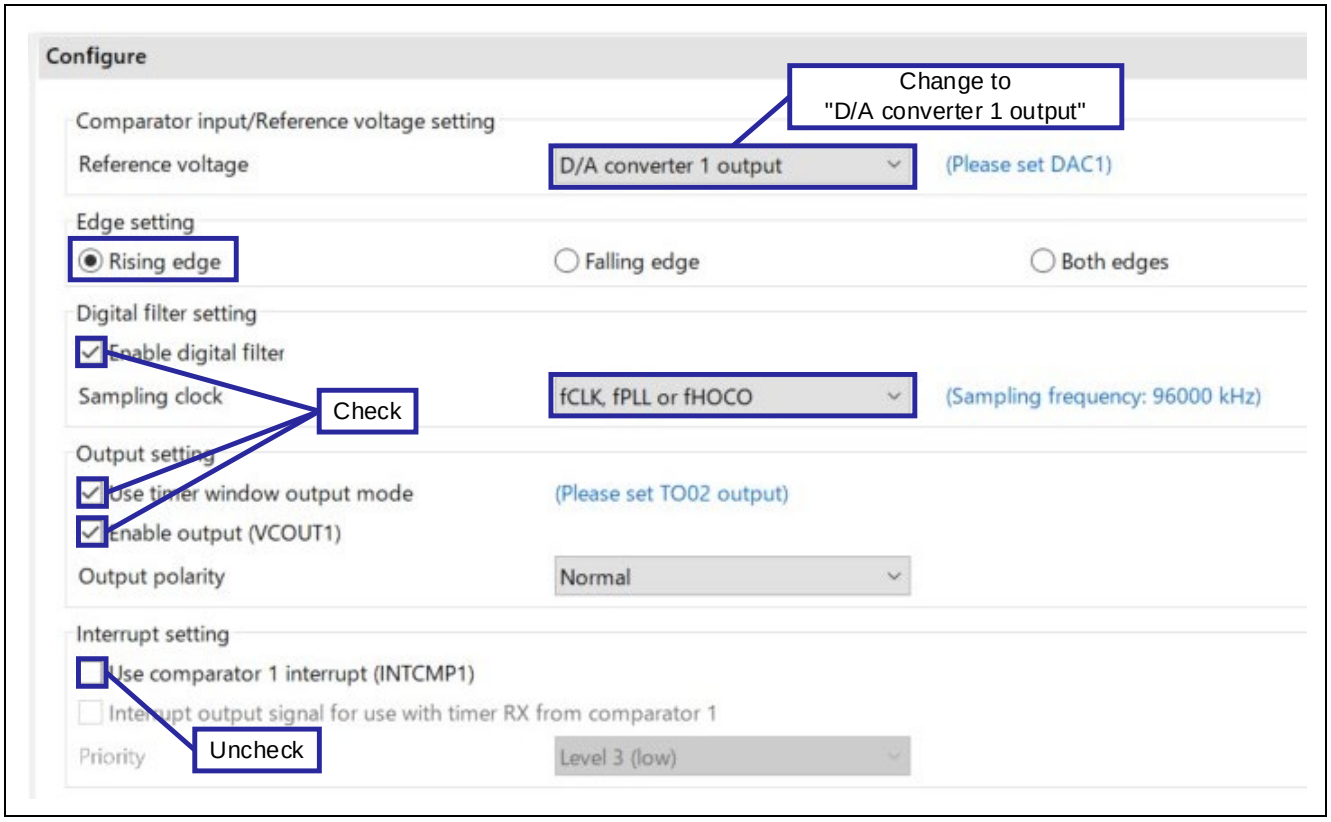
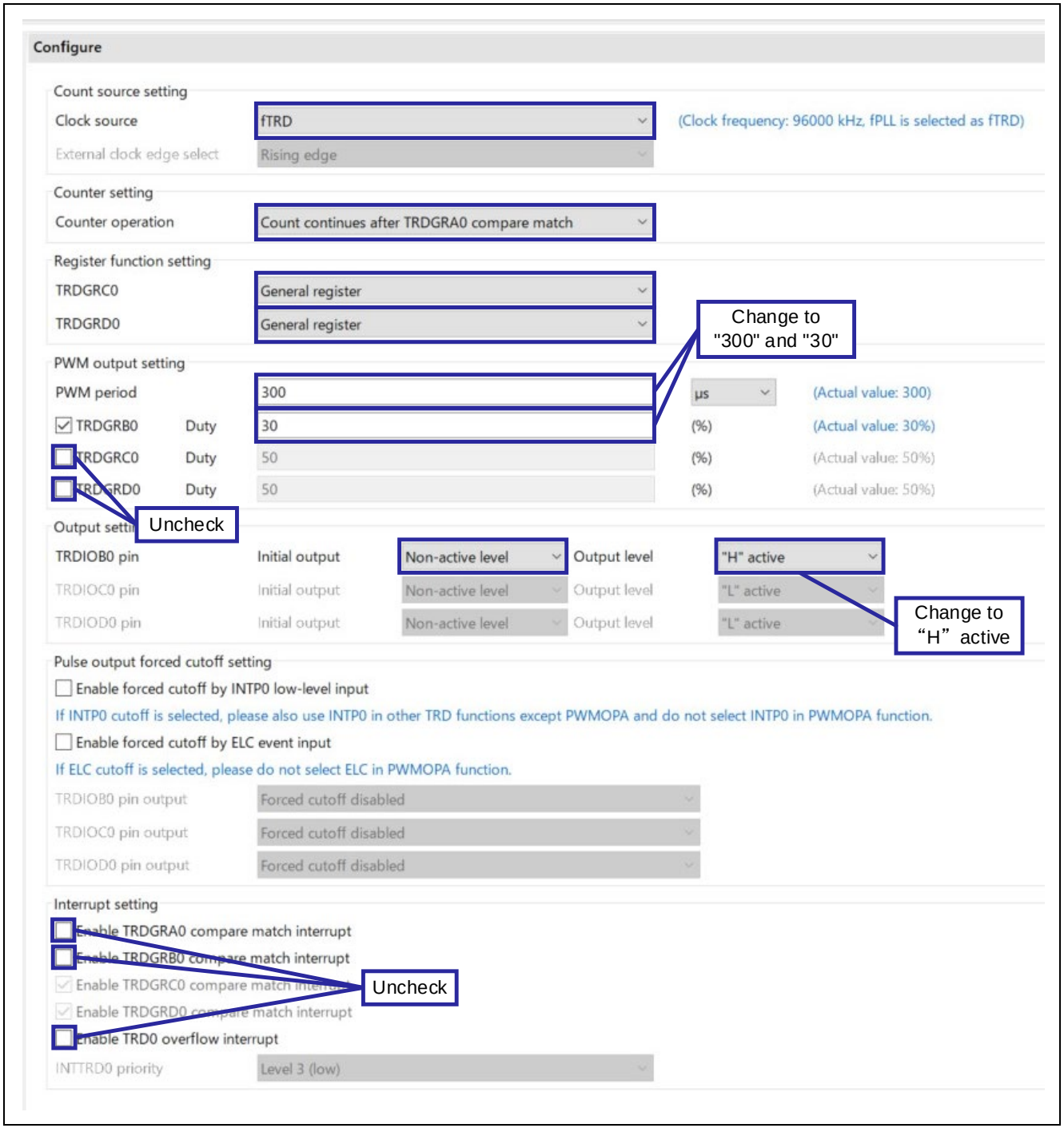


Table 4-4 Component Configurations (Timer RD2)

Item	Content
Component	PWM output
Configuration Name	Config_TRD0
Resource	PWM function
Component	TRD0

Figure 4-6 Configuration of TRD20



4.2 Folder Structure

Table 4-5 shows the structure of the source files/header files used in the sample code. Note that files automatically generated by the integrated development environment and files from the BSP environment are excluded.

Table 4-5 Folder Structure

Folder/File Name	Description	Generated by Smart Configurator
\r01an6784_timer_comp<DIR>NOTE 2	Sample project folder	
\src<DIR>	Program storage folder	
main.c	Sample Code Source File	
\smc_gen<DIR>	Smart Configurator Generated Folder	√
\Config_COMP1<DIR>	Program Storage Folder for COMP1	√
Config_COMP1.c	Source File for COMP1	√
Config_COMP1.h	Header File for COMP1	√
Config_COMP1_user.c	Interrupt Source File for COMP1	√NOTE 1
\Config_DAC1<DIR>	Program Storage Folder for DAC1	√
Config_DAC1.c	Source File for DAC1	√
Config_DAC1.h	Header File for DAC1	√
Config_DAC1_user.c	Interrupt Source File for DAC1	√NOTE 1
\Config_TAU0_0<DIR>	Program Storage Folder for TAU00	√
Config_TAU0_0.c	Source File for TAU00	√
Config_TAU0_0.h	Header File for TAU00	√
Config_TAU0_0_user.c	Interrupt Source File for TAU00	√NOTE 1
\Config_TRD0<DIR>	Program Storage Folder for TRD20	√
Config_TRD0.c	Source File for TRD20	√
Config_TRD0.h	Header File for TRD20	√
Config_TRD0_user.c	Interrupt Source File for TRD20	√NOTE 1
¥general<DIR>	Initialization, Common Program Storage Folder	√
¥r_bsp<DIR>	BSP Program Storage Folder	√
¥r_config<DIR>	Configuration Program Storage Folder	√

Note: "<DIR>" indicates a directory.
Note 1: Not used in the sample code.
Note 2: The sample code for IAR contains the r01an6784_timer_comp.ipcf file.
For details on the .ipcf file, please refer to "RL78 Smart Configurator User's Guide: IAR (R20AN0581).

4.3 List of Option Byte Settings

Table 4-6 shows the option byte settings.

Table 4-6 Option Byte Settings

Address	Setting Value	Description
000C0H/040C0H	1110 1111B (EFH)	Watchdog Timer stopped operation (Count stops after reset release)
000C1H/040C1H	1111 1011B (FBH)	LVD0 reset mode. Detection voltage: Rising 2.97V / Falling 2.91V
000C2H/040C2H	1110 1010B (EAH)	Flash operation mode: High-speed main mode. High-speed on-chip oscillator frequency: 8MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debug operation allowed

4.4 List of Constants

The sample code does not use any constants.

4.5 List of Global Variables

The sample code does not use any global variables.

4.6 List of Functions

Table 4-7 lists the functions used in the sample code. However, functions generated by the Smart Configurator that have not been modified are excluded.

Table 4-7 List of Functions

Function Name	Description	Source File
main	Main process	main.c

4.7 Function Specifications

The function specifications of the sample code are presented.

[Function Name] main

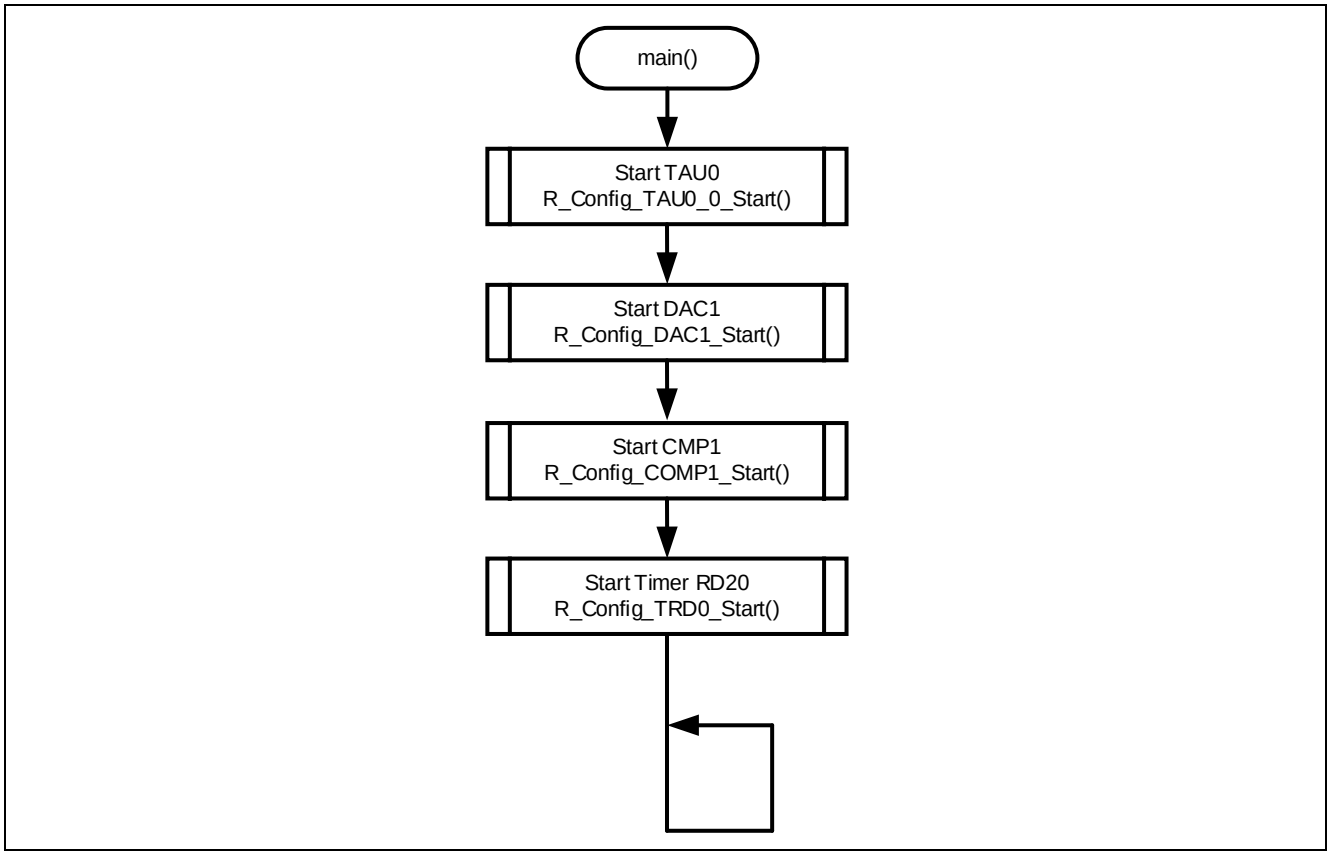
Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Explanation	Initialize the operation of TAU0 channel 0, channel 2, DAC1, CMP1, and timer RD20.
Arguments	-
Return value	-
Remarks	-

4.8 Flowchart

4.8.1 Main Process

Figure 4-7 shows the flowchart for the main process.

Figure 4-7 Main Process



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G24 User's Manual: Hardware (R01UH0961)

RL78 family User's Manual: Software (R01US0015)

RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)

RL78 Smart Configurator User's Gude: CS+ (R20AN0580)

RL78 Smart Configurator User's Gude: e2 studio (R20AN0579)

RL78 Smart Configurator User's Gude: IAR (R20AN0581)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.23	-	First Edition

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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