RL78/G24

Timer RD2 in Timer Mode (PWM Function)

Introduction

This document describes a method to output a PWM waveform using the timer mode's PWM function (hereinafter referred to as PWM function) in the RL78/G24 timer RD2.

Target Device

RL78/G24

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Specification overview

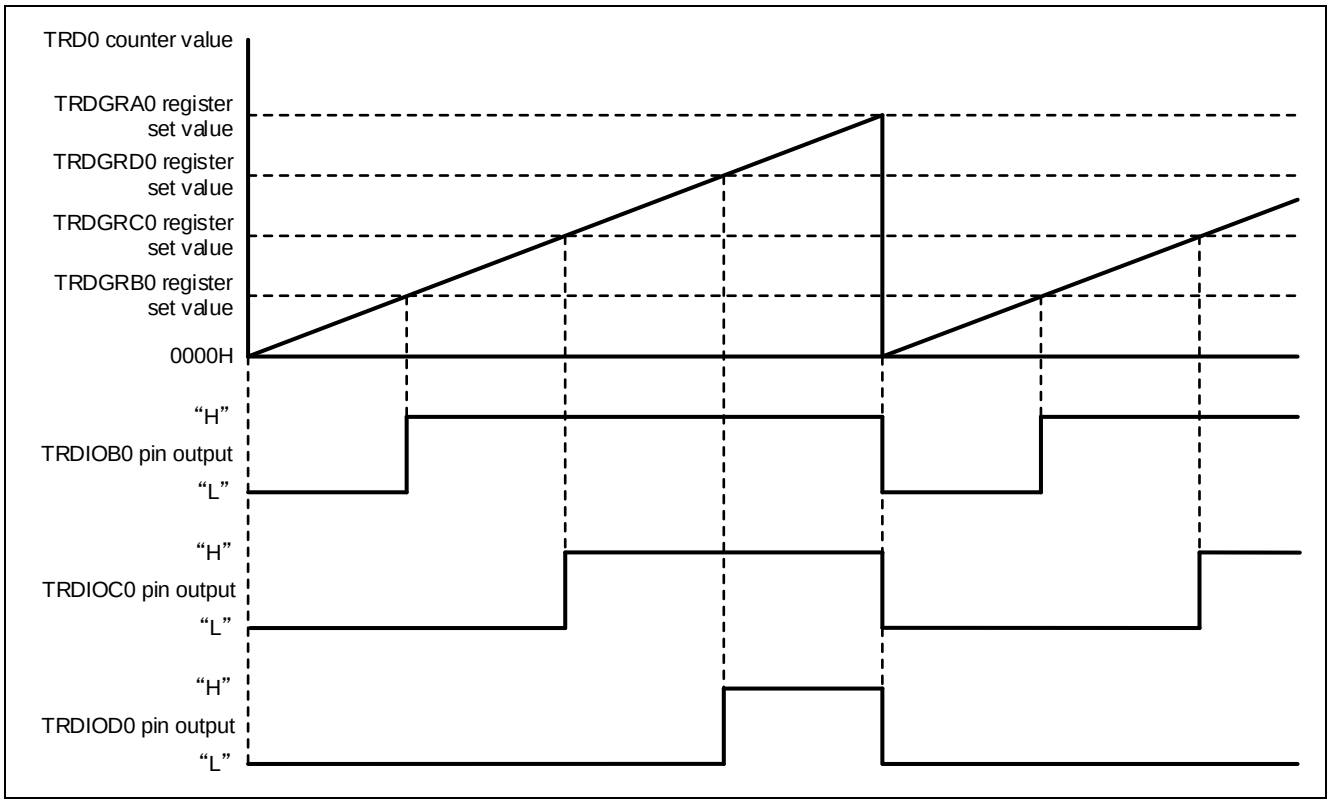
Three PWM waveforms with 100 µs periods are output.

Table 1-1 lists the Peripheral Function and Its Application. Figure 1-1 shows the Output Timing Diagram.

Table 1-1 Peripheral Functions and Their Usage

Peripheral	Usage
Timer RD2 (Timer RD20)	PWM waveform output

Figure 1-1 PWM Output Timing Diagram



1.2 Operation overview

Three PWM waveforms with 100 µs periods are output using the PWM function. Output signals are shown below.

·TRDIOB0 pin output: Inactive level low period (25 µs) → Active level high period (75 µs)

·TRDIOC0 pin output: Inactive level low period (50 µs) → Active level high period (50 µs)

·TRDIOD0 pin output: Inactive level low period (75 µs) → Active level high period (25 µs)

Timer RD2 settings are shown below.

<Settings>

· Set the timer RD2 for PWM output.

· Set the count source to fTRD (96MHz).

· Configure the counter to continue counting even after a compare match with the TRDGRA0.

· Set both the TRDGRC0 and TRDGRD0 register functionalities as general registers.

· For the PWM output setting, set the PWM period to 100µs and the duty cycles: 75% for TRDGRB0, 50% for TRDGRC0, and 25% for TRDGRD0.

· For TRDGRB0, TRDGRC0, and TRDGRD0, set the initial output to the non-active level and the output level to high active.

· Do not set pulse output forced cutoff.

· Enable the TRDGRA0 compare match interrupt.

1.2.1 Output Waveform

Below is a description for calculating the PWM period and PWM waveform output from each pin.

(1) PWM period:
Calculate the PWM period as follows:
100 [µs] = (1 / 96 [MHz]) × (TRDGRA0 + 1)
= 10.42 [ns] × 9600

(2) PWM output of the TRDIOB0 pin
Calculate the low inactive level period of the TRDIOB0 pin as follows:
25 [µs] = (1 / 96 [MHz]) × (TRDGRB0 + 1)
= 10.42 [ns] × 2400

(3) PWM output of the TRDIOC0 pin
Calculate the low inactive level period of the TRDIOC0 pin as follows:
50 [µs] = (1 / 96 [MHz]) × (TRDGRC0 + 1)
= 10.42 [ns] × 4800

(4) PWM output of the TRDIOD0 pin
Calculate the low inactive level period of the TRDIOD0 pin as follows:
75 [µs] = (1 / 96 [MHz]) × (TRDGRD0 + 1)
= 10.42 [ns] × 7200

Figure 1-2 shows the timing of the PWM function of timer RD2.

(1) The output at the TRDIOB0 terminal changes due to a compare match between the TRD0 counter value and the TRDGRB0 register set value.

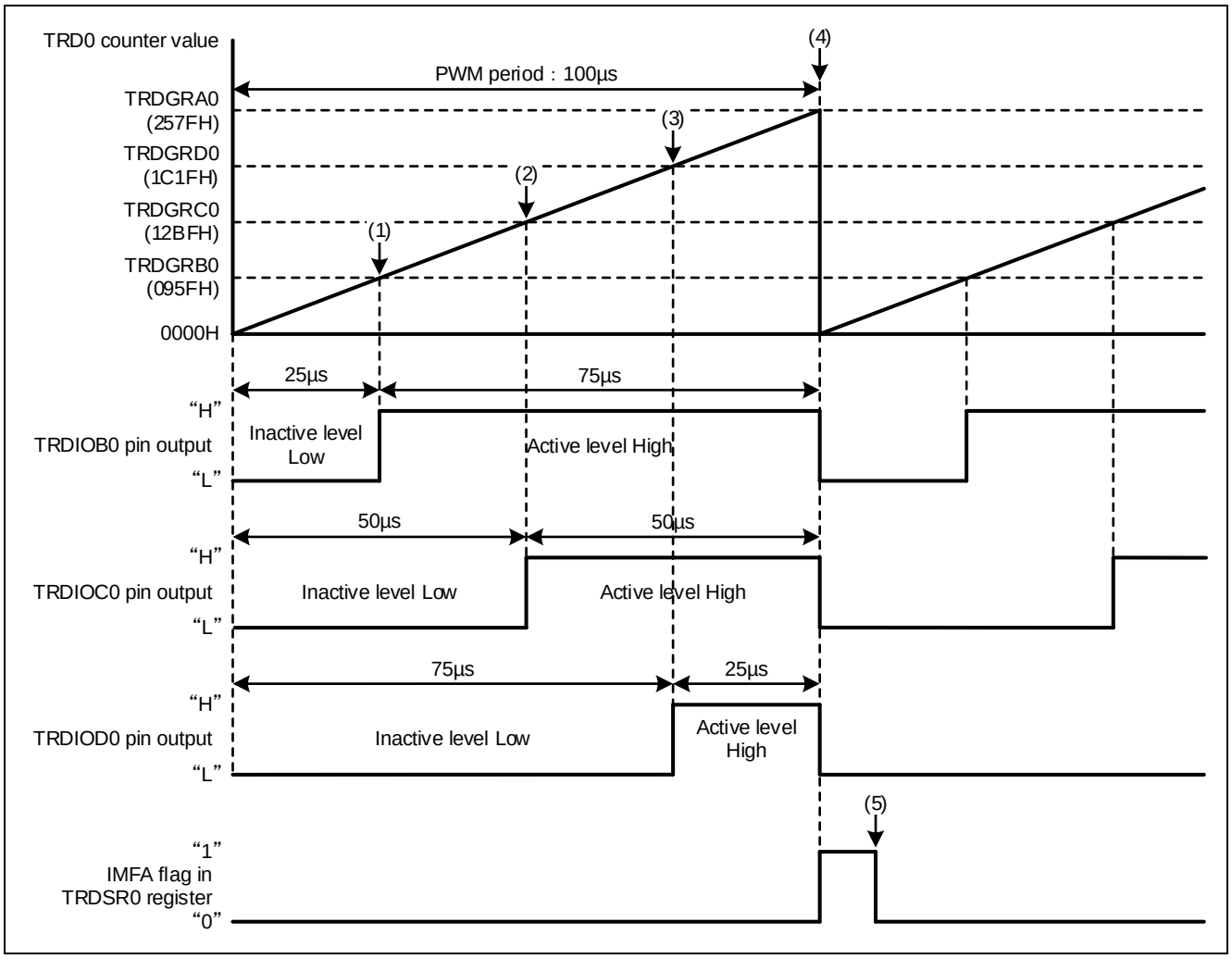
(2) The output at the TRDIOC0 terminal changes due to a compare match between the TRD0 counter value and the TRDGRC0 register set value.

(3) The output at the TRDIOD0 terminal changes due to a compare match between the TRD0 counter value and the TRDGRD0 register set value.

(4) Because of a compare match between the TRD0 counter value and the TRDGRA0 register set value, the TRD0 counter value is cleared. Additionally, the INTTRD0 interrupt occurs.

(5) Within the INTTRD0 interrupt processing, the program clears the compare match flag A (IMFA flag) in the timer RD status register 0 (TRDSR0 register).

Figure 1-2 Timing of the PWM function of timer RD2



2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

Table 2-1 Operation Confirmation Conditions

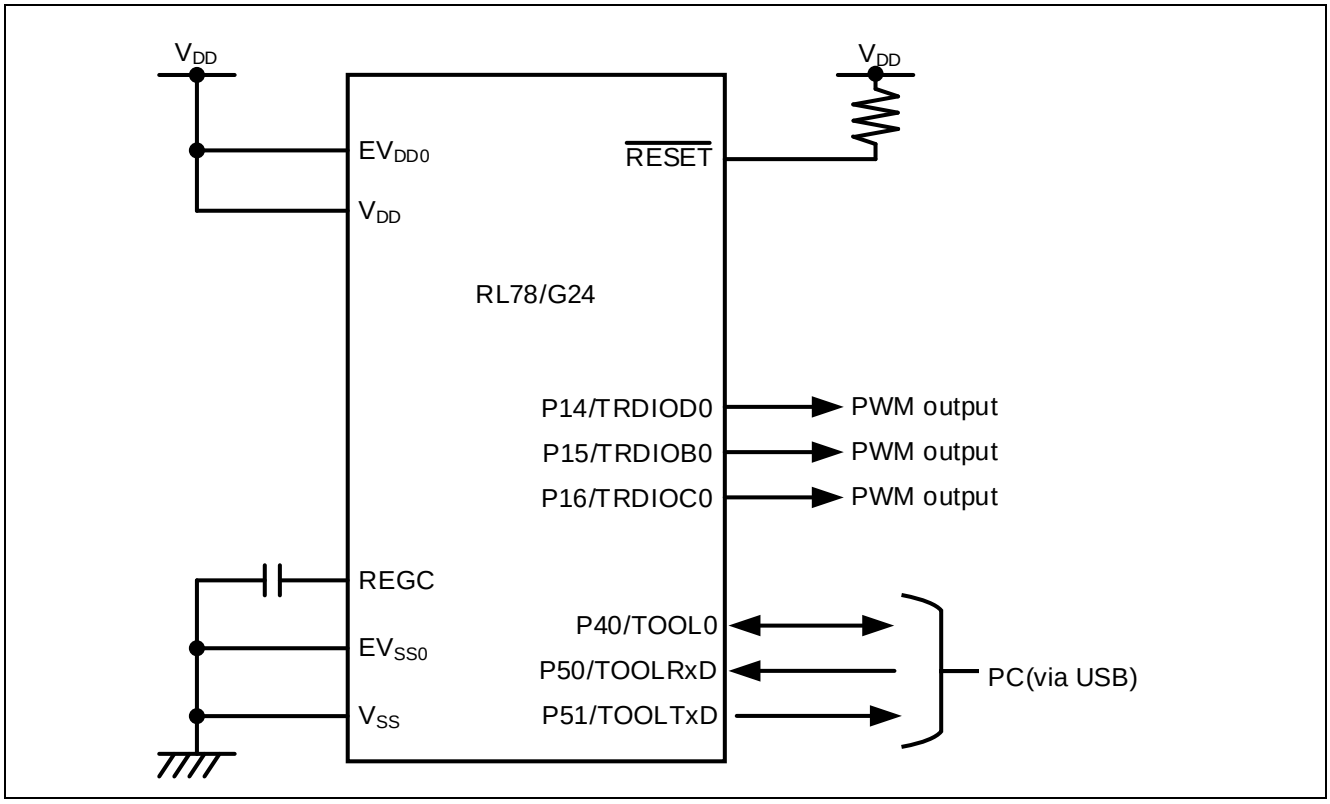
Item	Description
MCU used	RL78/G24 (R7F101GLG)
Operating frequency	· High-Speed On-Chip Oscillator Clock (fHOCO): 8MHz · PLL Oscillator Circuit Output (fPLL): 96MHz · CPU/Peripheral Hardware Clock (fCLK): 48MHz
Operating voltage	· 3.3V (Can operate between 2.7V to 5.5V) · LVD0 Operation (VLVD0): Reset Mode Rising edge = 2.97V Falling edge = 2.91V
Integrated development environment (CS+)	CS+ for CC V8.10.00 Manufactured by Renesas Electronics
C compiler (CS+)	CC-RL V1.12.01 Manufactured by Renesas Electronics
Integrated development environment (e^2 studio)	e^2 studio 2023-07 (23.7.0) Manufactured by Renesas Electronics
C compiler (e^2 studio)	CC-RL V1.12.00 Manufactured by Renesas Electronics
Integrated development Environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 Manufactured by IAR Systems
C compiler (IAR)	
Smart Configurator	V.1.7.0
Board Support Package (r_bsp)	V.1.60
Emulator	CS+, e^2 studio: COM port IAR: E2 Emulator Lite
Board used	RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ)

3. Hardware Description

3.1 Example of Hardware Configuration

Figure 3-1 shows the hardware configuration example used in the sample code for this application.

Figure 3-1 Example of Hardware Configuration



Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to VDD or VSS through a resistor).

Note 2. Connect any pins whose name begins with EVSS to VSS, and any pins whose name begins with EVDD to VDD, respectively.

Note 3. VDD must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of used Pins

Table 3-1 shows the pins used and their functions.

Table 3-1 Pins Used and Their Functions

Pin name	I/O	Function
P14/TRDIOD0	Input	PWM Output
P15/TRDIOB0	Input	PWM Output
P16/TRDIOC0	Input	PWM Output

Caution: In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Description

4.1 Smart Configurator Settings

This section presents the settings of the Smart Configurator used in this sample program. The items and settings in each table for the Smart Configurator are described as they appear in the configuration screen.

4.1.1 System Configuration

The system configuration used in this sample program are shown below.

Note that the system settings used in this sample program are the same for the integrated development environments e2 studio and CS+, but different for IAR. Please adjust the settings appropriately according to the environment you are using.

Firstly, Figure 4-1 shows the system configuration used in this sample program (for e2 studio and CS+).

If you are conducting a COM port debug on the RL78/G24 Fast Prototyping Board (RTK7RLG240C00000BJ), it is necessary to set the integrated development environments (e2 studio and CS+) appropriately. For details, please refer to the "RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)", specifically "7.1 Using COM Port Debugging with the e^2 studio" and "7.2 Using COM Port Debugging in CS+".

Figure 4-1 System Configuration (e^2 studio, CS+)

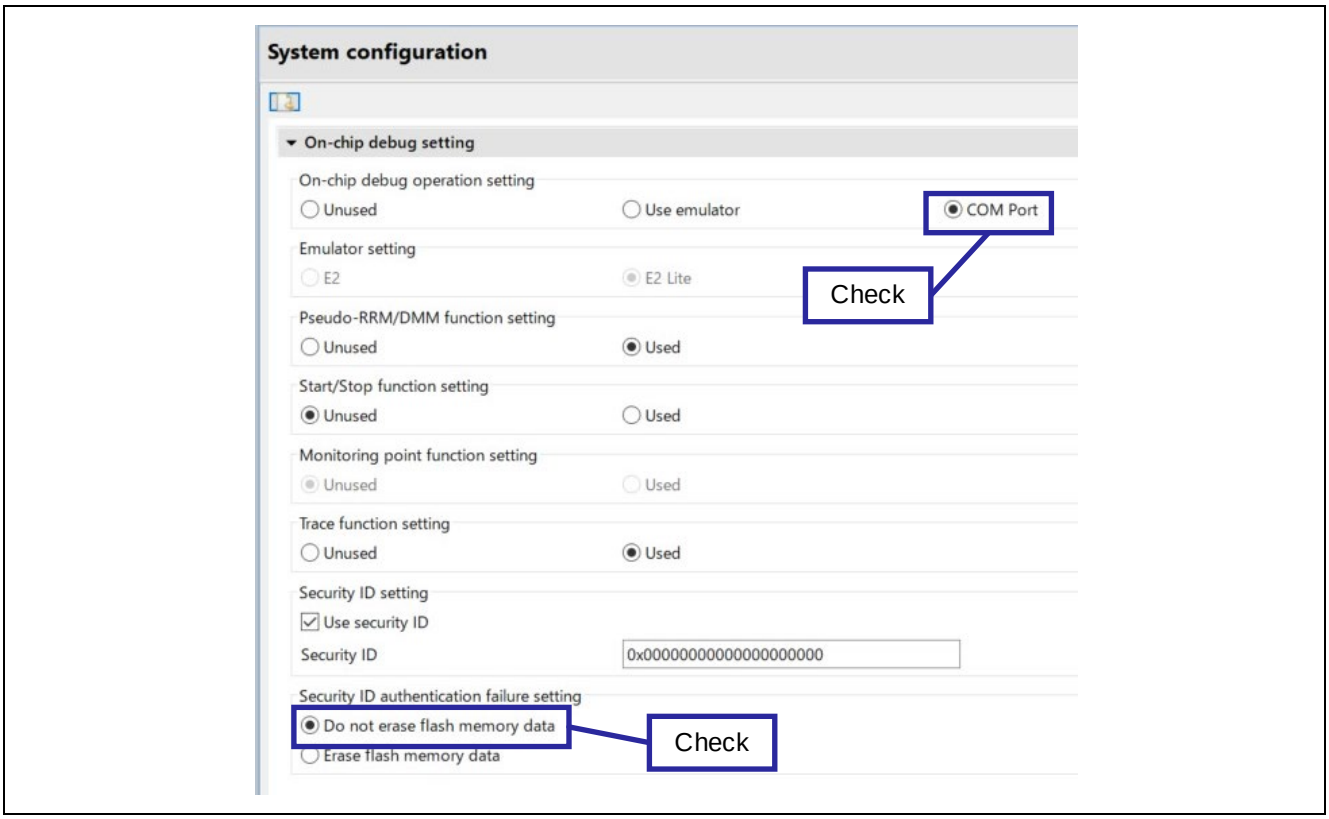
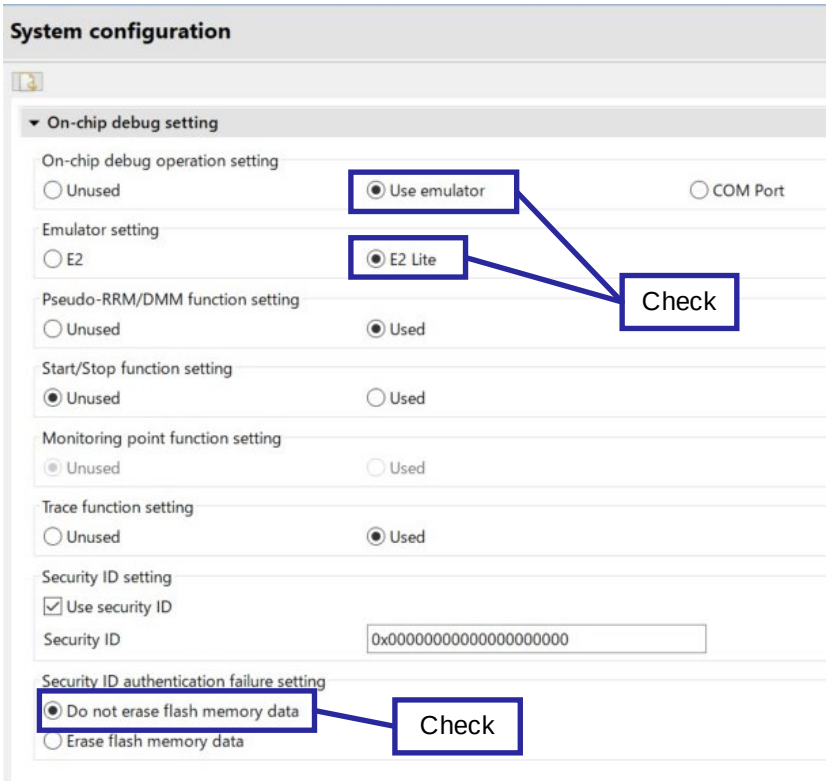


Figure 4-2 shows the system configurations used in this sample program for IAR.

Figure 4-2 System Configurations (IAR)



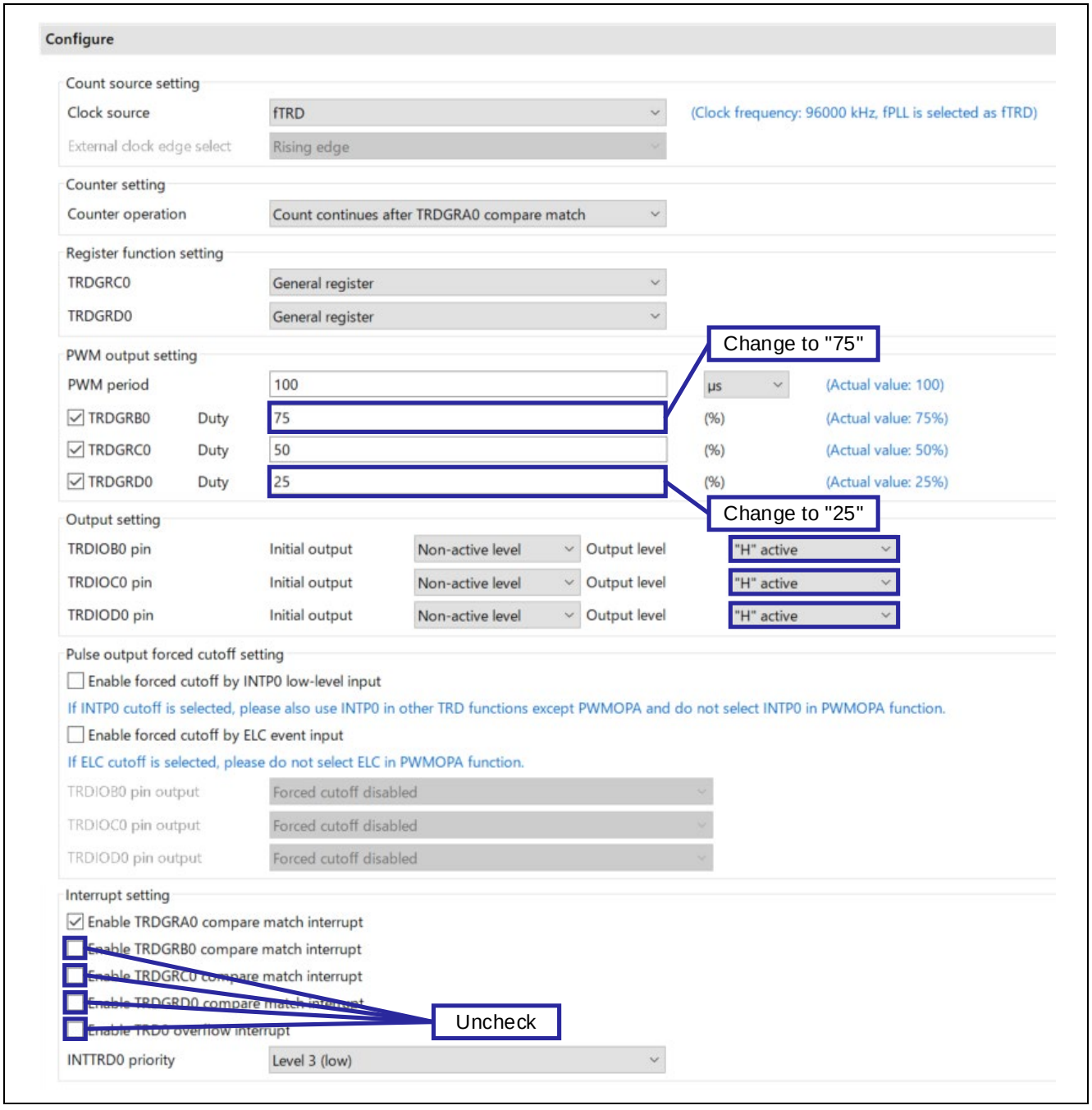
4.1.2 Component Configurations

This section presents the component configurations used in this sample program.

Table 4-1 Component Configurations (Timer RD2)

Item	Content
Component	PWM output
Configuration Name	Config_TRD0
Function	PWM function
Resource	TRD0

Figure 4-3 Configuration of Timer RD20



4.2 Folder Structure

Table 4-2 shows the structure of the source files/header files used in the sample code. Note that files automatically generated by the integrated development environment and files from the BSP environment are excluded.

Table 4-2 Folder Structure

Folder/File Name	Description	Generated by Smart Configurator
\r01an6893_trd2_pwm<DIR> NOTE 1	Sample code folder	
\src<DIR>	Program storage folder	
main.c	Sample code source file	
\smc_gen<DIR>	Smart configurator generated folder	√
\Config_TRD0<DIR>	TRD0 program storage folder	√
Config_TRD0.c	TRD0 source file	√
Config_TRD0.h	TRD0 header file	√
Config_TRD0_user.c	TRD0 interrupt source file	√
¥general<DIR>	Initialization and common program storage folder	√
¥r_bsp<DIR>	BSP program storage folder	√
¥r_config<DIR>	Program storage folder	√

Note: "<DIR>" indicates a directory.
Note 1: The sample code for IAR contains the r01an6893_trd2_pwm.ipcf file.
For details on the .ipcf file, please refer to "RL78 Smart Configurator User's Guide: IAR" (R20AN0581).

4.3 List of Option Byte Settings

Figure 4-3 shows the option byte settings.

Table 4-3 Option Byte Settings

Address	Setting Value	Description
000C0H/040C0H	1110 1111B (EFH)	Watchdog Timer stopped operation (Count stops after reset release)
000C1H/040C1H	1111 1011B (FBH)	LVD0 reset mode. Detection voltage: Rising 2.97V / Falling 2.91V
000C2H/040C2H	1110 1010B (EAH)	Flash operation mode: High-speed main mode. High-speed on-chip oscillator frequency: 8MHz
000C3H/040C3H	1000 0101B (85H)	On-chip debug operation allowed

4.4 List of Constants

Constant is not used in the sample code.

4.5 List of Variables

Table 4-4 shows the variables used in the sample code.

The following variables are generated by the Smart Configurator.

Table 4-4 Variables used in the sample code

Type	Variable Name	Contents	Function that uses the variable
uint8_t	g_trdsr0_dummy	dummy variable for the TRDSR0	r_Config_TRD0_trd0_interrupt

4.6 List of Functions

Table 4-5 lists the functions used in the sample code. However, functions generated by the Smart Configurator that have not been modified are excluded.

Table 4-5 List of Functions

Function Name	Description	Source File
main	main process	main.c
r_Config_TRD0_trd0_interrupt	IMFA flag clear process	Config_TRD0_user.c

4.7 Function Specifications

The function specifications of the sample code are presented.

[Function Name] main

Outline	Main process
Header	r_smc_entry.h
Declaration	void main (void);
Explanation	Start the operation of Timer RD20
Arguments	-
Return value	-
Remarks	-

[Function Name] r_Config_TRD0_trd0_interrupt

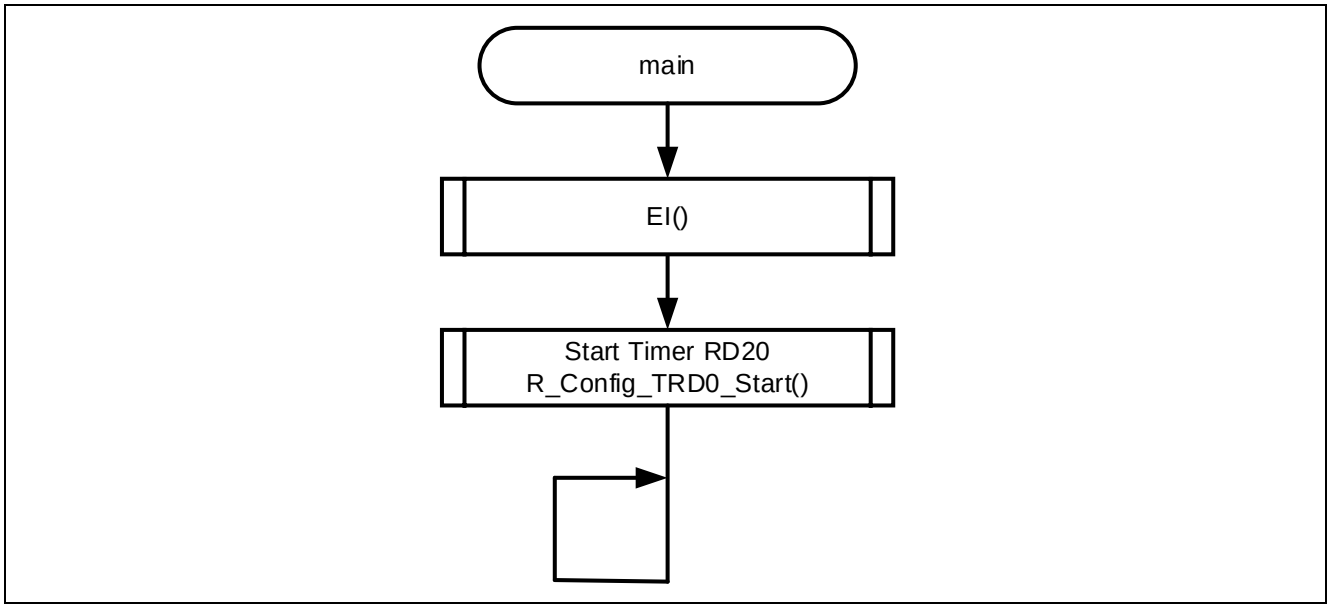
Outline	Compare Match Flag Clear Process
Header	Config_TRD0.h
Declaration	static void __near r_Config_TRD0_trd0_interrupt(void)
Explanation	IMFA flag clear process
Arguments	-
Return value	-
Remarks	-

4.8 Flowchart

4.8.1 Main Process

Figure 4-4 shows the flowchart for the main process.

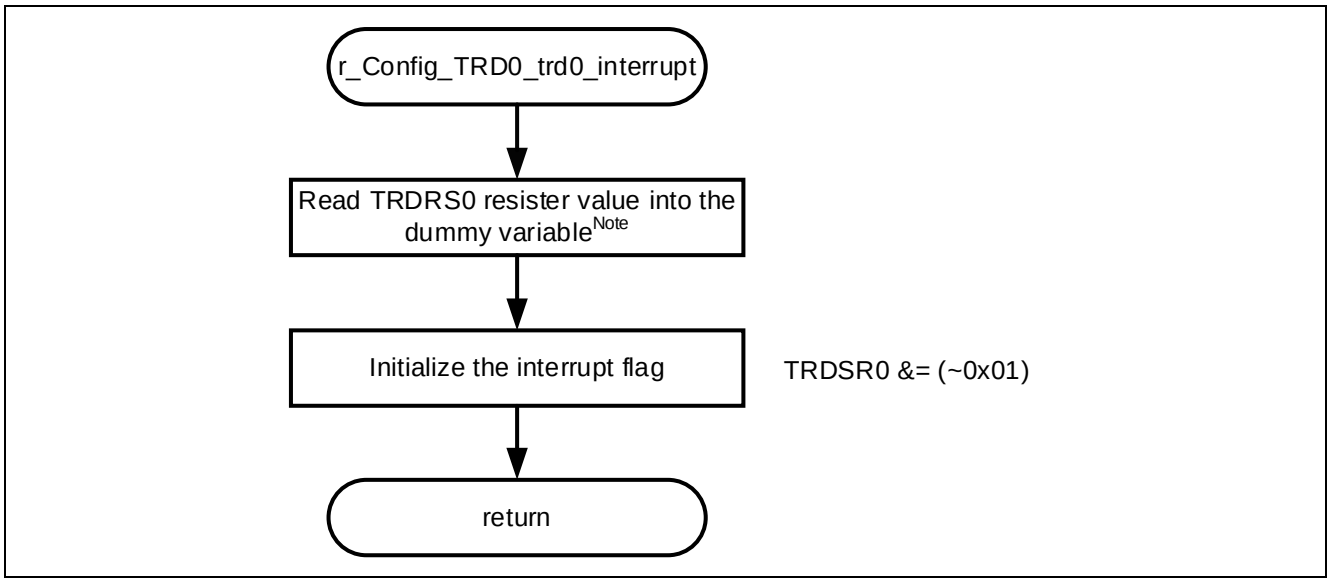
Figure 4-4 Main Process



4.9 r_Config_TRD0_trd0_interrupt function

Figure 4-6 shows the flowchart of r_Config_TRD0_trd0_interrupt function

Figure 4-5 r_Config_TRD0_trd0_interrupt function



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G24 User's Manual: Hardware (R01UH0961)

RL78 family User's Manual: Software (R01US0015)

RL78/G24 Fast Prototyping Board User's Manual (R20UT5091)

RL78 Smart Configurator User's Gude: CS+ (R20AN0580)

RL78 Smart Configurator User's Gude: e2 studio (R20AN0579)

RL78 Smart Configurator User's Gude: IAR (R20AN0581)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.07.23	-	First Edition

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
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   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
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   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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