RL78/G23

SMS Automatically Controlling SPI (Master) Communication

Introduction

This application note describes how to automatically control SPI master communication by using the SNOOZE mode sequencer (SMS) of the RL78/G23.

When an activation trigger is generated, the SNOOZE mode sequencer controls slave select pins and sends and receives data to implement SPI master communication.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification

1.1 Overview of Specification

In this application note, SPI master communication is automatically controlled by using the SNOOZE mode sequencer of the RL78/G23.

Pressing the switch connected to the P137 pin generates a trigger to start the SNOOZE mode sequencer.

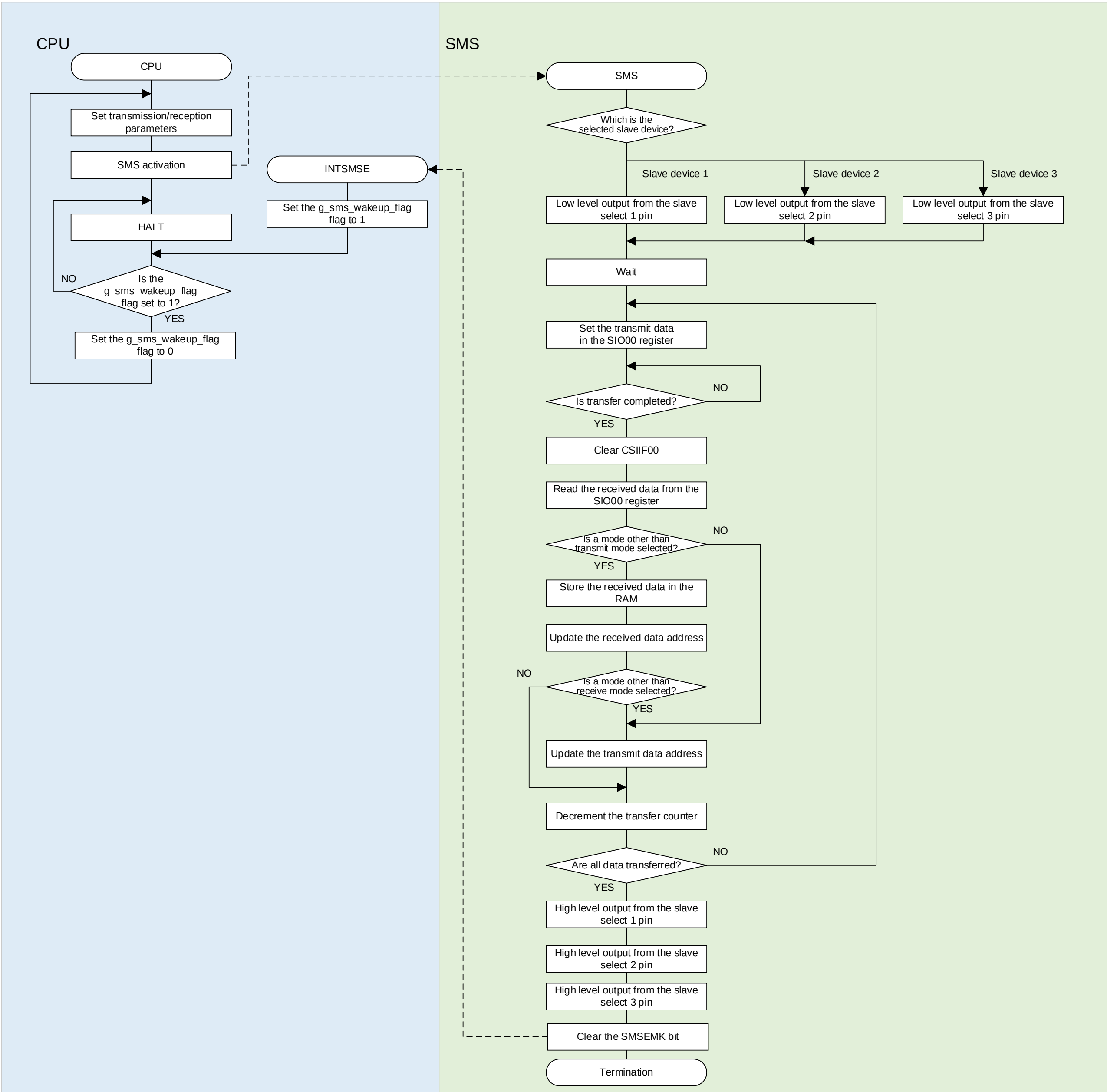
When the SNOOZE mode sequencer is started, it selects a slave device by controlling the slave select pin, reads data from the RAM, and then starts data transfer. When data transfer has finished, the received data is stored in the RAM. When all data transfer is completed, the SNOOZE mode sequencer clears selection of the slave device by controlling the slave select pin, and then generates an interrupt request.

Table 1-1 shows the peripheral functions to be used and Figure 1-1 shows an overview of operation.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
External interrupt (INTP3)	Triggers starting the SNOOZE mode sequencer.
SNOOZE mode sequencer	Controls slave select pins and performs CSI00 master transmission/reception.
CSI00	Data transmission/reception

Figure 1-1 Operation overview



1.1.1 Specification of SPI Master Communication Using the SNOOZE Mode Sequencer

SPI master communication using the SNOOZE mode sequencer supports three slave devices. A slave device is selected based on the value set for the p_sms_slave_select variable. The SNOOZE mode sequencer automatically controls the slave select pin at the beginning and end of the communication.

Item	Set value of the p_sms_slave_select variable	Slave select pin
Slave device 1	SLAVE1 (0x0000)	P50
Slave device 2	SLAVE2 (0x0001)	P51
Slave device 3	SLAVE3 (0x0002)	P52

SPI master communication using the SNOOZE mode sequencer supports the following operation modes. An operation mode is selected based on the value set for the p_sms_mode variable. In addition, specify the transmission/reception count for the p_sms_counter variable, the transmit data storage address for the p_sms_send_add variable, and the receive data storage address for the p_sms_receive_add variable. The SNOOZE mode sequencer automatically controls the number of transmission and reception cycles.

Operation mode	Set value of the p_sms_mode variable	Operation
Send mode	SEND (0x0000)	- Read the transmit data from the RAM, and then store it in the SIO00 register. - Read the received data from the SIO00 register, and then discard the value. - The transmit data storage address is updated. - The receive data storage address is not updated.
Receive mode	RECEIVE (0x0001)	- Read the transmit data from the RAM, and then store dummy data in the SIO00 register. - Read the received data from the SIO00 register, and then store it in the RAM. - The transmit data storage address is not updated. - The receive data storage address is updated.
Send/receive mode	SEND_RECEIVE (0x0002)	- Read the transmit data from the RAM, and then store it in the SIO00 register. - Read the received data from the SIO00 register, and then store it in the RAM. - The transmit data storage address is updated. - The receive data storage address is updated.

1.2 Outline of Operation

In this sample code, when a pressing of the switch connected to the P137 pin is detected, a low-level pulse is output from the P30 pin to generate an external interrupt request (INTP3). This external interrupt request triggers activation of the SNOOZE mode sequencer. After that, the HALT instruction is executed and the CPU enters the standby state.

The SNOOZE mode sequencer sets the slave select pin (P50) for low-level output and selects slave device 1. The SNOOZE mode sequencer then reads the transmit data from the RAM, and then starts data transfer to slave device 1. The SNOOZE mode sequencer waits until data transfer is completed. When data transfer is completed, the SNOOZE mode sequencer stores the received data in the RAM. When data transmission and reception is repeated 16 times and the last transmission and reception ends, the SNOOZE mode sequencer sets the slave select pin (P50) for high-level output and clears the selection of slave device 1. Finally, the SNOOZE mode sequencer generates an interrupt request to release the CPU from the standby state.

The CPU continues to detect the status of the switch connected to the P137 pin.

The following describes the major settings of the peripheral functions.

(1) Initial settings of the external interrupt

- Set the INTP3 pin so that the falling edge is the effective edge.

(2) Initial settings of the simple SPI

- Configure CSI00 for master transmit/receive operations.
- Set the transfer mode to single transfer mode.

(3) Initial settings of the SNOOZE mode sequencer

For details about the values to be set, see 4.7 Setting Up the SNOOZE Mode Sequencer

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2-1 Operation Confirmation Conditions

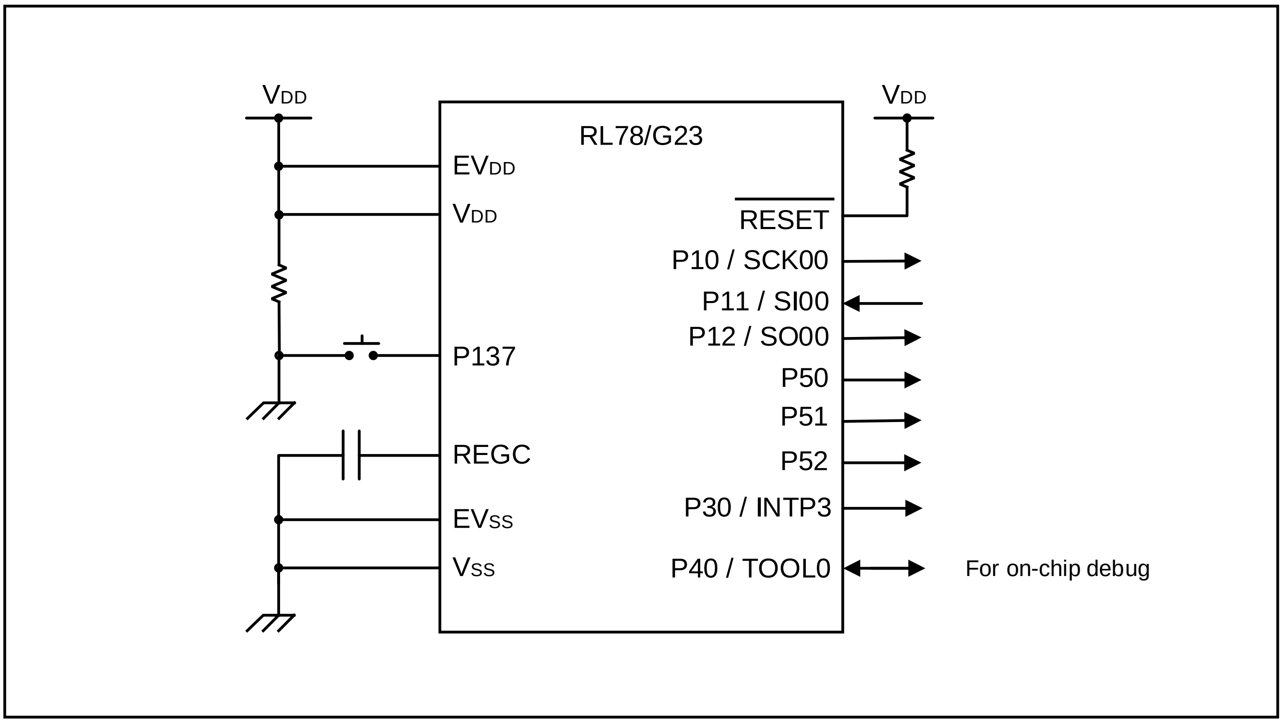
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	● High-speed on-chip oscillator clock (f_{IH}): 32 MHz ● Low-speed on-chip oscillator clock (f_{IL}): 32.768 kHz ● CPU/peripheral hardware clock: 32 MHz
Operating voltage	During V_{DD} operation: 3.3 V LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ V8.09.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2023-04 (23.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.12.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.2 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.2.2420 from IAR Systems Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note 1. This schematic circuit diagram is simplified to show the outline of connections. When creating circuits, design them so that they meet electrical characteristics by properly performing pin processing. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)

Note 2. Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Function
P10 / SCK00	Output	CSI00 serial clock
P11 / SI00	Input	CSI00 serial data
P12 / SO00	Output	CSI00 serial data
P30 / INTP3	Output	SNOOZE mode sequencer activation trigger
P50	Output	Slave select signal of slave device 1
P51	Output	Slave select signal of slave device 2
P52	Output	Slave select signal of slave device 3
P137	Input	Switch input

In this application note, the P30 and INTP3 pins, which are used as external interrupts, are set for output. This is because the high/low level of the output from the P30 pin is controlled by using a CPU instruction to generate an external interrupt request (from the INTP3 pin) that triggers the SNOOZE mode sequencer.

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V ～ 1.95 V) At falling edge TYP. 1.86 V (1.80 V ～ 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000100B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
SLAVE1	0x0000	Setting value of slave device 1
SLAVE2	0x0001	Setting value of slave device 2
SLAVE3	0x0002	Setting value of slave device 3
SEND	0x0000	Setting value for master transmission
RECEIVE	0x0001	Setting value for master reception
SEND_RECEIVE	0x0002	Setting value for master transmission/reception

4.3 List of Variables

Table **4-3** lists global variables.

Table 4-3 Global Variables

Type	Variable Name	Description	Function Used
*(volatile __near unsigned short *)0x3C2	p_sms_counter	Transmission/reception count (SMSG1 register)	main r_main_user_init
*(volatile __near unsigned short *)0x3C4	p_sms_mode	Operation mode (SMSG2 register)	main r_main_user_init
*(volatile __near unsigned short *)0x3C6	p_sms_slave_select	Slave device selection (SMSG3 register)	main r_main_user_init
*(volatile __near unsigned short *)0x3C8	p_sms_send_add	Transmit data storage address (SMSG4 register)	main r_main_user_init
*(volatile __near unsigned short *)0x3CA	p_sms_receive_add	Receive data storage address (SMSG5 register)	main r_main_user_init

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
main()	Main processing
r_main_user_init()	Main initial settings
r_main_sms_trigger()	SNOOZE mode sequencer activation
r_main_sms_csi00()	Communication status settings

4.5 Specification of Functions

The function specifications of the sample code are shown below.

main()

Outline	Main processing
Header	r_cg_macrodriver.h、Config_CSI00.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	void main(void);
Description	This function starts the SNOOZE mode sequencer, and then waits for completion of the SPI master communication.
Argument	None
Return Value	None

r_main_user_init()

Outline	Main initial settings
Header	r_cg_macrodriver.h、Config_CSI00.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	static void r_main_user_init(void);
Description	This function specifies the initial settings for the peripheral functions that are used for the application.
Argument	None
Return Value	None

r_main_sms_trigger()

Outline	SNOOZE mode sequencer activation
Header	r_cg_macrodriver.h、Config_CSI00.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h
Declaration	static void r_main_sms_trigger(void);
Description	This function generates a trigger to start the SNOOZE mode sequencer.
Argument	None
Return Value	None

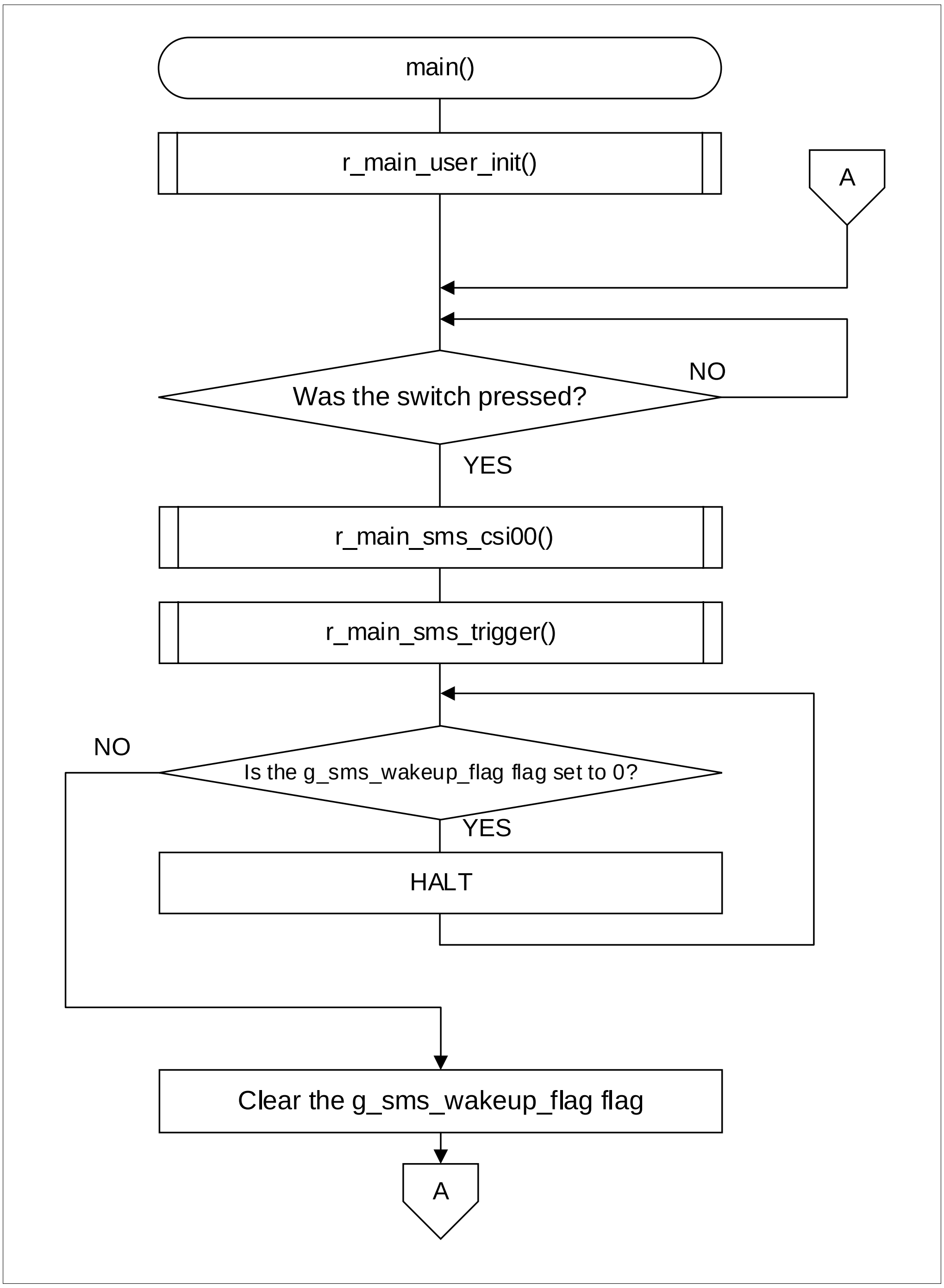
r_main_sms_csi00()		
Outline	Communication status settings	
Header	r_cg_macrodriver.h、Config_CSI00.h、Config_INTC.h、Config_SMS.h、r_cg_userdefine.h	
Declaration	static void r_main_sms_csi00(uint8_t * const tx_buf, uint16_t tx_num, uint8_t * const rx_buf);	
Description	This function specifies the transmission/reception count, transmit data storage address, and receive data storage address.	
Argument	tx_buf	Transmission/reception count
	tx_num	Transmit data storage address
	rx_buf	Receive data storage address
Return Value	None	

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 show flowcharts of the main processing.

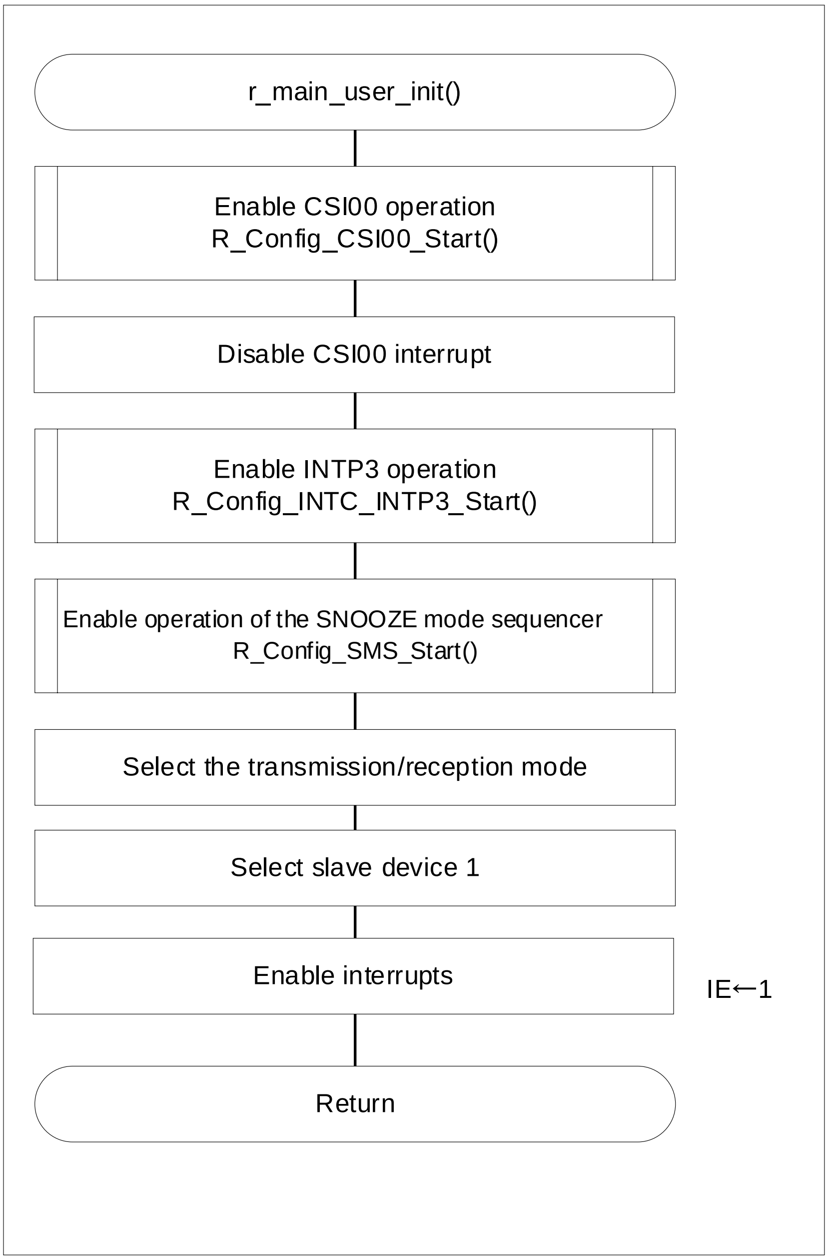
Figure 4-1 Main Processing



4.6.2 Main Initial Settings

Figure 4-2 shows the flowchart of the initial settings for main functions.

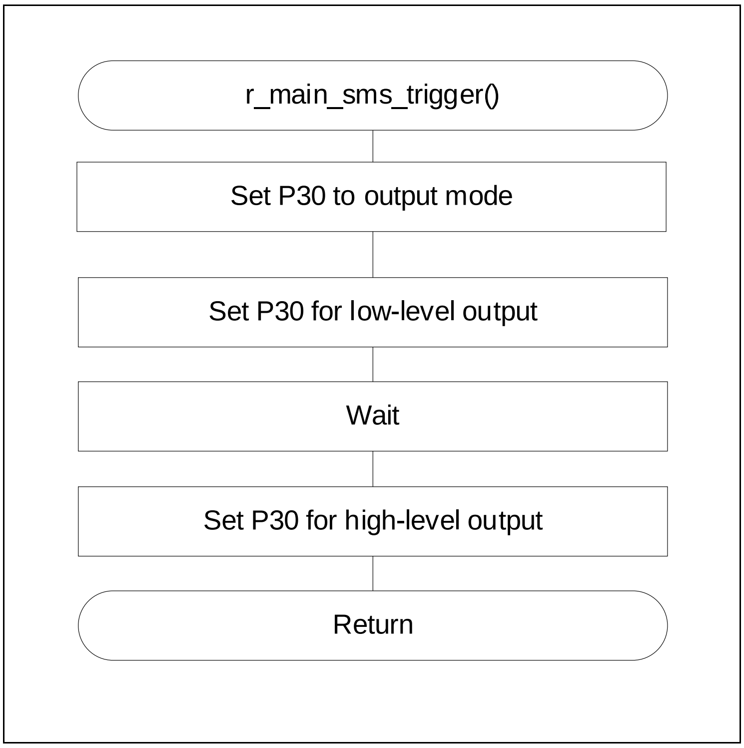
Figure 4-2 Main Initial Settings



4.6.3 SNOOZE Mode Sequencer Activation

Figure 4-3 shows the flowchart of the SNOOZE mode sequencer activation.

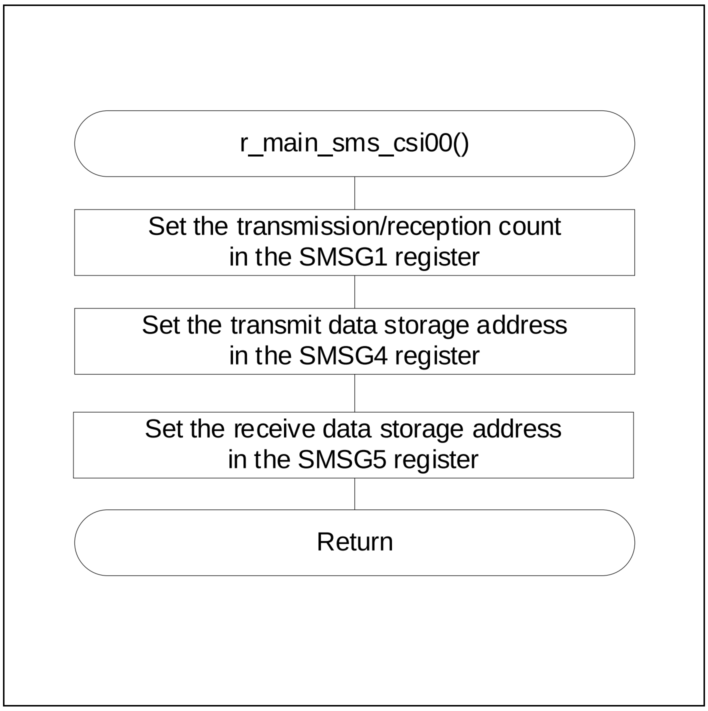
Figure 4-3 SNOOZE Mode Sequencer Activation



4.6.4 Communication Status Settings

Figure 4-4 shows the flowchart for communication status settings.

Figure 4-4 Communication Status Settings



4.7 Setting Up the SNOOZE Mode Sequencer

When the SNOOZE mode sequencer (SMS) is started by occurrence of a triggering event, it sequentially executes the processing commands that are stored in the sequencer instruction register (SMSI0-31). During execution of these commands, the sequencer general-purpose register (SMSG0-15) is used to store the source address, destination address, arithmetic data, and other data.

The SMSI0-31 and SMSG0-15 registers are set by coding an SMS program (.SMSASM file) in assembly language. You can also use the SNOOZE Mode Sequencer component of Smart Configurator to create an SMS program by combining processing blocks. The created SMS program is converted into C language by the assembler for SMS and then incorporated into the application program.

Figure 4-5 and Figure 4-6 shows a flowchart of the processing of the SNOOZE mode sequencer.

Figure 4-5 Processing of the SNOOZE Mode Sequencer (1/2)

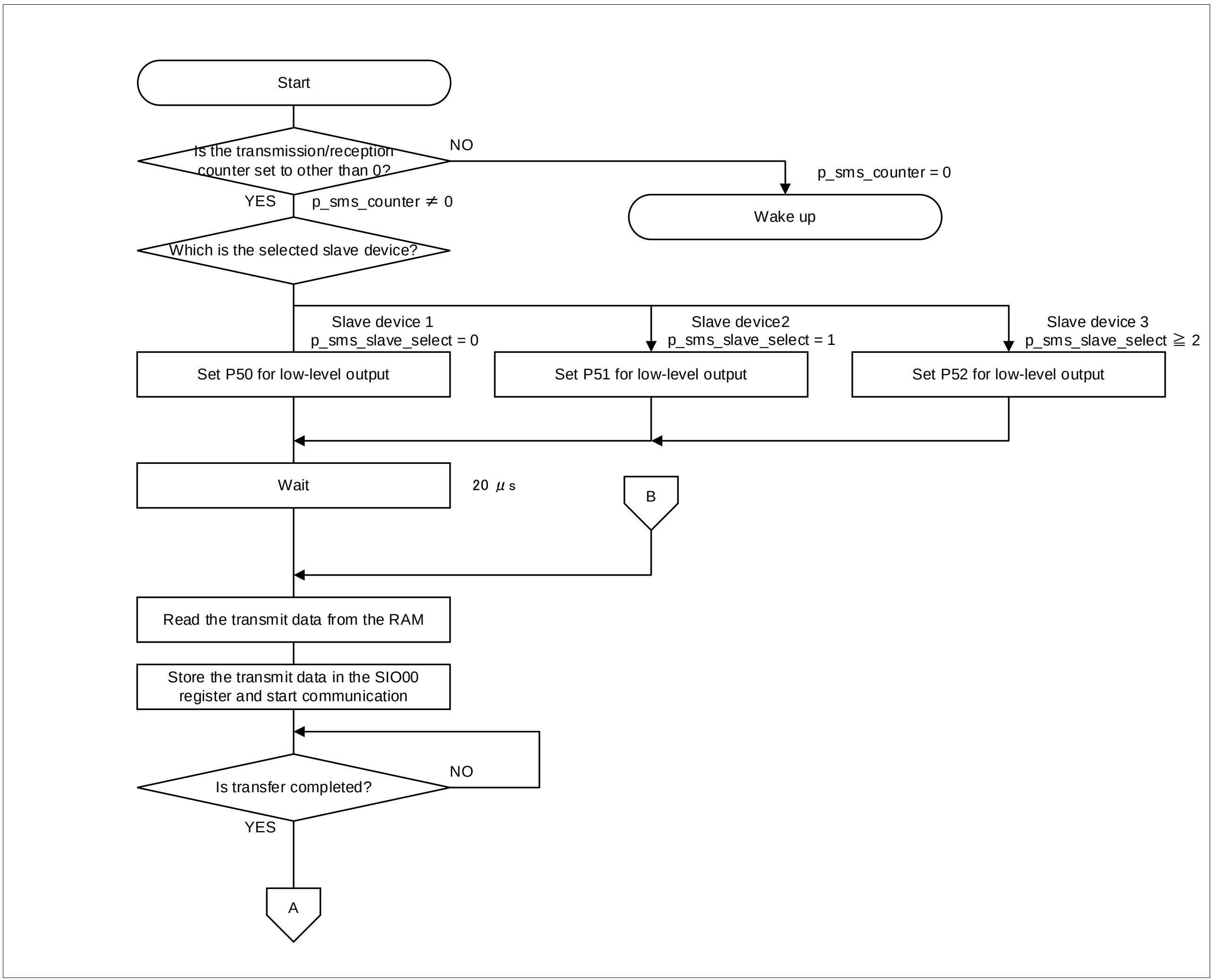


Figure 4-6 Processing of the SNOOZE Mode Sequencer (2/2)

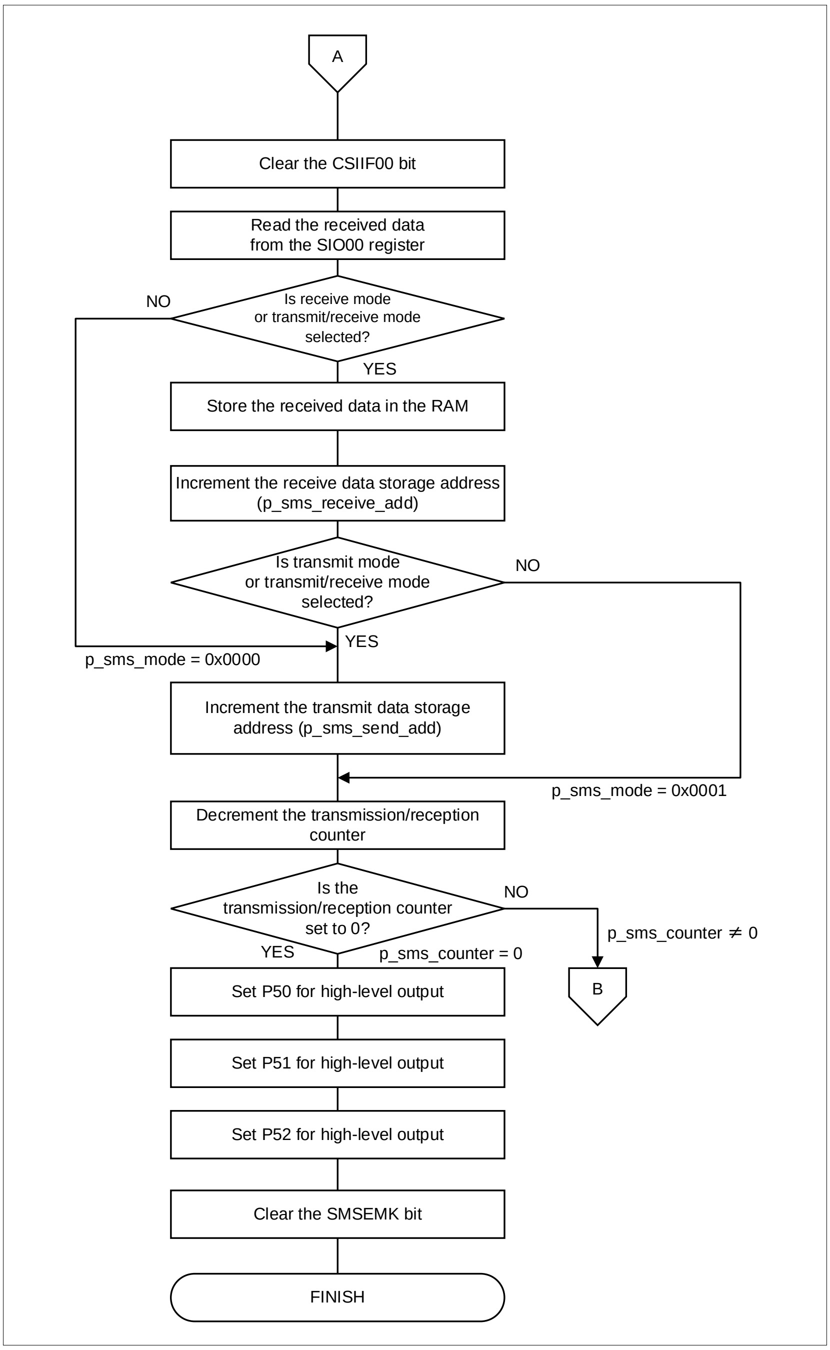


Table 4-5 Sequencer general-purpose registers 0-15

Register Symbol	Setting	Remark
SMSG0	0000H	fixed value: 0000H
SMSG1	0000H	Transmission/reception counter
SMSG2	0000H	Operation mode selection
SMSG3	0000H	Slave device selection
SMSG4	0000H	Transmit data storage address
SMSG5	0000H	Receive data storage address
SMSG6	0000H	Temporary storage of data
SMSG7	FF10H	SIO00 register address
SMSG8	FFE1H	IF0H register address
SMSG9	FF05H	P5 register address
SMSG10	0001H	Compare value: 0001H
SMSG11	FFE5H	MK0H register address
SMSG12	0000H	unused
SMSG13	0000H	unused
SMSG14	0000H	unused
SMSG15	FFFFH	fixed value: FFFFH

Table 4-6 Sequencer instruction registers 0-31

Register Symbol	Setting	Remark
SMSI0	7102H	CMPW SMSG1, SMSG0
SMSI1	81b2H	BZ $__28
SMSI2	7a32H	CMPW SMSG3, SMSG11
SMSI3	8042H	BZ $__7
SMSI4	8050H	BC $__9
SMSI5	5900H	CLR1 [SMSG9+0].0
SMSI6	8043H	BNZ $__10
SMSI7	5910H	CLR1 [SMSG9+0].1
SMSI8	8022H	BZ $__10
SMSI9	5920H	CLR1 [SMSG9+0].2
SMSI10	9145H	WAIT 20, 5
SMSI11	1460H	MOV SMSG6, [SMSG4+0]
SMSI12	0760H	MOV [SMSG7+0], SMSG6
SMSI13	b850H	WHILE0 [SMSG8+0].0
SMSI14	5850H	CLR1 [SMSG8+0].0
SMSI15	1760H	MOV SMSG6, [SMSG7+0]
SMSI16	7202H	CMPW SMSG2, SMSG0
SMSI17	8052H	BZ $__22
SMSI18	0560H	MOV [SMSG5+0], SMSG6
SMSI19	75a0H	ADDW SMSG5, SMSG10
SMSI20	72a2H	CMPW SMSG2, SMSG10
SMSI21	8022H	BZ $__23
SMSI22	74a0H	ADDW SMSG4, SMSG10
SMSI23	71a1H	SUBW SMSG1, SMSG10
SMSI24	8f33H	BNZ $__11
SMSI25	4900H	SET1 [SMSG9+0].0
SMSI26	4910H	SET1 [SMSG9+0].1
SMSI27	4920H	SET1 [SMSG9+0].2
SMSI28	f001H	CLI1 [SMSG11+0].4
SMSI29	f000H	FINISH
SMSI30~31	0000H	unused

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2022.11.18	-	First Edition
1.10	2024.1.9	4	Corrected Figure 1.1 Operation overview
		7	Corrected Table 2.1 Operation Confirmation Conditions
		19	Corrected Figure 4.6 Processing of the SNOOZE Mode Sequencer
		20	Corrected Table 4.5 Sequencer general-purpose registers 0-15
		21	Corrected Table 4.6 Sequencer instruction registers 0-31

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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