RL78/G23

High-speed On-chip Oscillator (HOCO) Clock Frequency Correction

Introduction

This application note explains how to correct the oscillation clock frequency of the high-speed on-chip oscillator (HOCO) by using the high-speed on-chip oscillator trimming register (HIOTRM) incorporated in RL78/G23.

An error in the oscillation frequency of the high-speed on-chip oscillator (HOCO) is detected using a subsystem clock or an external input signal and the high-speed on-chip oscillator trimming register (HIOTRM) is adjusted to set the oscillation frequency of the HOCO close to 32 MHz.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

1.1 Overview of Specifications

In this application note, an error in the clock oscillation frequency of the HOCO is detected using a subsystem clock or an external input signal. Then, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz.

Whether to use the subsystem clock or the external input signal is determined by the parameter switch. When the start switch is pressed, the 32-bit interval timer counts the frequency (pulse interval) or the pulse width of the subsystem clock or the external input signal. The HOCO is used for the count clock of the 32-bit interval timer. If the count value measured by the 32-bit interval timer is beyond the target range, the HIOTRM register is adjusted to set the oscillation frequency of the HOCO close to 32 MHz. The HIOTRM register is adjusted so that the count value is within the target range. The target range of the HOCO oscillation frequency is 32 MHz ± 0.1% (31.968 MHz to 32.032 MHz).

When the subsystem clock is used, the 32-bit interval timer measures the frequency (pulse interval) of the subsystem clock. To enhance accuracy, the pulse interval is measured four times to detect an error in the oscillation frequency of the HOCO.

When the external input signal is used, the 32-bit interval timer measures the frequency (pulse interval) of the timer input signal. A signal with a frequency of 512 Hz, a duty cycle of 50% is used as the timer input signal.

In this sample code, a pulse of 2 MHz ($f_{MAIN}/2^4$) is output from the clock output/buzzer output control circuit to always check correction results. To check the correction results, refer to the frequency of the output pulse on the PCLBUZ0 pin by using a frequency counter and the like.

Caution: Specified times and calibration methods in this sample code are used as examples. In this sample code, input from the start switch is used to start calibration, to simplify processing flows and to provide clear understanding. Adjust the timing of starting calibration and the intervals between start timings according to the system. This application note describes two calibration methods. Select the method most appropriate to the system for use.

Table 1-1 lists the peripheral functions to be used and their uses.

Table 1-1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Pin input edge detection interrupt	Used for the correction start switch.
32-bit interval timer channel 0, 1	Used for calibration of HOCO.
32-bit interval timer channel 2, 3	Used to prevent chattering on the correction start switch.
Clock output/buzzer output control circuit	Performs 2-MHz clock output.
Logic & Event Link Controller (ELCL)	Connects external input signal to the 32-bit interval timer

1.2 Outline of Operation

The following describes the settings of peripheral functions.

(1) Initialization of external interrupt (INTP0)

The settings are shown in Table 1-2

Table 1-2 Initial Setting Conditions of External Interrupt (INTP0)

Item	Description
Valid edge	Falling edge

(2) Initialization of 32-bit interval timer

Use in 16-bit capture mode.

The settings are shown in Table 1-3 and Table 1-4.

Table 1-3 Initial Setting Conditions of 32-bit interval timer (Channel 0 and 1)

Item	Description
Operating mode	16-bit capture mode
Operating clock (fITL0)	fIHP
Count source division ratio	fITL0 (non-devided)
Capture clock	fSXP

Table 1-4 Initial Setting Conditions of 32-bit interval timer (Channel 2 and 3)

Item	Description
Operating mode	16-bit capture mode
Operating clock (fITL1)	fSXP
Count source division ratio	fITL1 (non-devided)
Interval period	10 ms

(3) Initialization of Clock Output/Buzzer Output Controller

The settings are shown in Table Table 1-5.

Table 1-5 Initial setting Conditions of Clock Output/Buzzer Output Controller

Item	Description
Output Clock	2 MHz (fMAIN/2^4)

(4) Initialization of Logic and Event Link Controller

Link external input signal (P50) to 32-bit interval timer (as ITL capture trigger)
The settings are shown in Table 1-6.

Table 1-6 Initial setting Conditions of Logic and Event Link Controller

Item	Description
Event Source	Input pin (P50/SI11/INTP1)
Used Input Signal Selector	0
Used Event Controller	L1, Pass-through
Used Output Signal Selector	7
Destination	Capture trigger of ITL

1.3 Description of Calibration Methods

This section describes the two calibration methods to be used in this application note.

(1) Calibration with the subsystem clock

The subsystem clock cycle is measured on channel 0 and 1 of 32-bit interval timer used in 16-bit capture mode.

The subsystem clock (32.768 kHz, a cycle of 30.517578125 μs) is selected as the capture trigger, and the HOCO clock (32 MHz) is selected as the count clock. The subsystem clock cycle is measured using the input pulse interval measurement function of the TAU.

Select subsystem clock (32.768kHz, 30.517578125 μs per cycle) as capture trigger, and HOCO (32MHz) as count clock.

To enhance accuracy, the subsystem clock cycle is measured four times, and the four captured values are added up to calculate an error in the HOCO oscillation clock frequency.

The table below lists the calculated count values that are obtained through four times of capture when the frequency is 32 MHz, 32 MHz - 0.1% (31.968 MHz), or 32 MHz + 0.1% (32.032 MHz).

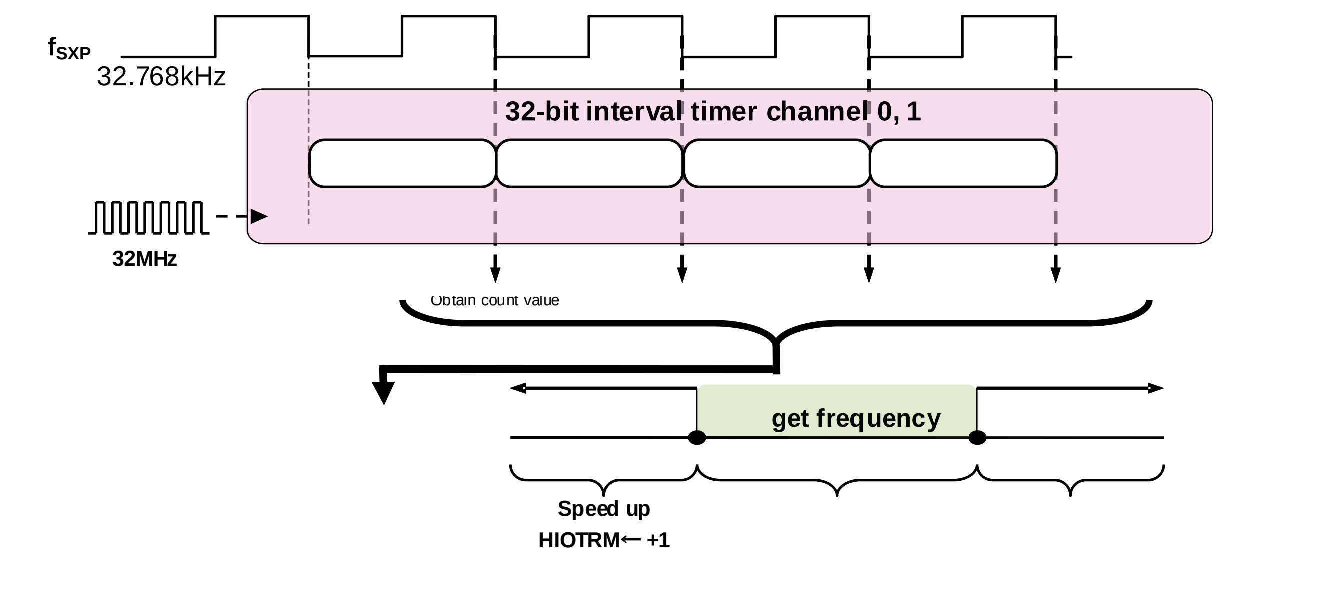
Table 1-7 Range of Count Values during the Use of Subsystem Clock

HOCO Clock Frequency (f_{IH})		Count Value Obtained through Four Times of Capture (Calculated Value)
32 MHz		3906.25
32 MHz – 0.1%	31.968 MHz	3902.34375
32 MHz + 0.1%	32.032 MHz	3910.15625

According to Table 1 - 7, the target range of the count value obtained through four times of capture is set to 3903 to 3909 when the target frequency range is 32 MHz ± 0.1% (31.968 to 32.032 MHz). If the obtained count value is 3902 or less, this means that the HOCO clock is slower than the target frequency. If it is 3910 or more, this means that the HOCO clock is faster than the target frequency. Determine the direction of correction of the HIOTRM register value (speeding up/slowing down), according to the count value, and perform calibration by incrementing the HIOTRM register value by ±1. When the count value is within the target range, the calibration is completed.

Figure 1-1 gives an example of calibration in which the subsystem clock is used.

Figure 1-1 Example of Calibration in which the Subsystem Clock is Used



(2) Calibration with the external input signal

The period of external input signal Is measured on channel 0 and 1 of 32-bit interval timer used in 16-bit capture mode.

A square wave (512Hz, a duty cycle of 50%) input to P50 is linked as a capture trigger by Logic and Event Link Controller (ELCL).

The HOCO clock (32 MHz) is selected as the count clock.

Accurate measurement of signal low-level width detects an error in the HOCO clock.

The table below lists the calculated count values that are obtained when the frequency is 32 MHz, 32 MHz - 0.1% (31.968 MHz), or 32 MHz + 0.1% (32.032 MHz).

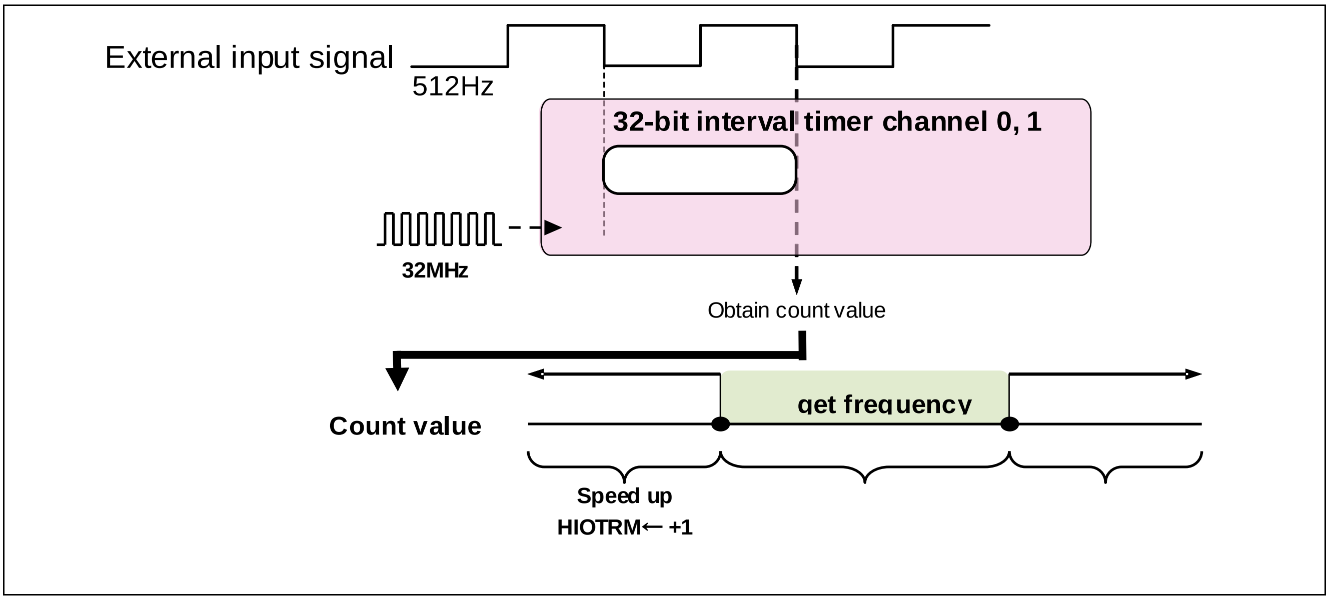
Table1-8 Count Values for Calibration with External Signal

HOCO Clock Frequency (f_{IH})		Count Value (Calculated Value)
32 MHz		62500
32 MHz – 0.1%	31.968 MHz	62437.5
32 MHz + 0.1%	32.032 MHz	62562.5

According to table 1.3, the target range of the count value is set to 62438 to 62561 for the target frequency range 32 MHz ± 0.1% (31.968 to 32.032 MHz). If the obtained count valued is 62437 or less, this means that the HOCO clock is slower than the target frequency. If it is 62562 or more, this means that the HOCO clock is faster than the target frequency. Determine the direction of correction of the HIOTRM register value (speeding up/slowing down), according to the count value, and perform calibration by incrementing the HIOTRM register value by ±1. When the count value is within the target range, the calibration is completed.

Figure 1.2 gives an example of calibration in which the external signal is used.

Figure 1-2 Example of Calibration in which the External Signal is Used



2. Operation Confirmation Conditions

The sample code of this application note has been tested under the following conditions.

Table2-1 Operation Confirmation Conditions

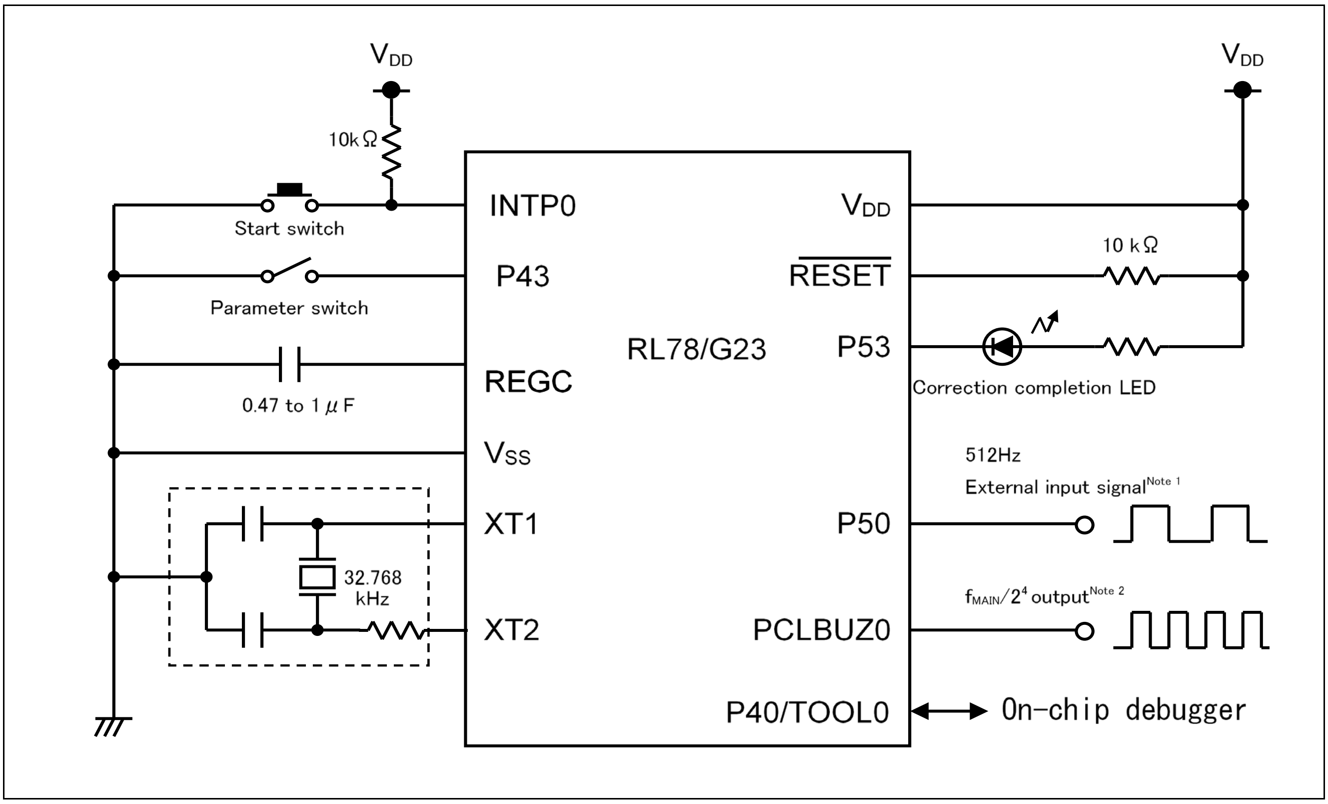
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Board used	RL78/G23 Fast Prototyping Board (RTK7RLG230CLG000BJ)
Operating frequency	High-speed on-chip oscillator clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	3.3 V (can be operated at 1.8 V to 5.5 V) LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ V8.05.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2 studio V2021-04 (21.4.0) from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.1 from IAR Systems Corp.
Smart configurator (SC)	V1.0.1 from Renesas Electronics Corp.
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of hardware configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



Note: 1. Input a signal with 512 Hz, a duty cycle of 50%.
2. Calibration sets the output frequency close to 2 MHz. Check the frequency using a frequency counter.

Caution: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

3.2 List of Pins Used

Table3-1 lists the pins used and their functions.

Table3-1 Pins used and their functions.

Pin Name	I/O	Description
P137/INTP0	Input	Start switch: Connects the switch for starting calibration.
P43	Input	Parameter switch: Connects the switch for selecting a calibration method.
P53	Output	Correction completion LED: Connects the LED that indicates correction completion.
P123/XT1	Input	Subsystem clock: Connects a 32.768-kHz crystal oscillator.
P124/XT2	Input	
P50	Input	External input signal pin: Input a signal with 512 Hz, a duty cycle of 50%.
P140/PCLBUZ0	Output	Clock output: Always outputs $f_{MAIN}/2^4$ (2 MHz).

Caution: In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H/010C1H	11111110B	LVD0 detection voltage: Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H/010C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H/010C3H	10000101B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constants

Constant Name	Setting Value	Description
HIOTRM_MAX	00111111B	Maximum value of the HIOTRM register
HIOTRM_MIN	00000000B	Minimum value of the HIOTRM register
CCNT_XT1_MAX	3910	Upper threshold of subsystem clock count
CCNT_XT1_MIN	3902	Lower threshold of subsystem clock count
CCNT_EXT_MAX	62562	Upper threshold of external input signal count
CCNT_EXT_MIN	62437	Lower threshold of external input signal count

4.3 List of Variables

Table 4-3 lists the global variables.

Table 4-3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	calibration_count	Calibration count value	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint8_t	calibrate_history	Calibration history	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	count_value	Count value (Used as an argument of R_Trimming_OCO)	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	max	Upper threshold of count	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()
uint16_t	min	Lower threshold of count	R_Main_UseXT1() R_Main_ExternalClock() R_Trimming_OCO()

4.4 List of Functions

Table 4-4 shows a list of functions.

Table 4-4 Functions

Function Name	Outline
R_Main_UseXT1	Calibration with the subsystem clock
R_Main_ExternalClock	Calibration with the external input signal
R_ELCL_Enable	Enable operation of ELCL
R_ELCL_Disable	Disable operation of ELCL
R_Trimming_OCO	HOCO clock correction

4.5 Specification of Functions

The function specifications of the sample code are shown below.

[Function Name] R_Main_UseXT1

Outline	Calibration with the subsystem clock
Header	None
Declaration	void R_Main_UseXT1(void)
Description	This function captures the subsystem clock count value and performs correction processing.
Argument	None
Return Value	None
Outline	None

[Function Name] R_Main_ExternalClock

Outline	Calibration with the external input signal
Header	None
Declaration	void R_Main_ExternalClock(void)
Description	This function captures the external input signal count value and performs correction processing.
Argument	None
Return Value	None
Outline	None

[Function Name] R_ELCL_Enable

Outline	Enable operation of ELCL
Header	None
Declaration	void R_ELCL_Enable(void);
Description	Link external input signal (P50) to 32-bit interval timer
Argument	None
Return Value	None
Outline	None

[Function Name]R_ELCL_Disable

Outline	Disable operation of ELCL
Header	None
Declaration	void R_ELCL_Disable(void);
Description	Disable operation of ELCL
Argument	None
Return Value	None
Outline	None

[Function Name]R_Trimming_OCO

Outline	HOCO clock correction
Header	None
Declaration	uint8_t R_Trimming_OCO(uint16_t count)
Description	This function sets the HIOTRM according to the argument and then determines whether to continue calibration.
Argument	count : [Target clock count value]
Return Value	[0]: Calibration ends. [1]: Calibration continues.
Outline	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4-1 and Figure 4-2 shows the flowchart of the main processing.

Figure 4-1 Main Processing (1 / 2)

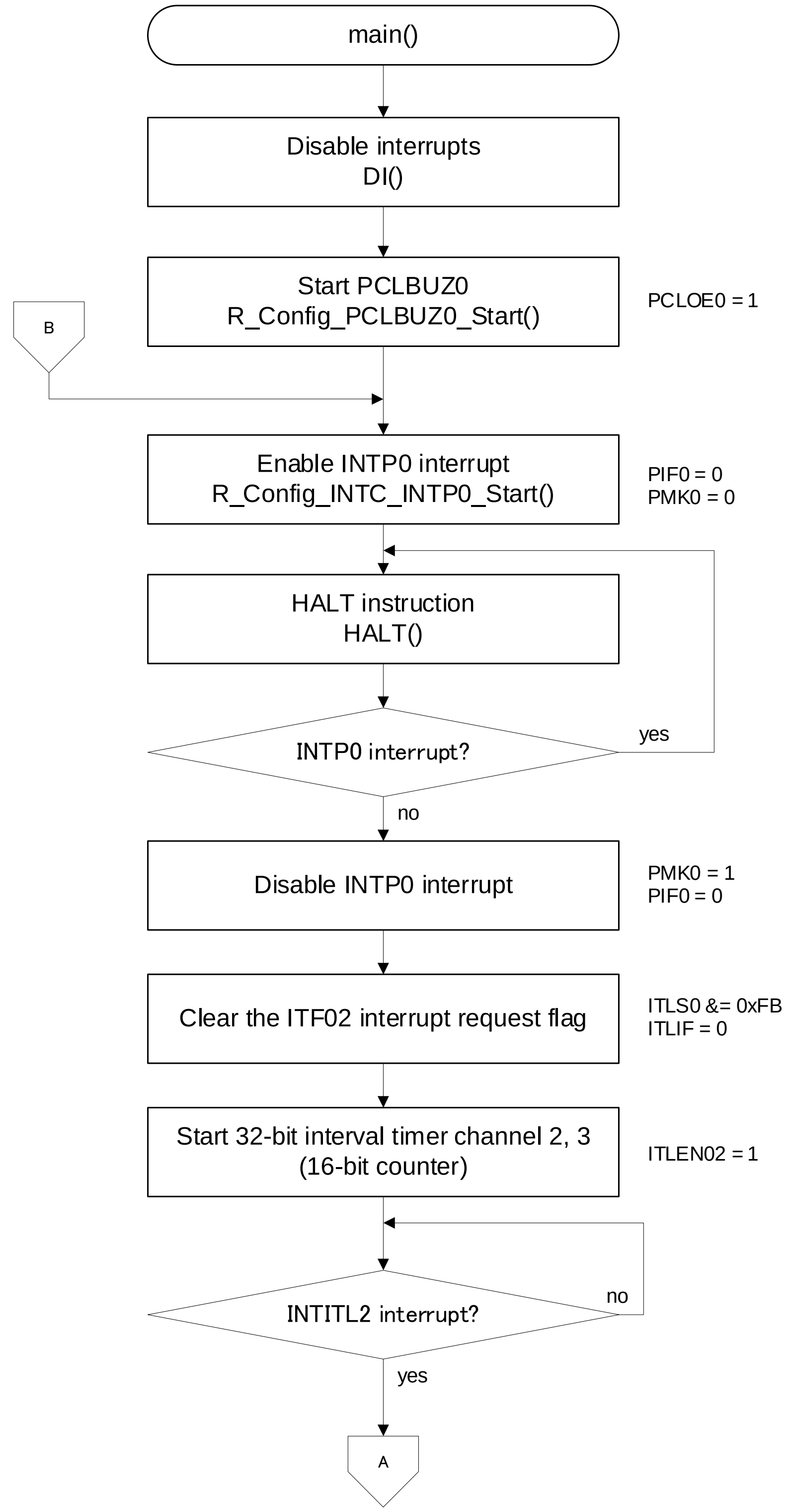
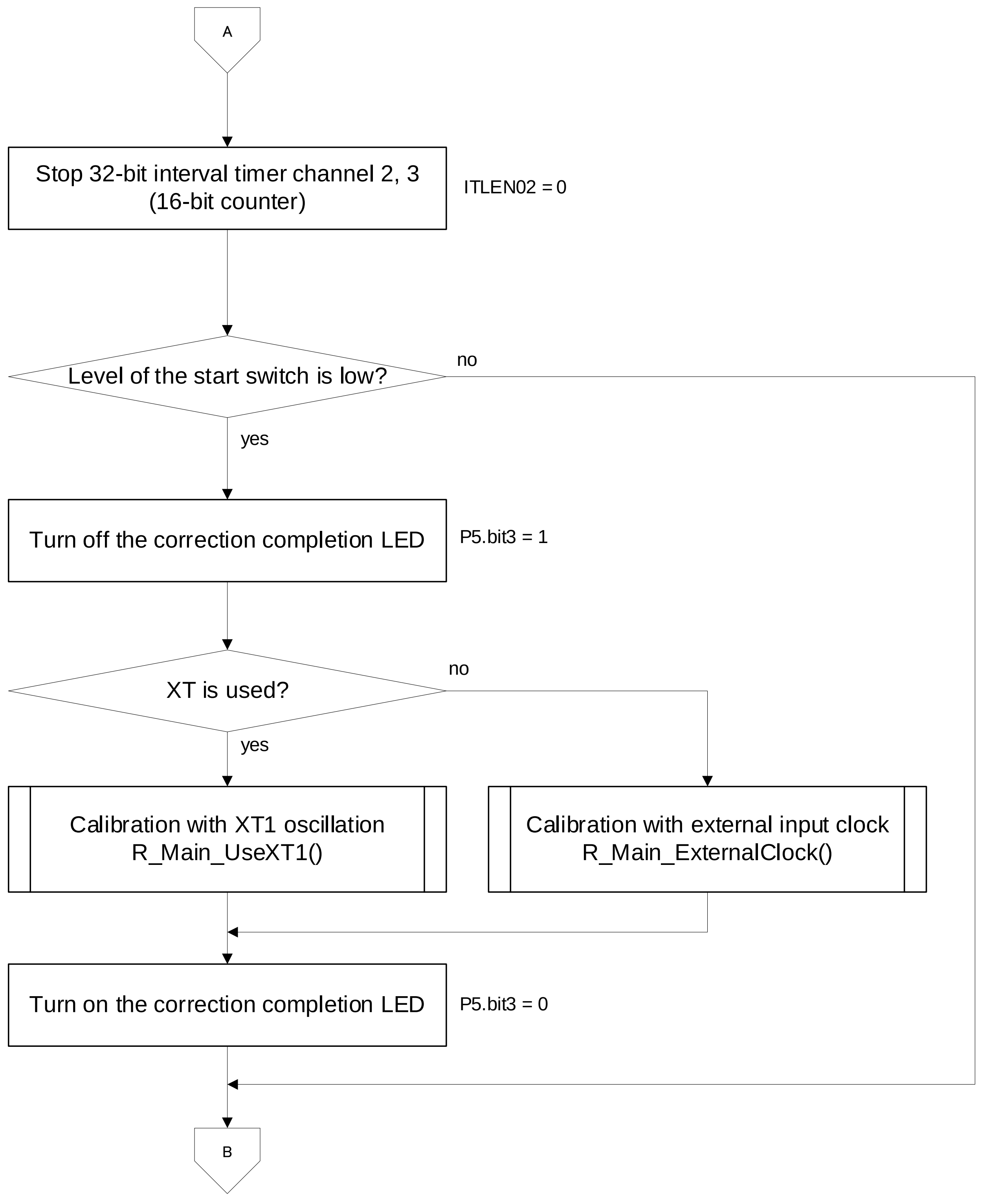


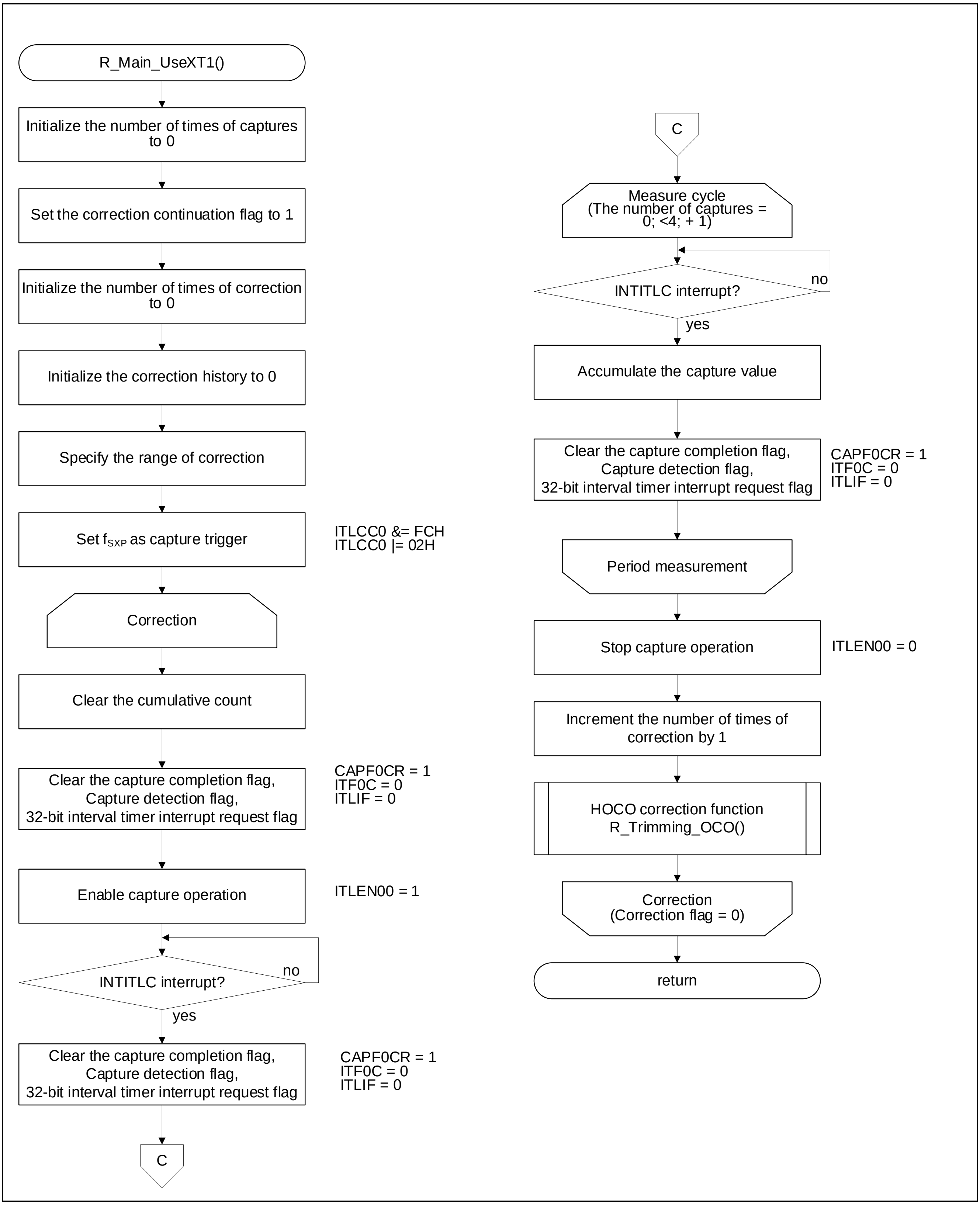
Figure 4-2 Main Processing (2 / 2)



4.6.2 Calibration with XT1 Oscillation

Figure 4-2 show the flowchart for calibration with XT1 oscillation.

Figure 4-2 Calibration with XT1 Oscillation



4.6.3 Calibration with External Input Clock

Figure 4-3 and Figure 4-4 show the flowcharts for calibration with an external input clock.

Figure 4-3 Calibration with External Input Clock (1/2)

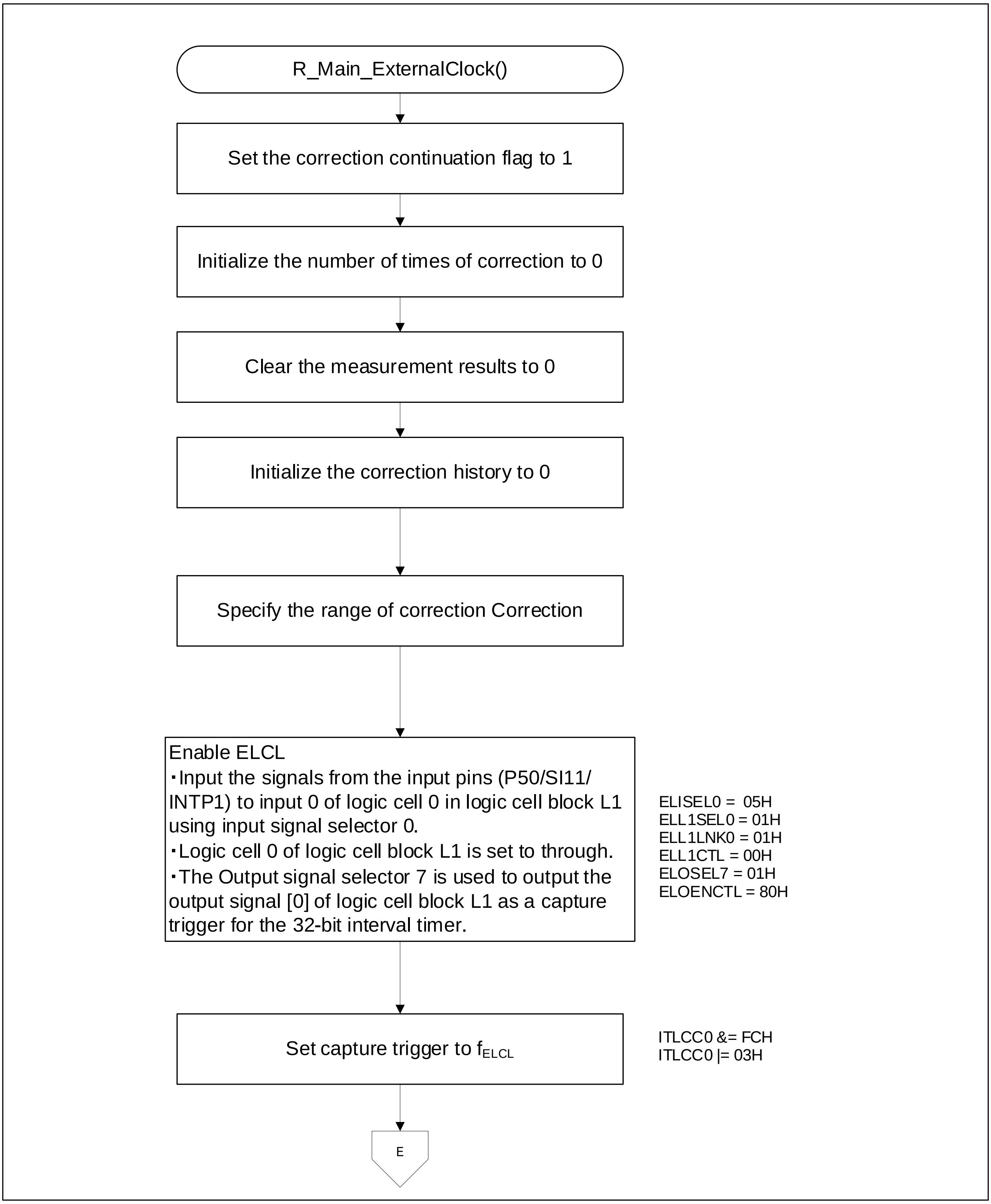
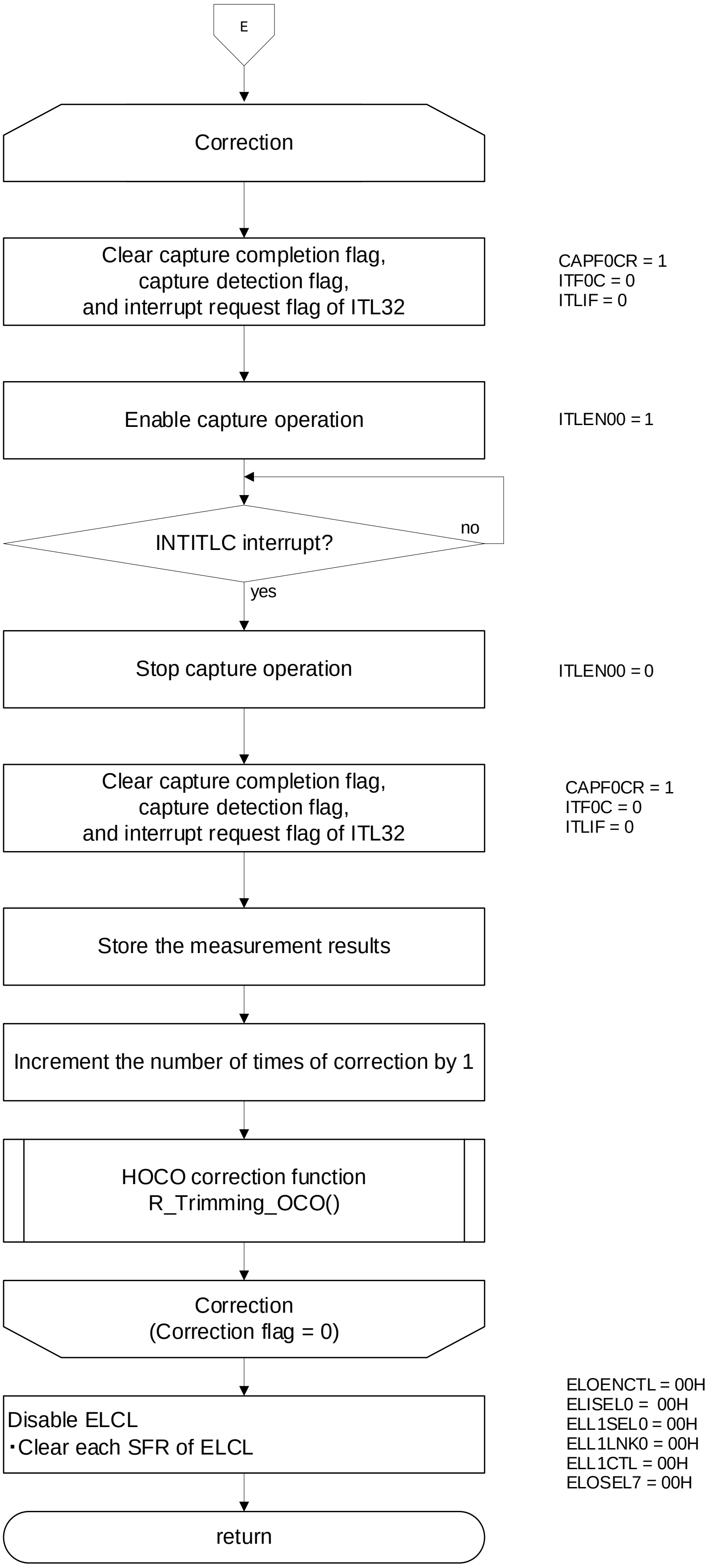


Figure 4-4 Calibration with External Input Clock (2/2)



4.6.4 HOCO Correction Function

Figure 4-5 and Figure 4-6 show the flowcharts for the HOCO correction function.

Figure 4-5 HOCO Correction Function (1/2)

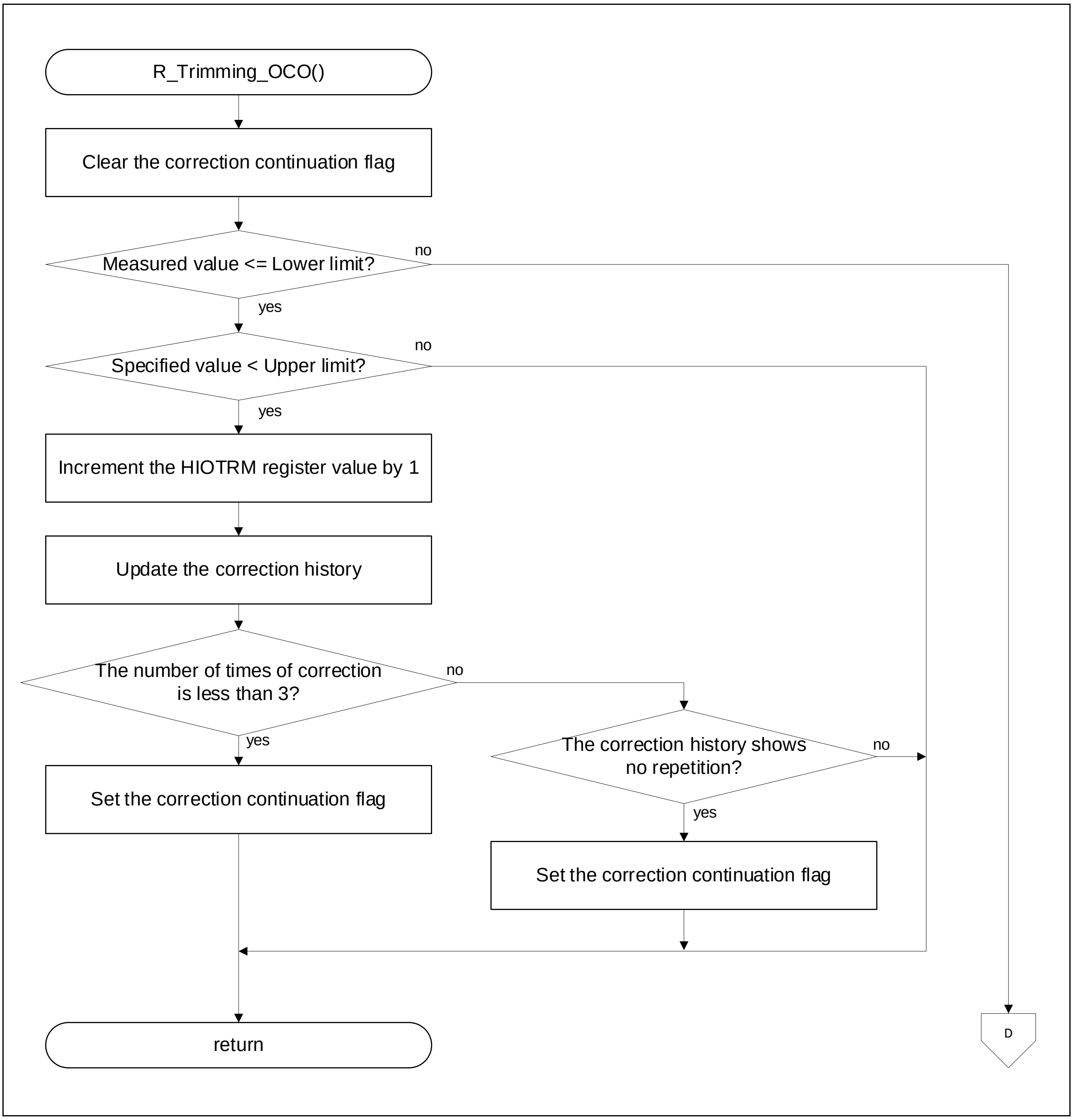
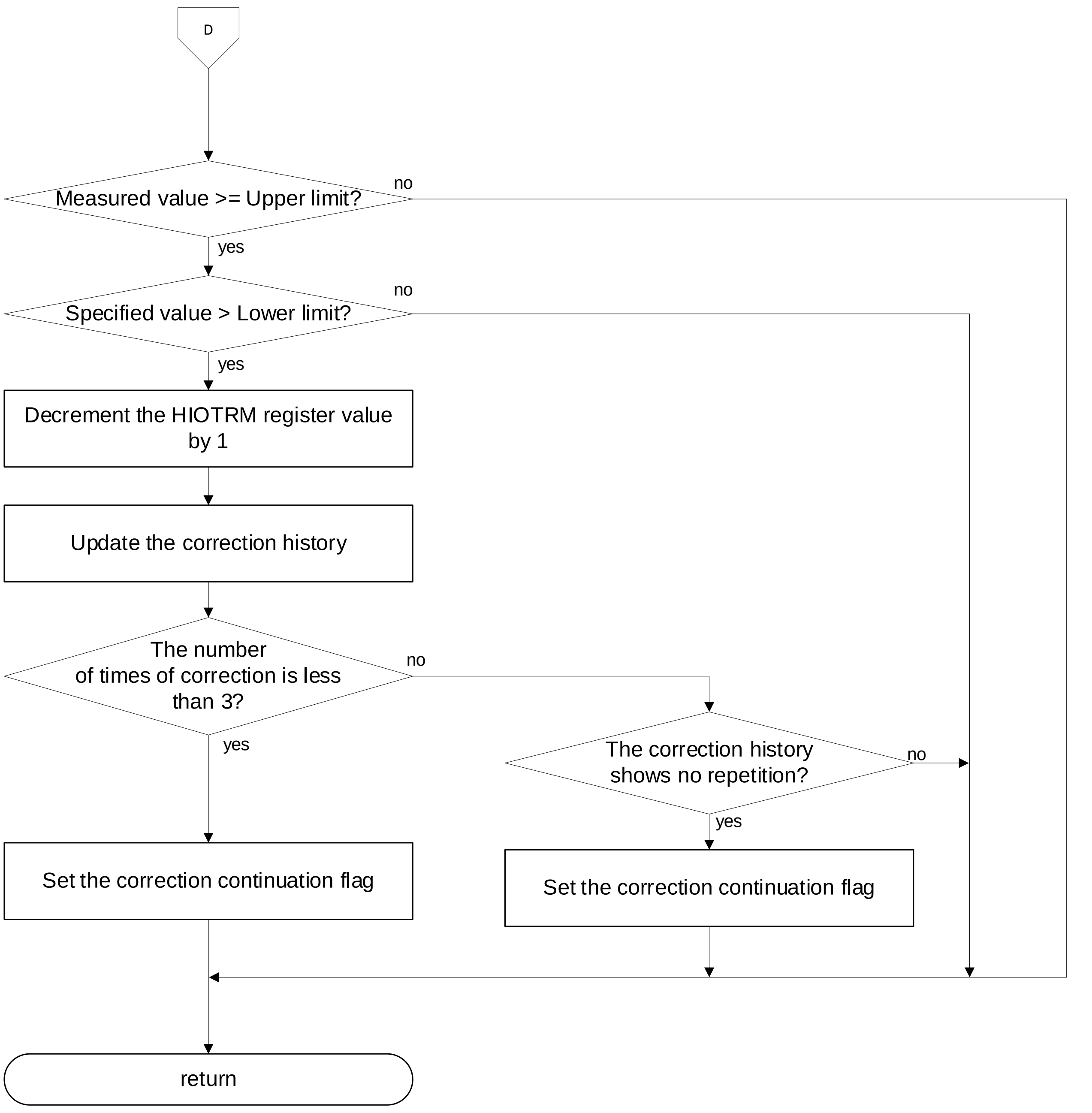


Figure 4-6 HOCO Correction Function (2/2)



4.7 Changes on peripheral driver

In this application note, the source code of the peripheral driver generated by the Smart Configurator is used with the following changes.

For the setting values for Smart Configurator, please refer to the sample program.

Function	Before changes	After changes
void R_Config_ITL012_ITL013_Create(void);	/* Stop 32-bit interval timer */ ITLCTL0 = 0x00U; /* Mask INTITL interrupt */ ITLMKF0 |= _04_ITL_CHANNEL2_COUNT_MATCH_MASK; ITLS0 &= (uint16_t)~_04_ITL_CHANNEL2_COUNT_MATCH_DETECTE; ITLMK = 1U; /* disable INTITL interrupt */ ITLIF = 0U; /* clear INTITL interrupt flag */ /* Set INTITL low priority */ ITLPR1 = 1U; ITLPR0 = 1U; /* 32-bit interval timer used as 16-bit timer */ ITLCTL0 |= _40_ITL_MODE_16BIT; ITLCSEL0 &= _F8_ITL_CLOCK_FITL0_CLEAR; ITLCSEL0 |= _04_ITL_CLOCK_FITL0_FSXL; ITLFDIV01 &= _F8_ITL_ITL012_FITL0_CLEAR; ITLFDIV01 |= _00_ITL_ITL012_FITL0_1; ITLCMP01 = _0147_ITL_ITLCMP01_VALUE; R_Config_ITL012_ITL013_Create_UserInit();	/* Stop 32-bit interval timer */ ITLCTL0 = 0x00U; /* Mask INTITL interrupt */ ITLMKF0 |= _04_ITL_CHANNEL2_COUNT_MATCH_MASK; ITLS0 &= (uint16_t)~_04_ITL_CHANNEL2_COUNT_MATCH_DETECTE; ITLMK = 1U; /* disable INTITL interrupt */ ITLIF = 0U; /* clear INTITL interrupt flag */ /* Set INTITL low priority */ ITLPR1 = 1U; ITLPR0 = 1U; /* 32-bit interval timer used as 16-bit timer */ ITLCTL0 |= _40_ITL_MODE_16BIT; ITLCSEL1 &= _8F_ITL_CLOCK_FITL1_CLEAR; ITLCSEL1 |= _40_ITL_CLOCK_FITL1_FSXL; ITLCMP01 = _0x0CCC; R_Config_ITL012_ITL013_Create_UserInit();

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User’s Manual: Hardware (R01UH0896)
RL78 family user's manual software (R01US0015)
The latest versions can be downloaded from the Renesas Electronics website.

Technical update
The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.01.21	—	First Edition
1.01	May.18.21	9	Updated the Operation Confirmation Condition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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